

**FREQUENCY GENERATOR FOR PCIE GEN1/2, USB3.0, QPI & SATA**
**ICS9FG104E**

## Description

The ICS9FG104E is a frequency generator that provides 4 differential HCSL output pairs. It can be used to drive PCIe Gen1/2, SATA and USB3.0 devices. The part can use either a 14.31818 MHz or 25 MHz crystal. The 9FG104E can also be driven by a reference input clock instead of a crystal. It provides outputs with cycle-to-cycle jitter of less than 50 ps and output-to-output skew of less than 35 ps.

## Recommended Application

Frequency Generator for CPU, PCIe Gen1/2, SATA and USB3.0

## Output Features

- 4 - HCSL differential outputs
- 1 - 3.3V REF output (either 14.318M or 25M depending on XTAL)

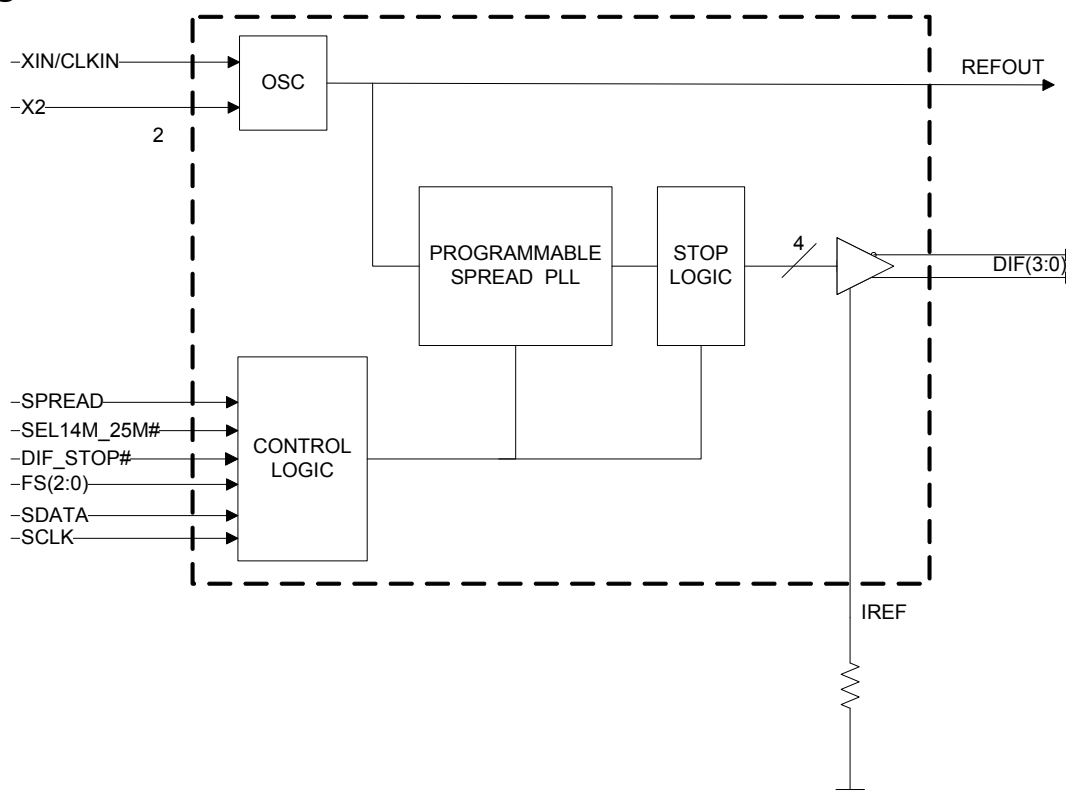
## Features/Benefits

- Generates common frequencies from 14.318MHz or 25MHz
- Crystal or reference input
- 4 - 0.7V current-mode HCSL output pairs
- Supports Serial-ATA at 100MHz
- Two spread spectrum modes: -0.5% down spread and +/-0.25% center spread; Lower EMI
- 31.5KHz spread modulation rate; passes USB3 compliance testing
- Unused outputs may be disabled in either driven or Hi-Z state for power management
- I-temp version available; supports embedded applications

## Key Specifications

- Cycle to cycle jitter: < 50ps
- Phase jitter: PCIe Gen1/2 <3ps rms
- Output to output skew <35ps
- +/-300 ppm frequency accuracy on output clocks
- +/-50ppm on all output frequencies with Spread Off

## Block Diagram



## Pin Configuration

|           |    |                |    |              |
|-----------|----|----------------|----|--------------|
| XIN/CLKIN | 1  | <b>9FG104E</b> | 28 | VDDA         |
| X2        | 2  |                | 27 | GNDA         |
| VDD       | 3  |                | 26 | IREF         |
| GND       | 4  |                | 25 | vFS0         |
| REFOUT    | 5  |                | 24 | vFS1         |
| vFS2      | 6  |                | 23 | DIF_0        |
| DIF_3     | 7  |                | 22 | DIF_0#       |
| DIF_3#    | 8  |                | 21 | VDD          |
| VDD       | 9  |                | 20 | GND          |
| GND       | 10 |                | 19 | DIF_1        |
| DIF_2     | 11 |                | 18 | DIF_1#       |
| DIF_2#    | 12 |                | 17 | ^SEL14M_25M# |
| SDATA     | 13 |                | 16 | vSPREAD      |
| SCLK      | 14 |                | 15 | DIF_STOP#    |

^ Pin has internal 120K pull up

v Pin has internal 120K pull down

## Power Groups

| Pin Number |       | Description                        |
|------------|-------|------------------------------------|
| VDD        | GND   |                                    |
| 3          | 4     | REFOUT, Digital Inputs             |
| 9,21       | 10,20 | DIF Outputs                        |
| 28         | 27    | IREF, Analog VDD, GND for PLL Core |

## Frequency Select Table

| SEL14M_25M#<br>(FS3) | FS2 | FS1 | FS0 | OUTPUT(MHz) |
|----------------------|-----|-----|-----|-------------|
| 0                    | 0   | 0   | 0   | 100.00      |
| 0                    | 0   | 0   | 1   | 125.00      |
| 0                    | 0   | 1   | 0   | 133.33      |
| 0                    | 0   | 1   | 1   | 166.67      |
| 0                    | 1   | 0   | 0   | 200.00      |
| 0                    | 1   | 0   | 1   | 266.00      |
| 0                    | 1   | 1   | 0   | 333.00      |
| 0                    | 1   | 1   | 1   | 400.00      |
| 1                    | 0   | 0   | 0   | 100.00      |
| 1                    | 0   | 0   | 1   | 125.00      |
| 1                    | 0   | 1   | 0   | 133.33      |
| 1                    | 0   | 1   | 1   | 166.67      |
| 1                    | 1   | 0   | 0   | 200.00      |
| 1                    | 1   | 0   | 1   | 266.00      |
| 1                    | 1   | 1   | 0   | 333.00      |
| 1                    | 1   | 1   | 1   | 400.00      |

## Pin Descriptions

| PIN # | PIN NAME     | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                           |
|-------|--------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | XIN/CLKIN    | IN       | Crystal input or Reference Clock input                                                                                                                                                                                                |
| 2     | X2           | OUT      | Crystal output, Nominally 14.318MHz                                                                                                                                                                                                   |
| 3     | VDD          | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 4     | GND          | PWR      | Ground pin.                                                                                                                                                                                                                           |
| 5     | REFOUT       | OUT      | Reference Clock output                                                                                                                                                                                                                |
| 6     | vFS2         | IN       | Frequency select pin. This pin has an internal 120k pull down resistor                                                                                                                                                                |
| 7     | DIF_3        | OUT      | 0.7V differential true clock output                                                                                                                                                                                                   |
| 8     | DIF_3#       | OUT      | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 9     | VDD          | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 10    | GND          | PWR      | Ground pin.                                                                                                                                                                                                                           |
| 11    | DIF_2        | OUT      | 0.7V differential true clock output                                                                                                                                                                                                   |
| 12    | DIF_2#       | OUT      | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 13    | SDATA        | I/O      | Data pin for SMBus circuitry, 3.3V tolerant.                                                                                                                                                                                          |
| 14    | SCLK         | IN       | Clock pin of SMBus circuitry, 5V tolerant.                                                                                                                                                                                            |
| 15    | DIF_STOP#    | IN       | Active low input to stop differential output clocks.                                                                                                                                                                                  |
| 16    | vSPREAD      | IN       | Asynchronous, active high input to enable spread spectrum functionality. This pin has a 120Kohm pull down resistor.                                                                                                                   |
| 17    | ^SEL14M_25M# | IN       | Select 14.31818 MHz or 25 Mhz input frequency. This pin has an internal 120kohm pull up resistor.<br>1 = 14.31818 MHz, 0 = 25 MHz                                                                                                     |
| 18    | DIF_1#       | OUT      | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 19    | DIF_1        | OUT      | 0.7V differential true clock output                                                                                                                                                                                                   |
| 20    | GND          | PWR      | Ground pin.                                                                                                                                                                                                                           |
| 21    | VDD          | PWR      | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 22    | DIF_0#       | OUT      | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 23    | DIF_0        | OUT      | 0.7V differential true clock output                                                                                                                                                                                                   |
| 24    | vFS1         | IN       | 3.3V Frequency select latched input pin with internal 120kohm pull down resistor.                                                                                                                                                     |
| 25    | vFS0         | IN       | 3.3V Frequency select latched input pin with internal 120kohm pull down resistor.                                                                                                                                                     |
| 26    | IREF         | OUT      | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 27    | GNDA         | PWR      | Ground pin for the PLL core.                                                                                                                                                                                                          |
| 28    | VDDA         | PWR      | 3.3V power for the PLL core.                                                                                                                                                                                                          |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS9FG104E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Symbol   | Parameter                                 | Min  | Max | Units |
|----------|-------------------------------------------|------|-----|-------|
| VDDxx    | 3.3V Supply Voltage                       |      | 4.6 | V     |
| Ts       | Storage Temperature                       | -65  | 150 | °C    |
| Tambient | Ambient Operating Temp•(Commerical Grade) | 0    | +70 | °C    |
| Tambient | Ambient Operating Temp•(Industrial Grade) | -40  | +85 | °C    |
| Tcase    | Case Temperature                          |      | 115 | °C    |
| ESD prot | Input ESD protection•human body model     | 2000 |     | V     |

## Electrical Characteristics–REF-14.318/25 MHz

T<sub>A</sub> = T<sub>AMBIENT</sub>; V<sub>DD</sub> = 3.3 V +/-5%; R<sub>S</sub>=33Ω, C<sub>L</sub> = 5 pF (unless otherwise specified)

| PARAMETER           | SYMBOL                  | CONDITIONS                                       | MIN | TYP | MAX | UNITS | Notes |
|---------------------|-------------------------|--------------------------------------------------|-----|-----|-----|-------|-------|
| Output High Voltage | V <sub>OH</sub>         | I <sub>OH</sub> = -1 mA                          | 2.4 |     |     | V     | 1     |
| Output Low Voltage  | V <sub>OL</sub>         | I <sub>OL</sub> = 1 mA                           |     |     | 0.4 | V     | 1     |
| Rise Time           | t <sub>r1</sub>         | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 1   | 1.4 | 2.5 | ns    | 1     |
| Fall Time           | t <sub>f1</sub>         | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 1   | 1.4 | 2.5 | ns    | 1     |
| Duty Cycle          | d <sub>t1</sub>         | V <sub>T</sub> = 1.5 V                           | 45  | 53  | 55  | %     | 1     |
| Jitter              | t <sub>jcy-cycCOM</sub> | V <sub>T</sub> = 1.5 V (commercial)              |     | 87  | 200 | ps    | 1     |
| Jitter              | t <sub>jcy-cycIND</sub> | V <sub>T</sub> = 1.5 V (industrial)              |     | 87  | 250 | ps    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Trim capacitors must be used to tune the REF to the exact Crystal Frequency.

## Electrical Characteristics–Differential Phase Jitter Parameters

| PARAMETER     | SYMBOL                  | CONDITIONS                                   | MIN | TYP | MAX | UNITS    | Notes |
|---------------|-------------------------|----------------------------------------------|-----|-----|-----|----------|-------|
| Jitter, Phase | t <sub>jphasePLL</sub>  | PCIe Gen 1                                   |     | 25  | 86  | ps (p-p) | 1,2   |
|               | t <sub>jphaseLo</sub>   | PCIe Gen 1/2<br>10kHz < f < 1.5MHz           |     | 0.8 | 3   | ps (RMS) | 1,2   |
|               | t <sub>jphaseHigh</sub> | PCIe Gen 1/2<br>1.5MHz < f < Nyquist (50MHz) |     | 1.8 | 3.1 | ps (RMS) | 1,2   |
|               | t <sub>jphQPI</sub>     | QPI 133MHz 4.8G/6.4Gb, 12UI                  |     | 0.2 | 0.5 | ps (RMS) | 1,3   |
|               | t <sub>jphFBD3.2G</sub> | FBD specs<br>(11 to 33MHz)                   |     | 1.4 | 3   | ps (RMS) | 1     |
|               | t <sub>jphFBD4.8G</sub> | FBD specs<br>(11 to 33MHz)                   |     | 1.1 | 2.5 | ps (RMS) | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>See <http://www.pcisig.com> for complete specs

<sup>3</sup>First number is 4.8G link speed, second number is 6.4G link speed. From Intel Clock Jit tool

## Electrical Characteristics–Input/Supply/Common Output Parameters

$T_A = T_{\text{AMBIENT}}$ ; Supply Voltage  $V_{DD} = 3.3 \text{ V} \pm 5\%$

| PARAMETER                                                 | SYMBOL                       | CONDITIONS                                                       | MIN                   | TYP      | MAX                   | UNITS | NOTES |
|-----------------------------------------------------------|------------------------------|------------------------------------------------------------------|-----------------------|----------|-----------------------|-------|-------|
| Tambient                                                  | $T_{\text{COM}}$             | Commercial Temperature                                           | 0                     |          | 70                    | °C    |       |
| Tambient                                                  | $T_{\text{IND}}$             | Industrial Temperature                                           | -40                   |          | 85                    | °C    |       |
| Input High Voltage                                        | $V_{\text{IH}}$              | 3.3 V $\pm 5\%$                                                  | 2                     |          | $V_{\text{DD}} + 0.3$ | V     | 1     |
| Input Low Voltage                                         | $V_{\text{IL}}$              | 3.3 V $\pm 5\%$                                                  | $V_{\text{SS}} - 0.3$ |          | 0.8                   | V     | 1     |
| Input High Current                                        | $I_{\text{IH}}$              | $V_{\text{IN}} = V_{\text{DD}}$                                  | -5                    |          | 5                     | uA    | 1     |
| Input Low Current                                         | $I_{\text{IL1}}$             | $V_{\text{IN}} = 0 \text{ V}$ ; Inputs with no pull-up resistors | -5                    |          |                       | uA    | 1     |
|                                                           | $I_{\text{IL2}}$             | $V_{\text{IN}} = 0 \text{ V}$ ; Inputs with pull-up resistors    | -200                  |          |                       | uA    | 1     |
| Operating Supply Current<br>( $T_A = \text{Commercial}$ ) | $\text{IDD}_{\text{VDD}}$    | $C_L = \text{Full load}$ ; $f_{\text{out}} = 400 \text{ MHz}$    |                       | 106      | 125                   | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDA}}$   |                                                                  |                       | 22       | 25                    | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDD}}$    | $C_L = \text{Full load}$ ; $f_{\text{out}} = 100 \text{ MHz}$    |                       | 87       | 100                   | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDA}}$   |                                                                  |                       | 22       | 25                    | mA    | 1     |
| DIF_STOP# Current<br>( $T_A = \text{Commercial}$ )        | $\text{IDD}_{\text{VDDPD}}$  | All DIF pairs stopped in driven mode                             |                       | 86       | 100                   | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDAPD}}$ |                                                                  |                       | 20       | 25                    | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDPD}}$  | All DIF pairs stopped in Hi-Z mode                               |                       | 28       | 35                    | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDAPD}}$ |                                                                  |                       | 19       | 25                    | mA    | 1     |
| Operating Supply Current<br>( $T_A = \text{Industrial}$ ) | $\text{IDD}_{\text{VDD}}$    | $C_L = \text{Full load}$ ; $f_{\text{out}} = 400 \text{ MHz}$    |                       | 109      | 125                   | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDA}}$   |                                                                  |                       | 21       | 25                    | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDD}}$    | $C_L = \text{Full load}$ ; $f_{\text{out}} = 100 \text{ MHz}$    |                       | 90       | 100                   | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDA}}$   |                                                                  |                       | 20       | 25                    | mA    | 1     |
| DIF_STOP# Current<br>( $T_A = \text{Industrial}$ )        | $\text{IDD}_{\text{VDDPD}}$  | All DIF pairs stopped in driven mode                             |                       | 87       | 100                   | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDAPD}}$ |                                                                  |                       | 20       | 25                    | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDPD}}$  | All DIF pairs stopped in Hi-Z mode                               |                       | 27       | 35                    | mA    | 1     |
|                                                           | $\text{IDD}_{\text{VDDAPD}}$ |                                                                  |                       | 20       | 25                    | mA    | 1     |
| Input Frequency <sup>3</sup>                              | $F_i$                        | SEL14M_25M# = 0                                                  | 22.5                  | 25.00    | 27.5                  | MHz   | 3     |
|                                                           |                              | SEL14M_25M# = 1                                                  | 12.886                | 14.31818 | 15.75                 | MHz   | 3     |
| Pin Inductance <sup>1</sup>                               | $L_{\text{pin}}$             |                                                                  |                       |          | 7                     | nH    | 1     |
| Input/Output Capacitance <sup>1</sup>                     | $C_{\text{IN}}$              | Logic Inputs                                                     | 1.5                   |          | 5                     | pF    | 1     |
|                                                           | $C_{\text{OUT}}$             | Output pin capacitance                                           |                       |          | 6                     | pF    | 1     |
| Clk Stabilization <sup>1,2</sup>                          | $T_{\text{STABcom}}$         | From $V_{\text{DD}}$ Power-Up to 1st clock (Commercial)          |                       | 1.2      | 1.8                   | ms    | 1,2   |
|                                                           | $T_{\text{STABind}}$         | From $V_{\text{DD}}$ Power-Up to 1st clock (Industrial)          |                       | 1.8      | 3                     | ms    | 1,2   |
| Modulation Frequency                                      | $f_{\text{MOD}}$             | SEL14M_25M# = 0                                                  | 30                    | 31.4     | 33                    | kHz   | 1,3,4 |
| Modulation Frequency                                      | $f_{\text{MOD}}$             | SEL14M_25M# = 1                                                  | 30                    | 31.6     | 33                    | kHz   | 1,3,4 |
| DIF output enable                                         | $t_{\text{DIFOE}}$           | DIF output enable after DIF_Stop# de-assertion                   |                       |          | 15                    | ns    | 1     |
| Input Rise and Fall times                                 | $t_R/t_F$                    | 20% to 80% of VDD                                                |                       |          | 5                     | ns    | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Input frequency should be measured at the REF pin and tuned to 0 PPM to meet ppm frequency accuracy on PLL outputs.

<sup>4</sup>These values assume 25MHz or 14.31818MHz inputs respectively. Using a higher or lower frequency will scale these frequencies accordingly. The output frequency selected by the FS inputs will also scale. For example, 27MHz input with an FS selection of 100MHz will yield an output frequency of  $27/25 \times 100 = 108\text{MHz}$ .

## Electrical Characteristics–DIF 0.7V Current Mode Differential Pair

$T_A = T_{AMBIENT}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\Omega$

| PARAMETER              | SYMBOL               | CONDITIONS                                                                       | MIN     | TYP     | MAX     | UNITS | Notes |
|------------------------|----------------------|----------------------------------------------------------------------------------|---------|---------|---------|-------|-------|
| Voltage High           | VHigh                | Statistical measurement on single ended signal using oscilloscope math function. | 660     | 750     | 850     | mV    | 1     |
| Voltage Low            | VLow                 |                                                                                  | -150    | 3       | 150     |       | 1     |
| Max Voltage            | Vovs                 | Measurement on single ended signal using absolute value.                         |         |         | 1150    | mV    | 1     |
| Min Voltage            | Vuds                 |                                                                                  | -300    |         |         |       | 1     |
| Crossing Voltage (abs) | Vcross(abs)          |                                                                                  | 250     | 336     | 550     | mV    | 1     |
| Crossing Voltage (var) | d-Vcross             | Crossing variation over all edges                                                |         | 40      | 140     | mV    | 1     |
| Long Accuracy          | ppm                  | 14.3M input, SS OFF                                                              | -300    |         | 300     | ppm   | 1,2,5 |
|                        |                      | 14.3M input, SS ON                                                               | -300    |         | 300     | ppm   | 1,2,5 |
|                        |                      | 25M input SS OFF                                                                 | -50     |         | 50      | ppm   | 1,2,5 |
|                        |                      | 25M input, SS ON                                                                 | -300    |         | 300     | ppm   | 1,2,5 |
| Average period         | Tperiod              | 400MHz nominal                                                                   | 2.49988 | 2.5000  | 2.50013 | ns    | 2     |
|                        |                      | 400MHz spread                                                                    | 2.4993  |         | 2.5133  | ns    | 2,3   |
|                        |                      | 333.33MHz nominal                                                                | 2.99985 | 3.0000  | 3.00015 | ns    | 2     |
|                        |                      | 333.33MHz spread                                                                 | 2.9991  |         | 3.016   | ns    | 2,3   |
|                        |                      | 266.66MHz nominal                                                                | 3.74981 | 3.7500  | 3.75019 | ns    | 2     |
|                        |                      | 266.66MHz spread                                                                 | 3.7489  |         | 3.77    | ns    | 2,3   |
|                        |                      | 200MHz nominal                                                                   | 4.9998  | 5.0000  | 5.0003  | ns    | 2     |
|                        |                      | 200MHz spread                                                                    | 4.9985  |         | 5.0266  | ns    | 2,3   |
|                        |                      | 166.66MHz nominal                                                                | 5.9997  | 6.0000  | 6.0003  | ns    | 2     |
|                        |                      | 166.66MHz spread                                                                 | 5.9982  |         | 6.0320  | ns    | 2,3   |
|                        |                      | 133.33MHz nominal                                                                | 7.4996  | 7.5000  | 7.5004  | ns    | 2     |
|                        |                      | 133.33MHz spread                                                                 | 7.4978  |         | 5.4000  | ns    | 2,3   |
|                        |                      | 100.00MHz nominal                                                                | 9.9995  | 10.0000 | 10.0005 | ns    | 2     |
|                        |                      | 100.00MHz spread                                                                 | 9.9970  |         | 10.0533 | ns    | 2,3   |
| Absolute min period    | T <sub>absmin</sub>  | 400MHz nominal/spread                                                            | 2.4143  |         |         | ns    | 1,2   |
|                        |                      | 333.33MHz nominal/spread                                                         | 2.9141  |         |         | ns    | 1,2   |
|                        |                      | 266.66MHz nominal/spread                                                         | 3.6639  |         |         | ns    | 1,2   |
|                        |                      | 200MHz nominal/spread                                                            | 4.8735  |         |         | ns    | 1,2   |
|                        |                      | 166.66MHz nominal/spread                                                         | 5.8732  |         |         | ns    | 1,2   |
|                        |                      | 133.33MHz nominal/spread                                                         | 7.3728  |         |         | ns    | 1,2   |
|                        |                      | 100.00MHz nominal/spread                                                         | 9.8720  |         |         | ns    | 1,2   |
| Rise Time              | t <sub>r</sub>       | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V                               | 175     | 241     | 700     | ps    | 1     |
| Fall Time              | t <sub>f</sub>       | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V                                | 175     | 260     | 700     | ps    | 1     |
| Rise Time Variation    | d-t <sub>r</sub>     |                                                                                  |         | 18      | 125     | ps    | 1     |
| Fall Time Variation    | d-t <sub>f</sub>     |                                                                                  |         | 19      | 125     | ps    | 1     |
| Duty Cycle             | d <sub>t3</sub>      | Measured Differentially                                                          | 45      | 50.0    | 55      | %     | 1     |
| Skew, output to output | t <sub>sk3</sub>     | V <sub>T</sub> = 50%                                                             |         | 21      | 35      | ps    | 1     |
| Jitter, Cycle to cycle | t <sub>jcy-cyc</sub> | Measured Differentially                                                          |         | 17      | 50      | ps    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is tuned to 0 PPM.

<sup>3</sup> Figures are for down spread.

<sup>4</sup> This figure is the peak-to-peak phase jitter as defined by PCI-SIG for a PCI Express reference clock. Please visit <http://www.pcisig.com> for additional details

<sup>5</sup> +/- 50 ppm at any frequency with spread off

## General SMBus Serial Interface Information for ICS9FG104E

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation |           |        |                      |
|-----------------------------|-----------|--------|----------------------|
| Controller (Host)           |           | X Byte | IDT (Slave/Receiver) |
| T                           | starT bit |        |                      |
| Slave Address               |           |        |                      |
| WR                          | WRite     |        |                      |
|                             |           |        | ACK                  |
| Beginning Byte = N          |           |        |                      |
|                             |           |        | ACK                  |
| Data Byte Count = X         |           |        |                      |
|                             |           |        | ACK                  |
| Beginning Byte N            |           |        |                      |
|                             |           |        | ACK                  |
| O                           |           |        |                      |
| O                           |           |        | O                    |
| O                           |           |        | O                    |
|                             |           |        | O                    |
| Byte N + X - 1              |           |        |                      |
|                             |           |        | ACK                  |
| P                           | stoP bit  |        |                      |

| Read Address      | Write Address     |
|-------------------|-------------------|
| DD <sub>(H)</sub> | DC <sub>(H)</sub> |

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |                 |        |                      |
|----------------------------|-----------------|--------|----------------------|
| Controller (Host)          |                 | X Byte | IDT (Slave/Receiver) |
| T                          | starT bit       |        |                      |
| Slave Address              |                 |        |                      |
| WR                         | WRite           |        |                      |
|                            |                 |        | ACK                  |
| Beginning Byte = N         |                 |        |                      |
|                            |                 |        | ACK                  |
| RT                         | Repeat starT    |        |                      |
| Slave Address              |                 |        |                      |
| RD                         | ReaD            |        |                      |
|                            |                 |        | ACK                  |
|                            |                 |        |                      |
|                            |                 |        | Data Byte Count=X    |
| ACK                        |                 |        |                      |
|                            |                 |        | Beginning Byte N     |
| ACK                        |                 |        |                      |
|                            |                 |        | O                    |
| O                          |                 |        | O                    |
| O                          |                 |        | O                    |
| O                          |                 |        |                      |
|                            |                 |        | Byte N + X - 1       |
| N                          | Not acknowledge |        |                      |
| P                          | stoP bit        |        |                      |

SMBus Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

| Byte 0 | Pin # | Name                                                                             | Control Function | Type                                  | 0               | 1 | Default |
|--------|-------|----------------------------------------------------------------------------------|------------------|---------------------------------------|-----------------|---|---------|
| Bit 7  | 17    | FS3 <sup>1</sup>                                                                 | RW               | See Frequency Selection Table, Page 1 |                 |   | Pin 17  |
| Bit 6  | 6     | FS2 <sup>1</sup>                                                                 | RW               |                                       |                 |   | Pin 6   |
| Bit 5  | 24    | FS1 <sup>1</sup>                                                                 | RW               |                                       |                 |   | Pin 24  |
| Bit 4  | 25    | FS0 <sup>1</sup>                                                                 | RW               |                                       |                 |   | Pin 25  |
| Bit 3  | 16    | Spread Enable <sup>1</sup>                                                       | RW               | Off                                   | On              |   | Pin 16  |
| Bit 2  | -     | Enable Software Control of Frequency, Spread Enable (Spread Type always Software | RW               | Hardware Select                       | Software Select |   | 0       |
| Bit 1  |       | DIF_STOP# drive mode                                                             | RW               | Driven                                | Hi-Z            |   | 0       |
| Bit 0  |       | SPREAD TYPE                                                                      | RW               | Down                                  | Center          |   | 0       |

**Notes:**

1. These bits reflect the state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M\_25M# pin.

SMBus Table: Output Enable Register

| Byte 1 | Pin # | Name     | Control Function | Type | 0       | 1      | Default |
|--------|-------|----------|------------------|------|---------|--------|---------|
| Bit 7  | -     | Reserved |                  |      |         |        | 1       |
| Bit 6  | -     | DIF_3 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 5  | -     | DIF_2 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 4  | -     | Reserved |                  |      |         |        | 1       |
| Bit 3  | -     | Reserved |                  |      |         |        | 1       |
| Bit 2  | -     | DIF_1 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 1  | -     | DIF_0 EN | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 0  | -     | Reserved |                  |      |         |        | 1       |

SMBus Table: Output Stop Control Register

| Byte 2 | Pin # | Name          | Control Function      | Type | 0        | 1         | Default |
|--------|-------|---------------|-----------------------|------|----------|-----------|---------|
| Bit 7  | -     | Reserved      |                       |      |          |           | 0       |
| Bit 6  | -     | DIF_3 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 5  | -     | DIF_2 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 4  | -     | Reserved      |                       |      |          |           | 0       |
| Bit 3  | -     | Reserved      |                       |      |          |           | 0       |
| Bit 2  | -     | DIF_1 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 1  | -     | DIF_0 STOP EN | Free Run/ Stop Enable | RW   | Free-run | Stop-able | 0       |
| Bit 0  | -     | Reserved      |                       |      |          |           | 0       |

**SMBus Table: Frequency Select Readback Register**

| Byte 3 | Pin # | Name                              | Control Function | Type | 0                                        | 1  | Default |
|--------|-------|-----------------------------------|------------------|------|------------------------------------------|----|---------|
| Bit 7  | 27    | SEL14M_25M# <sup>1</sup><br>(FS3) | State of pin 17  | R    | See Frequency Selection<br>Table, Page 1 |    | Pin 17  |
| Bit 6  | 6     | FS2 <sup>1</sup>                  | State of pin 6   | R    |                                          |    | Pin 6   |
| Bit 5  | 44    | FS1 <sup>1</sup>                  | State of pin 24  | R    |                                          |    | Pin 24  |
| Bit 4  | 45    | FS0 <sup>1</sup>                  | State of pin 25  | R    |                                          |    | Pin 25  |
| Bit 3  | 16    | SPREAD <sup>1</sup>               | State of pin 26  | R    | Off                                      | On | Pin 16  |
| Bit 2  |       | Reserved                          |                  |      |                                          |    | 0       |
| Bit 1  |       | Reserved                          |                  |      |                                          |    | 0       |
| Bit 0  |       | Reserved                          |                  |      |                                          |    | 0       |

**Notes:**

1. These bits reflect the state of the corresponding pins, regardless of whether software programming is enabled or not.

**SMBus Table: Vendor & Revision ID Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0            | 1 | Default |
|--------|-------|------|------------------|------|--------------|---|---------|
| Bit 7  | -     | RID3 | REVISION ID      | R    | Rev E = 1000 |   | X       |
| Bit 6  | -     | RID2 |                  | R    |              |   | X       |
| Bit 5  | -     | RID1 |                  | R    |              |   | X       |
| Bit 4  | -     | RID0 |                  | R    |              |   | X       |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | -            | - | 0       |
| Bit 2  | -     | VID2 |                  | R    | -            | - | 0       |
| Bit 1  | -     | VID1 |                  | R    | -            | - | 0       |
| Bit 0  | -     | VID0 |                  | R    | -            | - | 1       |

**SMBus Table: DEVICE ID**

| Byte 5 | Pin # | Name | Control Function   | Type | 0 | 1 | Default |
|--------|-------|------|--------------------|------|---|---|---------|
| Bit 7  | -     | DID7 | Device ID = 08 hex | R    | - | - | 0       |
| Bit 6  | -     | DID6 |                    | R    | - | - | 0       |
| Bit 5  | -     | DID5 |                    | R    | - | - | 0       |
| Bit 4  | -     | DID4 |                    | R    | - | - | 0       |
| Bit 3  | -     | DID3 |                    | R    | - | - | 1       |
| Bit 2  | -     | DID2 |                    | R    | - | - | 0       |
| Bit 1  | -     | DID1 |                    | R    | - | - | 0       |
| Bit 0  | -     | DID0 |                    | R    | - | - | 0       |

**SMBus Table: Byte Count Register**

| Byte 6 | Pin # | Name | Control Function                                                                                            | Type | 0 | 1 | Default |
|--------|-------|------|-------------------------------------------------------------------------------------------------------------|------|---|---|---------|
| Bit 7  | -     | BC7  | Writing to this register<br>will configure how many<br>bytes will be read back,<br>default is 07 = 7 bytes. | RW   | - | - | 0       |
| Bit 6  | -     | BC6  |                                                                                                             | RW   | - | - | 0       |
| Bit 5  | -     | BC5  |                                                                                                             | RW   | - | - | 0       |
| Bit 4  | -     | BC4  |                                                                                                             | RW   | - | - | 0       |
| Bit 3  | -     | BC3  |                                                                                                             | RW   | - | - | 0       |
| Bit 2  | -     | BC2  |                                                                                                             | RW   | - | - | 1       |
| Bit 1  | -     | BC1  |                                                                                                             | RW   | - | - | 1       |
| Bit 0  | -     | BC0  |                                                                                                             | RW   | - | - | 1       |

SMBus Table: Reserved Register

| Byte 7 | Pin # | Name     | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---|---|---------|
| Bit 7  | -     | Reserved |                  |      |   |   | 0       |
| Bit 6  | -     | Reserved |                  |      |   |   | 0       |
| Bit 5  | -     | Reserved |                  |      |   |   | 0       |
| Bit 4  | -     | Reserved |                  |      |   |   | 0       |
| Bit 3  | -     | Reserved |                  |      |   |   | 0       |
| Bit 2  | -     | Reserved |                  |      |   |   | 0       |
| Bit 1  | -     | Reserved |                  |      |   |   | 0       |
| Bit 0  | -     | Reserved |                  |      |   |   | 0       |

SMBus Table: Reserved Register

| Byte 8 | Pin # | Name     | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---|---|---------|
| Bit 7  | -     | Reserved |                  |      |   |   | 0       |
| Bit 6  | -     | Reserved |                  |      |   |   | 0       |
| Bit 5  | -     | Reserved |                  |      |   |   | 0       |
| Bit 4  | -     | Reserved |                  |      |   |   | 0       |
| Bit 3  | -     | Reserved |                  |      |   |   | 0       |
| Bit 2  | -     | Reserved |                  |      |   |   | 0       |
| Bit 1  | -     | Reserved |                  |      |   |   | 0       |
| Bit 0  | -     | Reserved |                  |      |   |   | 0       |

SMBus Table: M/N Programming Enable

| Byte 9 | Pin # | Name       | Control Function | Type | 0       | 1      | Default |
|--------|-------|------------|------------------|------|---------|--------|---------|
| Bit 7  | -     | M/N_Enable | M/N Prog. Enable | RW   | Disable | Enable | 0       |
| Bit 6  | -     | Reserved   |                  |      |         |        | 1       |
| Bit 5  | 5     | REFOUT_En  | REFOUT Enable    | RW   | Disable | Enable | 1       |
| Bit 4  | -     | Reserved   |                  |      |         |        | 0       |
| Bit 3  | -     | Reserved   |                  |      |         |        | 0       |
| Bit 2  | -     | Reserved   |                  |      |         |        | 0       |
| Bit 1  | -     | Reserved   |                  |      |         |        | 0       |
| Bit 0  | -     | Reserved   |                  |      |         |        | 0       |

SMBus Table: PLL Frequency Control Register

| Byte 10 | Pin # | Name       | Control Function                | Type | 0                                                                                                                                                                                                                               | 1 | Default |
|---------|-------|------------|---------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---------|
| Bit 7   | -     | PLL N Div8 | N Divider Prog bit 8            | RW   | The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $f_{XTAL} \times \frac{[NDiv(9:0)+8]}{[MDiv(5:0)+2]}$ |   | X       |
| Bit 6   | -     | PLL N Div9 | N Divider Prog bit 9            | RW   |                                                                                                                                                                                                                                 |   | X       |
| Bit 5   | -     | PLL M Div5 | M Divider Programming bit (5:0) | RW   |                                                                                                                                                                                                                                 |   | X       |
| Bit 4   | -     | PLL M Div4 |                                 | RW   |                                                                                                                                                                                                                                 |   | X       |
| Bit 3   | -     | PLL M Div3 |                                 | RW   |                                                                                                                                                                                                                                 |   | X       |
| Bit 2   | -     | PLL M Div2 |                                 | RW   |                                                                                                                                                                                                                                 |   | X       |
| Bit 1   | -     | PLL M Div1 |                                 | RW   |                                                                                                                                                                                                                                 |   | X       |
| Bit 0   | -     | PLL M Div0 |                                 | RW   |                                                                                                                                                                                                                                 |   | X       |

SMBus Table: PLL Frequency Control Register

| Byte 11 | Pin # | Name       | Control Function                                                | Type | 0                                                                                                                                                                                                                                                | 1 | Default |
|---------|-------|------------|-----------------------------------------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---------|
| Bit 7   | -     | PLL N Div7 | N Divider Programming<br>Byte11 bit(7:0) and<br>Byte10 bit(7:6) | RW   | The decimal representation<br>of M and N Divider in Byte<br>11 and 12 will configure the<br>PLL VCO frequency. Default<br>at power up = latch-in or<br>Byte 0 Rom table. VCO<br>Frequency = $f_{XTAL} \times$<br>$[NDiv(9:0)+8] / [MDiv(5:0)+2]$ |   | X       |
| Bit 6   | -     | PLL N Div6 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |
| Bit 5   | -     | PLL N Div5 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |
| Bit 4   | -     | PLL N Div4 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |
| Bit 3   | -     | PLL N Div3 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |
| Bit 2   | -     | PLL N Div2 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |
| Bit 1   | -     | PLL N Div1 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |
| Bit 0   | -     | PLL N Div0 |                                                                 | RW   |                                                                                                                                                                                                                                                  |   | X       |

SMBus Table: PLL Spread Spectrum Control Register

| Byte 12 | Pin # | Name     | Control Function                        | Type | 0                                                                                               | 1 | Default |
|---------|-------|----------|-----------------------------------------|------|-------------------------------------------------------------------------------------------------|---|---------|
| Bit 7   | -     | PLL SSP7 | Spread Spectrum<br>Programming bit(7:0) | RW   | These Spread Spectrum bits<br>in Byte 13 and 14 will<br>program the spread<br>percentage of PLL |   | X       |
| Bit 6   | -     | PLL SSP6 |                                         | RW   |                                                                                                 |   | X       |
| Bit 5   | -     | PLL SSP5 |                                         | RW   |                                                                                                 |   | X       |
| Bit 4   | -     | PLL SSP4 |                                         | RW   |                                                                                                 |   | X       |
| Bit 3   | -     | PLL SSP3 |                                         | RW   |                                                                                                 |   | X       |
| Bit 2   | -     | PLL SSP2 |                                         | RW   |                                                                                                 |   | X       |
| Bit 1   | -     | PLL SSP1 |                                         | RW   |                                                                                                 |   | X       |
| Bit 0   | -     | PLL SSP0 |                                         | RW   |                                                                                                 |   | X       |

SMBus Table: PLL Spread Spectrum Control Register

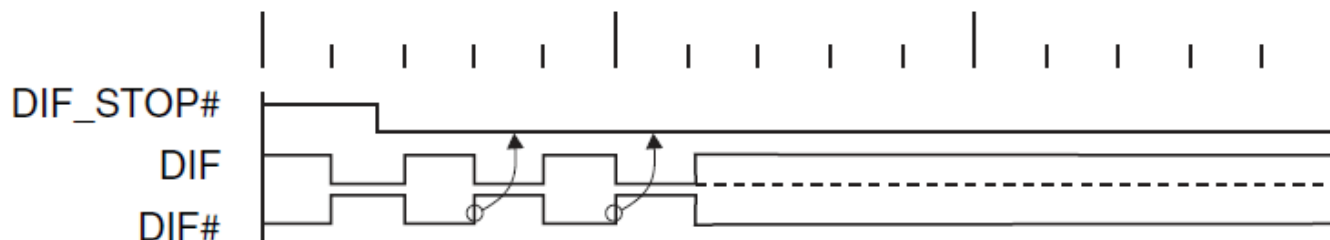
| Byte 13 | Pin # | Name      | Control Function                         | Type | 0                                                                                               | 1 | Default |
|---------|-------|-----------|------------------------------------------|------|-------------------------------------------------------------------------------------------------|---|---------|
| Bit 7   | -     | Reserved  |                                          |      |                                                                                                 |   | 0       |
| Bit 6   | -     | PLL SSP14 | Spread Spectrum<br>Programming bit(14:8) | RW   | These Spread Spectrum bits<br>in Byte 13 and 14 will<br>program the spread<br>percentage of PLL |   | X       |
| Bit 5   | -     | PLL SSP13 |                                          | RW   |                                                                                                 |   | X       |
| Bit 4   | -     | PLL SSP12 |                                          | RW   |                                                                                                 |   | X       |
| Bit 3   | -     | PLL SSP11 |                                          | RW   |                                                                                                 |   | X       |
| Bit 2   | -     | PLL SSP10 |                                          | RW   |                                                                                                 |   | X       |
| Bit 1   | -     | PLL SSP9  |                                          | RW   |                                                                                                 |   | X       |
| Bit 0   | -     | PLL SSP8  |                                          | RW   |                                                                                                 |   | X       |

SMBus Table: Reserved Test Register

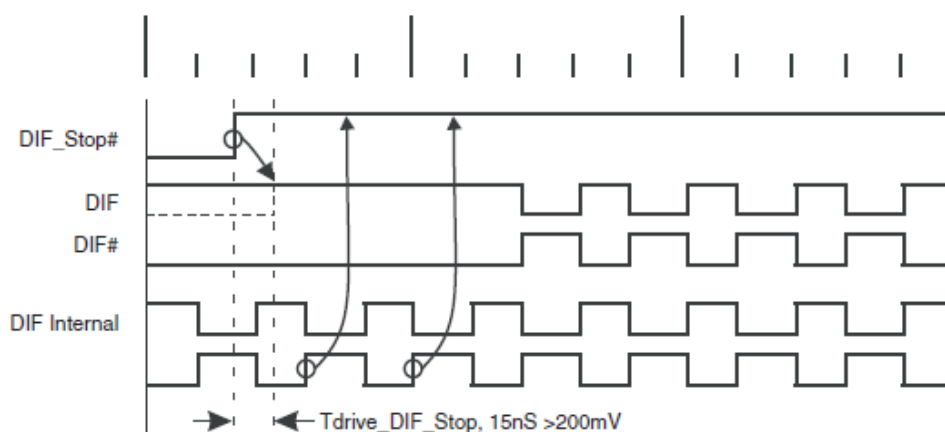
| Byte 14 | Pin # | Name                                                                                       | Control Function | Type | 0 | 1 | Default |
|---------|-------|--------------------------------------------------------------------------------------------|------------------|------|---|---|---------|
| Bit 7   | -     | Reserved Test Register. Do not write to this register, erratic device operation may occur. |                  |      |   |   | 1       |
| Bit 6   | -     |                                                                                            |                  |      |   |   | 0       |
| Bit 5   | -     |                                                                                            |                  |      |   |   | 0       |
| Bit 4   | -     |                                                                                            |                  |      |   |   | 0       |
| Bit 3   | -     |                                                                                            |                  |      |   |   | 0       |
| Bit 2   | -     |                                                                                            |                  |      |   |   | 0       |
| Bit 1   | -     |                                                                                            |                  |      |   |   | 0       |
| Bit 0   | -     |                                                                                            |                  |      |   |   | 0       |

**DIF\_STOP# - Assertion (transition from '1' to '0')**

Asserting DIF\_STOP# pin stops all DIF outputs that are set to be stoppable after their next transition. When the SMBus DIF\_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '0', DIF output will stop DIF\_True = HIGH and DIF\_Complement = LOW. When the SMBus DIF\_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '1', DIF outputs will be tri-stated.

**DIF\_STOP# - De-assertion (transition from '0' to '1')**

With the de-assertion of DIF\_STOP# all stopped DIF outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is 2 - 6 DIF clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped DIF outputs will be driven High within 15nS of DIF\_Stop# de-assertion to a voltage greater than 200mV.



| DIF Reference Clock                             |  |                    |      |
|-------------------------------------------------|--|--------------------|------|
| Common Recommendations for Differential Routing |  | Dimension or Value | Unit |
| L1 length, route as non-coupled 50ohm trace     |  | 0.5 max            | inch |
| L2 length, route as non-coupled 50ohm trace     |  | 0.2 max            | inch |
| L3 length, route as non-coupled 50ohm trace     |  | 0.2 max            | inch |
| Rs                                              |  | 33                 | ohm  |
| Rt                                              |  | 49.9               | ohm  |

| Down Device Differential Routing                                 |  | Dimension or Value  | Unit |
|------------------------------------------------------------------|--|---------------------|------|
| L4 length, route as coupled microstrip 100ohm differential trace |  | 2 min to 16 max     | inch |
| L4 length, route as coupled stripline 100ohm differential trace  |  | 1.8 min to 14.4 max | inch |

| Differential Routing to PCI Express Connector                    |  | Dimension or Value    | Unit |
|------------------------------------------------------------------|--|-----------------------|------|
| L4 length, route as coupled microstrip 100ohm differential trace |  | 0.25 to 14 max        | inch |
| L4 length, route as coupled stripline 100ohm differential trace  |  | 0.225 min to 12.6 max | inch |

Figure 1: Down Device Routing

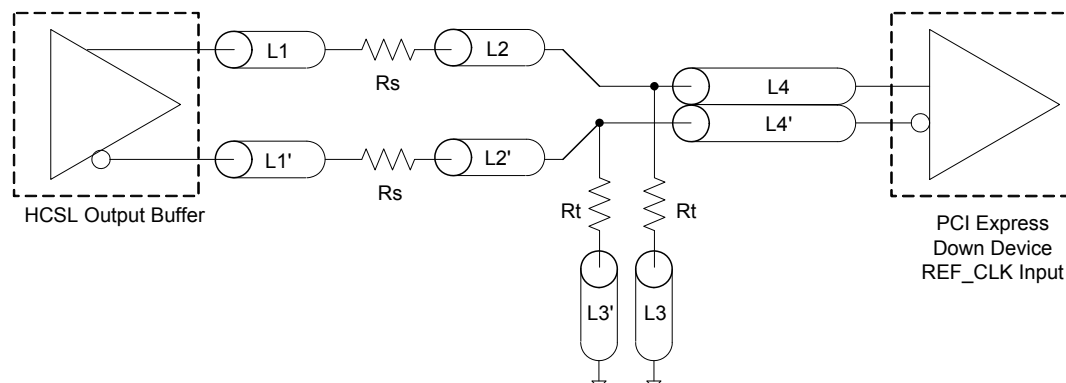
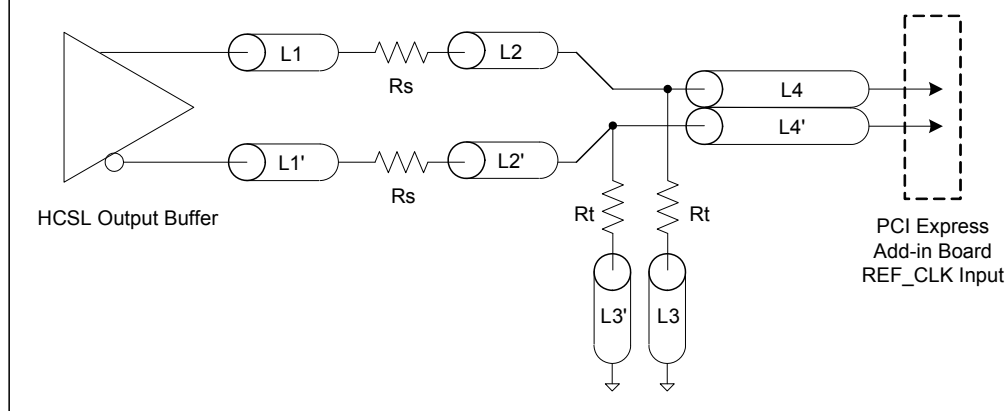
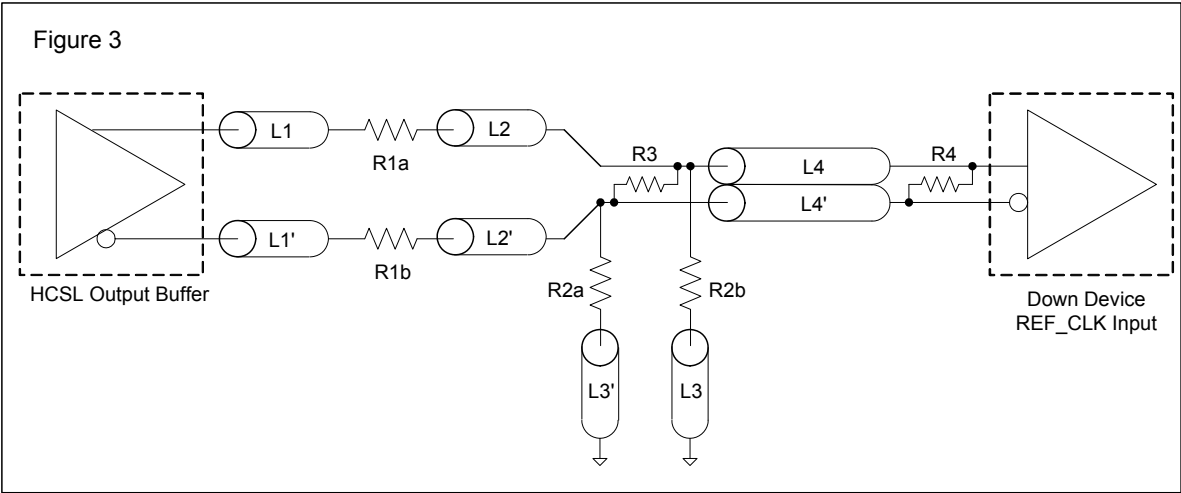


Figure 2: PCI Express Connector Routing

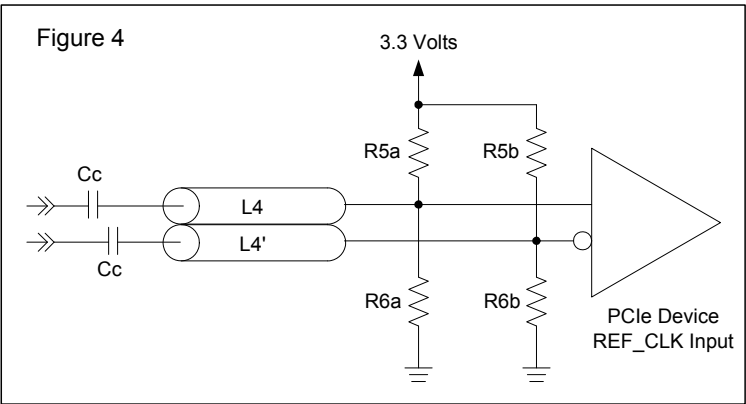


| Alternative Termination for LVDS and other Common Differential Signals (figure 3) |       |      |    |      |      |     |                                |
|-----------------------------------------------------------------------------------|-------|------|----|------|------|-----|--------------------------------|
| Vdiff                                                                             | Vp-p  | Vcm  | R1 | R2   | R3   | R4  | Note                           |
| 0.45v                                                                             | 0.22v | 1.08 | 33 | 150  | 100  | 100 |                                |
| 0.58                                                                              | 0.28  | 0.6  | 33 | 78.7 | 137  | 100 |                                |
| 0.80                                                                              | 0.40  | 0.6  | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60                                                                              | 0.3   | 1.2  | 33 | 174  | 140  | 100 | Standard LVDS                  |

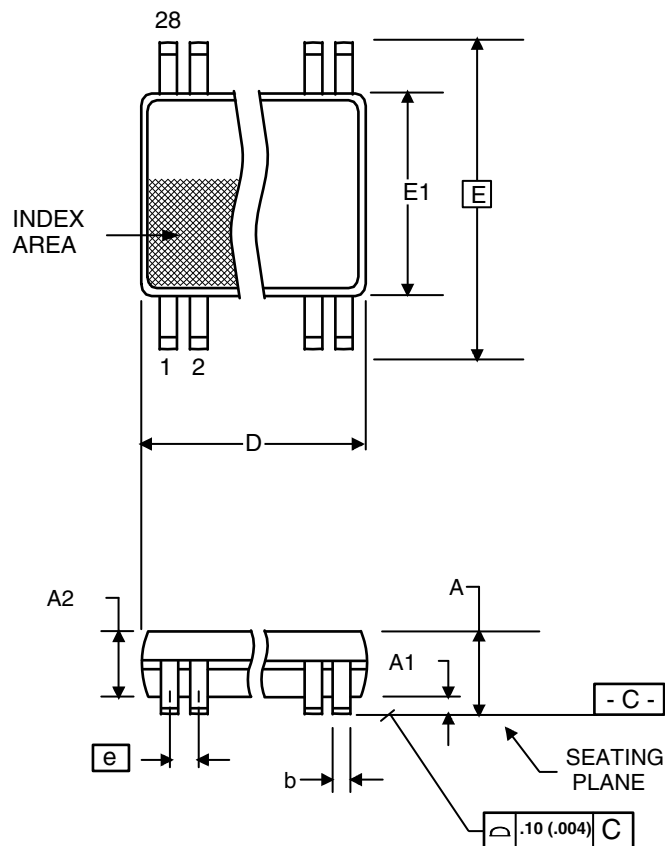
R1a = R1b = R1  
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) |             |      |
|---------------------------------------------------|-------------|------|
| Component                                         | Value       | Note |
| R5a, R5b                                          | 8.2K 5%     |      |
| R6a, R6b                                          | 1K 5%       |      |
| Cc                                                | 0.1 $\mu$ F |      |
| Vcm                                               | 0.350 volts |      |



## Package Outline and Package Dimensions (28-SSOP)



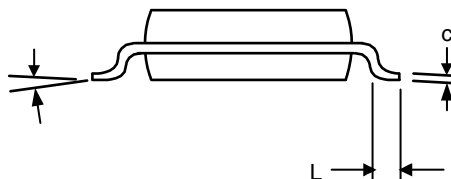
209 mil SSOP

| SYMBOL   | In Millimeters    |      | In Inches         |      |
|----------|-------------------|------|-------------------|------|
|          | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|          | MIN               | MAX  | MIN               | MAX  |
| A        | --                | 2.00 | --                | .079 |
| A1       | 0.05              | --   | .002              | --   |
| A2       | 1.65              | 1.85 | .065              | .073 |
| b        | 0.22              | 0.38 | .009              | .015 |
| c        | 0.09              | 0.25 | .0035             | .010 |
| D        | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| E        | 7.40              | 8.20 | .291              | .323 |
| E1       | 5.00              | 5.60 | .197              | .220 |
| e        | 0.65 BASIC        |      | 0.0256 BASIC      |      |
| L        | 0.55              | 0.95 | .022              | .037 |
| N        | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| $\alpha$ | 0°                | 8°   | 0°                | 8°   |

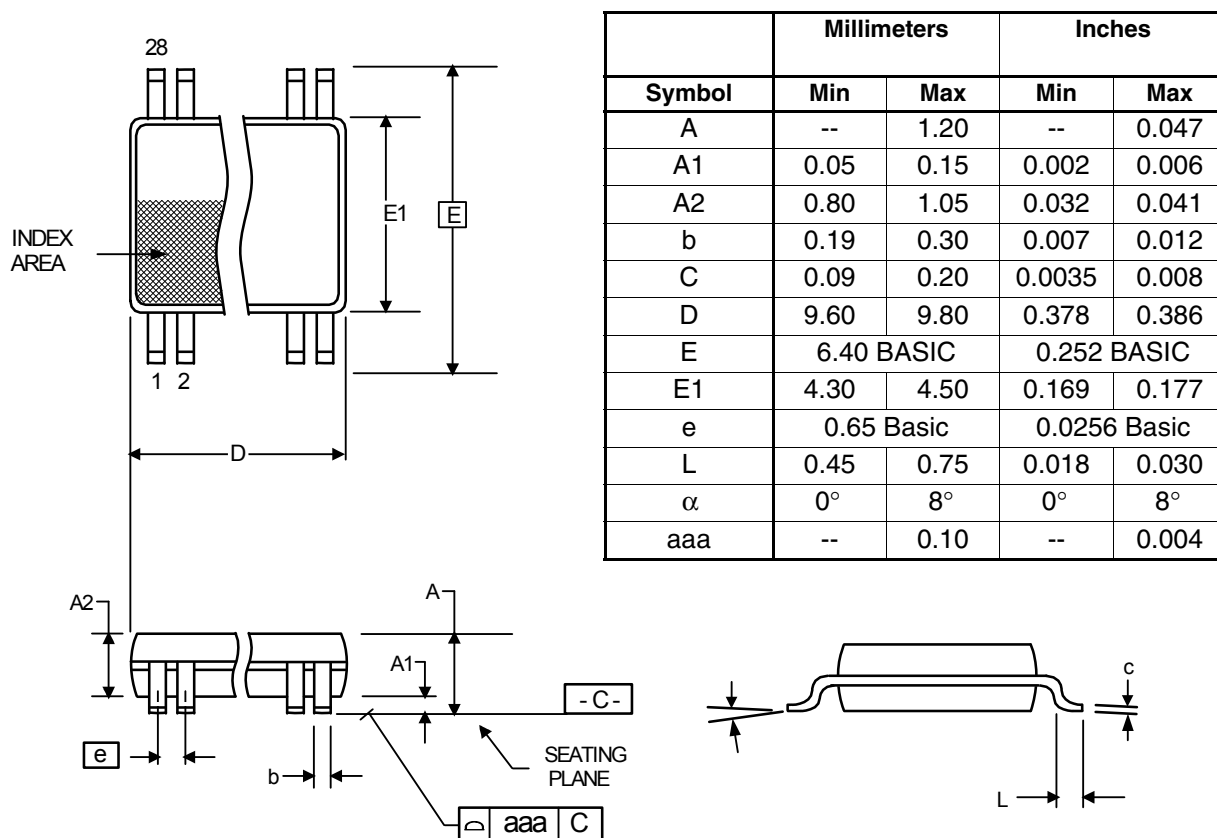
VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 28 | 9.90  | 10.50 | .390     | .413 |

Reference Doc.: JEDEC Publication 95, MO-150



## Package Outline and Package Dimensions (28-TSSOP)



## Ordering Information

| Part/Order Number | Shipping Packaging | Package      | Temperature  |
|-------------------|--------------------|--------------|--------------|
| 9FG104EFLF        | Tubes              | 28-pin SSOP  | 0 to +70°C   |
| 9FG104EFLFT       | Tape and Reel      | 28-pin SSOP  | 0 to +70°C   |
| 9FG104EFILF       | Tubes              | 28-pin SSOP  | -40 to +85°C |
| 9FG104EFILFT      | Tape and Reel      | 28-pin SSOP  | -40 to +85°C |
| 9FG104EGLF        | Tubes              | 28-pin TSSOP | 0 to +70°C   |
| 9FG104EGLFT       | Tape and Reel      | 28-pin TSSOP | 0 to +70°C   |
| 9FG104EGILF       | Tubes              | 28-pin TSSOP | -40 to +85°C |
| 9FG104EGILFT      | Tape and Reel      | 28-pin TSSOP | -40 to +85°C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"E" is the device revision designator (will not correlate with the datasheet revision).

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**Revision History**

| Rev. | Issue Date | Issuer | Description                                                                                                                                                                                                                                                                                                                                              | Page # |
|------|------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| A    | 6/21/2012  | RDW    | Moved from Advance to final                                                                                                                                                                                                                                                                                                                              |        |
| B    | 10/11/2012 | RDW    | Electrical Tables updated to harmonize with the 9FG108E                                                                                                                                                                                                                                                                                                  |        |
| C    | 10/23/2012 | AT     | Correct typo on front page for output-to-output skew. Should be 35ps, not 65ps. Electrical table spec is correct and shows the 35ps value.                                                                                                                                                                                                               | 1      |
| D    | 10/29/2012 | AT     | Update the Jitter parameters in the table "Electrical Characteristics – REF 14.318/25MHz" to distinguish between commercial and industrial conditions. Added a separate line for each condition. For commercial, values were changed from 87ps Min & 250ps Max to 87ps Min & 200ps Max. For industrial, values are kept the same – 87ps Min & 250ps Max. | 4      |

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