19-3936; Rev 0; 2/06

16-Bit, Parallel-Input, Voltage-Output DACs with Internal Reference

General Description

The MAX5650/MAX5651/MAX5652 parallel-input, voltage-output, 16-bit, digital-to-analog converters (DACs) provide monotonic 16-bit output voltage over the full extended operating temperature range. The MAX5650/MAX5651 include an internal precision low drift (10ppm/°C) bandgap voltage reference, while the MAX5652 requires an external reference. The MAX5650 operates from a +5V single supply and has a +4.096V internal reference. The MAX5651 operates from either a +3V or +5V single supply and has a +2.048V internal reference. The MAX5652 operates from either a +3V or +5V single supply and accepts an input reference voltage between +2V and AV_{DD}. TheMAX5650/MAX5651/MAX5652 parallel inputs are double buffered and configurable as a single 16-bit wide input or a 2-byte input. The MAX5650/MAX5651/MAX5652 unbuffered DAC voltage output ranges from 0 to V_{REF}.

The MAX5650/MAX5651/MAX5652 feature an active-low hardware clear input ($\overline{CLR}$) that clears the registers and the output to zero-scale (0000 hex) or midscale (8000 hex), depending on the state of the MID/$\overline{ZERO}$ input. These devices include matched scaling resistors for use with a precision external op amp (such as the MAX400) to generate a bipolar output-voltage swing.

The MAX5650/MAX5651/MAX5652 are available in a 32-pin, 5mm x 5mm TQFN package and are guaranteed over the extended temperature range (-40°C to +85°C).

For 14-bit, pin-compatible versions of the MAX5650/MAX5651/MAX5652, refer to the MAX5653/MAX5654/MAX5655 datasheet.

For 12-bit, pin-compatible versions of the MAX5650/MAX5651/MAX5652, refer to the MAX5656/MAX5657/MAX5658 datasheet.

Applications

- Automatic Test Equipment
- Process Control
- Digital Calibration
- Actuator Control
- Servo Loops
- Waveform Generators
- Motor Control

Selector Guide

PART	SUPPLY VOLTAGE (V)	REFERENCE (V)	INL (LSB, max)
MAX5650ETJ	+4.75 to +5.25	Internal, +4.096	±4
MAX5651ETJ	+2.7 to +5.25	Internal, +2.048	—
MAX5652ETJ	+2.7 to +5.25	External	—

Pin Configuration appears at end of data sheet.

Features

- ♦ **16-Bit Resolution**
- ♦ **Parallel 16-Bit or 2-Byte Double Buffered Interface**
- ♦ **Guaranteed Monotonic**
- ♦ **Maximum INL: ±4 LSB**
- ♦ **Fast 2µs Settling Time**
- ♦ **Clear Input ($\overline{CLR}$) Sets Output to Zero-Scale or Midscale**
- ♦ **Integrated Precision Resistors for Bipolar Operation**
- ♦ **Integrated Precision Bandgap Reference:**
  - **+4.096V (MAX5650)**
  - **+2.048V (MAX5651)**

Ordering Information

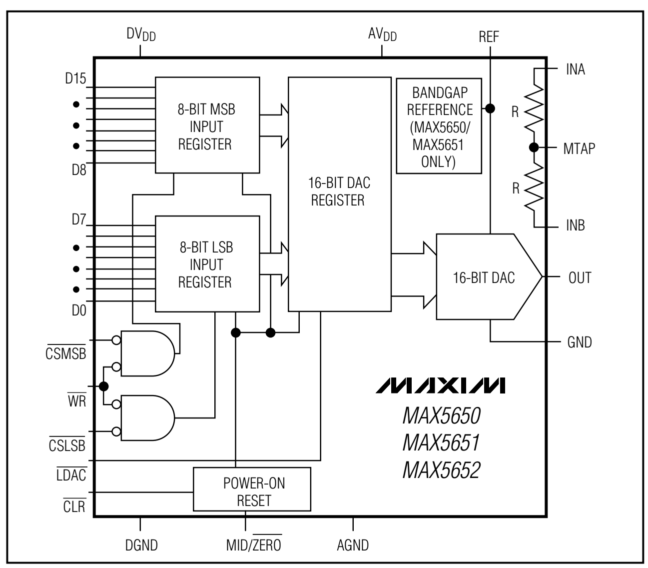
PART	PIN-PACKAGE	PACKAGE CODE
MAX5650ETJ	32 TQFN-EP* (5mm x 5mm)	T3255-4
MAX5651ETJ**	32 TQFN-EP* (5mm x 5mm)	T3255-4
MAX5652ETJ**	32 TQFN-EP* (5mm x 5mm)	T3255-4

Note: All devices specified over the -40°C to +85°C temperature range.

**EP = Exposed paddle. Connect to AGND or leave unconnected.*

***Future product—contact factory for availability.*

Functional Diagram



16-Bit, Parallel-Input, Voltage-Output DACs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to DV_{DD} ....±6V
AV_{DD} to AGND, GND .... -0.3V to +6V
DV_{DD} to DGND .... -0.3V to +6V
DGND to GND .... -0.3V to +0.3V
DGND, GND to AGND .... -0.3V to +0.3V
D0–D15, $\overline{CSLSB}$, $\overline{CSMSB}$, $\overline{WR}$, $\overline{LDAC}$, $\overline{CLR}$, MID/$\overline{ZERO}$,
to DGND ....-0.3V to (DV_{DD} + 0.3V)
REF to AGND ....-0.3V to (AV_{DD} + 0.3V)
OUT, MTAP, INA to AGND, GND ....-0.3V to AV_{DD}
INB to AGND ....-6V to +6V
INB to MTAP ....-6V to +6V
Maximum Current into Any Pin ....±50mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 20.8mW/°C above +70°C)....2758.6mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5650

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, AGND = DGND = GND = 0V, V_{REF} = internal, R_L = ∞, C_L = 10pF, C_{REF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		16			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic		±0.5	±1	LSB
Integral Nonlinearity	INL				±4	LSB
Zero-Code Offset Error	ZSE				±80	µV
Zero-Code Temperature Coefficient	ZSTC	(Note 2)		±0.05		ppmFS/°C
Gain Error		(Note 3)			±10	LSB
Gain-Error Temperature Coefficient		(Note 2)		±0.1		ppm/°C
DAC Output Resistance	R_{OUT}	(Note 4)		6.2		kΩ
Bipolar Resistor Ratio		R_{INB} / R_{INA}		1		Ω/Ω
Bipolar Resistor Ratio Error					±0.05	%
Bipolar Resistor Ratio Temperature Coefficient		(Note 2)		±0.5		ppm/°C
Bipolar Resistor Value		R_{INB} and R_{INA} (Note 4)		12.4		kΩ
VOLTAGE REFERENCE (R_{REF} = 10kΩ, $C_{REF(MIN)}$ = 1µF)						
Voltage Reference	V_{REF}	T_A = +25°C	4.081	4.106	4.111	V
Reference Voltage Temperature Coefficient	TCV_{REF}	(Note 2)		10		ppm/°C
Reference Load Regulation	V_{OUT} / I_{OUT}	0 ≤ I_{OUT} ≤ V_{REF} / 10kΩ		0.1	0.6	µV/µA
Short-Circuit Current				6		mA
Reference Load	I_{REF}				400	µA
Reference Power-Up Time		Settle to 0.5 LSB		4		ms
Power-Supply Rejection Ratio	PSRR	AV_{DD} = DV_{DD} = 4.75V to 5.25V (FS code)			0.5	mV/V

ELECTRICAL CHARACTERISTICS—MAX5650 (continued)

($AV_{DD} = DV_{DD}$ = +4.75V to +5.25V, AGND = DGND = GND = 0V, V_{REF} = internal, $R_L = \infty$, C_L = 10pF, C_{REF} = 1µF, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE—ANALOG SECTION						
Output Settling Time		7F60H to 80A0H or 80A0H to 7F60H to 0.5 LSB		2		µs
DAC Glitch Impulse		Major carry transition		10		nV·s
Digital Feedthrough		Code = 0000 hex; $\overline{CSLSB}$ = $\overline{CSMSB}$ = DV_{DD}, D0–D15 transition from 0 to DV_{DD}		3		nV·s
DYNAMIC PERFORMANCE—VOLTAGE REFERENCE SECTION						
Noise Voltage (Note 6)		Frequency = 0.1Hz to 10Hz		15		$µV_{P-P}$
		Frequency = 10Hz to 1kHz		12		$µV_{RMS}$
V_{REF} Glitch Impulse		For zero-scale to full-scale or full-scale to zero-scale transition		10		nV·s
STATIC PERFORMANCE—DIGITAL INPUTS						
Input High Voltage	V_{IH}	(Note 8)	2.4			V
Input Low Voltage	V_{IL}	(Note 8)			0.8	V
Input Current	I_{IN}				±1	µA
Input Capacitance	C_{IN}			5		pF
POWER SUPPLY						
Analog Supply Range	AV_{DD}		4.75		5.25	V
Digital Supply Range	DV_{DD}	(Note 9)	AV_{DD} - 0.3		AV_{DD} + 0.3	V
Positive Supply Current	I_{AVDD} + I_{DVDD}	All digital inputs at DV_{DD} or 0V, $AV_{DD} = DV_{DD}$			2	mA
TIMING CHARACTERISTICS (Figure 4)						
$\overline{CSMSB}$ and $\overline{CSLSB}$ Pulse Width	t_{CS}		40			ns
$\overline{WR}$ Pulse Width	t_{WR}		40			ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time	t_{CWS}		0			ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time	t_{CWH}		0			ns
Data Valid to $\overline{WR}$ Setup Time	t_{DWS}		40			ns
Data Valid to $\overline{WR}$ Hold Time	t_{DWH}		0			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}		40			ns
$\overline{CLR}$ Pulse Width	t_{CLR}		40			ns

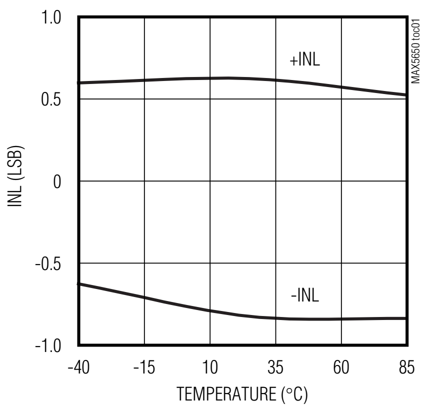
Note 1: 100% production tested at T_A = +25°C and T_A = +85°C. Guaranteed by design at T_A = -40°C.
Note 2: Temperature coefficient is determined by the box method in which the maximum change over the temperature range is divided by ΔT.
Note 3: Gain error is measured at the full-scale code and is calculated with respect to the reference voltage (REF).
Note 4: Resistor tolerance is typically ±20%.
Note 5: Guaranteed by design, not production tested.
Note 6: Noise is measured at the reference output.
Note 7: Min/max range guaranteed by gain-error test. Operation outside min/max limits results in degraded performance.
Note 8: The devices draw higher supply current when the digital inputs are driven between (DV_{DD} - 0.5V) and (DGND + 0.5V). See Digital Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.
Note 9: For optimal performance $AV_{DD} = DV_{DD}$.

16-Bit, Parallel-Input, Voltage-Output DACs with Internal Reference

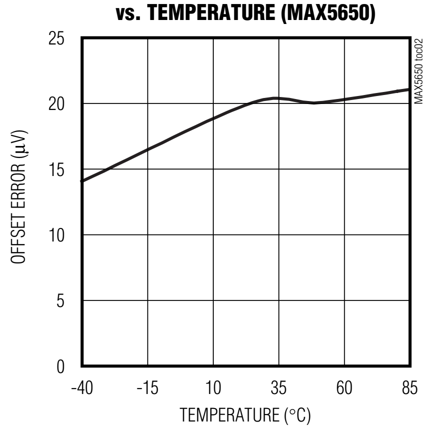
Typical Operating Characteristics

($AV_{DD} = DV_{DD} = +5V$, AGND = DGND = GND = 0V, $R_L = \infty$, $C_L = 10pF$, $C_{REF} = 1\mu F$ for the MAX5650/MAX5651, $T_A = +25°C$, unless otherwise noted.)

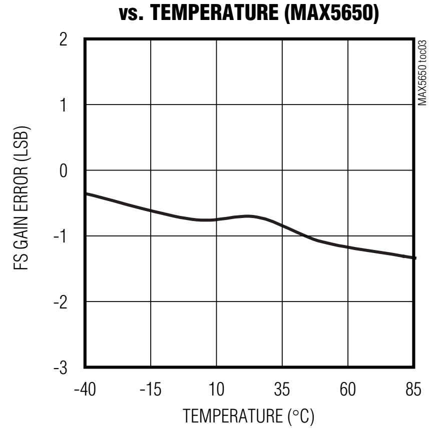
INTEGRAL NONLINEARITY vs. TEMPERATURE



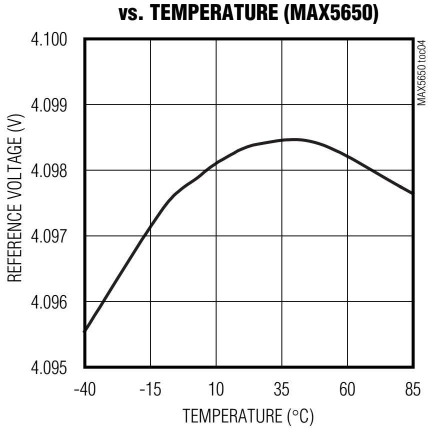
ZERO-CODE OFFSET ERROR vs. TEMPERATURE (MAX5650)



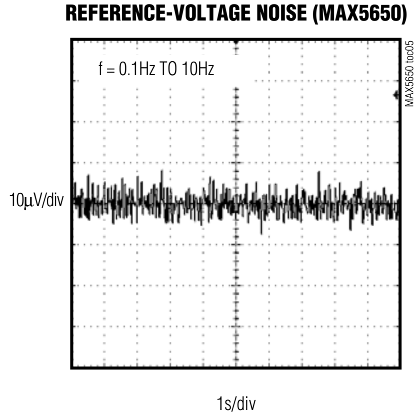
GAIN ERROR vs. TEMPERATURE (MAX5650)



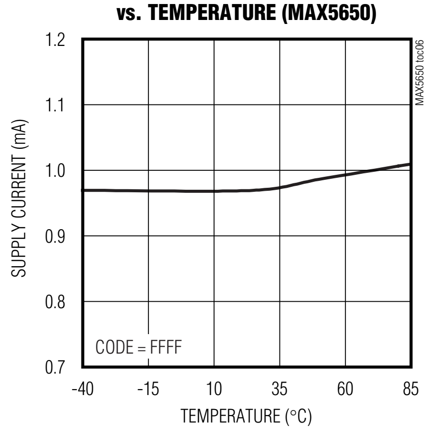
REFERENCE VOLTAGE vs. TEMPERATURE (MAX5650)



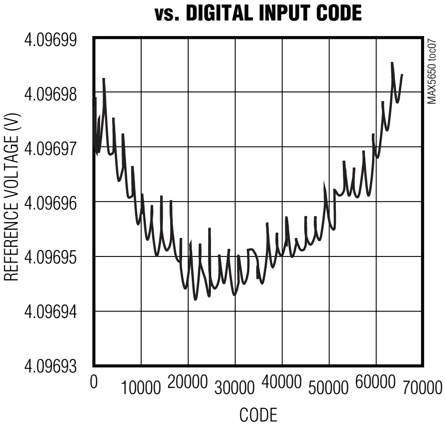
REFERENCE-VOLTAGE NOISE (MAX5650)



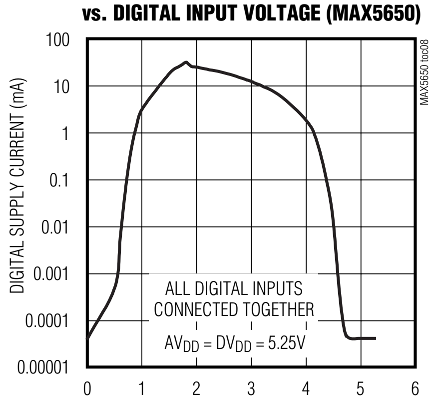
TOTAL SUPPLY CURRENT vs. TEMPERATURE (MAX5650)



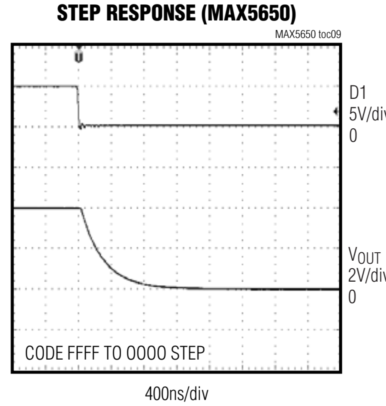
REFERENCE VOLTAGE vs. DIGITAL INPUT CODE



DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE (MAX5650)



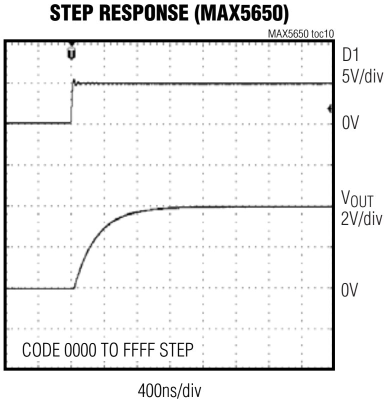
FULL-SCALE STEP RESPONSE (MAX5650)



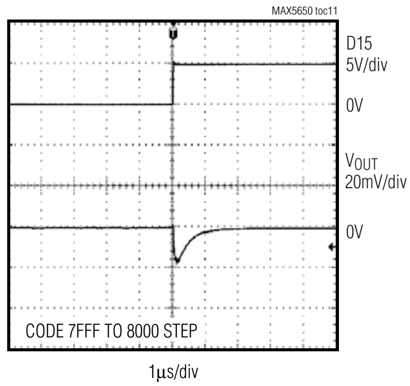
Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD}$ = +5V, AGND = DGND = GND = 0V, $R_L = \infty$, C_L = 10pF, C_{REF} = 1µF for the MAX5650/MAX5651, T_A = +25°C, unless otherwise noted.)

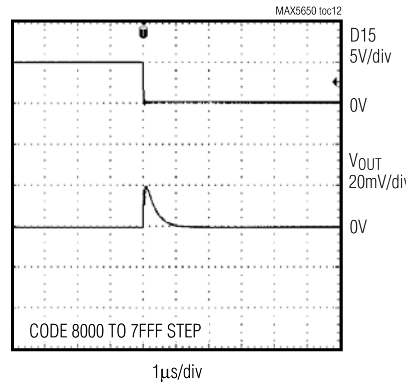
FULL-SCALE STEP RESPONSE (MAX5650)



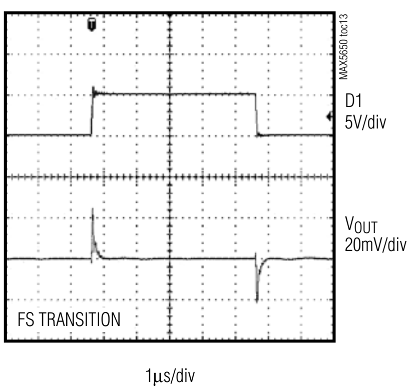
MAJOR-CARRY GLITCH



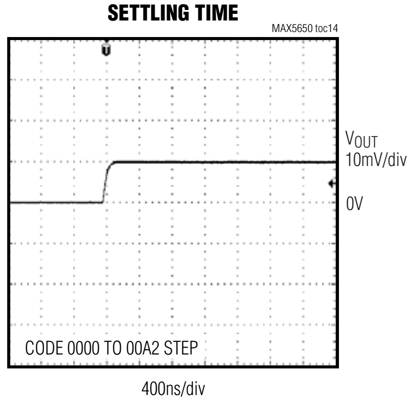
MAJOR-CARRY GLITCH



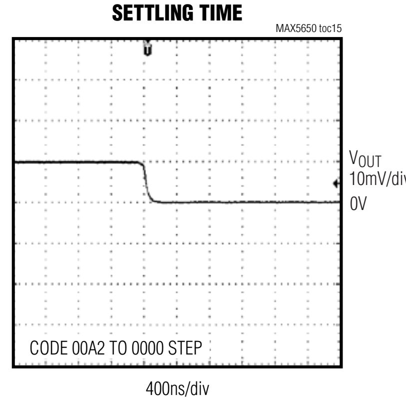
DIGITAL FEEDTHROUGH (MAX5650)



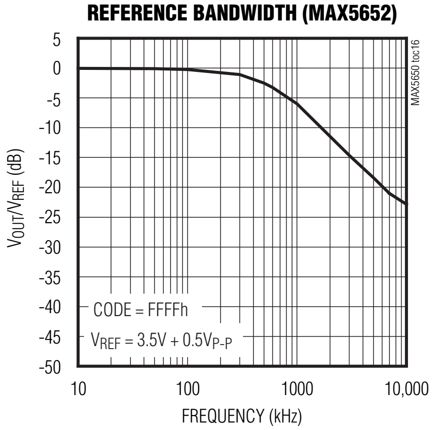
SMALL-SIGNAL SETTLING TIME



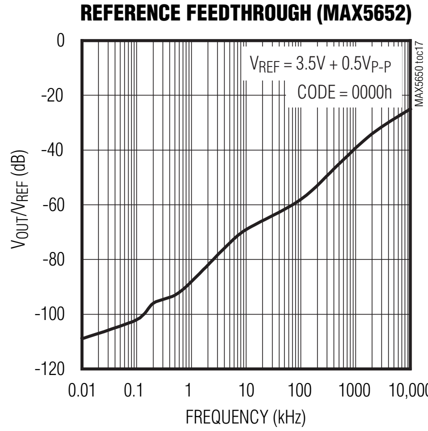
SMALL-SIGNAL SETTLING TIME



REFERENCE BANDWIDTH (MAX5652)



REFERENCE FEEDTHROUGH (MAX5652)



Pin Description

PIN	NAME	FUNCTION
1	D0	Data Input Bit 0 (LSB)
2	D1	Data Input Bit 1
3	D2	Data Input Bit 2
4	D3	Data Input Bit 3
5	D4	Data Input Bit 4
6	D5	Data Input Bit 5
7	D6	Data Input Bit 6
8	D7	Data Input Bit 7
9	D8	Data Input Bit 8
10	D9	Data Input Bit 9
11	D10	Data Input Bit 10
12	D11	Data Input Bit 11
13	D12	Data Input Bit 12
14	D13	Data Input Bit 13
15	D14	Data Input Bit 14
16	D15	Data Input Bit 15 (MSB)
17	DGND	Digital Ground
18	DV_{DD}	Digital Supply. Bypass DV_{DD} to DGND with a 0.1µF capacitor as close to the device as possible.
19	$\overline{CSLSB}$	Lower 8-Bit Active-Low Chip Select. When $\overline{CSLSB}$ is driven low the data inputs D0–D7 are loaded to the input and DAC registers depending on the state of $\overline{WR}$ and $\overline{LDAC}$ (see Table 1).
20	$\overline{CSMSB}$	Upper 8-Bit Active-Low Chip Select. When $\overline{CSMSB}$ is driven low the data inputs D8–D15 are loaded to the input and DAC registers depending on the state of $\overline{WR}$ and $\overline{LDAC}$ (see Table 1).
21	$\overline{WR}$	Active-Low Write Input. While chip select ($\overline{CSLSB}$ and/or $\overline{CSMSB}$) is low, the data on D0–D7 and/or D8–D15 is presented to the input register when $\overline{WR}$ is low. A rising edge on $\overline{WR}$ then latches the data to the input register (see Table 1). Hold $\overline{WR}$ low to make the input register transparent.
22	$\overline{LDAC}$	Asynchronous Active-Low Load DAC Input. When $\overline{LDAC}$ is low, the data in the input register is presented to the DAC register. A rising edge on $\overline{LDAC}$ then latches the data to the DAC register (see Table 1). Hold $\overline{WR}$ and $\overline{LDAC}$ low to perform a write-through operation.
23	$\overline{CLR}$	Asynchronous Active-Low Clear DAC Input. Pull $\overline{CLR}$ low to clear the input and DAC registers and set the DAC output to midscale (8000 hex), if MID/$\overline{ZERO}$ is high, or zero scale (0000 hex), if MID/$\overline{ZERO}$ is low.
24	MID/$\overline{ZERO}$	Midscale/Zero-Scale Clear Output Value Select. Pull MID/$\overline{ZERO}$ low for zero-scale clear output (0000 hex) or high for midscale clear output (8000 hex).
25	MTAP	Internal Scaling Resistor Midpoint Tap. Connect to the inverting input of an external op amp.
26	INB	Internal Resistor Input B. Free end of internal resistor (R_{INB}). Connect to the output of an external output buffer for bipolar operation.
27	AV_{DD}	Analog Supply. Bypass AV_{DD} to AGND with a 0.1µF capacitor as close to the device as possible.
28	AGND	Analog Ground
29	INA	Internal Resistor Input A. Free end of internal resistor (R_{INA}). Connect to REF for bipolar operation.

Pin Description (continued)

PIN	NAME	FUNCTION
30	REF	Internal Reference Voltage Output (MAX5650/MAX5651). Connect a 1µF < C_{REF} < 47µF between REF and AGND as close to the device as possible. The internal reference voltage of the MAX5650 is +4.096V and +2.048V for the MAX5651.
		External Reference Voltage Input (MAX5652). Connect to an external voltage reference source between +2V and AV_{DD}.
31	OUT	DAC Output
32	GND	DAC Ground
—	EP	Exposed paddle. Connect to AGND or leave unconnected.

Typical Application Circuits

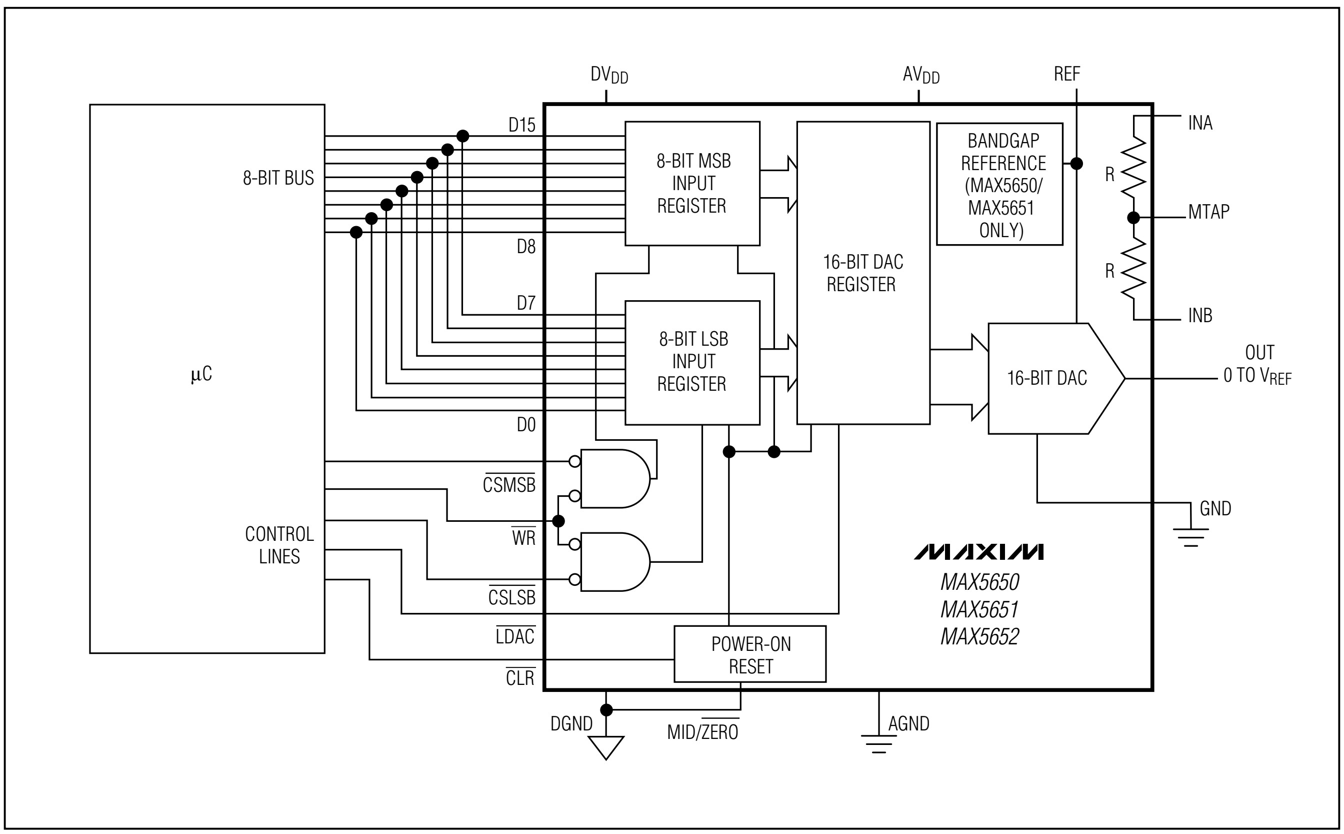


Figure 1. Typical Application Circuit for µC Byte-Wide Interface

16-Bit, Parallel-Input, Voltage-Output DACs with Internal Reference

Typical Application Circuits (continued)

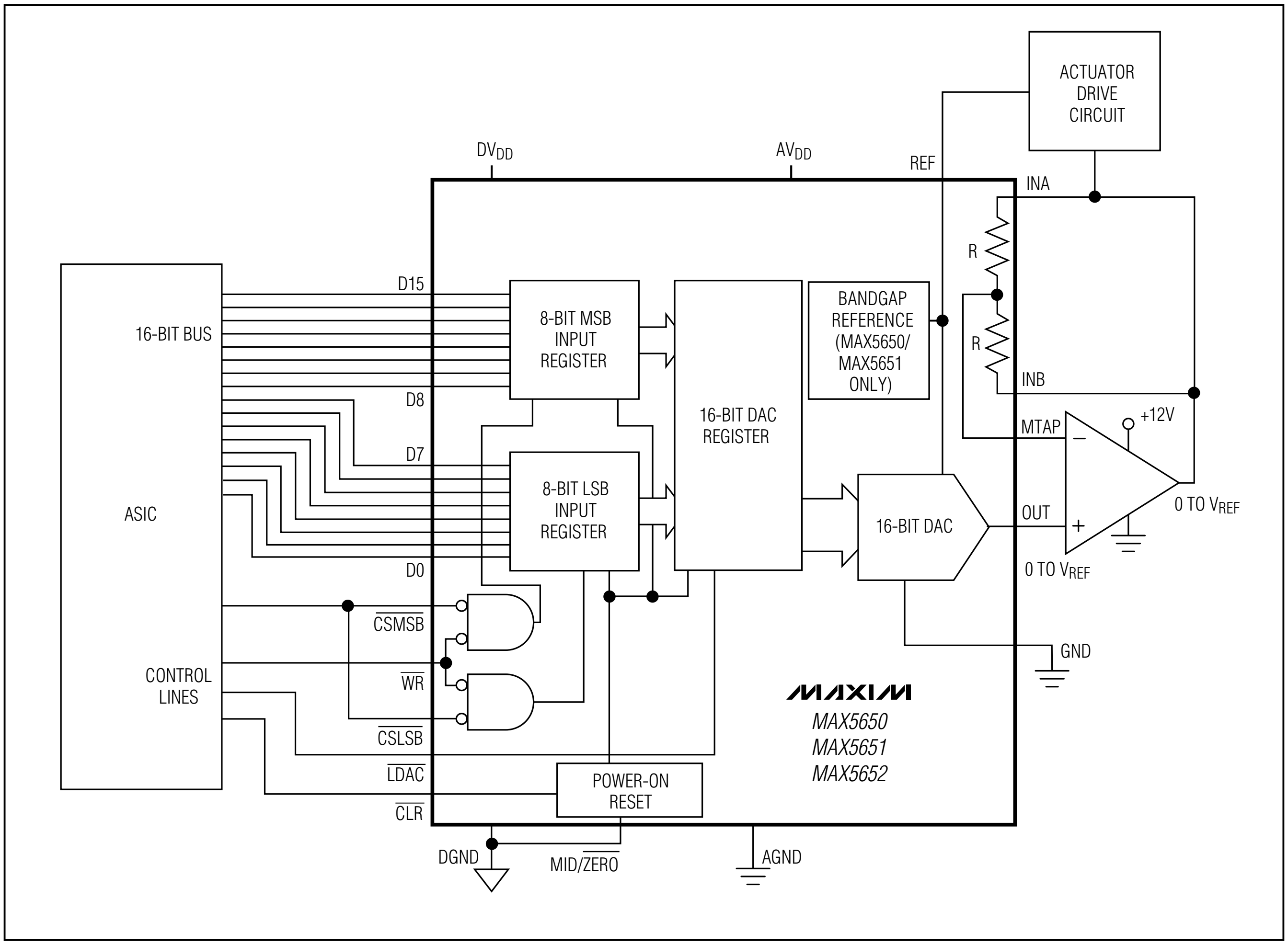


Figure 2. Typical Application Circuit for Unipolar Configuration

Typical Application Circuits (continued)

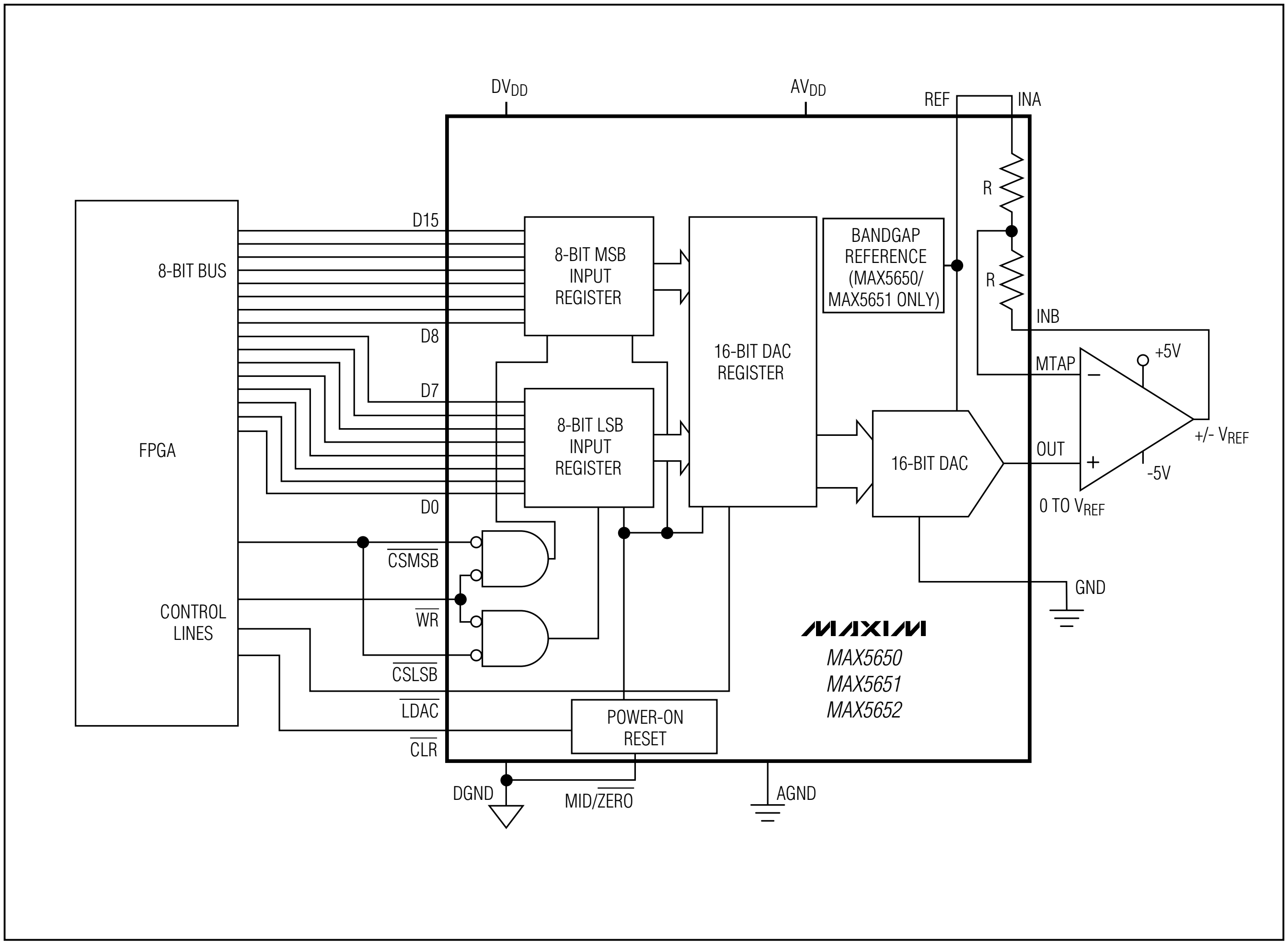


Figure 3. Typical Application Circuit for Bipolar Configuration

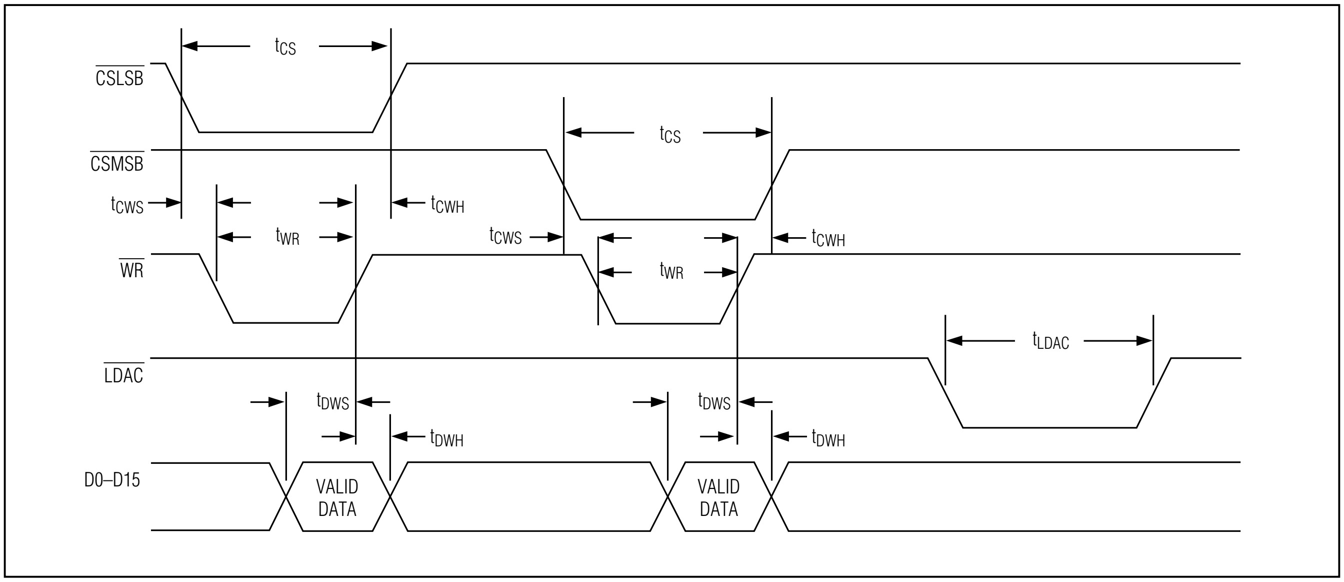


Figure 4. Timing Diagram

Detailed Description

The MAX5650/MAX5651/MAX5652 parallel-input, voltage-output DACs offer full 16-bit performance with less than ±4 LSB integral nonlinearity and less than ±1 LSB differential nonlinearity, ensuring monotonic performance over the full operating temperature range. The DAC is composed of an inverted R2R ladder with the unbuffered output available directly at OUT, allowing 16-bit performance from the reference voltage to the DAC ground (GND). The parallel inputs are double-buffered and configurable as a single 16-bit wide input or a 2-byte input. The MAX5650/MAX5651 include internal precision low-drift (10ppm/°C) bandgap voltage references of +4.096V and +2.048V, respectively. The MAX5652 accepts an external reference voltage between +2V and AV_{DD}. The MAX5650 operates with a supply voltage range of +4.75V to +5.25V, while the MAX5651/MAX5652 operate with a supply voltage range of +2.7V to +5.25V.

Voltage Reference

The MAX5650/MAX5651 provide a 10ppm/°C (typ) internal precision bandgap voltage reference with a load regulation specification of less than 0.6µV/µA (maximum) over the entire operating temperature range. The reference voltage for the MAX5650 is +4.096V, while the reference voltage for the MAX5651 is +2.048V. Connect a capacitor ranging between 1µF and 47µF from REF to ground as close to the device as possible. Use a low-ESR ceramic capacitor such as the GRM series from Murata.

The MAX5652 accepts an external reference with a voltage range extending from +2V to AV_{DD}. The output voltage of the DAC is determined as follows:

$$V_{OUT} = V_{REF} \times N / 65536$$

where N is the numeric value of the DAC's binary input code (0 to 65535) and V_{REF} is the reference voltage.

At a full-scale transition, the instantaneous charge demand from the external reference is about 550pC. For a reference with a 1µF load capacitor, the charge demand causes an instantaneous reference voltage drop of 550µV. A 10µF load capacitor causes a voltage drop of 55µV. This glitch recovers in a time inversely proportional to the bandwidth of the voltage reference, which should be sufficiently fast to recover before the next DAC transition to avoid accumulation of the glitch energy and a shift in the average reference voltage. For a +4.096V reference with 1µF bypass capacitor, it takes three time constants to recover to 0.5 LSB accuracy. Therefore, a 96kHz bandwidth reference recovers in 5µs while a 960kHz bandwidth reference recovers in 0.5µs.

For further voltage-reference selection assistance, visit www.maxim-ic.com/appnotes.cfm/appnote_number/754.

Digital Interface

The MAX5650/MAX5651/MAX5652 accept a single 16-bit wide input or an 8 plus 8-bit wide input. Data latches or transfers directly to the DAC depending on the state of the control inputs CLR, CSLSB, CSMSB, LDAC, MID/ZERO, and WR. All digital inputs are compatible with both TTL and CMOS logic.

The double buffered input consists of an input register and a DAC register (see the *Functional Diagram*). Data is loaded into the input register using CSLSB, CSMSB, and WR. The input register is transparent when WR and CSLSB and/or CSMSB are low. The rising edge of WR, while CSLSB is low, latches the lower byte (D0–D7) into the input register. The rising edge of WR, while CSMSB is low, latches the upper byte (D8–D15) into the input register. The sequence of loading the MSB and LSB does not matter. See Figure 1 for byte-wide interface circuit.

The DAC register is transparent when LDAC is low. The rising edge of LDAC latches data into the DAC register. The DAC's analog output reflects the data held in the DAC register. Both the input register and DAC register are transparent when CSLSB, CSMSB, WR, and LDAC are driven low. In this case, any change at D0–D15 appears at the output instantly. See Table 1 for the truth table.

Table 1. Truth Table

CLR	CSLSB	CSMSB	WR	LDAC	FUNCTION
1	0	1	0	1	Loads least significant byte into the input register. DAC output remains unchanged.
1	0	1	_/¯	1	Latches least significant byte into the input register. DAC output remains unchanged.
1	1	0	0	1	Loads most significant byte into the input register. DAC output remains unchanged.
1	1	0	_/¯	1	Latches most significant byte into the input register. DAC output remains unchanged.
1	X	X	1	0	Transfers data from the input register into the DAC register and updates the DAC output.
1	X	X	1	_/¯	Latches data from the input register into the DAC register. DAC output remains unchanged.
1	1	0	0	0	Most significant input and DAC registers are transparent. DAC output updates immediately with the most significant input data and least significant input register data.
1	X	X	1	1	No operation.
1	0	0	0	0	Both most significant and least significant input registers and DAC register are transparent. DAC output updates immediately with the most significant and least significant input data.
1	0	0	0	1	Loads all 16 bits into the input register. DAC output remains unchanged.
1	0	1	0	0	Least significant input and DAC registers are transparent. DAC output updates immediately with the least significant input data and most significant register data.
1	1	1	X	0	Transfers data held in the input register to the DAC register and updates the DAC output.
1	1	1	X	1	No operation.
0	X	X	X	X	Sets the input and DAC registers and DAC output to midscale (if MID/ZERO = 1) or zero-scale (if MID/ZERO = 0).

0 = Low state.

1 = High state.

X = Don't care.

_/¯ *= Rising edge.*

16-Bit, Parallel-Input, Voltage-Output DACs with Internal Reference

The MAX5650/MAX5651/MAX5652 provide an asynchronous clear input ($\overline{CLR}$). Asserting $\overline{CLR}$ resets the input and DAC registers and DAC output to midscale if the MID/$\overline{ZERO}$ input is high and to zero scale when MID/$\overline{ZERO}$ is low.

Power-On Reset (POR)

The MAX5650/MAX5651/MAX5652 provide an internal POR circuit. On power-up, the input and DAC registers and DAC output are set to 0000 hex if MID/$\overline{ZERO}$ is low or 8000 hex if MID/$\overline{ZERO}$ is high. Wait 10µs after power-up before pulling $\overline{CSMSB}$ or $\overline{CSLSB}$ low.

Internal Scaling Resistors

The MAX5650/MAX5651/MAX5652 include two internal scaling resistors of 12.4kΩ (typ) each that are matched to 0.05% or better. Use these resistors with a precision external op amp to generate a bipolar output swing (see the *Bipolar Operation* section). The free ends of these resistors are accessible at INA and INB while the midpoint is accessible at MTAP. Connect INB to the output of the op amp and INA to REF for bipolar operation. Negative voltages are only allowed at INB (see the *Absolute Maximum Ratings* section).

Applications Information

Unipolar Buffered/Unbuffered Operation

Unbuffered operation reduces power consumption as well as the offset error contributed by the external output buffer (see Figure 1). The R2R DAC output is available directly at OUT, allowing 16-bit performance from $+V_{REF}$ to GND without degradation at zero scale.

The typical application circuit (Figure 2) shows the MAX5650/MAX5651/MAX5652 configured for a buffered unipolar voltage-output operation. Use the integrated precision matched resisters for op-amp input impedance matching. Table 2 shows digital codes and corresponding output voltages for unipolar buffered or unbuffered operation.

Bipolar Operation

For bipolar voltage-output operation, use an external op amp (such as the MAX400) in conjunction with the internal scaling resistors (see Figure 3). Connect the free end of the internal resistor (INB) to the output of the external op amp and the free end of the other resistor (INA) to REF. Connect the midpoint of the resistors to the inverting input of the op amp. Connect the output of the DAC to the noninverting input of the external op amp. The resulting transfer function is as follows:

$$V_{OUT} = V_{REF}\ [(2D / 65{,}536) - 1]$$

where D is the decimal value of the DACs binary input code. Table 3 shows digital codes and corresponding output voltages for bipolar operation.

Table 2. Unipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	V_{REF} x (65,535 / 65,536)
1000 0000 0000 0000	V_{REF} x (32,768 / 65,536) = $0.5V_{REF}$
0000 0000 0000 0001	V_{REF} x (1 / 65,536)
0000 0000 0000 0000	0V

Table 3. Bipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	$+V_{REF}$ x (32,767 / 32,768)
1000 0000 0000 0001	$+V_{REF}$ x (1 / 32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ (1 / 32,768)
0000 0000 0000 0000	$-V_{REF}$ x (32,768 / 32,768) = $-V_{REF}$

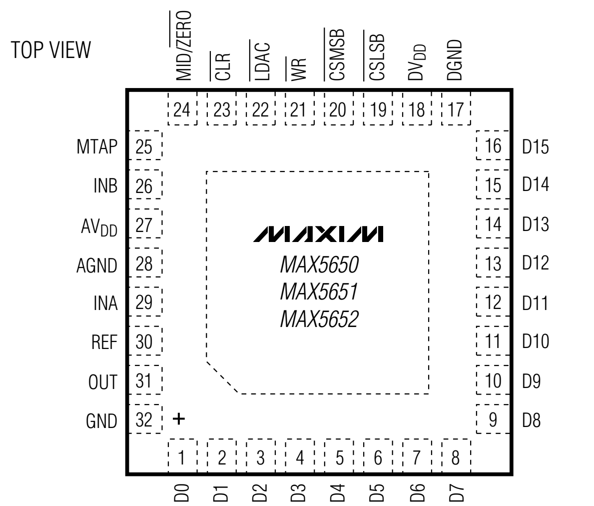
Power-Supply and Layout Considerations

Careful PC board layout is important for optimal system performance. Wire-wrapped boards, sockets, and breadboards are not recommended. Keep analog and digital signals separate to reduce noise injection and digital feedthrough. Connect AGND and DGND to the highest quality ground available. Star-connect all ground return paths back to AGND or use a multilayer board with a low-inductance ground plane. Connect analog and digital ground planes together at a low-impedance power-supply source. For the MAX5652, keep the trace between the reference source to the reference input short and low impedance. Bypass each supply with a 0.1µF capacitor as close as possible to the IC for optimal 16-bit performance.

Chip Information

PROCESS: BiCMOS

Pin Configuration

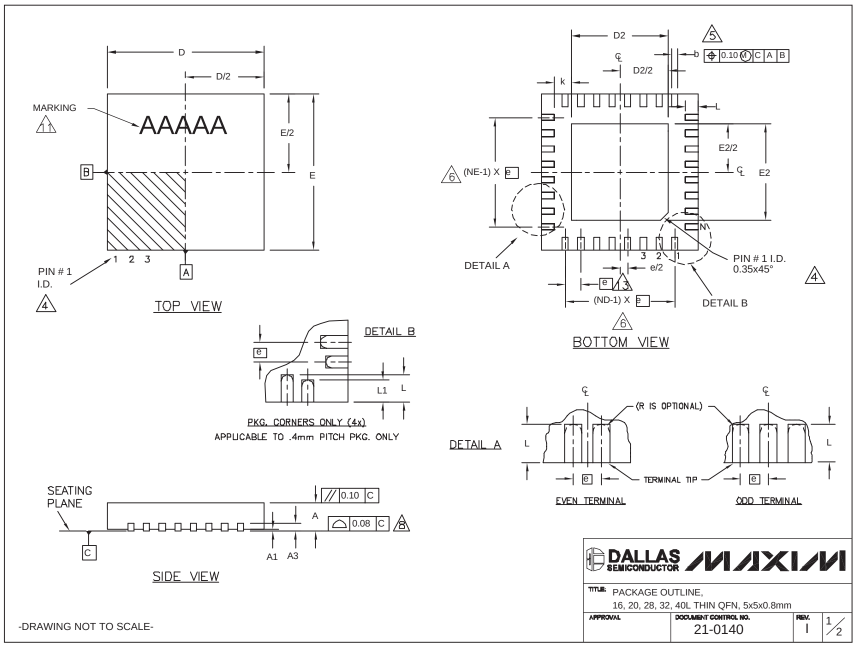


TQFN
5mm x 5mm

16-Bit, Parallel-Input, Voltage-Output DACs with Internal Reference

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L exceptions	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. I | 2/2

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