Single-chip 4-bit microcontroller for CD-DA

BU34675

The BU34675 is a compact 4-bit, single-chip microcontroller that includes all the I / O required for CD system control. Circuits on the chip include a pulse width measurement counter (PWC), SIO, and an LCD controller / driver for a 28-segment display. The LCD segments can all be switched in software to CMOS output, and the extensive I / O allows many functions with a low pin count.

●Applications

Portable CD-DA, CD / radio / cassette players

●Features

1) Low-voltage, high-speed operation (V_{DD} = 2.3 to 5.5V at 4.4MHz).
2) Pulse width measurement counter on chip (for remote control reception).
3) SIO provided for communication with the DSP.
4) Seven-segment, four-common LCD controller / driver on chip.
5) All segments of the LCD controller / driver output can be switched to CMOS output using software.

●Absolute maximum ratings (Ta = 25°C)

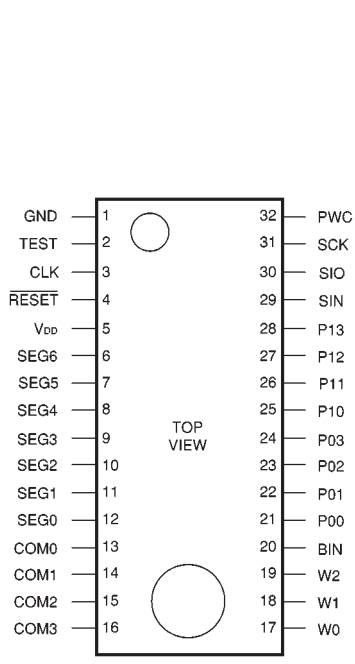
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	−0.3～+7.0	V
Power dissipation	Pd	500	mW
Operating temperature	Topr	−25～+75	℃
Storage temperature	Tstg	−55～+125	℃

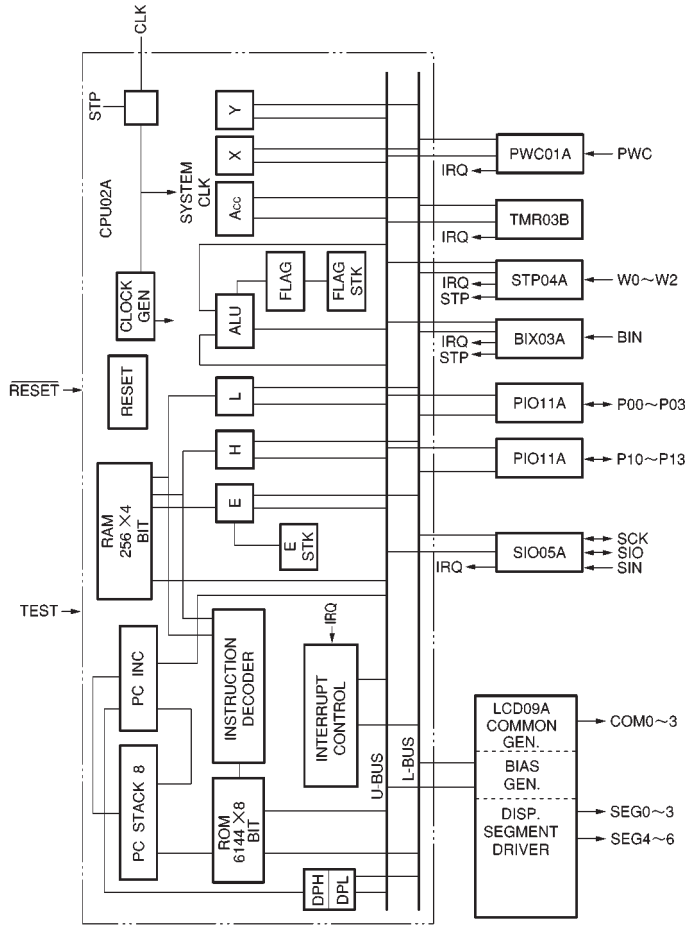
∗ Reduced by 5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	2.3	—	5.5	V
Input high level voltage (without hysteresis)	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low level voltage (without hysteresis)	V_{IL}	0	—	0.3V_{DD}	V
Input high level voltage (with hysteresis)	V_{IHS}	0.7V_{DD}	—	V_{DD}	V
Input low level voltage (with hysteresis)	V_{ILS}	0	—	0.25V_{DD}	V

●Block diagram





✻ The PROM is not on the chip.

✻ The address and data busses are not available for external connection (addressing external memory is not possible).

✻ The ALU uses four bits.

●Pin descriptions

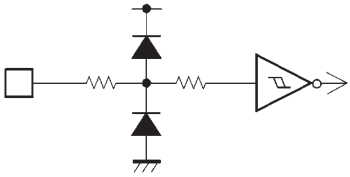
Pin No.	Pin name	I / O	Function	Type
21～24 25～28 (PIO11A block)	P00～P03 P10～P13	I / O	・4-bit input or output ・I / O bits can be set individually by program (output is N-ch open drain) ・Pull-up resistors can be switched on and off by program (setting possible for each bit) ・At reset, input turns off pull-up resistors*1	D
17～19 (STP04A block)	W0～W2	I	・General purpose 3-bit input ・With software, this can be used for STOP or HALT release input, or as interrupt request signal input (can be set for each bit) ・Pull-up resistors can be switched on and off by program (setting possible for each bit) ・At reset, pull-up resistors off	C
20 (BIX03A block)	BIN	I	・General purpose 1-bit input ・With software this can be used for STOP or HALT release input, or as interrupt request signal input ・Pull-up resistors can be switched on and off by program ・At reset, pull-up resistors off	C
29	SIN	I	・8-bit serial data input	A
30	SIO	I / O	・8-bit serial data I / O ・I / O selectable by program	E
31 (SI005A block)	SCK	I / O	・Clock I / O for serial data transmission/reception ・Software can be used to select among three internal clocks and one external clock	E
6～9 10～12	SEG6～3 SEG2～0	O	・Either LCD segment output and CMOS low current output can be selected by program (the upper three pins are for each segment, and the lower four pins are for setting all at once) ・At reset, all revert to low-current CMOS output ("L" polarity is output)	F
13～16 (LCD09A block)	COM0～ COM3	O	・LCD common output ・COM3 is low-current CMOS output when 1/3 duty is selected	F
32 (PWC01A block)	PWC	I	・Pulse input	A
3	CLK	I	・External clock input	G
2	TEST	I	・Test input (the chip test pin has an internal pull-down resistor, and is to be left open normally)	B
4	$\overline{\text{RESET}}$	I	・Reset input (set to "L" to reset the CPU)	A
5	V_{DD}	—	・Power supply	—
1	GND	—	・Ground	—

Format :Refer to the I / O circuit diagrams on the following page.

*1 The pins are in the high impedance state immediately after reset,so depending on the application, pin processing may be required.

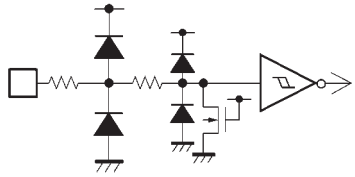
●Input / output circuits

TYPE A



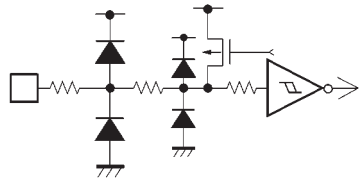
・Hysteresis input.

TYPE B



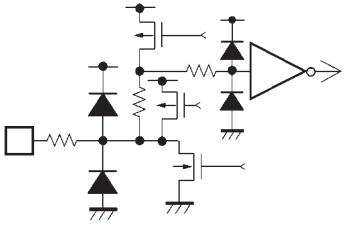
・Pull down resistor internal hysteresis input.

TYPE C



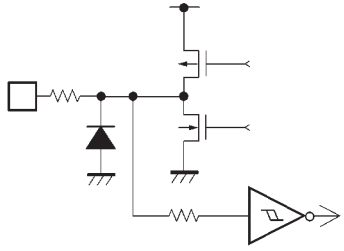
・Hysteresis input that allows switching pull-up resistors on and off using a program.

TYPE D



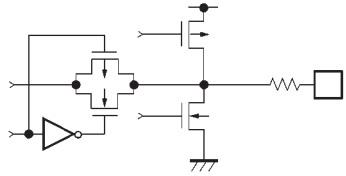
・Normal input/output that allows switching pull-up resistors on and off using a program and 6 has an N-ch open-drain output.

TYPE E



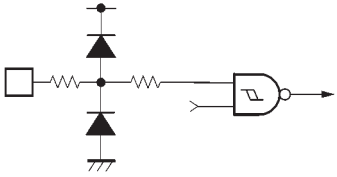
・Hysteresis input without CMOS output that can be controlled by program.

TYPE F



・LCD driver output. CMOS output can be selected for the SEG.

TYPE G



・Hysteresis input.

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{DD} = 5V)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
STOP circuit current	I_{DDST}	—	—	—	1	μA	STOP mode
HALT circuit current	I_{DDHT}	—	—	700	—	μA	HALT mode f_{OSC}=4.4MHz
Operation circuit current	I_{DDOP}	—	—	2	—	mA	f_{OSC}=4.4MHz
Clock frequency	f_{OSC}	CLK	2	—	4.4	MHz	—
Input high level voltage 1	V_{IH1}	P00～P03, P10～P13	3.5	—	—	V	When input
Input high level voltage 2	V_{IH2}	W0～W2, BIN, SIN, SIO, SCK, PWC, TEST, $\overline{RESET}$	3.75	—	—	V	Hysteresis input When SIO and SCK are input
Input high level voltage 3	V_{IH3}	CLK	3.9	—	—	V	—
Input low level voltage 1	V_{IL1}	P00～P03, P10～P13	—	—	1.5	V	When input
Input low level voltage 2	V_{IL2}	W0～W2, BIN, SIN, SIO, SCK, PWC, TEST, $\overline{RESET}$	—	—	1.25	V	Hysteresis input When SIO and SCK are input
Input low level voltage 3	V_{IL3}	CLK	—	—	1.1	V	—
Input high level current 1	I_{IH1}	P00～P03, P10～P13, W0～W2, BIN, SIN, SIO, SCK, PWC, $\overline{RESET}$, CLK	—	—	1	μA	No pull-down resistor Pxx, SIO, and SCK are input V_{IN}=V_{DD}
Input high level current 2	I_{IH2}	TEST	35	70	140	μA	Pull-down resistor on chip V_{IN}=V_{DD}
Input low level current 1	I_{IL1}	P00～P03, P10～P13, W0～W2, BIN、SIN、SIO, SCK, PWC, $\overline{RESET}$, TEST, CLK	—	—	−1	μA	No pull-up resistor Pxx, SIO, and SCK are input V_{IN}=GND
Input low level current 2	I_{IL2}	P00～P03, P10～P13, W0～W2, BIN	−90	−125 (40kΩ)	−160	μA	Pull-up resistor on chip V_{IN} = GND
Output high level voltage 1	V_{OH1}	SIO, SCK	4.5	—	—	V	When SIO and SCK are output I_{OH}=−500 μA
Output high level voltage 2	V_{OH2}	SEG0～SEG6, COM0～COM3	4.5	—	—	V	I_{OH}=−250 μA
Output low level voltage 1	V_{OL1}	P00～P03, P10～P13, SIO, SCK	—	—	0.4	V	When Pxx, SIO and SCK are output I_{OL}=1.6mA
Output low level voltage 2	V_{OL2}	SEG0～SEG6, COM0～COM3	—	—	0.7	V	I_{OL}=1.0mA
Output leak current	I_L	P00～P03, P10～P13	—	—	1	μA	When Pxx is output high impedance
LCD 2 / 3 level output voltage	V_1	COM0～COM3, SEG0～SEG6	—	3.3	—	V	—
LCD 1 / 3 level output voltage	V_2	COM0～COM3, SEG0～SEG6	—	1.6	—	V	—

✻ One machine cycle requires 1 / 6 of the oscillator frequency.

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{DD} = 3V)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
STOP circuit current	I_{DDST}	—	—	—	1	μA	STOP mode
HALT circuit current	I_{DDHT}	—	—	200	—	μA	HALT mode f_{OSC} = 4.4MHz
Operation circuit current	I_{DDOP}	—	—	0.7	—	mA	f_{OSC} = 4.4MHz
Clock frequency	f_{OSC}	CLK	2	—	4.4	MHz	—
Input high level voltage 1	V_{IH1}	P00～P03, P10～P13	2.1	—	—	V	When input
Input high level voltage 2	V_{IH2}	W0～W2, BIN, SIN, SIO, SCK, PWC, TEST, $\overline{RESET}$	2.25	—	—	V	Hysteresis input When SIO and SCK are input
Input high level voltage 3	V_{IH3}	CLK	2.4	—	—	V	—
Input low level voltage 1	V_{IL1}	P00～P03, P10～P13	—	—	0.9	V	When input
Input low level voltage 2	V_{IL2}	W0～W2, BIN, SIN, SIO, SCK, PWC, TEST, $\overline{RESET}$	—	—	0.75	V	Hysteresis input When SIO and SCK are input
Input low level voltage 3	V_{IL3}	CLK	—	—	0.65	V	—
Input high level current 1	I_{IH1}	P00～P03, P10～P13, W0～W2, BIN, SIN, SIO, SCK, PWC, $\overline{RESET}$, CLK	—	—	1	μA	No pull-down resistor Pxx, SIO, and SCK are input $V_{IN}=V_{DD}$
Input high level current 2	I_{IH2}	TEST	10	20	35	μA	Pull-down resistor on chip $V_{IN}=V_{DD}$
Input low level current 1	I_{IL1}	P00～P03, P10～P13, W0～W2, BIN、SIN, SIO, SCK, PWC, $\overline{RESET}$, TEST, CLK	—	—	−1	μA	No pull-up resistor Pxx, SIO, and SCK are input V_{IN}=GND
Input low level current 2	I_{IL2}	P00～P03, P10～P13, W0～W2, BIN	−20	−40 (125kΩ)	−60	μA	Pull-up resistor on chip V_{IN}=GND
Output high level voltage 1	V_{OH1}	SIO, SCK	2.5	—	—	V	When SIO and SCK are output I_{OH}=−500 μA
Output high level voltage 2	V_{OH2}	SEG0～SEG6, COM0～COM3	2.5	—	—	V	I_{OH}=−250 μA
Output low level voltage 1	V_{OL1}	P00～P03, P10～P13, SIO, SCK	—	—	0.6	V	When Pxx, SIO and SCK are output I_{OL}=1.6mA
Output low level voltage 2	V_{OL2}	SEG0～SEG6, COM0～COM3	—	—	0.7	V	I_{OL}=0.8mA
Output leak current	I_L	P00～P03, P10～P13	—	—	1	μA	When Pxx is output high impedance
LCD 2 / 3 level output voltage	V_1	COM0～COM3, SEG0～SEG6	—	2	—	V	—
LCD 1 / 3 level output voltage	V_2	COM0～COM3, SEG0～SEG6	—	1	—	V	—

✻ One machine cycle requires 1 / 6 of the oscillator frequency.

●Explanation of the hardware

(1) Operates of a single power supply (V_{DD} = 2.3 to 5.5V).

(2) Memory size

ROM:	6144 × 8 bits
RAM:	256 × 4 bits
LCD display RAM :	7 × 4 bits

(3) Instruction time (one cycle instruction)
1.5µsec (at 4 MHz)

(4) Sub-routine nesting: . . . . . 8 levels

(5) Interrupts: 5
External 3
Internal (timer counter, serial I / O) 2

(6) ROM data table function (6k data table region)

(7) Two power save modes STOP / HALT

(8) On-chip 7-segment LCD driver that can drive a wide variety of display types
Bias . . . . . 1 / 3
Duty variation . . . . . 1 / 3, 1 / 4 (programmable)
Internal bias resistors (approximately 50kΩ × 3 stages)

(9) LCD segment output can be switched to CMOS output by software.
The COM3 pin and upper three segments are one-bit units, and the lower four segments are all selected together. At reset, switches to CMOS low-current output port with low level polarity.

(10) Remote control receiver circuit (pulse width measurement)

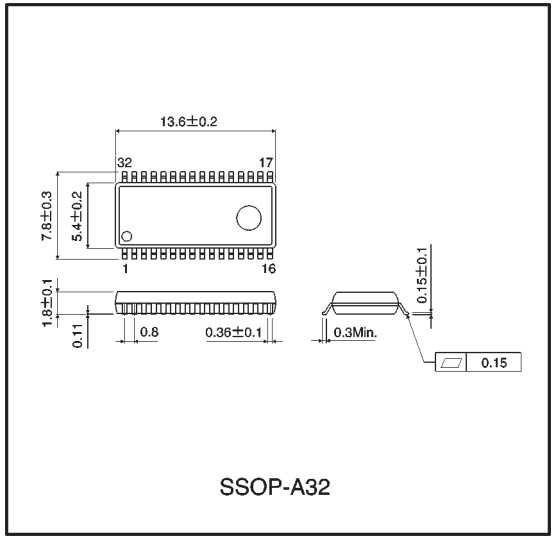
(11) On-chip 8-bit timer counter

(12) On-chip I / O system makes interfacing with external LSI easy (LSB first).

(13) 8 I / O lines that can be pulled up by software

(14) 4 input lines that can be pulled up by software

●External dimensions (Units: mm)



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