

# FDMS8570S

## N-Channel PowerTrench® SyncFET™

25 V, 60 A, 2.8 mΩ

### Features

- Max  $r_{DS(on)}$  = 2.8 mΩ at  $V_{GS} = 10$  V,  $I_D = 24$  A
- Max  $r_{DS(on)}$  = 3.3 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 22$  A
- High performance technology for extremely low  $r_{DS(on)}$
- SyncFET™ Schottky Body Diode
- RoHS Compliant

April 2012

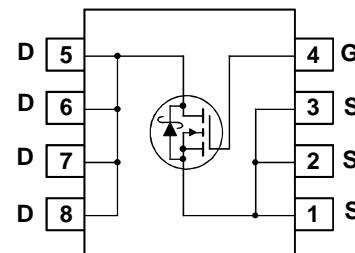
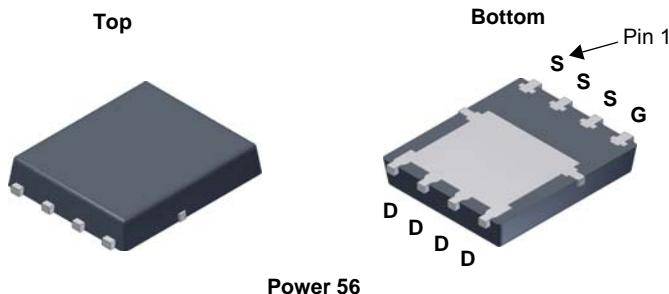


### General Description

This N-Channel SyncFET™ is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance. This device has the added benefit of an efficient monolithic Schottky body diode.

### Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	12	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	60	A
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	24	
	-Pulsed	100	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	48	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case $T_C = 25^\circ\text{C}$	2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
10OD	FDMS8570S	Power 56	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	25			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10 \text{ mA}, \text{referenced to } 25^\circ\text{C}$		23		$\text{mV/}^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		500		$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = +12 \text{ V}/-8 \text{ V}, V_{DS} = 0 \text{ V}$		$\pm 100$		nA

### On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1 \text{ mA}$	1.1	1.5	2.2	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10 \text{ mA}, \text{referenced to } 25^\circ\text{C}$		-3		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 24 \text{ A}$		2.1	2.8	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 22 \text{ A}$		2.4	3.3	
		$V_{GS} = 10 \text{ V}, I_D = 24 \text{ A}, T_J = 125^\circ\text{C}$		2.9	3.9	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 24 \text{ A}$		215		s

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 13 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	2825		$\text{pF}$
$C_{oss}$	Output Capacitance		662		$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance		94		$\text{pF}$
$R_g$	Gate Resistance		0.8		$\Omega$

### Switching Characteristics

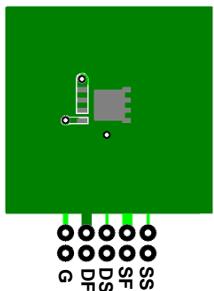
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13 \text{ V}, I_D = 24 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$	11		ns
$t_r$	Rise Time		4		ns
$t_{d(off)}$	Turn-Off Delay Time		33		ns
$t_f$	Fall Time		3		ns
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}$	42		nC
$Q_g$	Total Gate Charge		22		nC
$Q_{gs}$	Gate to Source Gate Charge		6.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		4.4		nC

### Drain-Source Diode Characteristics

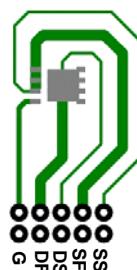
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$	(Note 2)	0.6	0.8	V
		$V_{GS} = 0 \text{ V}, I_S = 24 \text{ A}$	(Note 2)	0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 24 \text{ A}, di/dt = 300 \text{ A}/\mu\text{s}$		22		ns
				19		nC

NOTES:

1.  $R_{thJA}$  is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below.  $R_{thJC}$  is guaranteed by design while  $R_{thCA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 45 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.4 \text{ mH}$ ,  $I_{AS} = 15 \text{ A}$ ,  $V_{DD} = 23 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ . 100% test at  $L = 0.1 \text{ mH}$ ,  $I_{AS} = 23.8 \text{ A}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

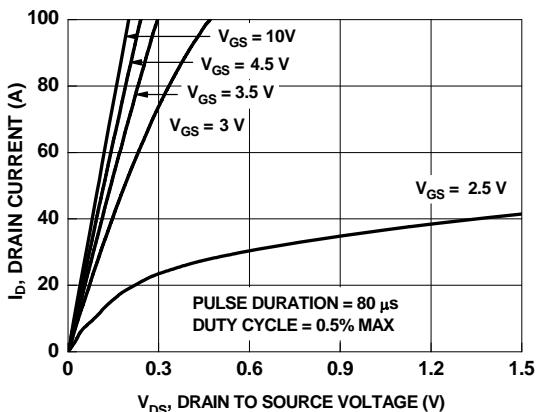


Figure 1. On Region Characteristics

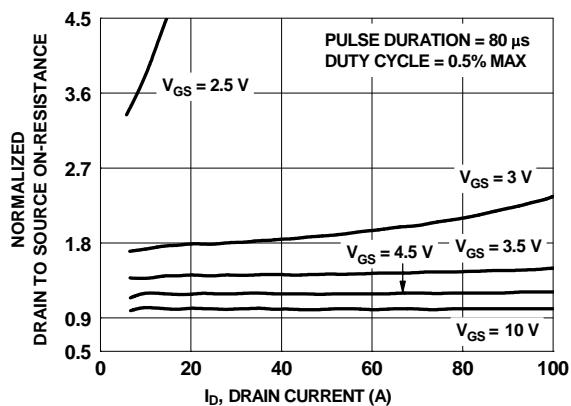


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

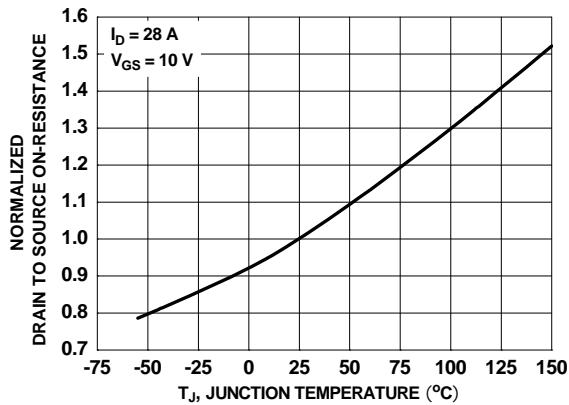


Figure 3. Normalized On Resistance vs Junction Temperature

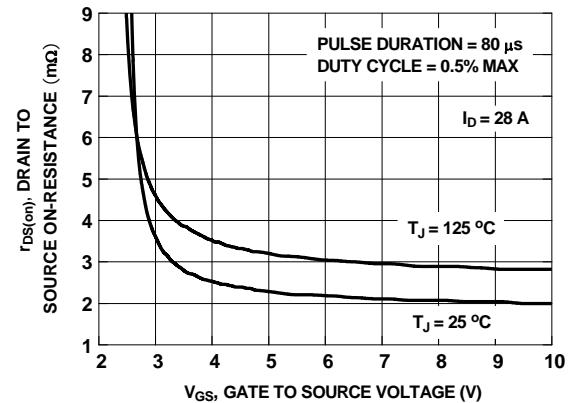


Figure 4. On-Resistance vs Gate to Source Voltage

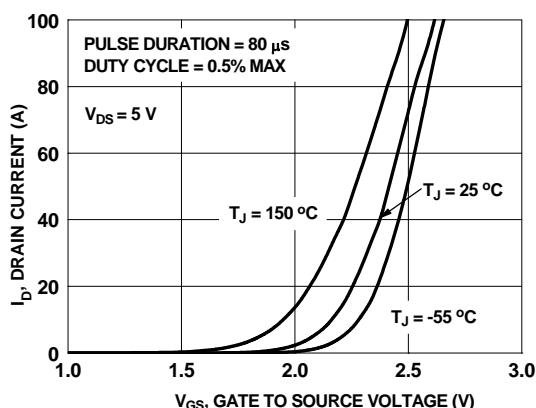


Figure 5. Transfer Characteristics

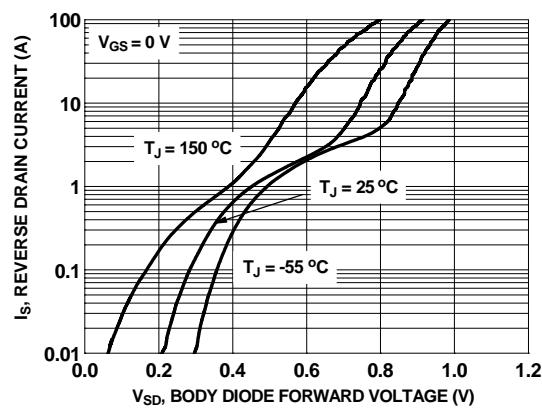


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

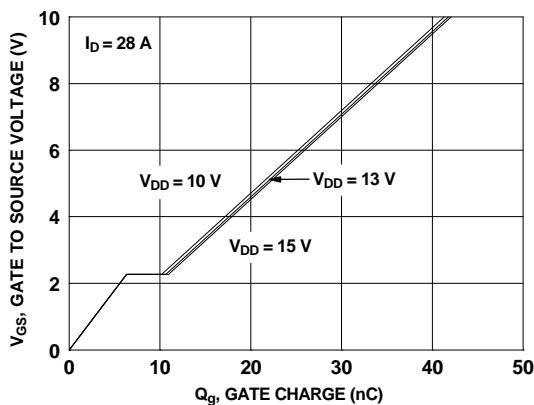


Figure 7. Gate Charge Characteristics

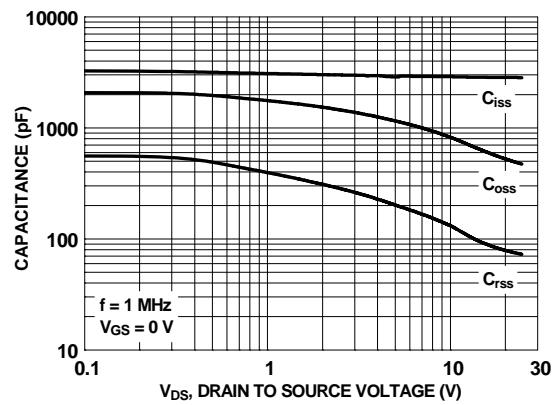


Figure 8. Capacitance vs Drain to Source Voltage

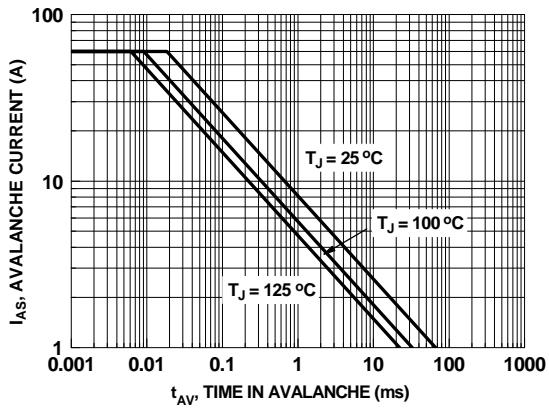


Figure 9. Unclamped Inductive Switching Capability

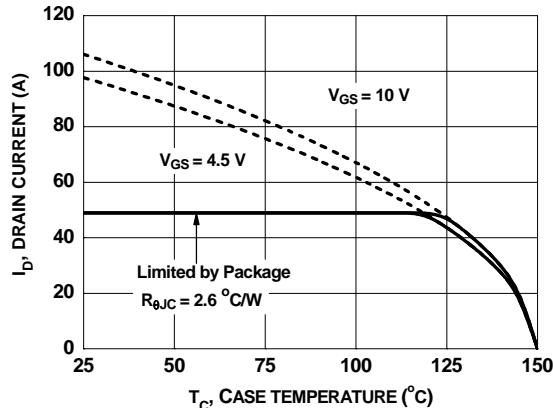


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

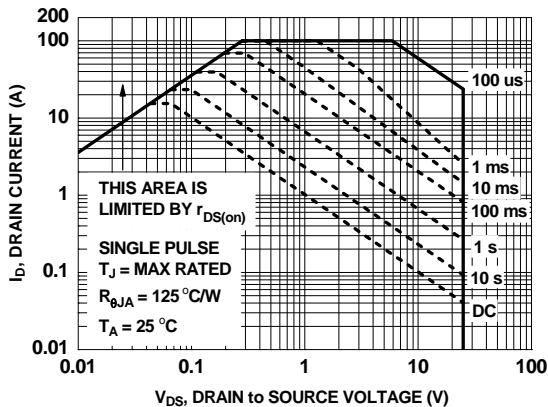


Figure 11. Forward Bias Safe Operating Area

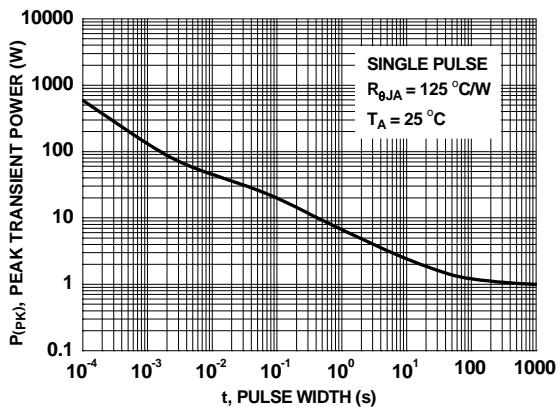


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

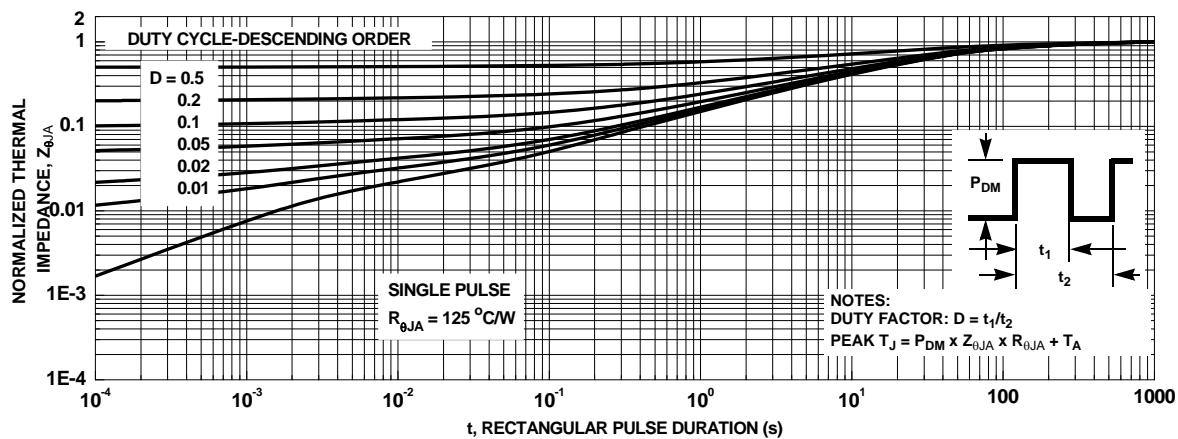


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

### SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8570S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

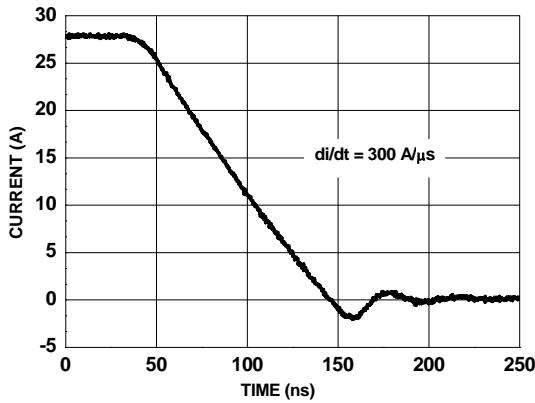


Figure 14. FDMS8570S SyncFET™ body diode reverse recovery characteristic

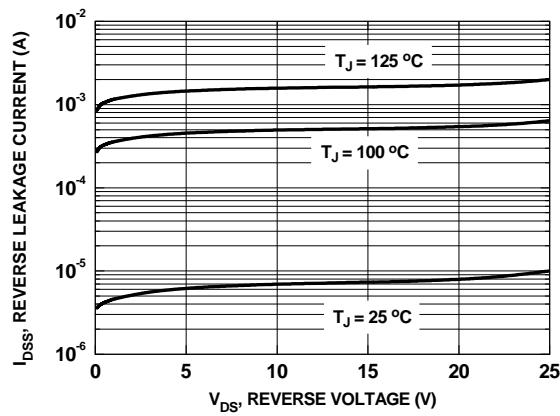
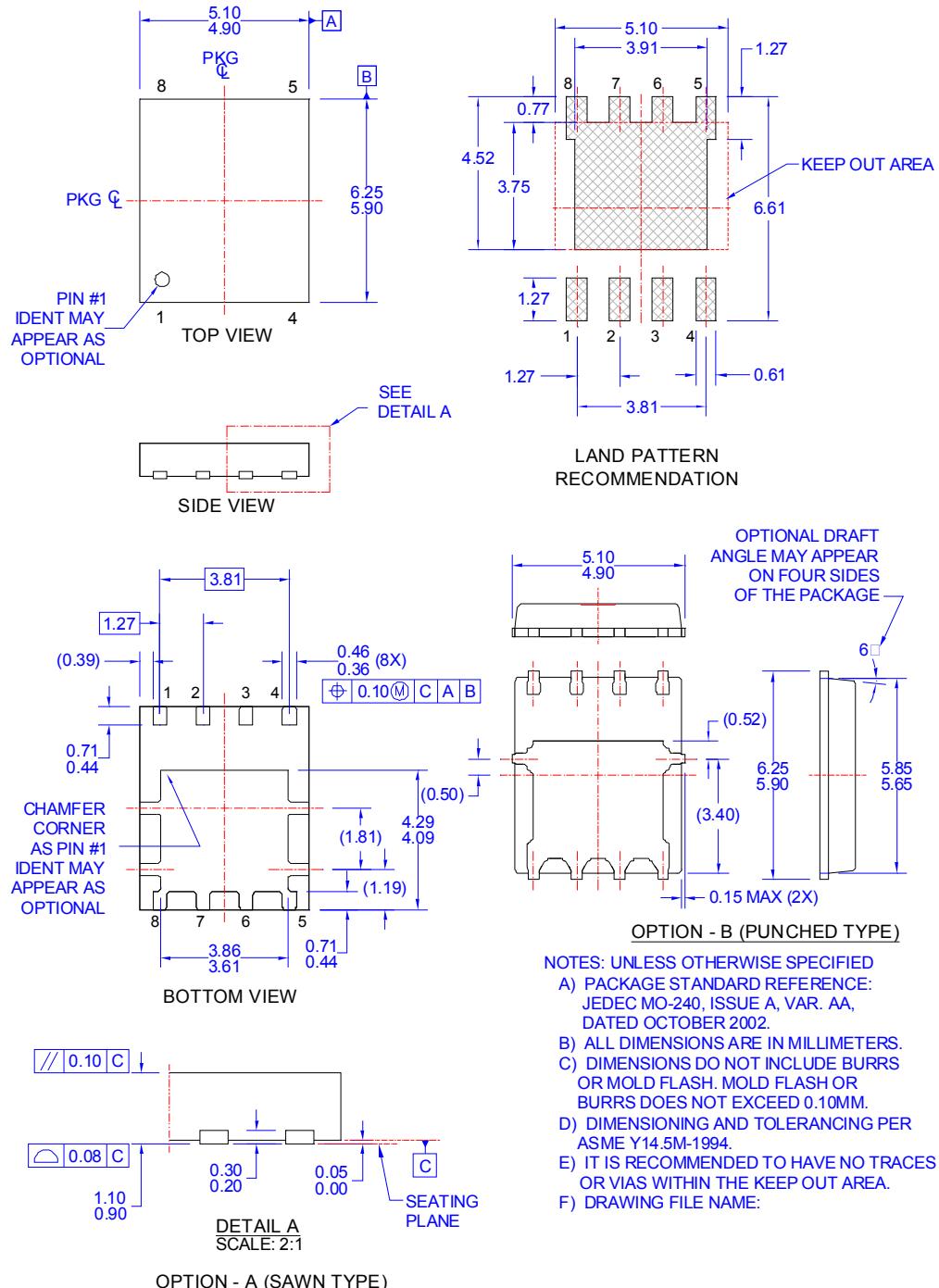


Figure 15. SyncFET™ body diode reverse leakage versus drain-source voltage

## Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE:  
JEDEC MO-240, ISSUE A, VAR. AA,  
DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS  
OR MOLD FLASH. MOLD FLASH OR  
BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER  
ASME Y14.5M-1994.
- E) IT IS RECOMMENDED TO HAVE NO TRACES  
OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME:


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CROSSVOLT™	GTO™	™	TinyPower™
CTL™	IntelliMAX™	Saving our world, 1mW/W/kW at a time™	TinyPWM™
Current Transfer Logic™	ISOPLANAR™	SignalWise™	TinyWire™
DEUXPEED®	Marking Small Speakers Sound Louder and Better™	SmartMax™	TransSiC®
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