



STD888T4

Medium Current, High Performance, Low Voltage PNP Transistor

General features

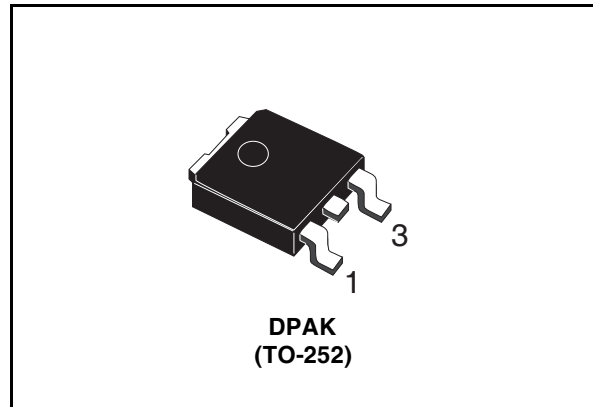
- Very low Collector to Emitter saturation voltage
- D.C. Current gain, $h_{FE} > 100$
- 5A continuous collector current
- Surface mounting DPAK(TO-252) power package in tape & reel packing
- In compliance with the 2002/93/EC European Directive

Description

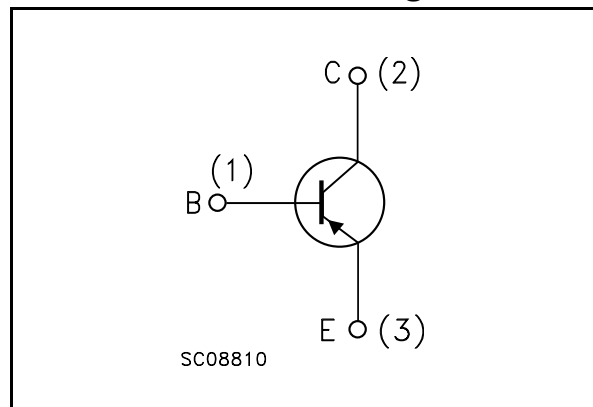
The device is manufactured in low voltage PNP Planar Technology by using a "Base Island" layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.

Applications

- Power management in portable equipment
- Voltage regulation in bias supply circuits
- Switching regulator in battery charger applications
- Heavy load driver



Internal schematic diagram



Order codes

Part Number	Marking	Package	Packing
STD888T4	D888	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage ($I_E = 0$)	-45	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	-30	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	-6	V
I_C	Collector current	-5	A
I_{CM}	Collector peak current ($t_P < 5\text{ms}$)	-10	A
P_{tot}	Total dissipation at $T_c = 25^\circ\text{C}$	15	W
T_{stg}	Storage temperature	-65 to 150	$^\circ\text{C}$
T_J	Max. operating junction temperature	150	$^\circ\text{C}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	8.33	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current ($I_{\text{E}} = 0$)	$V_{\text{CB}} = -30\text{V}$ $V_{\text{CB}} = -30\text{V}; T_{\text{C}} = 100^{\circ}\text{C}$			-10 100	μA μA
I_{EBO}	Emitter cut-off current ($I_{\text{C}} = 0$)	$V_{\text{EB}} = -6\text{V}$			-10	μA
$V_{(\text{BR})\text{CEO}}^{(2)}$	Collector-emitter breakdown voltage ($I_{\text{B}} = 0$)	$I_{\text{C}} = -10\text{mA}$	-30			V
$V_{(\text{BR})\text{CBO}}$	Collector-base breakdown voltage ($I_{\text{E}} = 0$)	$I_{\text{C}} = -100\mu\text{A}$	-45			V
$V_{(\text{BR})\text{EBO}}$	Emitter-base breakdown voltage ($I_{\text{C}} = 0$)	$I_{\text{E}} = -100\mu\text{A}$	-6			V
$V_{\text{CE(sat)}}^{(2)}$	Collector-emitter saturation voltage	$I_{\text{C}} = -0.5\text{A}$ $I_{\text{B}} = -5\text{mA}$ $I_{\text{C}} = -2\text{A}$ $I_{\text{B}} = -50\text{mA}$ $I_{\text{C}} = -5\text{A}$ $I_{\text{B}} = -250\text{mA}$ $I_{\text{C}} = -6\text{A}$ $I_{\text{B}} = -250\text{mA}$ $I_{\text{C}} = -8\text{A}$ $I_{\text{B}} = -400\text{mA}$ $I_{\text{C}} = -10\text{A}$ $I_{\text{B}} = -500\text{mA}$			-0.15 -0.35 -0.7 -0.7 -1 -1.2	V V V V V V
$V_{\text{BE(sat)}}^{(2)}$	Base-emitter saturation voltage	$I_{\text{C}} = -2\text{A}$ $I_{\text{B}} = -50\text{mA}$ $I_{\text{C}} = -6\text{A}$ $I_{\text{B}} = -250\text{mA}$		-1.2	-1.1	V V
$h_{\text{FE}}^{(2)}$	DC current gain	$I_{\text{C}} = -10\text{mA}$ $V_{\text{CE}} = -1\text{V}$ $I_{\text{C}} = -500\text{mA}$ $V_{\text{CE}} = -1\text{V}$ $I_{\text{C}} = -5\text{A}$ $V_{\text{CE}} = -1\text{V}$ $I_{\text{C}} = -5\text{A}$ $V_{\text{CE}} = -1\text{V}$ $T_{\text{C}} = 100^{\circ}\text{C}$ $I_{\text{C}} = -8\text{A}$ $V_{\text{CE}} = -1\text{V}$ $I_{\text{C}} = -10\text{A}$ $V_{\text{CE}} = -1\text{V}$	120 100 70	200 200 100 100 55 35	300	
t_{d} t_{r} t_{s} t_{f}	Resistive load Delay time Rise time Storage time Fall time	$I_{\text{C}} = -3\text{A}$ $V_{\text{CC}} = -20\text{V}$ $I_{\text{B1}} = -I_{\text{B2}} = -60\text{mA}$ (see figure 7)		180 160 250 80	220 210 300 100	ns ns ns ns

Note (2) Pulsed duration = 300 μs , duty cycle $\leq 1.5\%$

2.1 Electrical characteristics (curves)

Figure 1. DC current gain

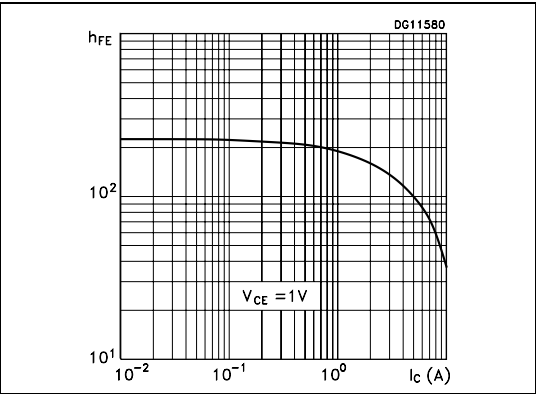


Figure 2. DC current gain

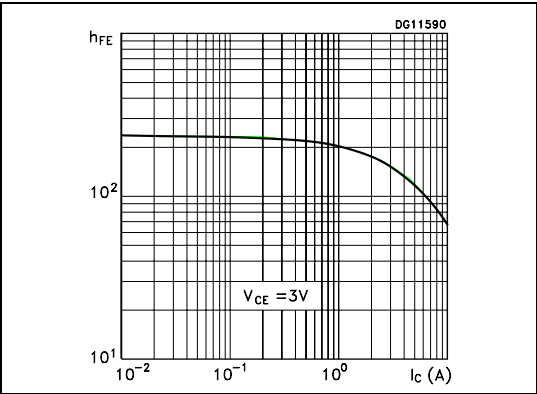


Figure 3. Collector-emitter saturation voltage

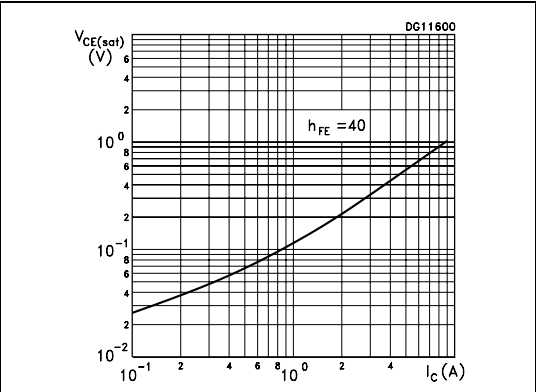


Figure 4. Base-emitter saturation voltage

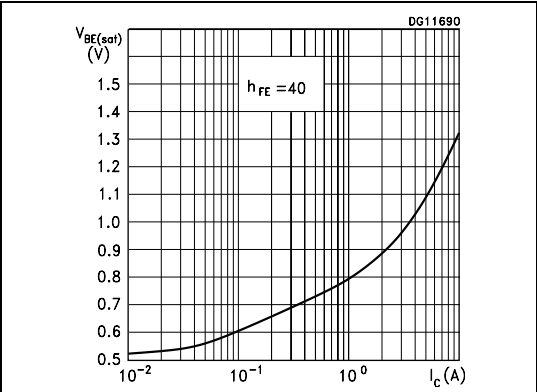


Figure 5. Switching time resistive load

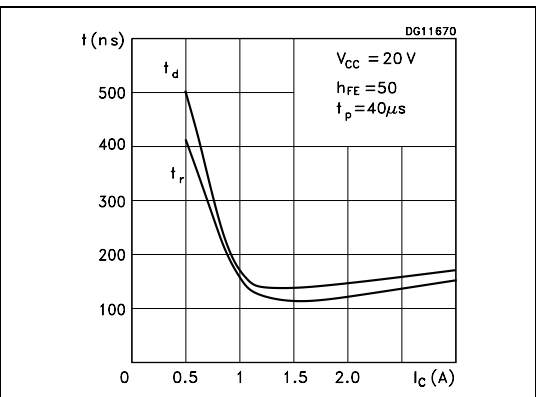
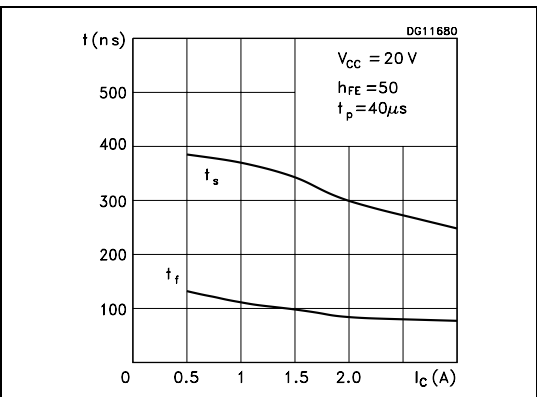
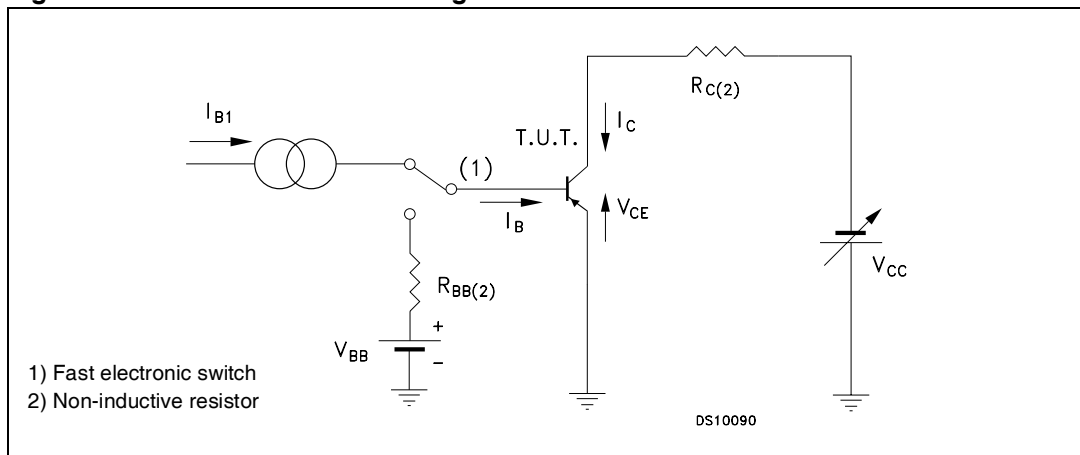


Figure 6. Switching time resistive load



2.2 Test circuits

Figure 7. Resistive load switching test circuit

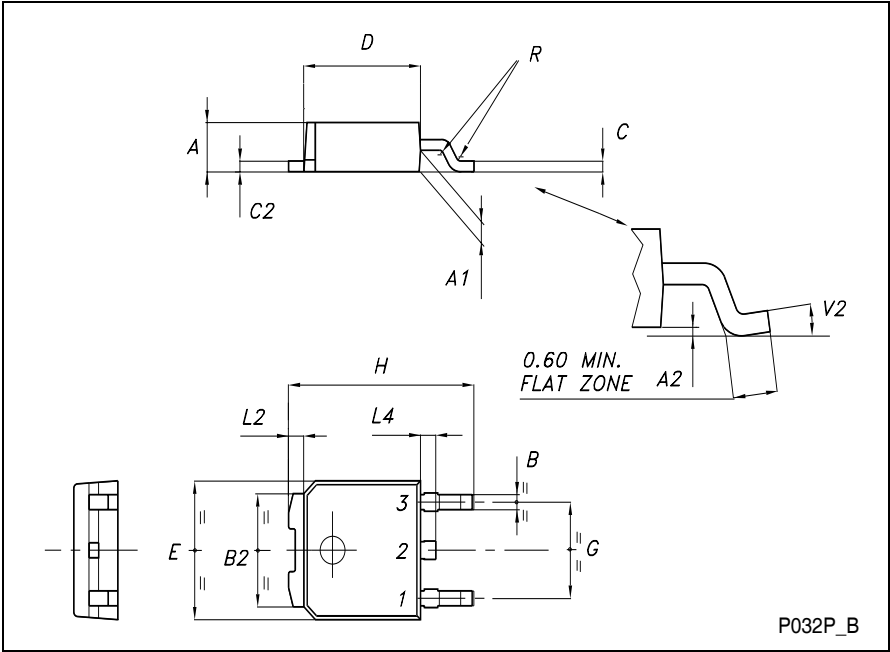


3 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



4 Revision history

Table 4. Revision history

Date	Revision	Changes
24-Mar-2004	1	Initial release.
03-Apr-2006	2	New template.

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