1EDI EiceDRIVER™ Compact

1EDI20N12AF

Single Channel MOSFET and GaN HEMT Gate Driver IC

1EDI20N12AF

Data Sheet

Rev. 2.0, 2015-06-01

Industrial Power Control

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Page or Item	Subjects (major changes since previous revision)
Rev. 2.0, 2015-06-01	
p17	dynamic parameter update
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p 8	application diagram

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Last Trademarks Update 2010-10-26

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1 Overview

Main Features

- Single channel isolated Gate Driver
- Input to output isolation voltage up to 1200 V
- For high voltage power FETs
- 4 A typical peak current at rail-to-rail outputs
- Separate source and sink outputs

Product Highlights

- Galvanically isolated Coreless Transformer Driver
- Low input to output capacitive coupling
- Suitable for operation at high ambient temperature
- Wide input voltage operating range
- ideally suited for driving cascoded or normally-off Gallium Nitride HEMTs

Typical Application

- AC and Brushless DC Motor Drives
- High Voltage PFC, DC/DC-Converter and DC/AC-Inverter
- Induction Heating Resonant Application
- UPS-Systems
- Welding
- Solar MPPT boost converter

Description

The 1EDI20N12AF is a galvanically isolated single channel FET driver in a PG-DSO-8-51 package that provides output currents of at least 2 A at separated output pins.

The input logic pins operate on a wide input voltage range from 3 V to 15 V using CMOS threshold levels to support even 3.3 V microcontroller.

Data transfer across the isolation barrier is realized by the Coreless Transformer Technology.

The undervoltage lockout (UVLO) functions for both input and output chip and an active shutdown feature are included to always guarantee safe operation.

Product Name	Gate Drive Current (min)	Package
1EDI20N12AF	±2.0 A MOSFET level optimized	PG-DSO-8-51
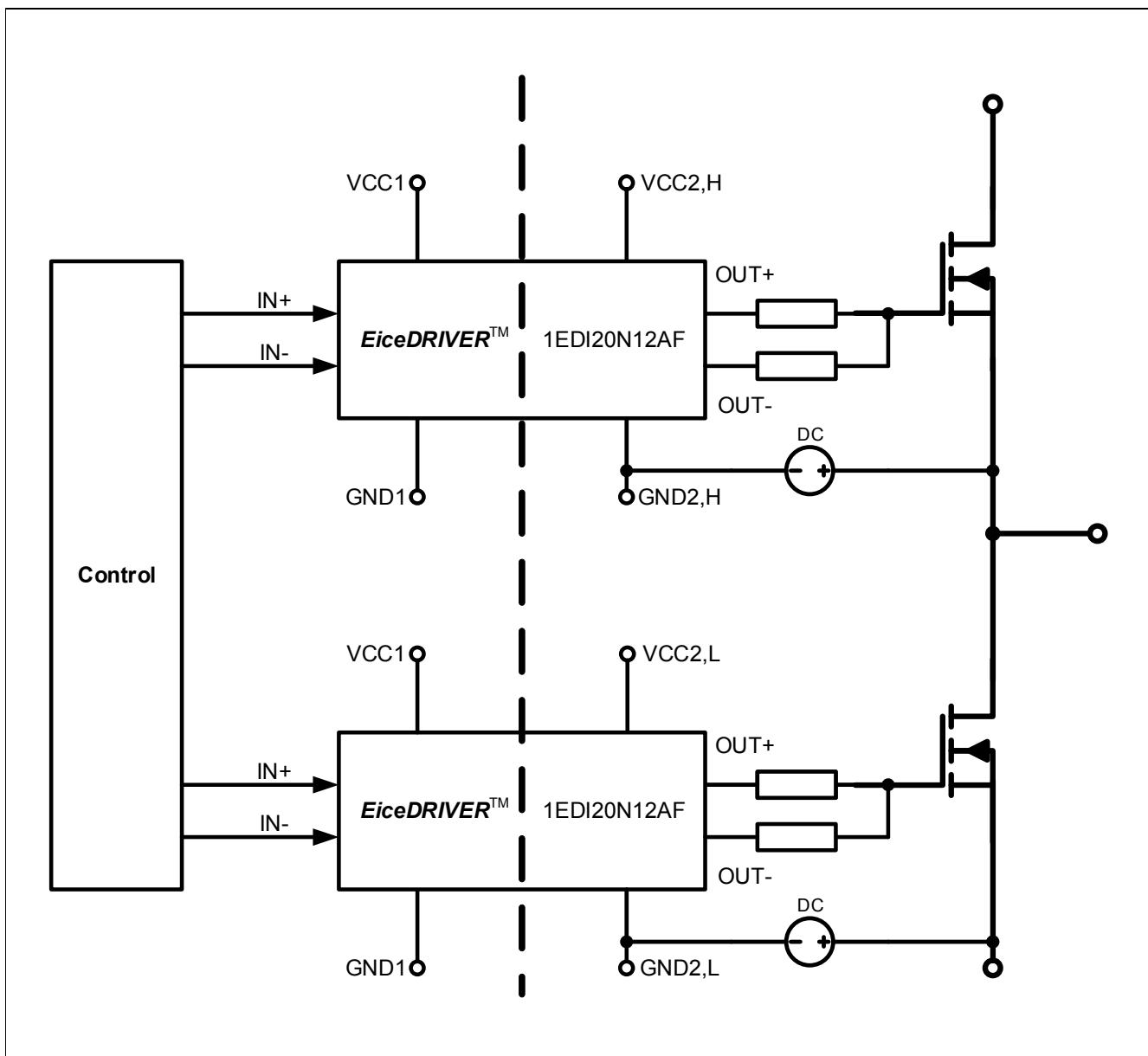
Figure 1   Typical Application

2 Block Diagram
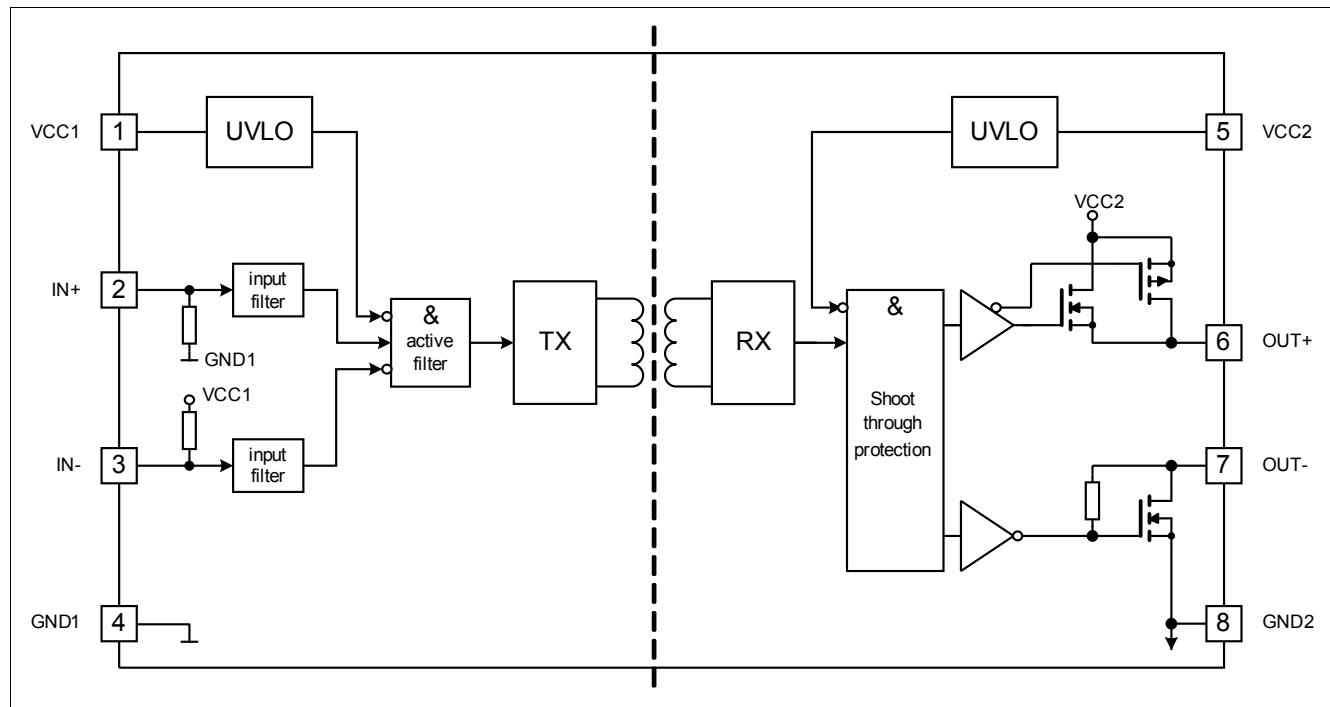
Figure 2 **Block Diagram 1EDI20N12AF**

3 Pin Configuration and Functionality

3.1 Pin Configuration

Table 1 Pin Configuration

Pin No.	Name	Function
1	VCC1	Positive Logic Supply
2	IN+	Non-Inverting Driver Input (active high)
3	IN-	Inverting Driver Input (active low)
4	GND1	Logic Ground
5	VCC2	Positive Power Supply Output Side
6	OUT+	Driver Source Output
7	OUT-	Driver Sink Output
8	GND2	Power Ground
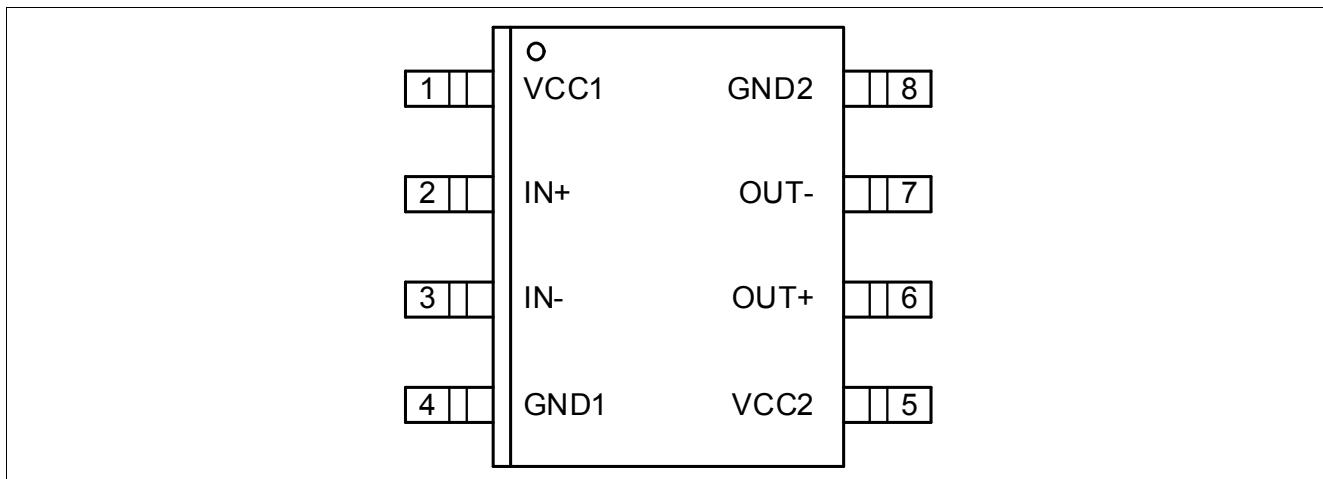
Figure 3 PG-DSO-8-51 (top view)

3.2 Pin Functionality

VCC1

Logic input supply voltage with wide operating range (3.3 V o 15 V).

IN+ Non Inverting Driver Input

IN+ non-inverted control signal for driver output if IN- is set to low. (Output sourcing active at IN+ = high and IN- = low)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at IN+. An internal pull-down-resistor favors off-state.

IN- Inverting Driver Input

IN- inverted control signal for driver output if IN+ is set to high. (Output sourcing active at IN- = low and IN+ = high)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at IN-. An internal pull-up-resistor favors off-state.

GND1

Ground connection of input circuit.

VCC2

Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin.

OUT+ Driver Source Output

Driver output pin sourcing current to turn on external switch transistor. During on-state the driving output is switched to VCC2. Switching of this output is controlled by IN+ and IN-, resp.. This output will also be turned off at an UVLO event.

During turn off the OUT+ terminal is able to sink approx. 100 mA.

OUT- Driver Sink Output)

Driver output pin sinking current to turn off external switch transistor. During off-state the driving output is switched to GND2. Switching of this output is controlled by IN+ and IN-, resp.. In case of UVLO an active shut down keeps the output low.

GND2 Reference Ground

Reference ground of the output driving circuit.

In case of a bipolar supply (positive and negative voltage with respect to switch source potential) this pin is connected to the negative supply voltage.

4 Functional Description

4.1 Introduction

The 1EDI EiceDRIVER™ Compact is a general purpose gate driver. Basic control and protection features support fast and easy design of highly reliable systems.

The galvanic isolation between input logic and driver output is achieved by utilizing on-chip Coreless Transformer Technology. The wide input range supports the direct connection of various signal sources like DSPs and microcontrollers.

The separated rail-to-rail driver outputs simplify gate resistor selection, save an external high current bypass diode and improve dV/dt control.
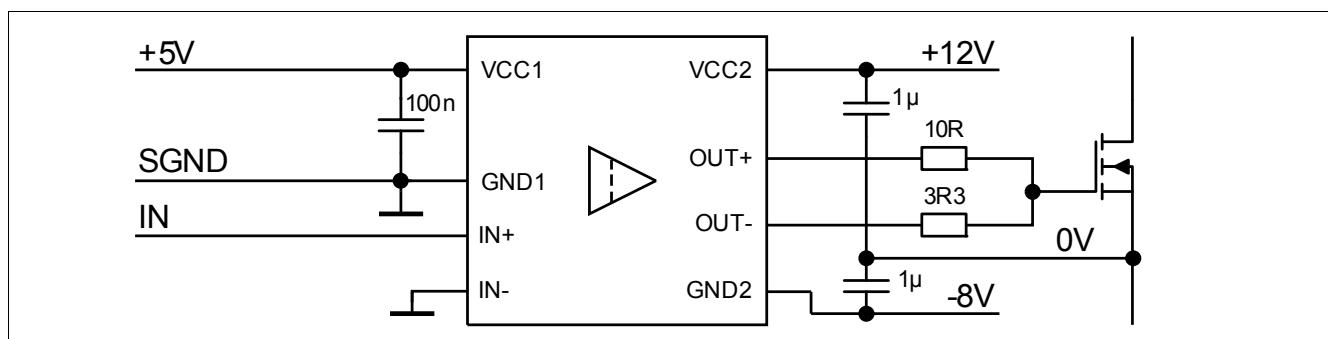
Figure 4   Application Example Bipolar Supply

4.2 Supply

The driver can operate over a wide supply voltage range, either unipolar or bipolar.

With bipolar supply the driver is typically operated with a positive voltage of 12 V at VCC2 and a negative voltage of -8V at GND2 relative to the source potential as seen in **Figure 4**. Negative supply can help to prevent a dynamic turn on.

For unipolar supply configuration the driver is typically supplied with a positive voltage of 12 V at VCC2. In this case, careful evaluation for turn off gate resistor selection is recommended to avoid dynamic turn on (see **Figure 5**).
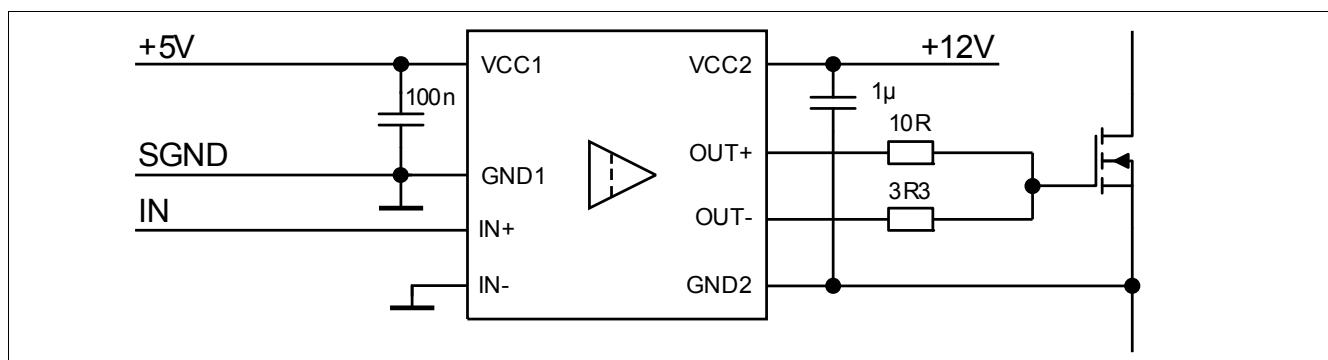
Figure 5   Application Example Unipolar Supply

4.3 Protection Features

4.3.1 Undervoltage Lockout (UVLO)

To ensure correct switching the device is equipped with an undervoltage lockout for input and output independently. Operation starts only after both VCC levels have increased beyond the respective V_{UVLOH} levels (see also **Figure 8**).

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The switch is turned off and the signals at IN+ and IN- are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1} again.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the switch is again turned off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} again.

*Note: V_{VCC2} is always referred to GND2; the output UVLO function thus depends on the total supply voltage.*

4.3.2 Active Shut-Down

The Active Shut-Down feature ensures a safe off-state if the output chip is not connected to the power supply, The gate is clamped at OUT- to GND2.

4.3.3 Short Circuit Clamping

During short circuit the gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT+ limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

4.4 Non-Inverting and Inverting Inputs

There are two possible input modes to control the switch. In the non-inverting mode IN+ controls the driver output while IN- is set to low. In the inverting mode IN- controls the driver output while IN+ is set to high, see **Figure 7**. A minimum input pulse width is required to filter occasional glitches.

4.5 Driver Outputs

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behaviour is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated in the driver.

5 Electrical Parameters

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as absolute limits, i.e. exceeding them may lead to destruction of the integrated circuit.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	**Max.**		
Power supply output side	V_{VCC2}	-0.3	40	V	[1]
Gate driver output	V_{OUT}	V_{GND2}-0.3	V_{VCC2}+0.3	V	–
Positive power supply input side	V_{VCC1}	-0.3	18.0	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	18.0	V	–
Input to output isolation voltage	V_{ISO}	-1200	1200	V	
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Power dissipation (Input side)	$P_{D, IN}$	–	25	mW	[2] @T_A = 25°C
Power dissipation (Output side)	$P_{D, OUT}$	–	400	mW	[2] @T_A = 25°C
Thermal resistance (Input side)	$R_{THJA,IN}$	–	145	K/W	[2] @T_A = 85°C
Thermal resistance (Output side)	$R_{THJA,OUT}$	–	165	K/W	[2] @T_A = 85°C
ESD capability	$V_{ESD,HBM}$	–	2	kV	Human Body Model[3]

1) With respect to GND2.
2) See **Figure 10** for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.
3) According to EIA/JESD22-A114-C (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

5.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Table 3   Operating Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	10	35	V	1)
Power supply input side	V_{VCC1}	3.1	17	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	17	V	–
Switching frequency	f_{sw}	–	4.0	MHz	2) 3)
Ambient temperature	T_A	-40	125	°C	–
Thermal coefficient, junction-top	$\Psi_{th,jt}$	–	4.8	K/W	3) @T_A = 85°C
Common mode transient immunity (CMTI)	$|dV_{ISO}/dt|$	–	100	kV/µs	3) @ 1000 V

1) With respect to GND2.
2) do not exceed max. power dissipation
3) Parameter is not subject to production test - verified by design/characterization

5.3 Electrical Characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 3, GND2 for pins 5 to 7).

5.3.1 Voltage Supply

Table 4   Voltage Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO threshold input chip	V_{UVLOH1}	–	2.85	3.1	V	–
	V_{UVLOL1}	2.55	2.75	–	V	–
UVLO hysteresis input chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	90	100	–	mV	–
UVLO threshold output chip (MOSFET Supply)	V_{UVLOH2}	–	9.1	10.0	V	–
	V_{UVLOL2}	8.0	8.5	–	V	–
UVLO hysteresis output chip (V_{UVLOH2} - V_{UVLOL2})	V_{HYS2}	550	600	–	mV	–

Table 4   **Voltage Supply** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / |
		Min.	Typ.	Max.		Test Condition
Quiescent current input chip	I_{Q1}	–	0.65	1.0	mA	V_{VCC1} = 5 V IN+ = High, IN- = Low =>OUT = High
Quiescent current output chip	I_{Q2}	–	1.2	2.0	mA	V_{VCC2} = 15 V IN+ = High, IN- = Low =>OUT = High

5.3.2   Logic Input

Note: Unless stated otherwise VCC1 = 5.0V

Table 5   **Logic Input**

| Parameter | Symbol | Values | | | Unit | Note / |
		Min.	Typ.	Max.		Test Condition
IN+,IN- low input voltage	V_{IN+L}, V_{IN-L}	–	–	30	%	of VCC1
IN+,IN- high input voltage	V_{IN+H}, V_{IN-H}	70	–	–	%	of VCC1
IN+,IN- low input voltage	V_{IN+L}, V_{IN-L}	–	–	1.5	V	–
IN+,IN- high input voltage	V_{IN+H}, V_{IN-H}	3.5	–	–	V	–
IN- input current	I_{IN-}	–	70	200	µA	V_{IN-} = GND1
IN+ input current	I_{IN+}	–	70	200	µA	V_{IN+} = VCC1

5.3.3   Gate Driver

Table 6   **Gate Driver**

| Parameter | Symbol | Values | | | Unit | Note / |
		Min.	Typ.	Max.		Test Condition
High level output peak current (source) 1EDI20N12AF	$I_{OUT+,PEAK}$	2.0	4.0	–	A	[1] IN+ = High, IN- = Low, V_{VCC2} = 15 V
Low level output peak current (sink) 1EDI20N12AF	$I_{OUT-,PEAK}$	2.0	3.5	–	A	[1] IN+ = Low, IN- = Low, V_{VCC2} = 15 V

[1] voltage across the device $V_{(VCC2 - OUT+)}$ or $V_{(OUT- - GND2)}$ < V_{VCC2}.

5.3.4 Short Circuit Clamping

Table 7   Short Circuit Clamping

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage (OUT+) (V_{OUT} - V_{VCC2})	V_{CLPout}	–	0.9	1.3	V	IN+ = High, IN- = Low, OUT = High I_{OUT} = 500 mA pulse test, t_{CLPmax} = 10 µs)

5.3.5 Dynamic Characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V and V_{VCC2} = 15 V.

Table 8   Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input IN to output propagation delay ON	T_{PDON}	90	115	137	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @ 25°C
Input IN to output propagation delay OFF	T_{PDOFF}	100	120	143	ns	
Input IN to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-15	5	25	ns	
Input pulse suppression IN+, IN-	T_{MININ+}, T_{MININ-}	30	40	–	ns	–
IN input to output propagation delay ON variation due to temp	T_{PDONt}	–	–	10	ns	[1]C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN input to output propagation delay OFF variation due to temp	T_{PDOFFt}	–	–	10	ns	[1]C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN input to output propagation delay distortion variation due to temp (T_{PDOFF}-T_{PDON})	$T_{PDISTOt}$	–	–	4	ns	[1]C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
Rise time	T_{RISE}	5	10	20	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%
Fall time	T_{FALL}	4	9	19	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%

1) The parameter is not subject to production test - verified by design/characterization

5.3.6 Active Shut Down

Table 9   Active Shut Down

Parameter	Symbol	Values			Unit	Note /
		Min.	**Typ.**	**Max.**		**Test Condition**
Active shut down voltage	V_{ACTSD}[1]	–	2.2	2.5	V	$I_{\text{OUT-}}/I_{\text{OUT-,PEAK}}$=0.1, V_{CC2} open

1) Referred to GND2

6 Timing Diagramms
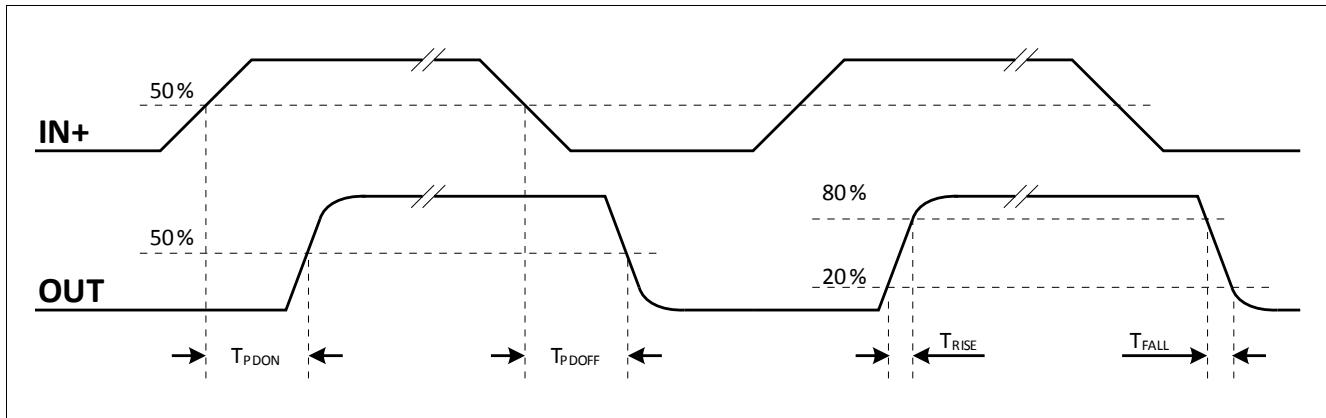
Figure 6 Propagation Delay, Rise and Fall Time
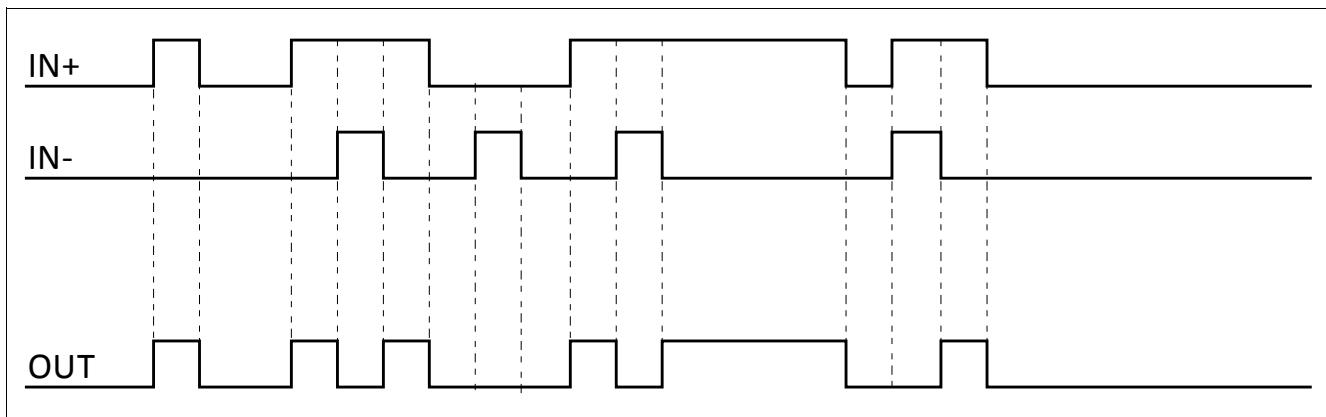
Figure 7 Typical Switching Behavior
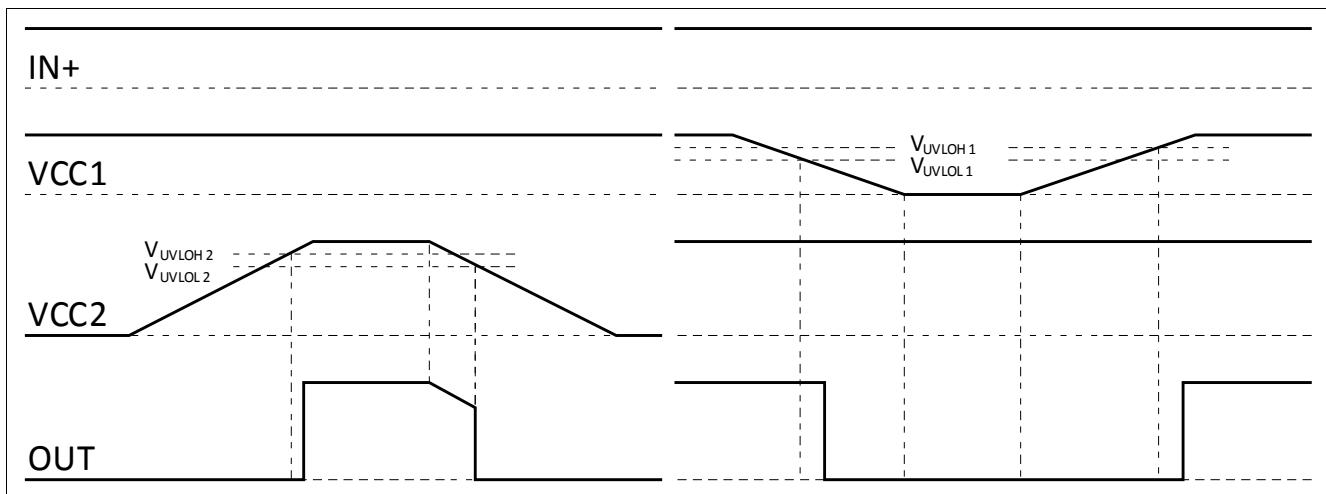

Figure 8 UVLO Behavior

7 Package Outlines

1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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02

Figure 9   PG-DSO-8-51 (Plastic (Green) Dual Small Outline Package)

8 Application Notes

8.1 Reference Layout for Thermal Data

The PCB layout shown in **Figure 10** represents the reference layout used for the thermal characterisation. Pin 4 (GND1) and pin 8 (GND2) require each a ground plane of 100 mm² for achieving maximum power dissipation. The 1EDI20N12AF is conceived to dissipate most of the heat generated through these pins.

The thermal coefficient junction-top ($\Psi_{th,jt}$) can be used to calculate the junction temperature at a given top case temperature and driver power dissipation:

$$T_j \; = \; \Psi_{th,jt} \cdot P_D + T_{top}$$
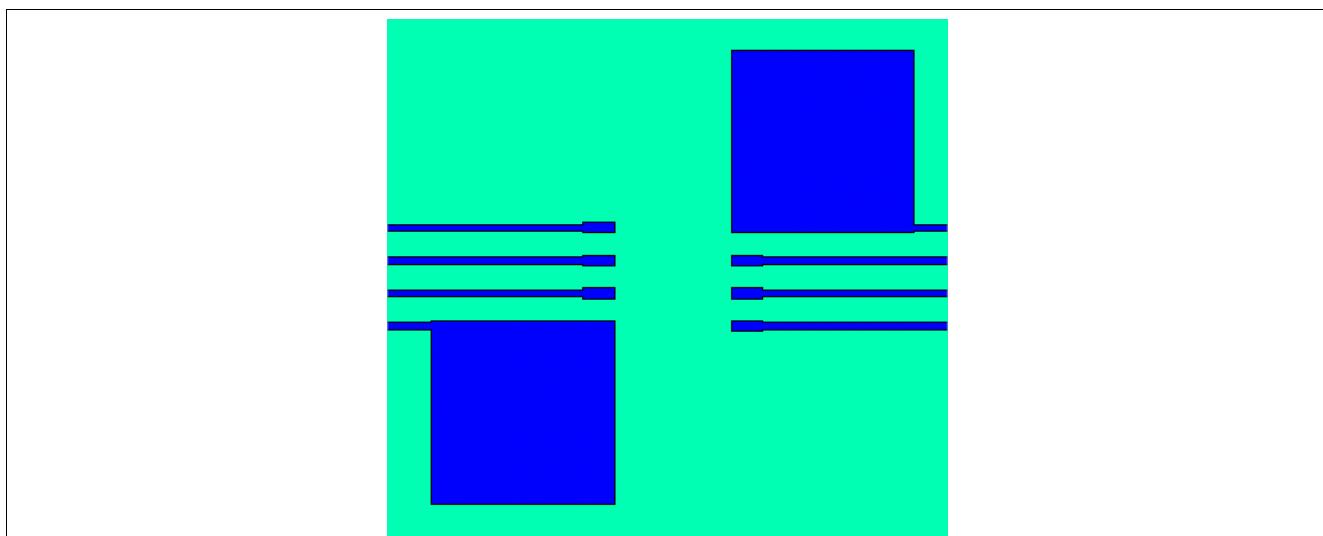
Figure 10   Reference Layout for Thermal Data (Copper thickness 35 µm)

8.2 Printed Circuit Board Guidelines

The following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and to reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.