# HM62256B Series

32,768-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-135D (Z)
Rev. 4.0
Nov. 29, 1995

## Description

The Hitachi HM62256B is a CMOS static RAM organized 32-kword × 8-bit. It realizes higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology. The device, packaged in 8 × 14 mm TSOP, 8 × 13.4 mm TSOP with thickness of 1.2 mm, 450-mil SOP (foot print pitch width), 600-mil plastic DIP, or 300-mil plastic DIP, is available for high density mounting. It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems.

## Features

- High speed
  Fast access time: 45/55/70/85 ns (max)
- Low power
  Standby: 1.0 µW (typ)
  Operation: 25 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- Directly TTL compatible
  All inputs and outputs
- Capability of battery back up operation

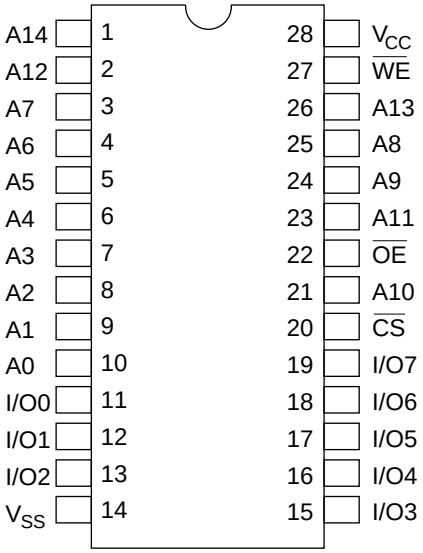
## Ordering Information

| Type No. | Access Time | Package |
|---|---|---|
| HM62256BLP-7 | 70 ns | 600-mil 28-pin plastic DIP (DP-28) |
| HM62256BLP-7SL | 70 ns | |
| HM62256BLSP-7 | 70 ns | 300-mil 28-pin plastic DIP (DP-28NA) |
| HM62256BLSP-7SL | 70 ns | |
| HM62256BLFP-7T | 70 ns | 450-mil 28-pin plastic SOP (FP-28DA) |
| HM62256BLFP-4SLT[*1] | 45 ns | |
| HM62256BLFP-5SLT | 55 ns | |
| HM62256BLFP-7SLT | 70 ns | |
| HM62256BLFP-7ULT | 70 ns | |
| HM62256BLT-8 | 85 ns | 8 mm × 14 mm 32-pin TSOP (TFP-32DA) |
| HM62256BLT-7SL | 70 ns | |
| HM62256BLTM-8 | 85 ns | 8 mm × 13.4 mm 28-pin TSOP (TFP-28DA) |
| HM62256BLTM-4SL[*1] | 45 ns | |
| HM62256BLTM-5SL | 55 ns | |
| HM62256BLTM-7SL | 70 ns | |
| HM62256BLTM-7UL | 70 ns | |

Note: 1. Under development

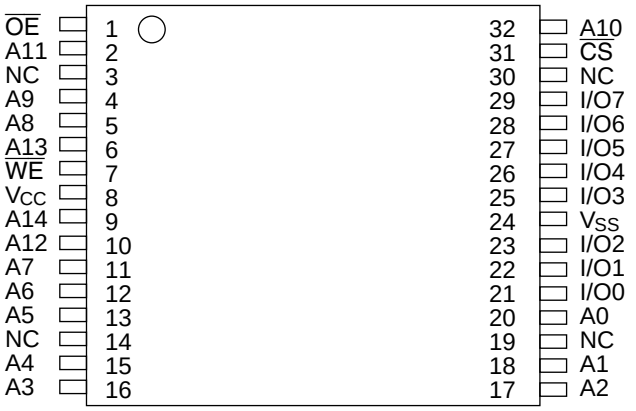
## Pin Arrangement

HM62256BLP/BLFP/BLSP Series



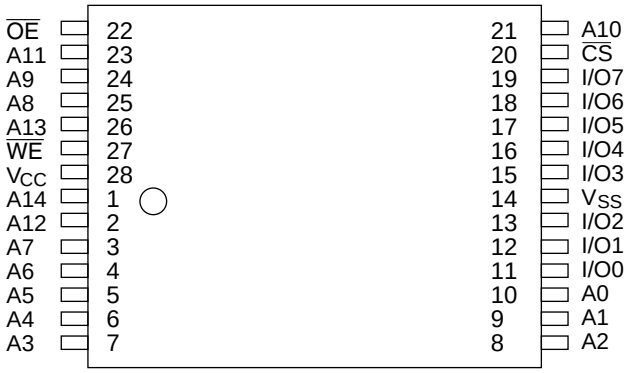

(Top View)

HM62256BLT Series




(Top View)

HM62256BLTM Series

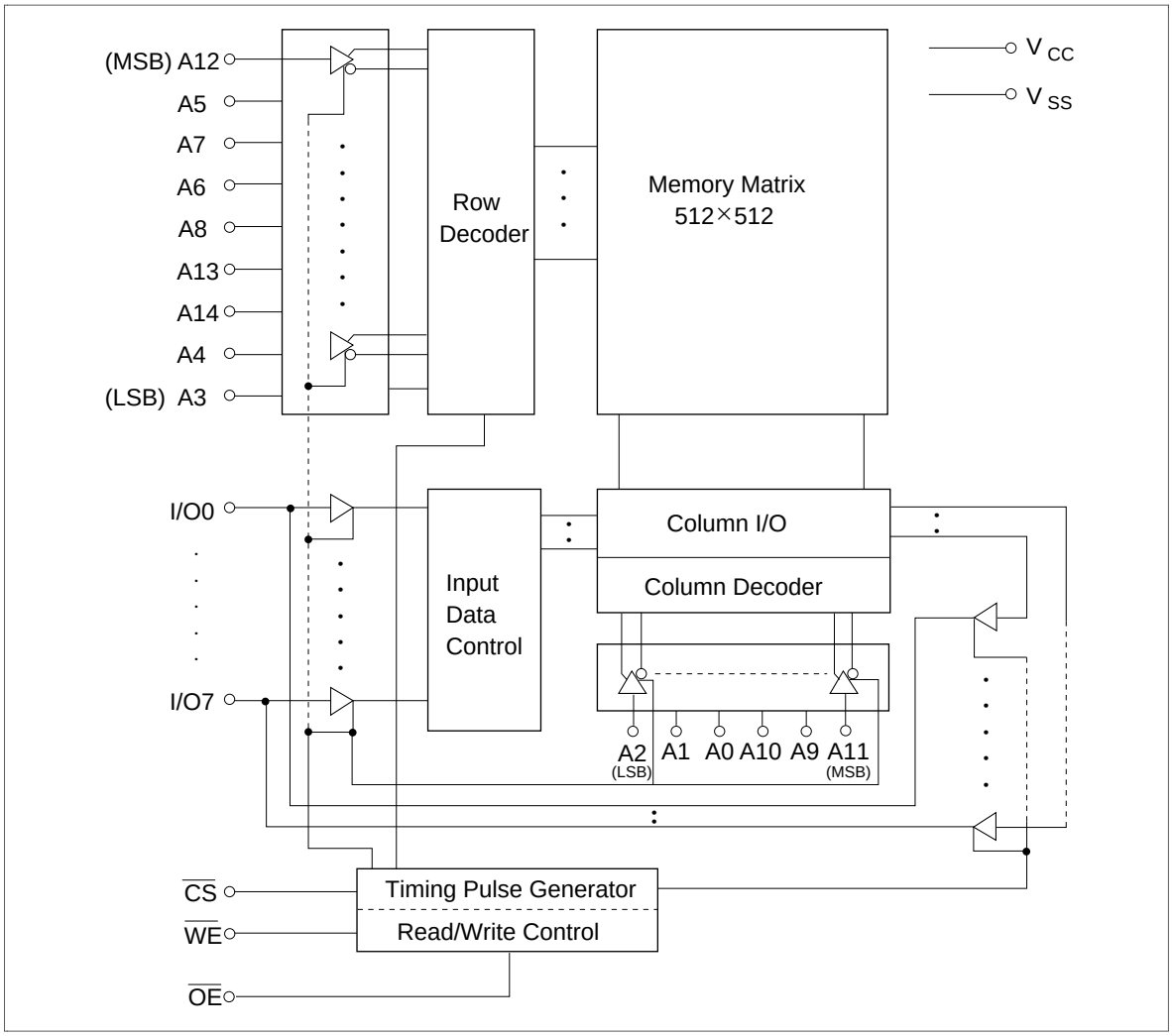



(Top View)

## Pin Description

| Symbol | Function |
|---|---|
| A0 – A14 | Address |
| I/O0 – I/O7 | Input/output |
| $\overline{CS}$ | Chip select |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| NC | No connection |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |

## Block Diagram




## Function Table

| $\overline{WE}$ | $\overline{CS}$ | $\overline{OE}$ | Mode | $V_{CC}$ Current | I/O Pin | Ref. Cycle |
|---|---|---|---|---|---|---|
| X | H | X | Not selected | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| H | L | H | Output disable | $I_{CC}$ | High-Z | — |
| H | L | L | Read | $I_{CC}$ | Dout | Read cycle (1)–(3) |
| L | L | H | Write | $I_{CC}$ | Din | Write cycle (1) |
| L | L | L | Write | $I_{CC}$ | Din | Write cycle (2) |

Note: X: H or L

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage[*1] | $V_{CC}$ | −0.5 to +7.0 | V |
| Terminal voltage[*1] | $V_T$ | −0.5[*2] to $V_{CC}$ + 0.3[*3] | V |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to + 70 | °C |
| Storage temperature | Tstg | −55 to +125 | °C |
| Storage temperature under bias | Tbias | −10 to +85 | °C |

Notes: 1. Relative to $V_{SS}$
2. $V_T$ min: −3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 7.0 V

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input high (logic 1) voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$+0.3 | V |
| Input low (logic 0) voltage | $V_{IL}$ | −0.5 [*1] | — | 0.8 | V |

Note: 1. $V_{IL}$ min: −3.0 V for pulse half-width ≤ 50 ns

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ±10%, $V_{SS}$ = 0 V)

| Parameter | | Symbol | Min | Typ*1 | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | | \|ILI\| | — | — | 1 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Output leakage current | | $\|I_{LO}\|$ | — | — | 1 | µA | $\overline{CS}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$, $V_{SS} \le V_{I/O} \le V_{CC}$ |
| Operating power supply current | | $I_{CC}$ | — | 6 | 15 | mA | $\overline{CS}$ = $V_{IL}$, others = $V_{IH}/V_{IL}$<br>$I_{I/O}$ = 0 mA |
| Average operating power supply current | HM62256B-4 | $I_{CC1}$ | — | — | 70 | mA | min cycle, duty = 100 %, $I_{I/O}$ = 0 mA<br>$\overline{CS}$ = $V_{IL}$, others = $V_{IH}/V_{IL}$ |
| | HM62256B-5 | $I_{CC1}$ | — | — | 60 | | |
| | HM62256B-7 | $I_{CC1}$ | — | 33 | 60 | | |
| | HM62256B-8 | $I_{CC1}$ | — | 29 | 50 | | |
| | | $I_{CC2}$ | — | 5 | 15 | mA | Cycle time = 1 µs, $I_{I/O}$ = 0 mA<br>$\overline{CS}$ = $V_{IL}$, $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0 |
| Standby power supply current | | $I_{SB}$ | — | 0.3 | 2 | mA | $\overline{CS}$ = $V_{IH}$ |
| | | $I_{SB1}$ | — | 0.2 | 100 | µA | Vin ≥ 0 V, $\overline{CS}$ ≥ $V_{CC}$ – 0.2 V, |
| | | | — | 0.2*2 | 50*2 | | |
| | | | | 0.2*3 | 10*3 | | |
| Output low voltage | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 2.1 mA |
| Output high voltage | | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –1.0 mA |

Notes: 1. Typical values are at $V_{CC}$ = 5.0 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-SL version.
3. This characteristics is guaranteed only for L-UL version.

## Capacitance (Ta = 25°C, f = 1.0 MHz)*1

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input capacitance*1 | Cin | — | — | 8 | pF | Vin = 0 V |
| Input/output capacitance*1 | $C_{I/O}$ | — | — | 10 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, unless otherwise noted.)

### Test Conditions

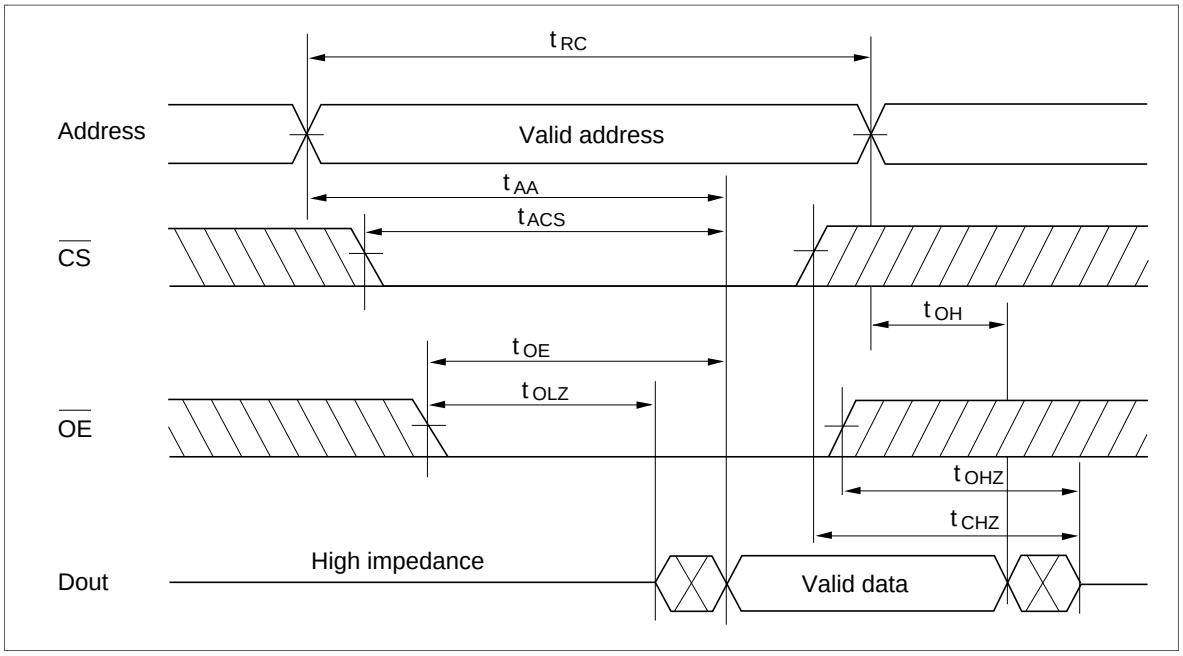
- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5 V
- Output load: HM62256B-4: 1 TTL Gate + $C_L$ (30 pF)(Including scope & jig)
  HM62256B-5: 1 TTL Gate + $C_L$ (50 pF)(Including scope & jig)
  HM62256B-7/8: 1 TTL Gate + $C_L$ (100 pF)(Including scope & jig)

### Read Cycle

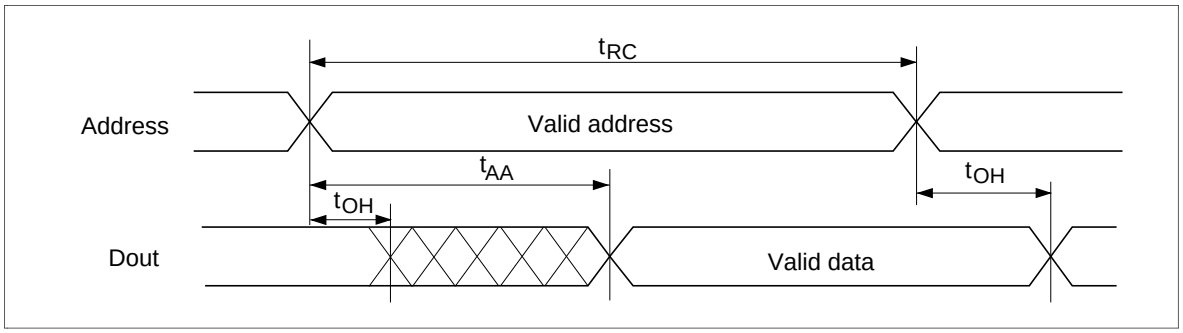
| | | HM62256B | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | -4 | | -5 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Read cycle time | $t_{RC}$ | 45 | — | 55 | — | 70 | — | 85 | — | ns | |
| Address access time | $t_{AA}$ | — | 45 | — | 55 | — | 70 | — | 85 | ns | |
| Chip select access time | $t_{ACS}$ | — | 45 | — | 55 | — | 70 | — | 85 | ns | |
| Output enable to output valid | $t_{OE}$ | | 30 | — | 35 | — | 40 | — | 45 | ns | |
| Chip selection to output in low-Z | $t_{CLZ}$ | 5 | — | 5 | — | 10 | — | 10 | — | ns | 2 |
| Output enable to output in low-Z | $t_{OLZ}$ | 5 | — | 5 | — | 5 | — | 5 | — | ns | 2 |
| Chip deselection in to output in high-Z | $t_{CHZ}$ | 0 | 20 | 0 | 20 | 0 | 25 | 0 | 30 | ns | 1, 2 |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 20 | 0 | 20 | 0 | 25 | 0 | 30 | ns | 1, 2 |
| Output hold from address change | $t_{OH}$ | 5 | — | 5 | — | 5 | — | 10 | — | ns | |

Notes: 1. $t_{CHZ}$ and $t_{OHZ}$ defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.

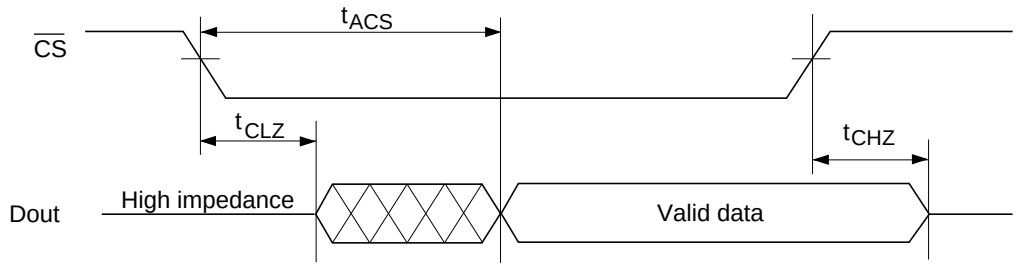
**Read Timing Waveform (1)** ($\overline{WE}$=$V_{IH}$)




**Read Timing Waveform (2)** ($\overline{WE}$=$V_{IH}$, $\overline{CS}$=$V_{IL}$, $\overline{OE}$=$V_{IL}$)



**Read Timing Waveform (3)** ($\overline{WE}$=$V_{IH}$, $\overline{OE}$=$V_{IL}$)[*1]



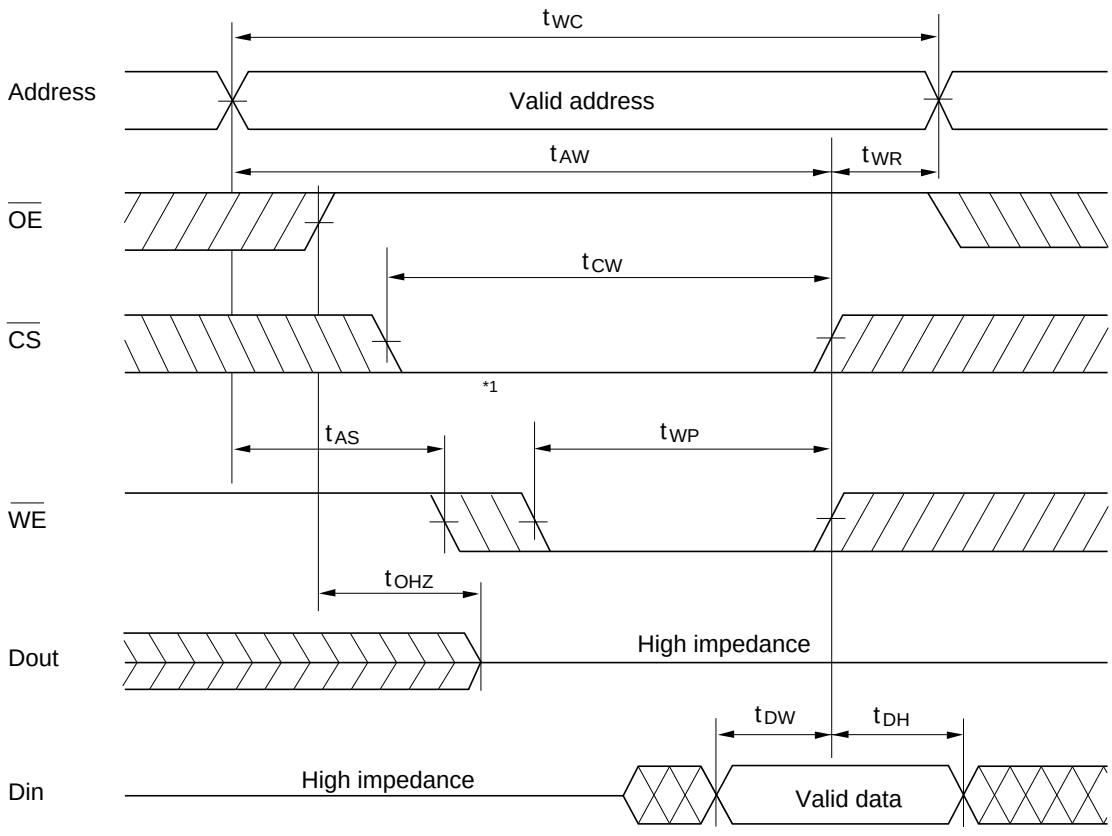

Note: 1. Address must be valid prior to or simultaneously with $\overline{CS}$ going low.

### Write Cycle

| | | HM62256B | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | -4 | | -5 | | -7 | | -8 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Write cycle time | $t_{WC}$ | 45 | — | 55 | — | 70 | — | 85 | — | ns | |
| Chip selection to end of write | $t_{CW}$ | 35 | — | 40 | — | 60 | — | 75 | — | ns | 4 |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 5 |
| Address valid to end of write | $t_{AW}$ | 35 | — | 40 | — | 60 | — | 75 | — | ns | |
| Write pulse width | $t_{WP}$ | 30 | — | 35 | — | 50 | — | 55 | — | ns | 3, 8 |
| Write recovery time | $t_{WR}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 6 |
| $\overline{WE}$ to output in high-Z | $t_{WHZ}$ | 0 | 20 | 0 | 20 | 0 | 25 | 0 | 40 | ns | 1, 2, 7 |
| Data to write time overlap | $t_{DW}$ | 20 | — | 25 | — | 30 | — | 35 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Output active from end of write | $t_{OW}$ | 5 | — | 5 | — | 5 | — | 5 | — | ns | 2 |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 20 | 0 | 20 | 0 | 25 | 0 | 40 | ns | 1, 2, 7 |

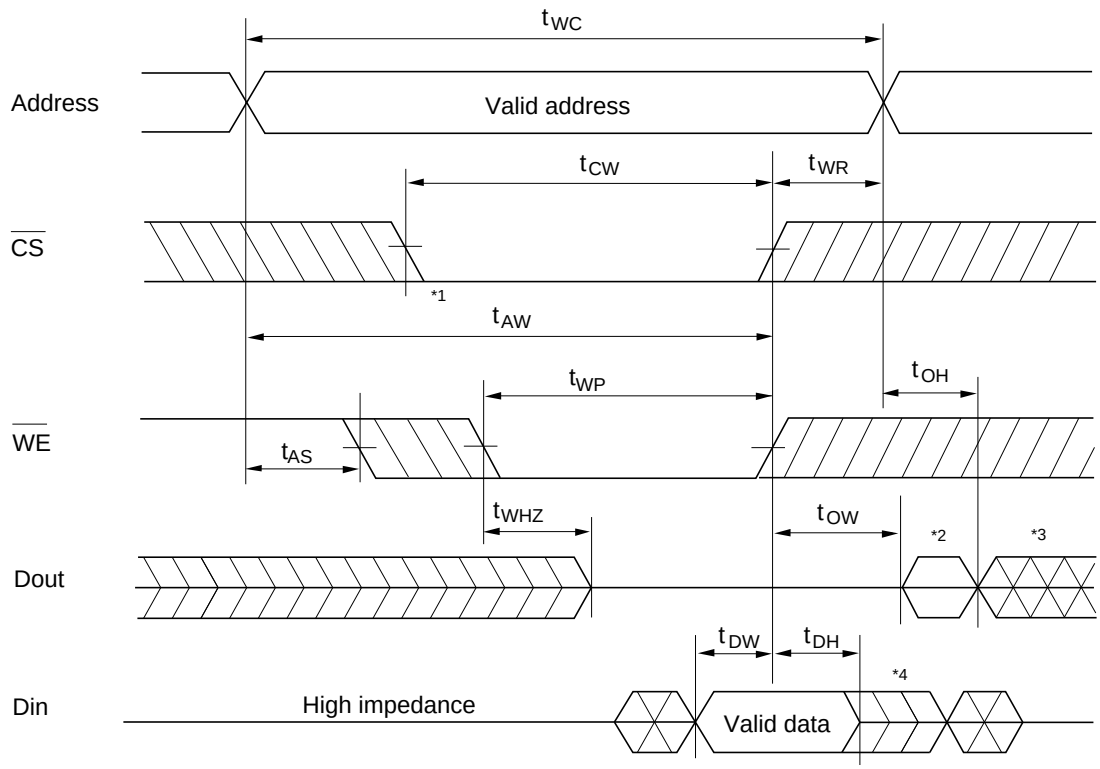
Notes:
1. $t_{OHZ}$ and $t_{WHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. $t_{WP}$ is measured from the beginning of write to the end of write.
4. $t_{CW}$ is measured from $\overline{CS}$ going low to the end of write.
5. $t_{AS}$ is measured from the address valid to the beginning of write.
6. $t_{WR}$ is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
7. Durng this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. In the write cycle with $\overline{OE}$ low fixed, $t_{WP}$ must satisfy the following equation to avoid a problem of data bus contention, $t_{WP} \geq t_{WHZ}$ max + $t_{DW}$ min.

**Write Timing Waveform (1)** ($\overline{OE}$ Clock)




Note: 1. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.

**Write Timing Waveform (2)** ($\overline{OE}$ Low Fixed) ($\overline{OE}$ = $V_{IL}$)



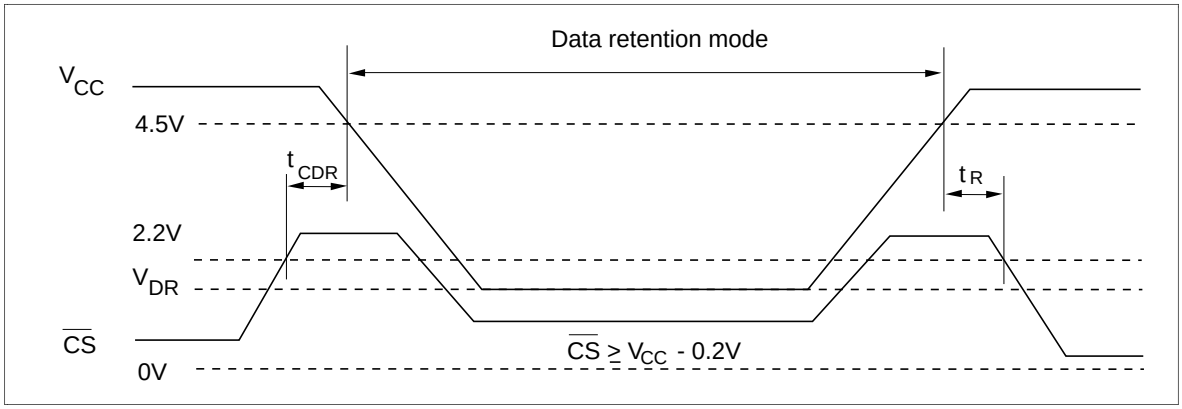

Notes: 1. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.
2. Dout is the same phase of the write data of this write cycle.
3. Dout is the read data of next address.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.

## Low $V_{CC}$ Data Retention Characteristics (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ*[1] | Max | Unit | Test Conditions*[6] |
|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | 5.5 | V | $\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V |
| Data retention current | $I_{CCDR}$ | — | 0.05 | 30*[2] | µA | $V_{CC}$ = 3.0 V, Vin ≥ 0 V |
| | | — | 0.05 | 10*[3] | | $\overline{CS} \geq V_{CC} - 0.2$ V, |
| | | — | 0.05 | 3*[4] | | |
| Chip deselect to data retention time | $t_{CDR}$ | 0 | — | — | ns | See retention waveform |
| Operation recovery time | $t_R$ | $t_{RC}$*[5] | — | — | ns | |

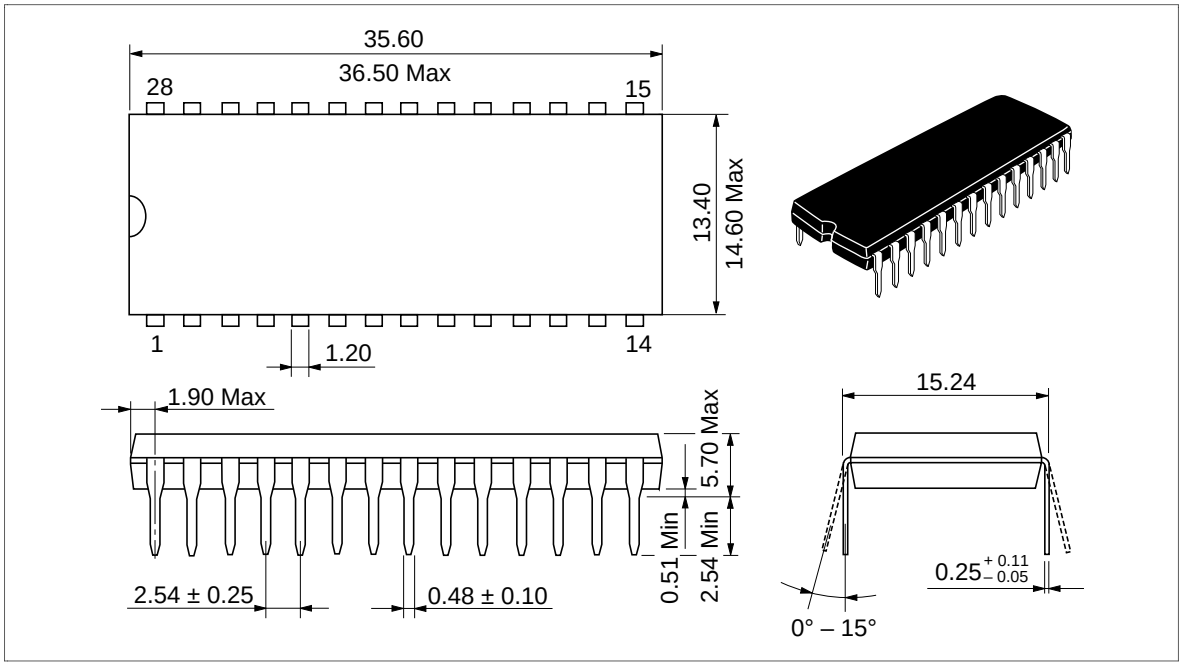
Notes: 1. Typical values are at $V_{CC}$ = 3.0 V, Ta = 25°C and not guaranteed.
2. 10 µA max at Ta = 0 to + 40°C.
3. This characteristics guaranteed for only L-SL version. 3 µA max at Ta = 0 to +40°C.
4. This characteristics guaranteed for only L-UL version. 0.6 µA max at Ta = 0 to +40°C.
5. $t_{RC}$ = read cycle time.
6. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

### Low $V_{CC}$ Data Retention Timing Waveform

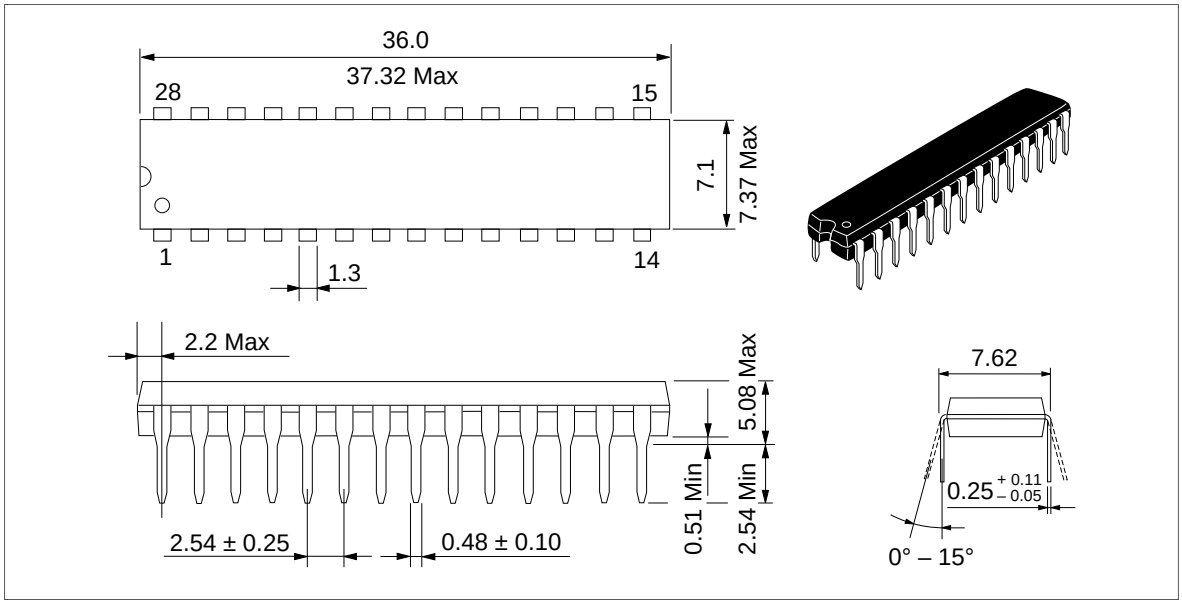


## Package Dimensions

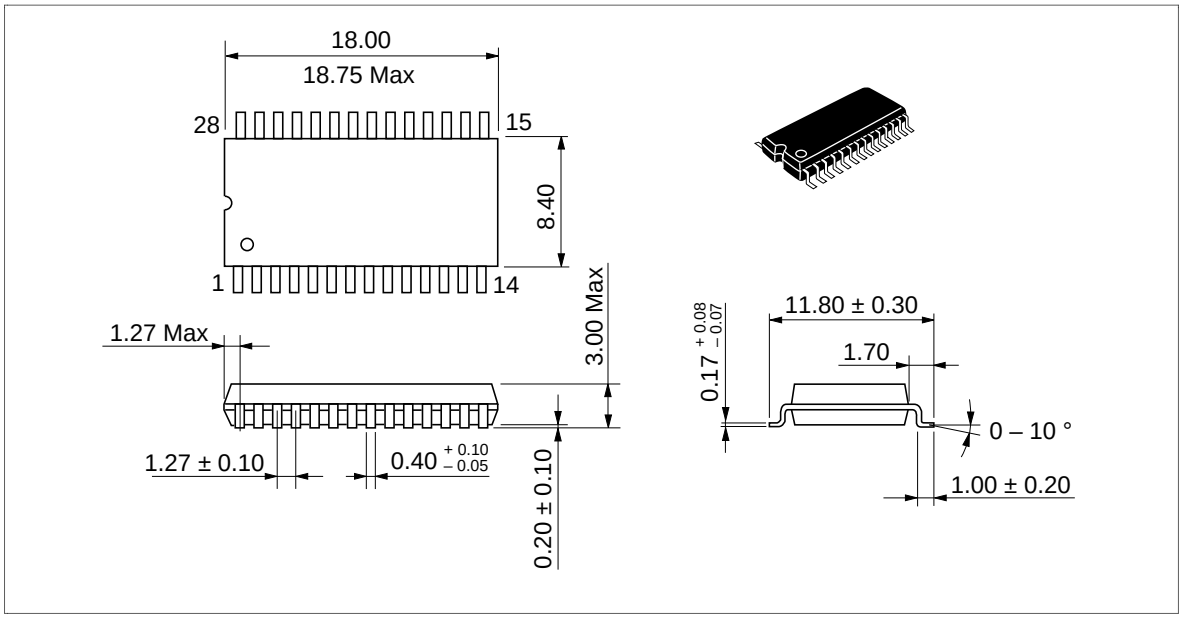
**HM62256BLP Series** (DP-28) Unit: mm




**HM62256BLSP Series** (DP-28NA) Unit: mm



**HM62256BLFP Series** (FP-28DA) Unit: mm




**HM62256BLT Series** (TFP-32DA) Unit: mm