

IRFPS37N50APbF

SMPS MOSFET

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
500V	0.13 Ω	36A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified (See AN 1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	36	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	23	
I_{DM}	Pulsed Drain Current ①	144	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	446	W
	Linear Derating Factor	3.6	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Full Bridge Converters
- Power Factor Correction Boost

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.13	Ω	$V_{GS} = 10V, I_D = 22A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	20	—	—	S	$V_{DS} = 50V, I_D = 22A$
Q_g	Total Gate Charge	—	—	180	nC	$I_D = 36A$
Q_{gs}	Gate-to-Source Charge	—	—	46		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	71		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	98	—		$I_D = 36A$
$t_{d(off)}$	Turn-Off Delay Time	—	52	—		$R_G = 2.15\Omega$
t_f	Fall Time	—	80	—		$R_D = 7.0\Omega$, See Fig. 10 ④
C_{iss}	Input Capacitance	—	5579	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	810	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	36	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	7905	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	221	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	400	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤

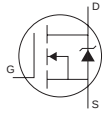
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	1260	mJ
I_{AR}	Avalanche Current①	—	36	A
E_{AR}	Repetitive Avalanche Energy①	—	44	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.28	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	36	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	144		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 36A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	570	860	ns	$T_J = 25^\circ\text{C}, I_F = 36A$
Q_{rr}	Reverse Recovery Charge	—	8.6	13	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

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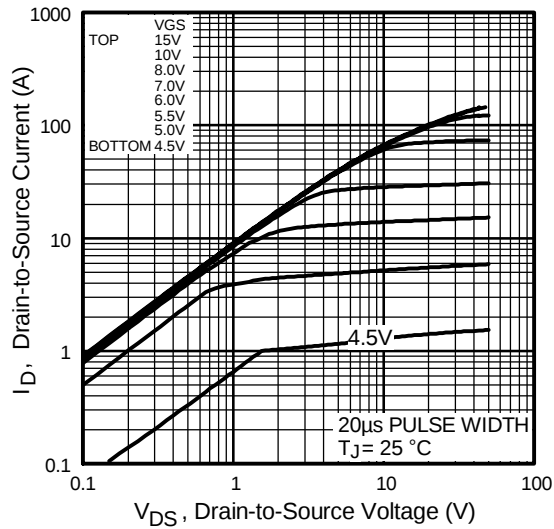


Fig 1. Typical Output Characteristics

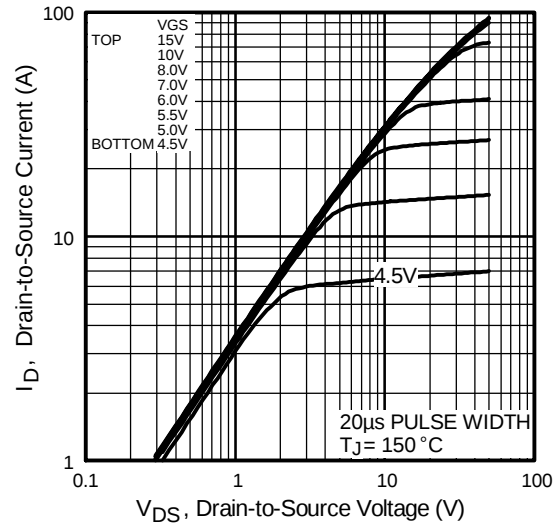


Fig 2. Typical Output Characteristics

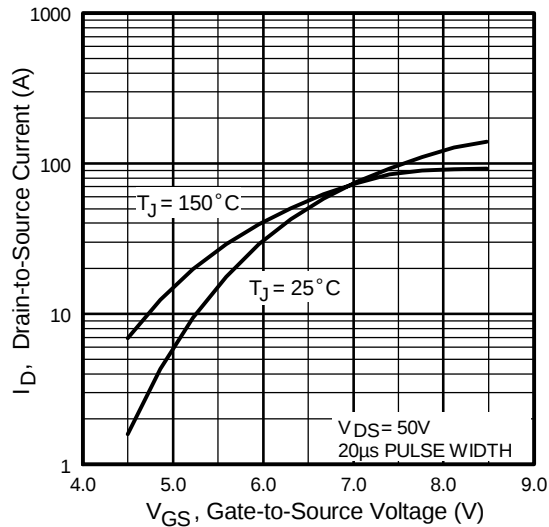


Fig 3. Typical Transfer Characteristics

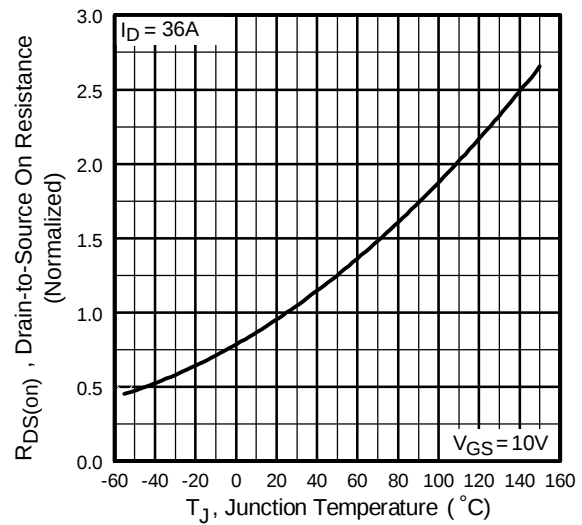


Fig 4. Normalized On-Resistance Vs. Temperature

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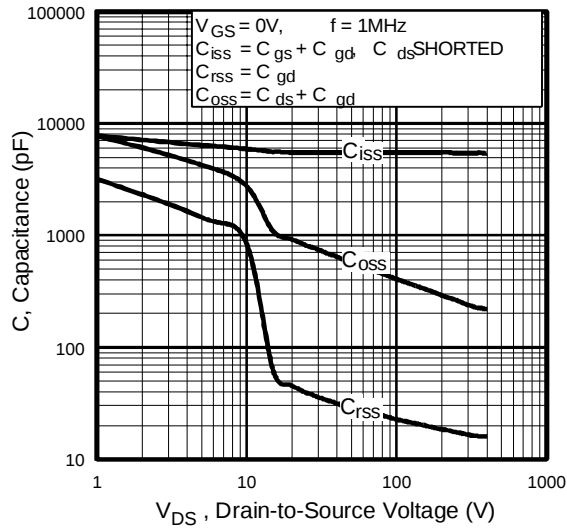


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

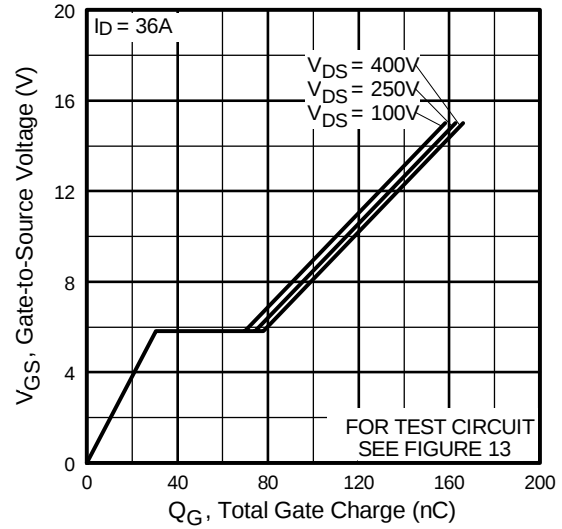


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

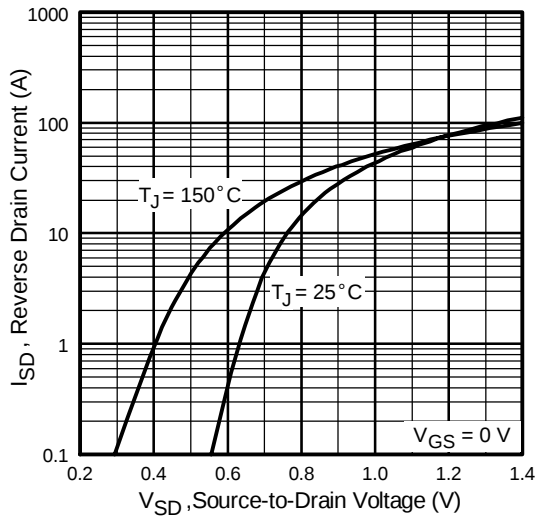


Fig 7. Typical Source-Drain Diode Forward Voltage

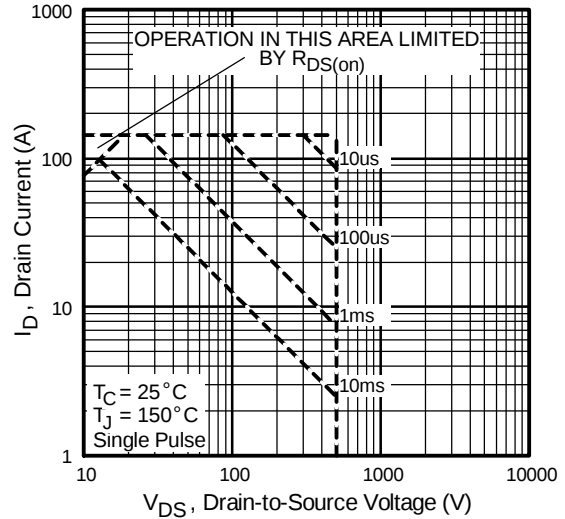


Fig 8. Maximum Safe Operating Area

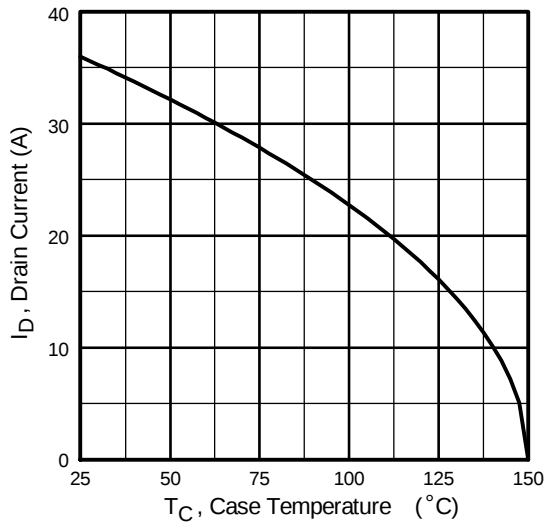


Fig 9. Maximum Drain Current Vs. Case Temperature

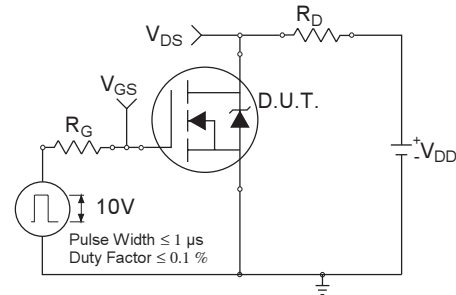


Fig 10a. Switching Time Test Circuit

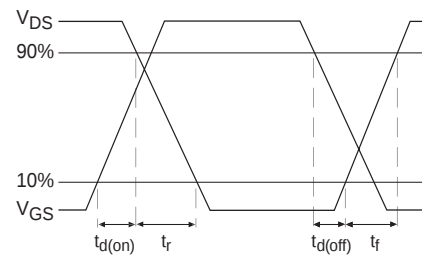


Fig 10b. Switching Time Waveforms

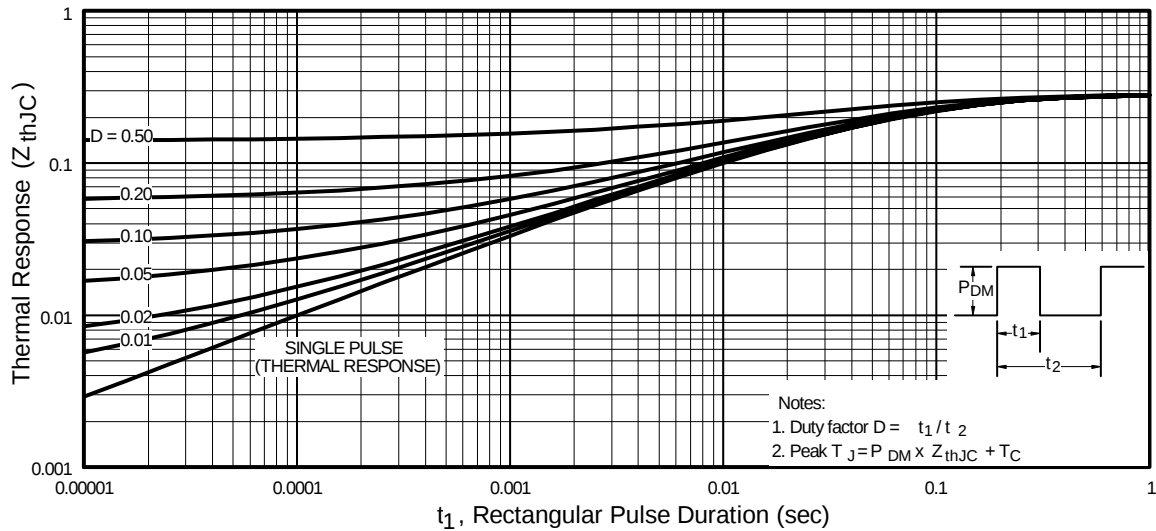


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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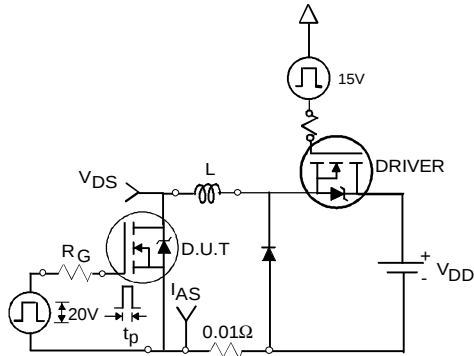


Fig 12a. Unclamped Inductive Test Circuit

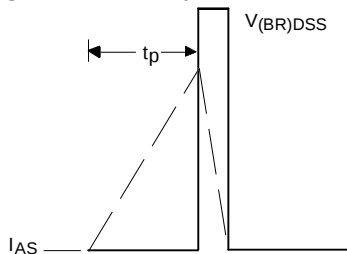


Fig 12b. Unclamped Inductive Waveforms

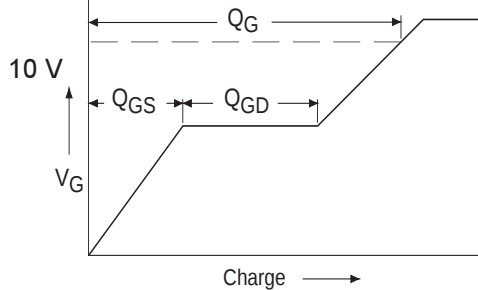


Fig 13a. Basic Gate Charge Waveform

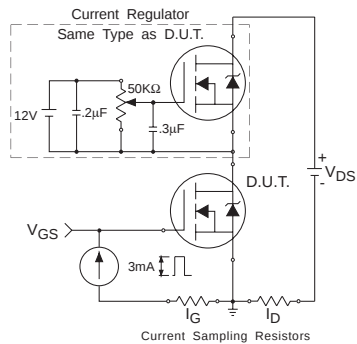


Fig 13b. Gate Charge Test Circuit

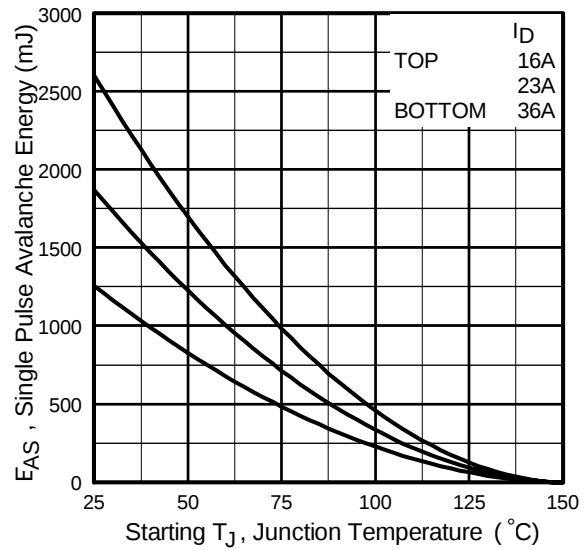


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

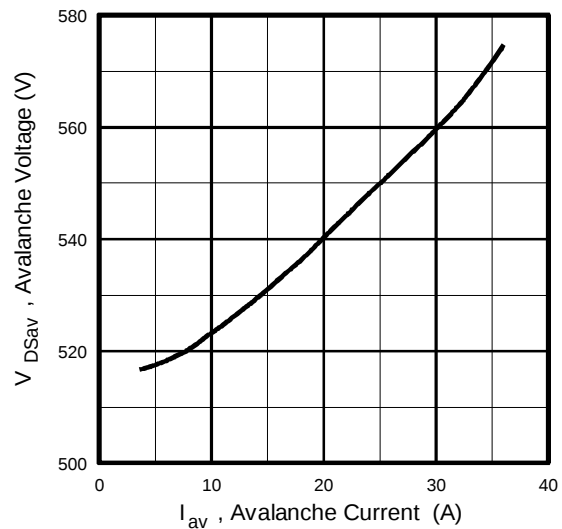
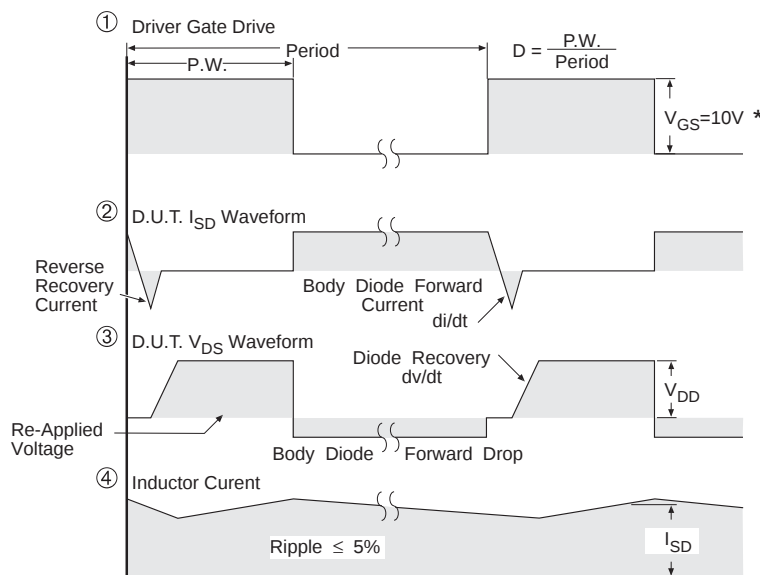
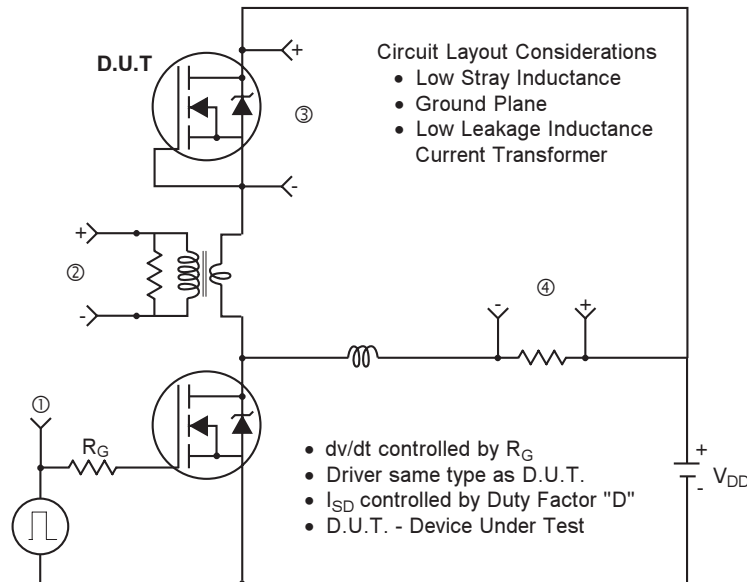


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

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Peak Diode Recovery dv/dt Test Circuit



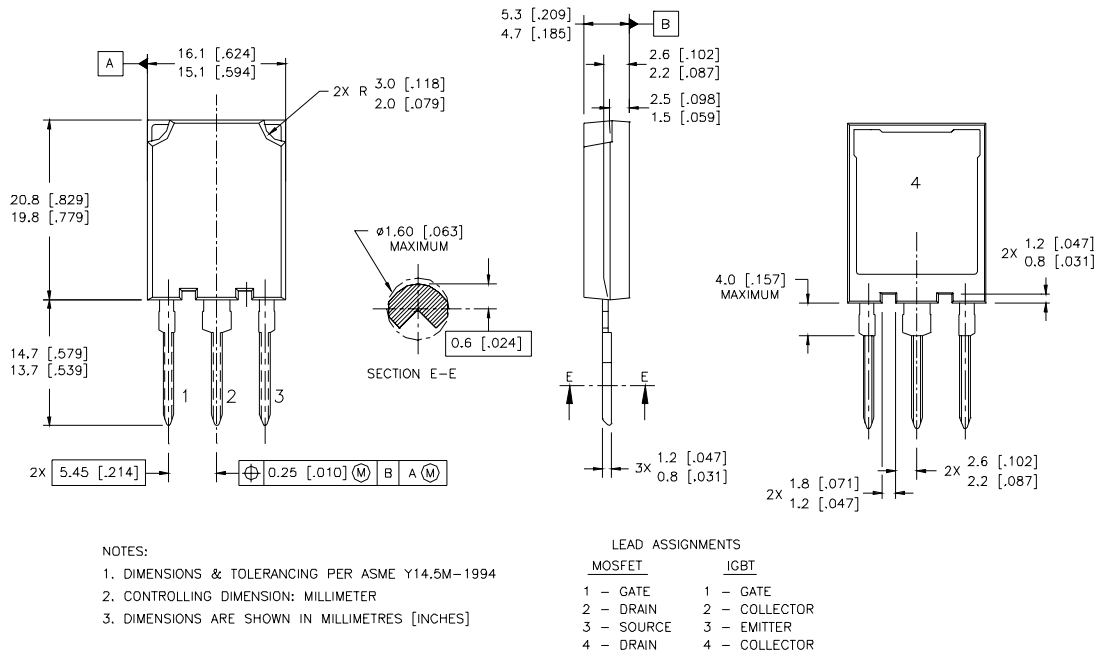
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-channel HEXFET® Power MOSFETs

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Case Outline and Dimensions — Super-247

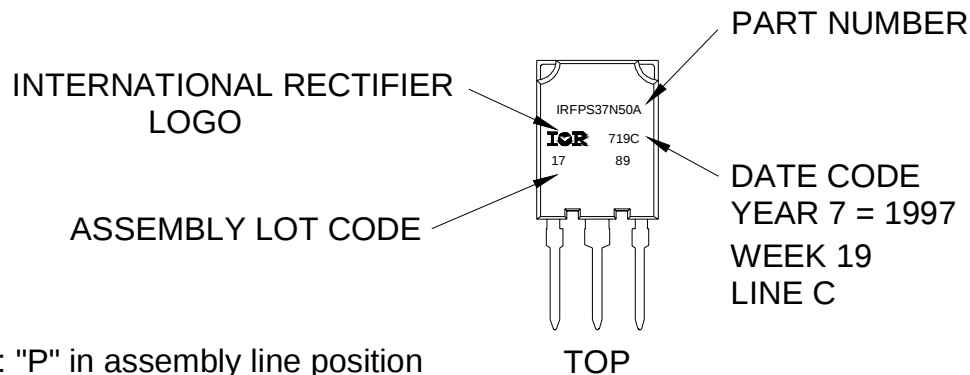


Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.94\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 36\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 36\text{A}$, $di/dt \leq 145\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position
indicates "Lead-Free"

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

Data and specifications subject to change without notice.

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