

Vacuum Fluorescent Display Tube Driver

Description

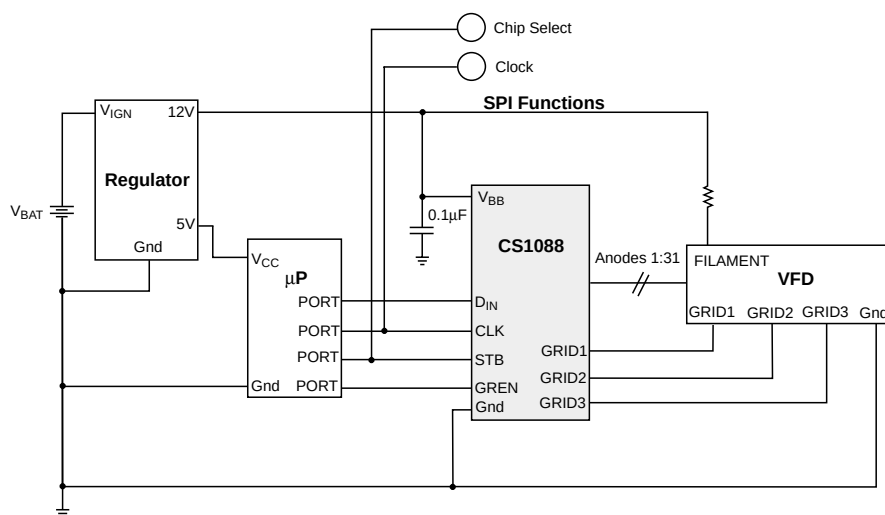
The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 34-bit shift register, a 34-bit transparent data latch, a metal mask ROM, six 20mA anode output drivers, twenty-five 2mA anode output

drivers, and three 50mA grid drivers with output enables. The metal mask programmable ROM (at factory request) allows the 31 anode outputs and 3 grid outputs to be assigned to any of the 34 serial data bits.

Absolute Maximum Ratings

Supply Voltage (V_{BB})	-0.6V to 18.0V
Input Voltages (D_{IN} , CLK, STB, GREN)	-0.6V to 6.0V
Junction Temperature Range	-40°C to 150°C
Storage Temperature Range	-55°C to 150°C
ESD Susceptibility (Human Body Model)	2kV
ESD Susceptibility (Machine Model)	200V
Lead Temperature Soldering	
Wave Solder (through hole styles only)	10 sec. max, 260°C peak
Reflow (SMD styles only)	60 sec. max above 183°C, 230°C peak

Application Diagram

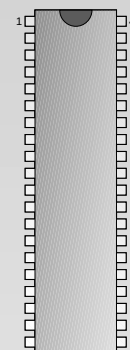


Features

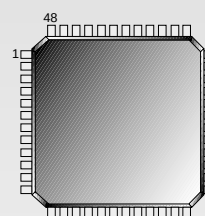
- **Metal Mask ROM**
- **Six 20mA Anode drivers**
- **Twenty-five, 2mA Anode Drivers**
- **Three, 50mA Grid Drivers**
- **Power On Reset**
- **Display Dimming Possible**

Package Options

40 Lead PDIP



48 Lead LQFP



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Electrical Characteristics: $8.0V \leq V_{BB} \leq 16.5V$, $Gnd = 0V$, $-40^{\circ}C \leq T_J \leq 105^{\circ}C$; unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ V_{BB} Input					
V_{BB} Input Voltage		8.0		16.5	V
I_{BB0} Current	No outputs active, $V_{BB} = 16.5V$		2	5	mA
Reset Mode	All outputs forced low.		6.5	7.5	V
■ D_{IN}, CLK, STB Inputs					
V_{IL} , Input Low Voltage				1.6	V
V_{IH} , Input High Voltage		3.3			V
I_{IL} , Input Current	$V_{IN} = V_{IH}$	0	7.5	20.0	μA
■ GREN Input					
V_{IL} , Input Low Voltage				1.6	V
V_{IH} , Input High Voltage		3.3			V
I_{IH} , Input Pull-down Current	$V_{IN} = 3.325V$		30	60	μA
■ GRID1, GRID2, GRID3 Outputs					
I_{OL}	Sink Current	1.0			mA
I_{OH}	Source Current	50			mA
V_{OL}	$I_{OUT} = 1mA$			0.5	V
V_{OH}	$I_{OUT} = -50mA$, $V_{BB} = 12V$	$V_{BB} - 0.75$		V_{BB}	V
■ AN24-AN29 Outputs					
I_{OL}	Sink Current	400			μA
I_{OH}	Source Current	20			mA
V_{OL}	$I_{OUT} = 400\mu A$			0.5	V
V_{OH}	$I_{OUT} = -20mA$, $V_{BB} = 12V$	$V_{BB} - 0.5$		V_{BB}	V
■ AN1-AN23, AN30-AN31 Outputs					
I_{OL}	Sink Current	100			μA
I_{OH}	Source Current	2.0			mA
V_{OL}	$I_{OUT} = 100\mu A$			0.5	V
V_{OH}	$I_{OUT} = -2mA$, $V_{BB} = 12V$	$V_{BB} - 0.5$		V_{BB}	V
■ AC Characteristics: Input and Output Timing					
F_C , CLK Frequency		0		1	MHz
T_{CL} , CLK Low Time		200			ns
T_{CH} , CLK High Time		200			ns
T_{CR} , CLK Rise Time				100	ns
T_{CF} , CLK Fall Time				100	ns
T_{SC} , STB Low to CLK High Time		50			ns
T_{ST} , STB High Time		500			ns
T_{AN} , STB High to Anode Output Propagation Delay				5.0	μs

Electrical Characteristics: $8.0V \leq V_{BB} \leq 16.5V$, Gnd = 0V, $-40^{\circ}C \leq T_A \leq 105^{\circ}C$; unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ AC Characteristics: Input and Output Timing: continued					
T_{GL} , Grid Turn On Propagation Delay	$V_{BB} = 12V$			2	μs
T_{G0} , Grid Turn Off Propagation Delay	$V_{BB} = 12V$			5	μs
T_{GR} , Grid Rise Time	At rated load.	0.5		2.0	μs
T_{GF} , Grid Fall Time	At rated load.	0.35		2.00	μs
T_{AR} , Anode Rise Time	At rated load.	0.40		2.00	μs
T_{AF} , Anode Fall Time	At rated load.	0.40		2.50	μs

Note: Grid and anode rise / fall times are measured from 10% and 90% points.

Output currents are at the maximum rated currents for the respective stages.

Package Lead Description

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
40 Lead DIP	48 Lead LQFP	(31 Anode Configuration)	
1	8	GRID1	50mA grid output.
2	9	GRID2	50mA grid output.
3	10	GRID3	50mA grid output.
4	11	AN1	2mA anode output.
5	13	AN2	2mA anode output.
6	14	AN3	2mA anode output.
7	15	AN4	2mA anode output.
8	16	AN5	2mA anode output.
9	17	AN6	2mA anode output.
10	19	AN7	2mA anode output.
11	20	AN8	2mA anode output.
12	21	AN9	2mA anode output.
13	22	AN10	2mA anode output.
14	23	AN11	2mA anode output.
15	25	AN12	2mA anode output.
16	26	AN13	2mA anode output.
17	27	AN14	2mA anode output.
18	28	AN15	2mA anode output.
19	29	AN16	2mA anode output.
20	31	Gnd	Ground connection.
21	32	AN17	2mA anode output.
22	33	AN18	2mA anode output.
23	34	AN19	2mA anode output.
24	35	AN20	2mA anode output.

Package Lead Description: continued

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
40 Lead DIP	48 Lead LQFP	(31 Anode Configuration)	
25	37	AN21	2mA anode output.
26	38	AN22	2mA anode output.
27	39	AN23	2mA anode output.
28	40	AN24	20mA anode output.
29	41	AN25	20mA anode output.
30	43	AN26	20mA anode output.
31	44	AN27	20mA anode output.
32	45	AN28	20mA anode output.
33	46	AN29	20mA anode output.
34	47	AN30	2mA anode output.
35	1	D _{IN}	Shift register data input.
36	2	CLK	Shift register clock input.
37	3	STB	Transfer contents of shift registers to output stages.
38	4	GREN	Grid outputs enable.
39	5	AN31	2mA anode output.
40	7	V _{BB}	Supply voltage input.
	6, 12, 18, 24 30, 36, 42, 48	NC	No connection.

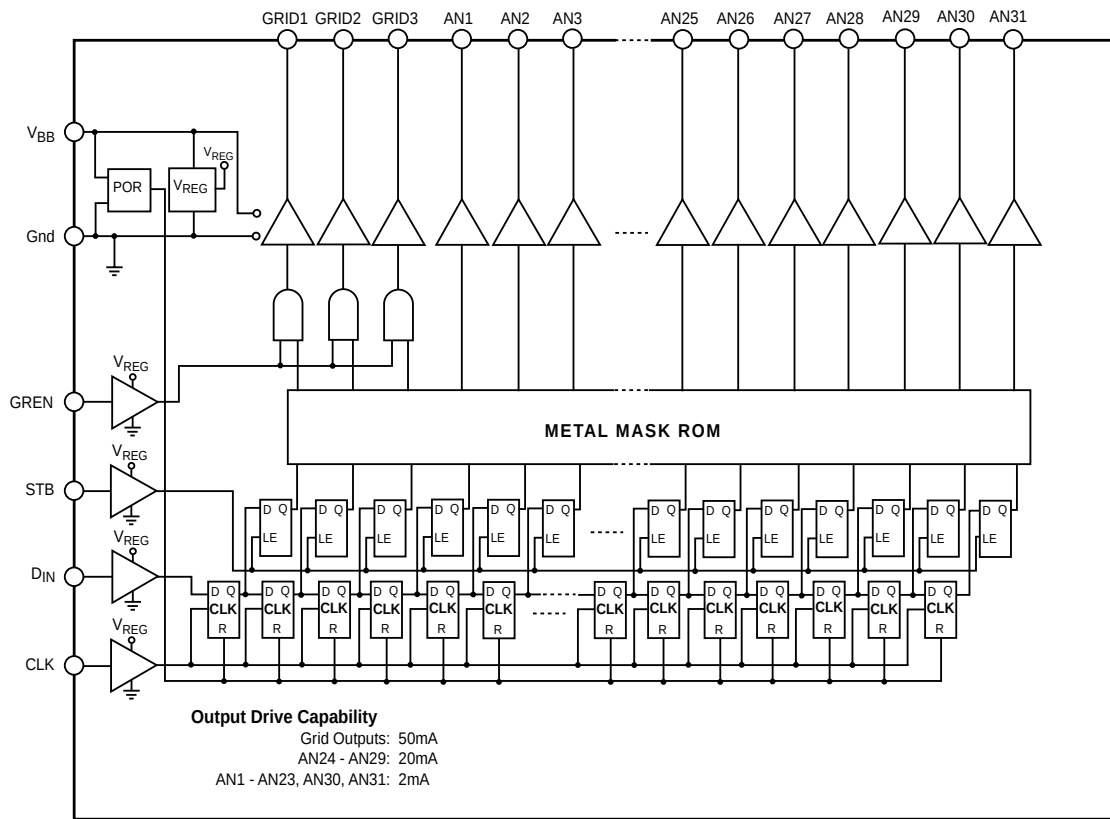
Operation Description

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the D_{IN} pin at the rising edge of the CLK input. Thirty four bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register / latch will cause the corresponding output to turn on. A logic low input to the shift

register / latch will cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN31 are always enabled.

Block Diagram



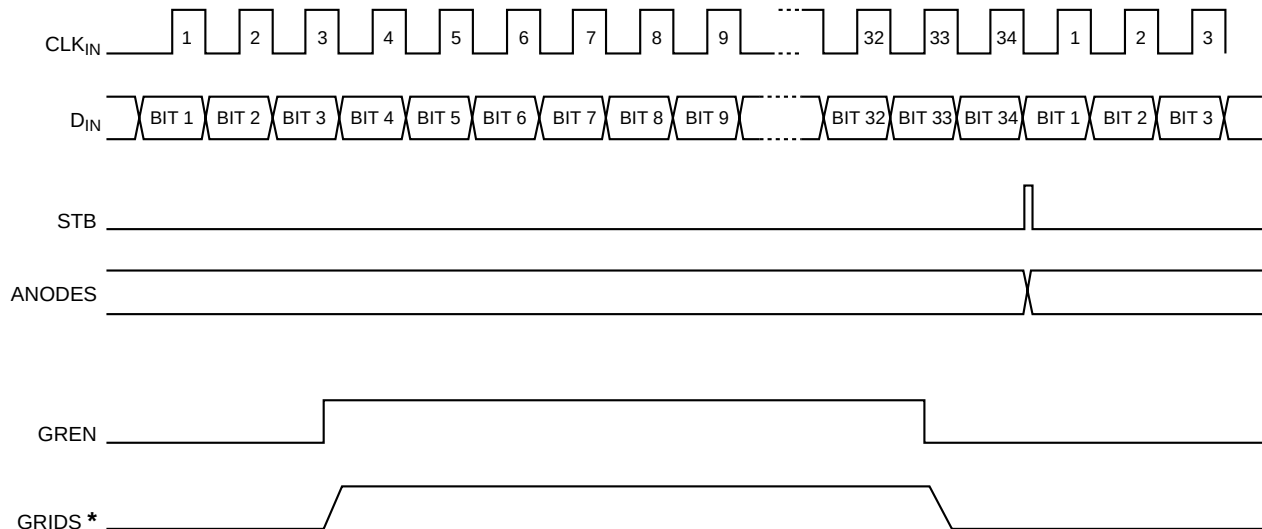
Application Information

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Pin Name	G1	G2	G3	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14

Bit #	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
Pin Name	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31

Table 1: Bit Pattern, G = Grid, A = Anode.

Typical Operation



* Selected grid goes high only if input bit pattern from shift register to grid is high.

Package Specification

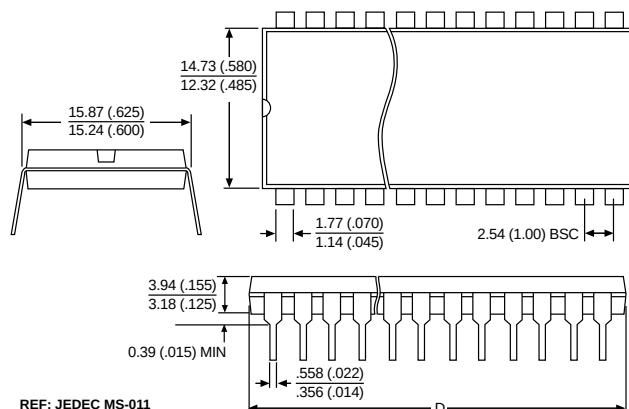
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
40 Lead PDIP	50.3	53.2	1.980	2.095

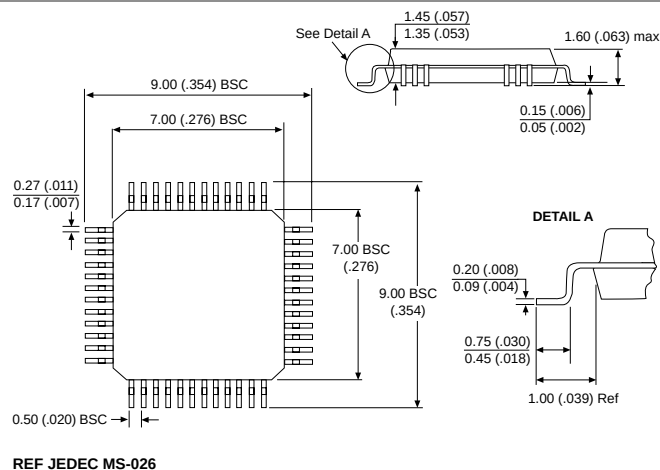
PACKAGE THERMAL DATA

Thermal Data		40 Lead PDIP	48 Lead LQFP	
$R_{\theta JC}$	typ	20	–	$^{\circ}\text{C/W}$
$R_{\theta JA}$	typ	45	–	$^{\circ}\text{C/W}$

Plastic DIP (N); 600 mil wide



48 Lead LQFP (FT) 7 × 7mm Body



Ordering Information

Part Number	Description
CS1088XN40	40 Lead PDIP
CS1088XFT48	48 Lead LQFP
CS1088XFTR48	48 Lead LQFP (tape & reel)

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