

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

## DESCRIPTION

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

DGG OR DL PACKAGE  
(TOP VIEW)

1	48	2	$\overline{OE}$
1Y1	47	1A1	
1Y2	46	1A2	
GND	45	GND	
1Y3	44	1A3	
1Y4	43	1A4	
$V_{CC}$	42	$V_{CC}$	
2Y1	41	2A1	
2Y2	40	2A2	
GND	39	GND	
2Y3	38	2A3	
2Y4	37	2A4	
3Y1	36	3A1	
3Y2	35	3A2	
GND	34	GND	
3Y3	33	3A3	
3Y4	32	3A4	
$V_{CC}$	31	$V_{CC}$	
4Y1	30	4A1	
4Y2	29	4A2	
GND	28	GND	
4Y3	27	4A3	
4Y4	26	4A4	
$\overline{OE}$	25	3 $\overline{OE}$	

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

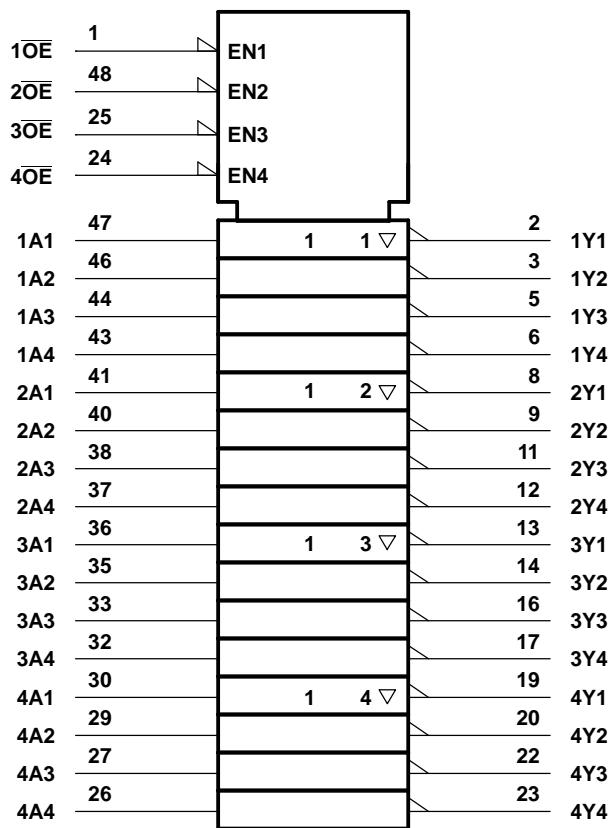
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**SN74ALVCH16240  
16-BIT BUFFER/DRIVER  
WITH 3-STATE OUTPUTS**

SCES045D—JULY 1995—REVISED AUGUST 2004

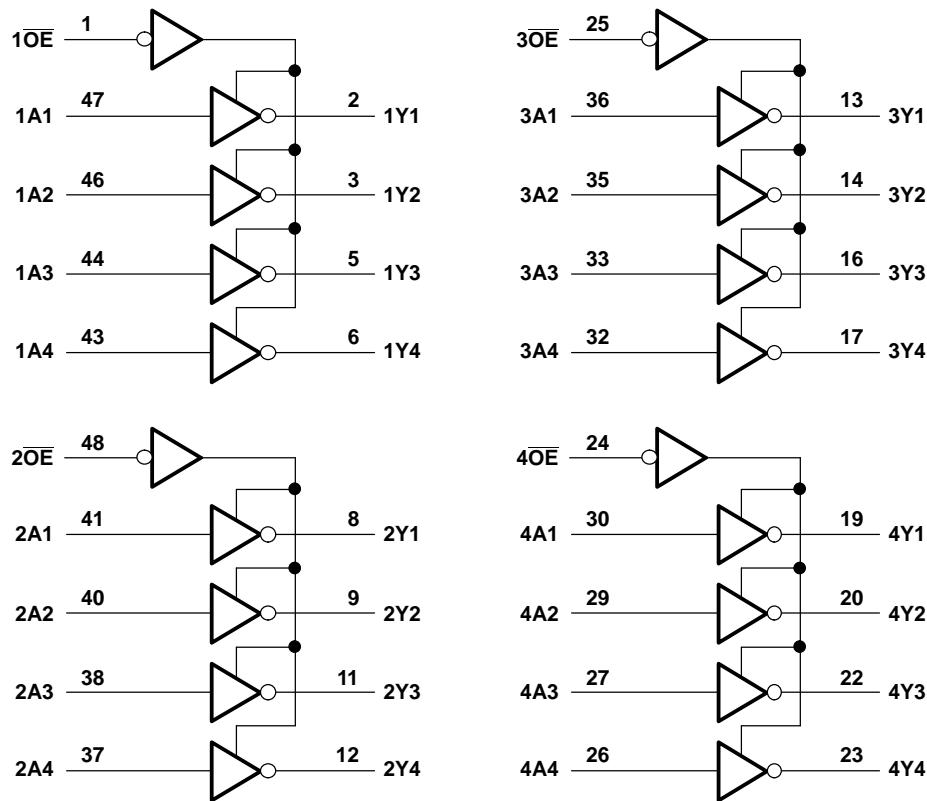
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**LOGIC SYMBOL<sup>(1)</sup>**



<sup>(1)</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current $V_I < 0$	-	-50	mA
$I_{OK}$	Output clamp current $V_O < 0$	-	-50	mA
$I_O$	Continuous output current	-	$\pm 50$	mA
	Continuous current through each $V_{CC}$ or GND	-	$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		89
		DL package		94
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.

**SN74ALVCH16240**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65 \text{ V}$	-4	mA
		$V_{CC} = 2.3 \text{ V}$	-12	
		$V_{CC} = 2.7 \text{ V}$	-12	
		$V_{CC} = 3 \text{ V}$	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	12	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 $\mu$ A	1.65 V to 3.6 V	V <sub>CC</sub>	- 0.2		V
	I <sub>OH</sub> = -4 mA	1.65 V		1.2		
	I <sub>OH</sub> = -6 mA	2.3 V		2		
	I <sub>OH</sub> = -12 mA	2.3 V		1.7		
		2.7 V		2.2		
		3 V		2.4		
V <sub>OL</sub>	I <sub>OL</sub> = -24 mA	3 V		2		V
	I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 3.6 V		0.2		
	I <sub>OL</sub> = 4 mA	1.65 V		0.45		
	I <sub>OL</sub> = 6 mA	2.3 V		0.4		
	I <sub>OL</sub> = 12 mA	2.3 V		0.7		
		2.7 V		0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		$\pm$ 5	$\mu$ A	
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V		25		$\mu$ A
	V <sub>I</sub> = 1.07 V	1.65 V		-25		
	V <sub>I</sub> = 0.7 V	2.3 V		45		
	V <sub>I</sub> = 1.7 V	2.3 V		-45		
	V <sub>I</sub> = 0.8 V	3 V		75		
	V <sub>I</sub> = 2 V	3 V		-75		
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V		$\pm$ 500	$\mu$ A	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V		$\pm$ 10	$\mu$ A	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V		40	$\mu$ A	
$\Delta$ I <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	$\mu$ A	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3		pF
	Data inputs			6		
C <sub>o</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7		pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V $\pm$ 0.2 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> = 3.3 V $\pm$ 0.3 V	UNIT		
			TYP	MIN	MAX	MIN	MAX		
t <sub>pd</sub>	A	Y	(1)	1	5.3	5.3	1	3.9	ns
t <sub>en</sub>	$\overline{OE}$	Y	(1)	1	6.4	6.1	1	5	ns
t <sub>dis</sub>	$\overline{OE}$	Y	(1)	1	5.4	4.8	1	4.4	ns

(1) This information was not available at the time of publication.

## OPERATING CHARACTERISTICS

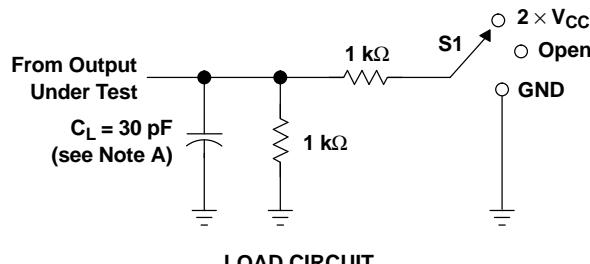
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	Outputs enabled	(1)	16	19	pF
	Outputs disabled	(1)	4	5	

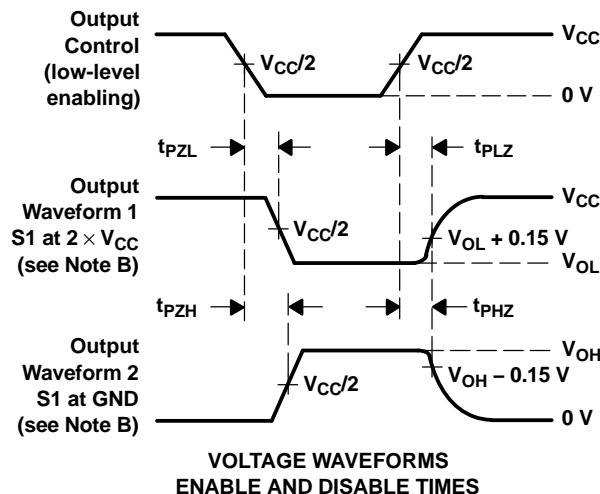
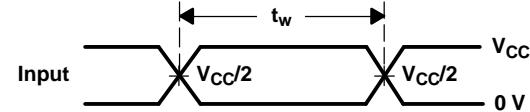
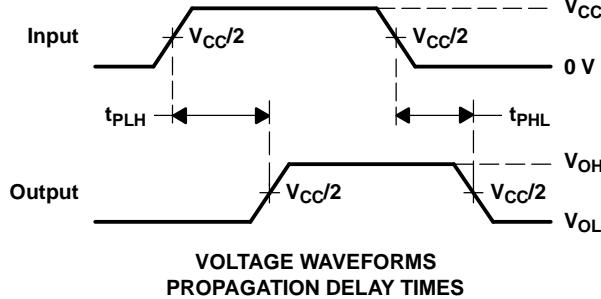
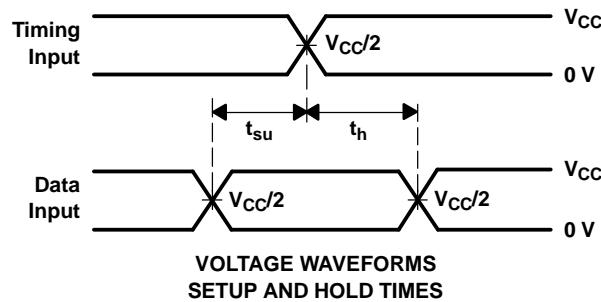
(1) This information was not available at the time of publication.

## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



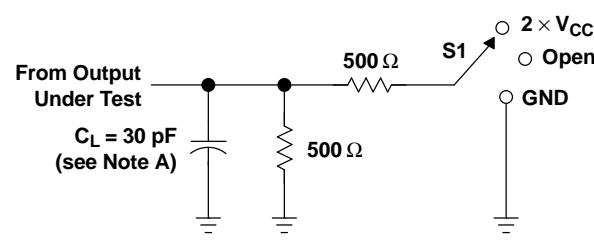
NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

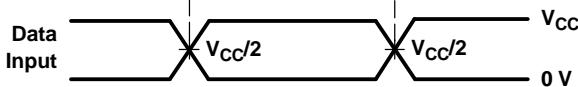
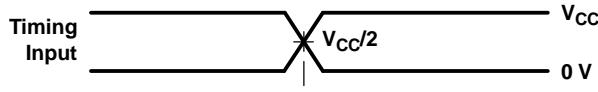
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

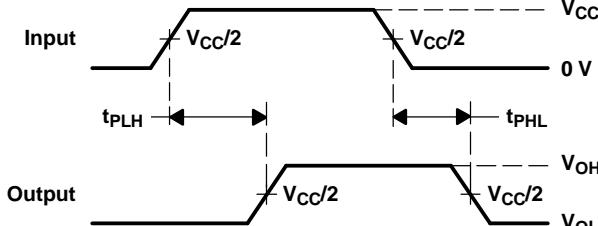


TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

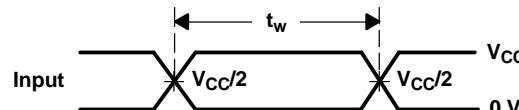
LOAD CIRCUIT



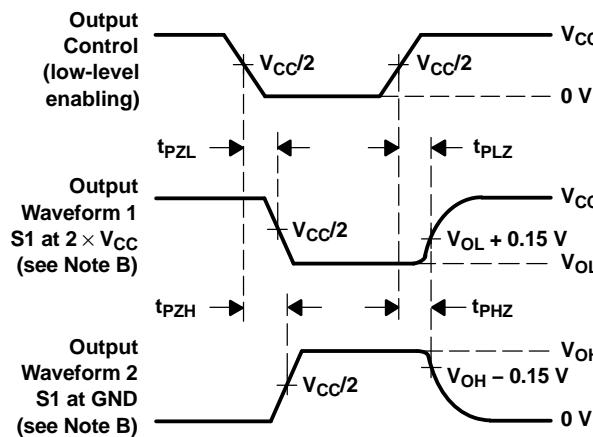
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



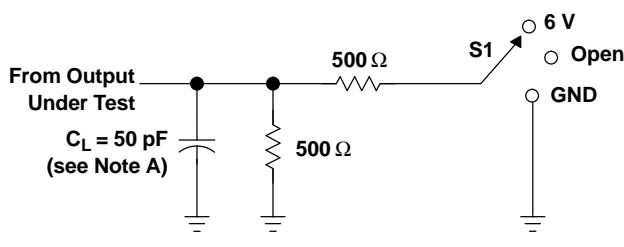
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

NOTES:

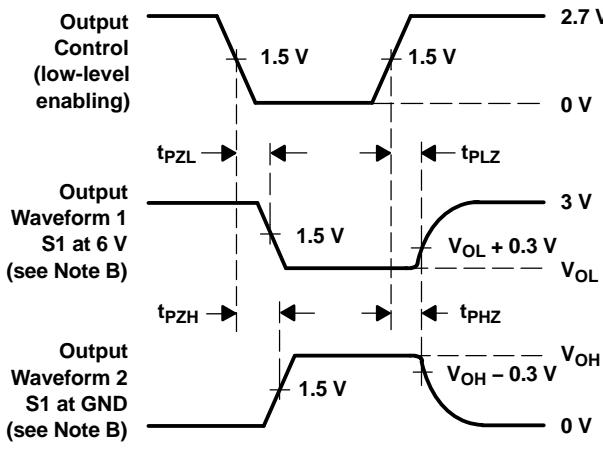
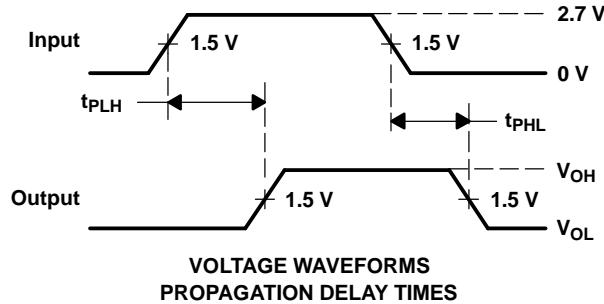
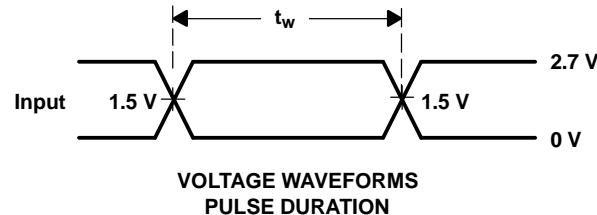
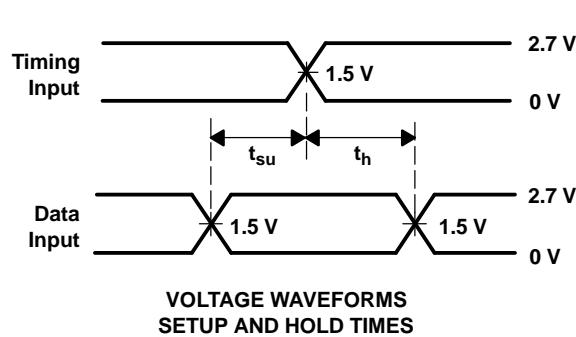
- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PLZ}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCH16240DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALVCH16240DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALVCH16240DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16240	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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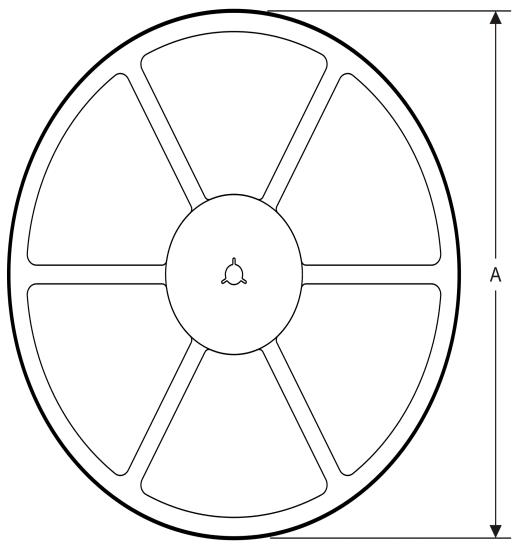
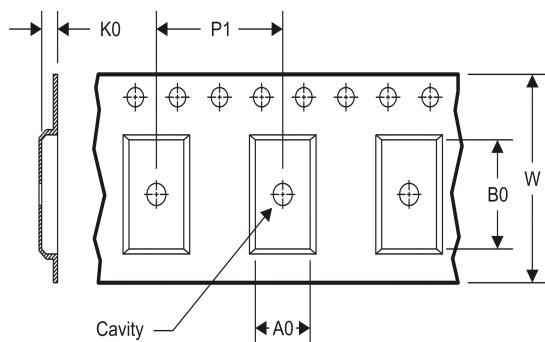
## PACKAGE OPTION ADDENDUM

10-Jun-2014

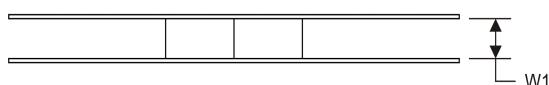
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16240DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

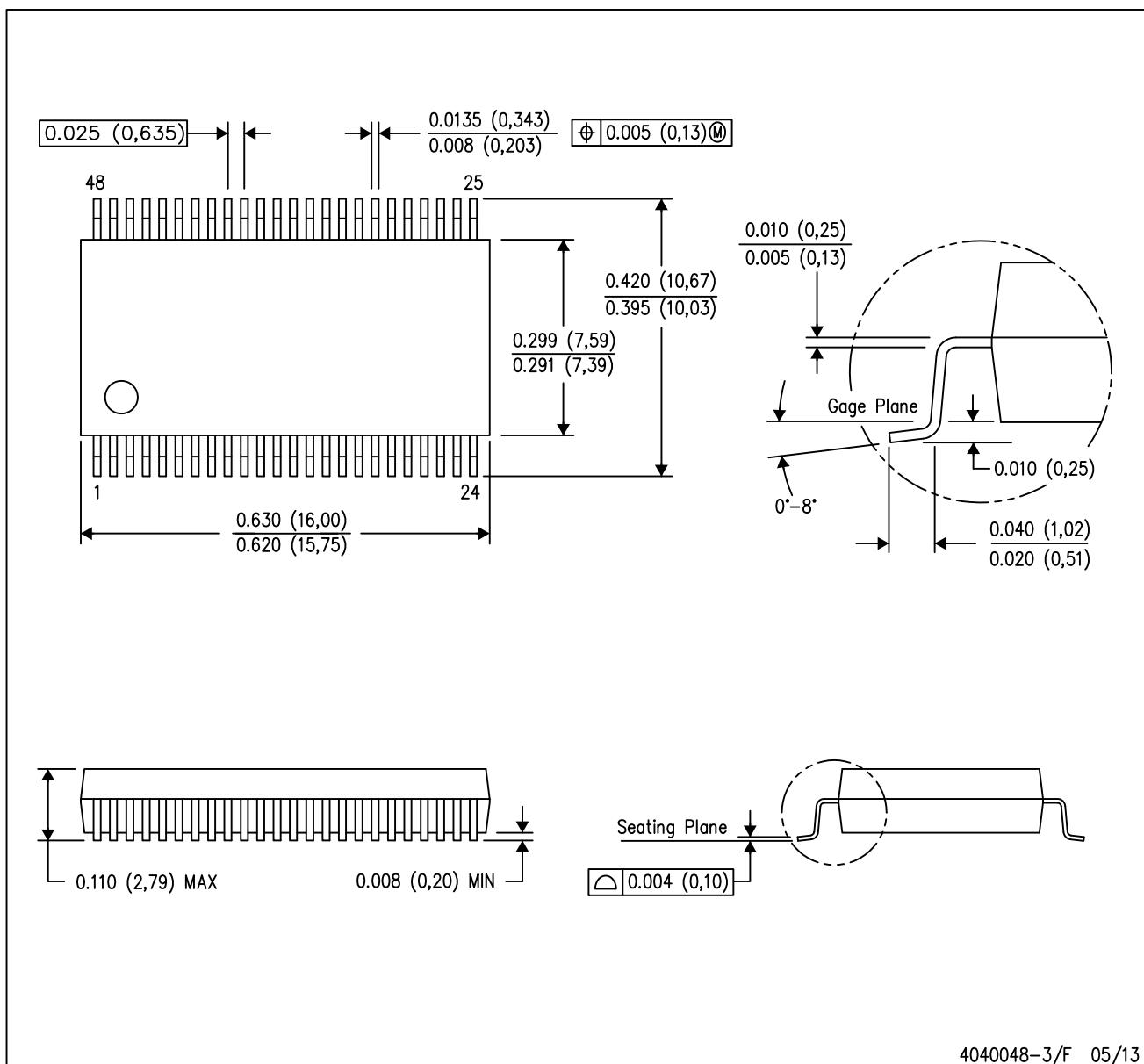
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16240DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

NOTES:

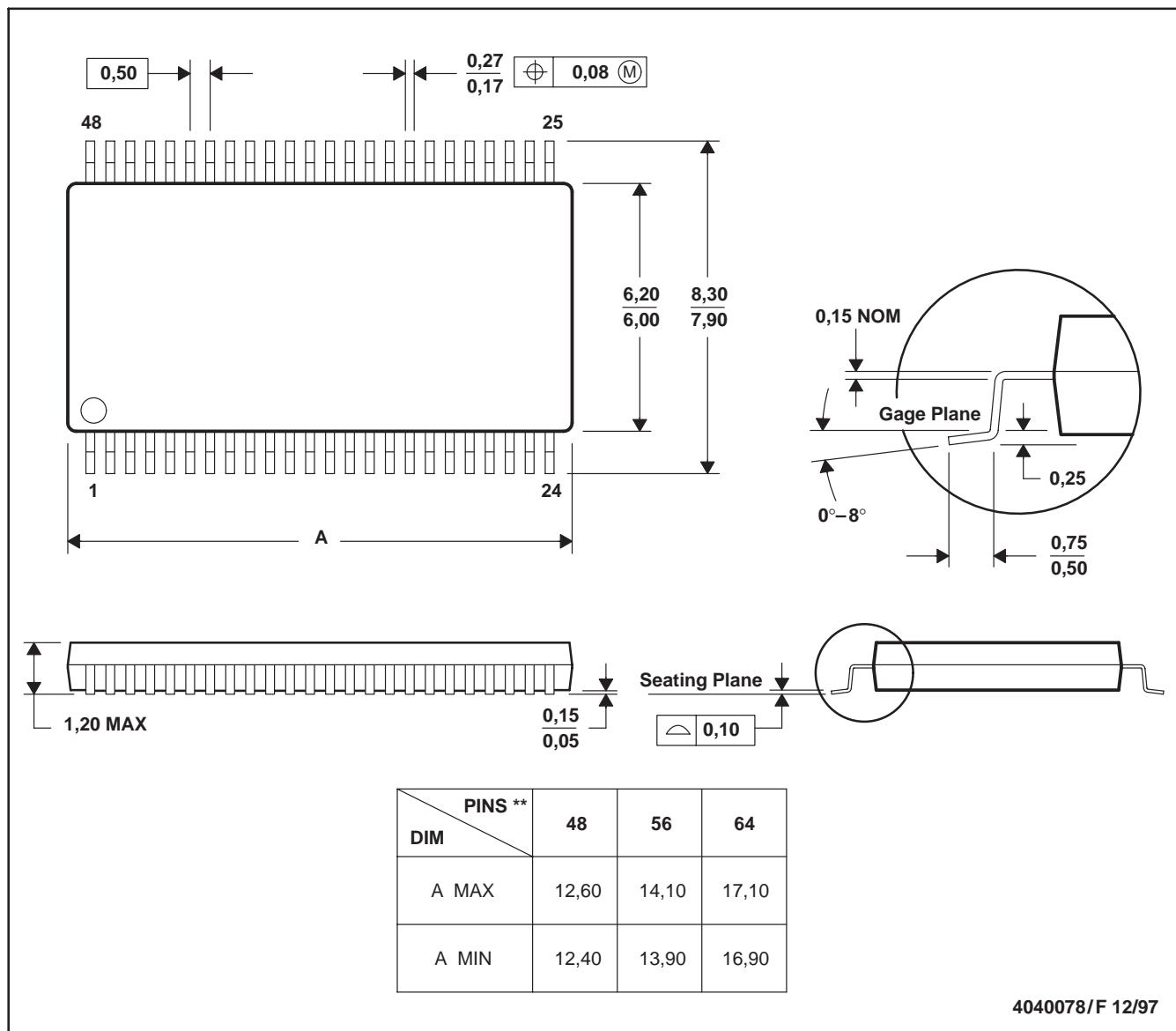
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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