

## FEATURES

- Improved Direct Replacement for AD7543 and DAC-8143
- Low Cost
- DNL and INL Over Temperature:  $\pm 0.5\text{LSB}$
- Easy, Fast and Flexible Serial Interface
- Daisy-Chain 3-Wire Interface for Multiple DAC Systems (LTC8143)
- 1LSB Maximum Gain Error Over Temperature Eliminates Adjustment
- Asynchronous Clear Input for Initialization
- Four-Quadrant Multiplication
- Low Power Consumption
- 16-Pin PDIP and SO Packages

## APPLICATIONS

- Process Control and Industrial Automation
- Remote Microprocessor-Controlled Systems
- Digitally Controlled Filters and Power Supplies
- Programmable Gain Amplifiers
- Automatic Test Equipment

## DESCRIPTION

The LTC<sup>®</sup>7543/LTC8143 are serial-input 12-bit multiplying digital-to-analog converters (DACs). They are superior pin compatible replacements for the AD7543 and DAC-8143. Improvements include better accuracy, better stability over temperature and supply variations, lower sensitivity to output amplifier offset, tighter timing specifications and lower output capacitance.

An easy-to-use serial interface includes an asynchronous CLEAR input for systems requiring initialization to a known state. The LTC8143 has a serial data output to allow daisy-chaining multiple DACs on a 3-wire interface bus.

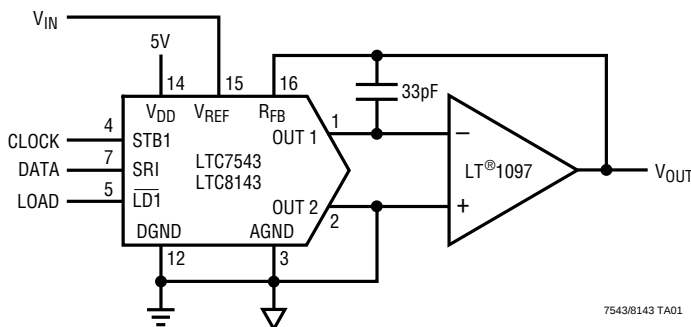
These DACs are extremely versatile. They can be used for 2-quadrant and 4-quadrant multiplying, programmable gain and single supply applications, such as noninverting voltage output and biased or offset ground mode.

Parts are available in 16-pin PDIP and SO packages and are specified over the extended industrial temperature range,  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

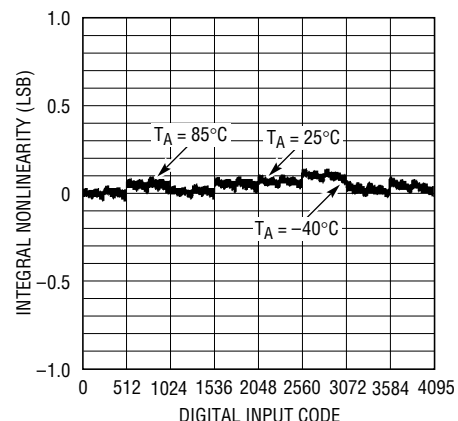
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## TYPICAL APPLICATION

Multiplying DAC Has Easy 3-Wire Serial Interface



Integral Nonlinearity Over Temperature



## ABSOLUTE MAXIMUM RATINGS

|                                            |                              |
|--------------------------------------------|------------------------------|
| $V_{DD}$ to AGND .....                     | -0.5V to 7V                  |
| $V_{DD}$ to DGND .....                     | -0.5V to 7V                  |
| AGND to DGND .....                         | $V_{DD} + 0.5V$              |
| DGND to AGND .....                         | $V_{DD} + 0.5V$              |
| Digital Inputs to DGND .....               | -0.5V to ( $V_{DD} + 0.5V$ ) |
| $V_{OUT1}$ , $V_{OUT2}$ to AGND .....      | -0.5V to ( $V_{DD} + 0.5V$ ) |
| $V_{REF}$ to AGND, DGND .....              | $\pm 25V$                    |
| $V_{RFB}$ to AGND, DGND .....              | $\pm 25V$                    |
| Maximum Junction Temperature .....         | 150°C                        |
| Operating Temperature Range .....          | -40°C to 85°C                |
| Storage Temperature Range .....            | -65°C to 150°C               |
| Lead Temperature (Soldering, 10 sec) ..... | 300°C                        |

## PACKAGE/ORDER INFORMATION

| TOP VIEW                                                        |   | ORDER PART NUMBER                                                                                          |
|-----------------------------------------------------------------|---|------------------------------------------------------------------------------------------------------------|
| OUT 1                                                           | 1 | 16 $R_{FB}$                                                                                                |
| OUT 2                                                           | 2 | 15 $V_{REF}$                                                                                               |
| AGND                                                            | 3 | 14 $V_{DD}$                                                                                                |
| STB1                                                            | 4 | 13 $CLR$                                                                                                   |
| $LD1$                                                           | 5 | 12 DGND                                                                                                    |
| NC (LTC7543)<br>SRO (LTC8143)                                   | 6 | 11 STB4                                                                                                    |
| SRI                                                             | 7 | 10 STB3                                                                                                    |
| STB2                                                            | 8 | 9 $LD2$                                                                                                    |
| N PACKAGE<br>16-LEAD PDIP                                       |   |                                                                                                            |
| SW PACKAGE<br>16-LEAD PLASTIC SO WIDE                           |   |                                                                                                            |
| $T_{JMAX} = 150^{\circ}C$ , $\theta_{JA} = 100^{\circ}C/W$ (N)  |   |                                                                                                            |
| $T_{JMAX} = 150^{\circ}C$ , $\theta_{JA} = 130^{\circ}C/W$ (SW) |   |                                                                                                            |
|                                                                 |   | LTC7543GKN<br>LTC7543KN<br>LTC7543GKSW<br>LTC7543KSW<br>LTC8143EN<br>LTC8143FN<br>LTC8143ESW<br>LTC8143FSW |

Consult factory for Military grade parts.

## ACCURACY CHARACTERISTICS – LTC7543

 $V_{DD} = 5V$ ,  $V_{REF} = 10V$ ,  $V_{OUT1} = V_{OUT2} = AGND = DGND = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified.

| SYMBOL    | PARAMETER                                                       | CONDITIONS                                                |   | LTC7543GK |              |                           | LTC7543K |              |                           | UNITS            |
|-----------|-----------------------------------------------------------------|-----------------------------------------------------------|---|-----------|--------------|---------------------------|----------|--------------|---------------------------|------------------|
|           |                                                                 |                                                           |   | MIN       | TYP          | MAX                       | MIN      | TYP          | MAX                       |                  |
|           | Resolution                                                      |                                                           | ● | 12        |              |                           | 12       |              |                           | Bits             |
| INL       | Integral Nonlinearity<br>(Relative Accuracy)                    | (Note 1)                                                  | ● |           |              | $\pm 0.5$                 |          |              | $\pm 0.5$                 | LSB              |
| DNL       | Differential Nonlinearity                                       | Guaranteed Monotonic, $T_{MIN}$ to $T_{MAX}$              | ● |           |              | $\pm 0.5$                 |          |              | $\pm 0.5$                 | LSB              |
| GE        | Gain Error                                                      | (Note 2)<br>$T_A = 25^{\circ}C$<br>$T_{MIN}$ to $T_{MAX}$ | ● |           |              | $\pm 1$                   |          |              | $\pm 2$                   | LSB              |
|           |                                                                 |                                                           | ● |           |              | $\pm 1$                   |          |              | $\pm 2$                   | LSB              |
|           | Gain Temperature Coefficient<br>( $\Delta Gain / \Delta Temp$ ) | (Note 3)                                                  | ● |           | 1            | 5                         |          | 1            | 5                         | ppm/ $^{\circ}C$ |
| $I_{LKG}$ | Output Leakage Current                                          | (Note 4)<br>$T_A = 25^{\circ}C$<br>$T_{MIN}$ to $T_{MAX}$ | ● |           |              | $\pm 1$<br>$\pm 10$       |          |              | $\pm 1$<br>$\pm 10$       | nA<br>nA         |
|           |                                                                 |                                                           | ● |           |              | $\pm 0.006$<br>$\pm 0.06$ |          |              | $\pm 0.006$<br>$\pm 0.06$ | LSB<br>LSB       |
| PSRR      | Power Supply Rejection Ratio                                    | $V_{DD} = 5V \pm 5\%$                                     | ● |           | $\pm 0.0001$ | $\pm 0.002$               |          | $\pm 0.0001$ | $\pm 0.002$               | %/%              |

**ACCURACY CHARACTERISTICS – LTC8143**

$V_{DD} = 5V$ ,  $V_{REF} = 10V$ ,  $V_{OUT1} = V_{OUT2} = AGND = DGND = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified.

| SYMBOL    | PARAMETER                                                     | CONDITIONS                                               |   | LTC8143E |         |        | LTC8143F |         |        | UNITS           |
|-----------|---------------------------------------------------------------|----------------------------------------------------------|---|----------|---------|--------|----------|---------|--------|-----------------|
|           |                                                               |                                                          |   | MIN      | TYP     | MAX    | MIN      | TYP     | MAX    |                 |
|           | Resolution                                                    |                                                          | ● | 12       |         |        | 12       |         |        | Bits            |
| INL       | Integral Nonlinearity<br>(Relative Accuracy)                  | (Note 1)                                                 | ● |          |         | ±0.5   |          |         | ±1     | LSB             |
| DNL       | Differential Nonlinearity                                     | Guaranteed Monotonic, $T_{MIN}$ to $T_{MAX}$             | ● |          |         | ±0.5   |          |         | ±1     | LSB             |
| GE        | Gain Error                                                    | (Note 2)<br>$T_A = 25^\circ C$<br>$T_{MIN}$ to $T_{MAX}$ | ● |          |         | ±1     |          |         | ±2     | LSB             |
|           |                                                               |                                                          | ● |          |         | ±2     |          |         | ±2     | LSB             |
|           | Gain Temperature Coefficient<br>( $\Delta Gain/\Delta Temp$ ) | (Note 3)                                                 | ● |          | 1       | 5      |          | 1       | 5      | ppm/ $^\circ C$ |
| $I_{LKG}$ | Output Leakage Current                                        | (Note 4)<br>$T_A = 25^\circ C$<br>$T_{MIN}$ to $T_{MAX}$ | ● |          |         | ±5     |          |         | ±5     | nA              |
|           |                                                               |                                                          | ● |          |         | ±25    |          |         | ±25    | nA              |
|           | Zero-Scale Error                                              | $T_A = 25^\circ C$<br>$T_{MIN}$ to $T_{MAX}$             | ● |          |         | ±0.03  |          |         | ±0.03  | LSB             |
|           |                                                               |                                                          | ● |          |         | ±0.15  |          |         | ±0.15  | LSB             |
| PSRR      | Power Supply Rejection Ratio                                  | $V_{DD} = 5V \pm 5\%$                                    | ● |          | ±0.0001 | ±0.002 |          | ±0.0001 | ±0.002 | %/%             |

**ELECTRICAL CHARACTERISTICS – LTC7543/LTC8143**

$V_{DD} = 5V$ ,  $V_{REF} = 10V$ ,  $V_{OUT1} = V_{OUT2} = AGND = DGND = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified.

| SYMBOL                              | PARAMETER                         | CONDITIONS                              |                   | LTC7543/LTC8143<br>ALL GRADES |       |     | UNITS             |
|-------------------------------------|-----------------------------------|-----------------------------------------|-------------------|-------------------------------|-------|-----|-------------------|
|                                     |                                   |                                         |                   | MIN                           | TYP   | MAX |                   |
| Reference Input                     |                                   |                                         |                   |                               |       |     |                   |
| R <sub>REF</sub>                    | V <sub>REF</sub> Input Resistance | (Note 5)                                | ●                 | 8                             | 11    | 15  | kΩ                |
| AC Performance (Note 3)             |                                   |                                         |                   |                               |       |     |                   |
|                                     | Output Current Settling Time      | (Notes 6, 7)                            | ●                 |                               | 0.25  | 1   | μs                |
|                                     | Multiplying Feedthrough Error     | V <sub>REF</sub> = ±10V, 10kHz Sinewave | ●                 |                               | 0.8   | 2   | mV <sub>P-P</sub> |
|                                     | Digital-to-Analog Glitch Energy   | (Notes 6, 8)                            | ●                 |                               | 2     | 20  | nV-sec            |
| THD                                 | Total Harmonic Distortion         | (Note 9)                                | ●                 |                               | −108  | −92 | dB                |
|                                     | Output Noise Voltage Density      | (Note 10)                               | ●                 |                               |       | 13  | nV/√Hz            |
| Analog Outputs (Note 3)             |                                   |                                         |                   |                               |       |     |                   |
| C <sub>OUT</sub>                    | Output Capacitance                | DAC Register Loaded to All 1s           | C <sub>OUT1</sub> | ●                             | 60    | 90  | pF                |
|                                     |                                   |                                         | C <sub>OUT2</sub> | ●                             | 20    | 60  | pF                |
|                                     |                                   | DAC Register Loaded to All 0s           | C <sub>OUT1</sub> | ●                             | 30    | 60  | pF                |
|                                     |                                   |                                         | C <sub>OUT2</sub> | ●                             | 50    | 90  | pF                |
| Digital Inputs                      |                                   |                                         |                   |                               |       |     |                   |
| V <sub>IH</sub>                     | Digital Input High Voltage        |                                         | ●                 | 2.4                           |       |     | V                 |
| V <sub>IL</sub>                     | Digital Input Low Voltage         |                                         | ●                 |                               |       | 0.8 | V                 |
| I <sub>IN</sub>                     | Digital Input Current             | V <sub>IN</sub> = 0V to V <sub>DD</sub> | ●                 |                               | 0.001 | ±1  | μA                |
| C <sub>IN</sub>                     | Digital Input Capacitance         | (Note 3), V <sub>IN</sub> = 0V          | ●                 |                               |       | 8   | pF                |
| Digital Outputs: SRO (LTC8143 Only) |                                   |                                         |                   |                               |       |     |                   |
| V <sub>OH</sub>                     | Digital Output High               | I <sub>OH</sub> = −200μA                | ●                 | 4                             |       |     | V                 |
| V <sub>OL</sub>                     | Digital Output Low                | I <sub>OL</sub> = 1.6mA                 | ●                 |                               |       | 0.4 | V                 |

**ELECTRICAL CHARACTERISTICS – LTC7543/LTC8143**

$V_{DD} = 5V$ ,  $V_{REF} = 10V$ ,  $V_{OUT1} = V_{OUT2} = AGND = DGND = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified.

| SYMBOL                                                                           | PARAMETER                                                      | CONDITIONS                                          | LTC7543/LTC8143<br>ALL GRADES |      |     | UNITS |    |
|----------------------------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------|-------------------------------|------|-----|-------|----|
|                                                                                  |                                                                |                                                     | MIN                           | TYP  | MAX |       |    |
| Timing Characteristics (Note 3)                                                  |                                                                |                                                     |                               |      |     |       |    |
| t <sub>DS1</sub>                                                                 | Serial Input to Strobe Setup Time<br>(t <sub>STB</sub> = 80ns) | STB1 Used as the Strobe                             | ●                             | 50   | 5   | ns    |    |
| t <sub>DS2</sub>                                                                 |                                                                | STB2 Used as the Strobe                             | ●                             | 20   | –5  | ns    |    |
| t <sub>DS3</sub>                                                                 |                                                                | STB3 Used as the Strobe                             | ●                             | 0    | –30 | ns    |    |
| t <sub>DS4</sub>                                                                 |                                                                | STB4 Used as the Strobe                             | ●                             | 0    | –30 | ns    |    |
| t <sub>DH1</sub>                                                                 | Serial Input to Strobe Hold Time<br>(t <sub>STB</sub> = 80ns)  | STB1 Used as the Strobe                             | ●                             | 30   | 10  | ns    |    |
| t <sub>DH2</sub>                                                                 |                                                                | STB2 Used as the Strobe                             | ●                             | 50   | 25  | ns    |    |
| t <sub>DH3</sub>                                                                 |                                                                | STB3 Used as the Strobe                             | ●                             | 80   | 55  | ns    |    |
| t <sub>DH4</sub>                                                                 |                                                                | STB4 Used as the Strobe                             | ●                             | 80   | 55  | ns    |    |
| t <sub>SRI</sub>                                                                 | Serial Input Data Pulse Width                                  |                                                     | ●                             | 80   |     | ns    |    |
| t <sub>STB1</sub> , t <sub>STB2</sub> ,<br>t <sub>STB3</sub> , t <sub>STB4</sub> | Strobe Pulse Width                                             | (Note 11)                                           | ●                             | 80   |     | ns    |    |
| t <sub>STB1</sub> , t <sub>STB2</sub> ,<br>t <sub>STB3</sub> , t <sub>STB4</sub> | Strobe Pulse Width                                             | (Note 12)                                           | ●                             | 80   |     | ns    |    |
| t <sub>LD1</sub> , t <sub>LD2</sub>                                              | Load Pulse Width                                               |                                                     | ●                             | 140  |     | ns    |    |
| t <sub>ASB</sub>                                                                 | LSB Strobed into Input Register<br>to Load DAC Register Time   |                                                     | ●                             | 0    |     | ns    |    |
| t <sub>CLR</sub>                                                                 | Clear Pulse Width                                              |                                                     | ●                             | 80   |     | ns    |    |
| SRO Timing Characteristics (LTC8143 Only)                                        |                                                                |                                                     |                               |      |     |       |    |
| t <sub>PD</sub>                                                                  | STB2, STB3, STB4 Strobe to SRO<br>Propagation Delay            | C <sub>L</sub> = 50pF                               | ●                             | 220  | 120 | ns    |    |
| t <sub>PD1</sub>                                                                 | STB1 to SRO Propagation Delay                                  | C <sub>L</sub> = 50pF                               | ●                             | 150  | 80  | ns    |    |
| Power Supply                                                                     |                                                                |                                                     |                               |      |     |       |    |
| V <sub>DD</sub>                                                                  | Supply Voltage                                                 |                                                     | ●                             | 4.75 | 5   | 5.25  | V  |
| I <sub>DD</sub>                                                                  | Supply Current                                                 | Digital Inputs = 0V or V <sub>DD</sub>              | ●                             |      |     | 0.1   | mA |
|                                                                                  |                                                                | Digital Inputs = V <sub>IH</sub> or V <sub>IL</sub> | ●                             |      |     | 2     | mA |

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:**  $\pm 0.5LSB = \pm 0.012\%$  of full scale.

**Note 2:** Using internal feedback resistor.

**Note 3:** Guaranteed by design, not subject to test.

**Note 4:**  $I_{OUT1}$  with DAC register loaded with all 0s or  $I_{OUT2}$  with DAC register loaded with all 1s.

**Note 5:** Typical temperature coefficient is 100ppm/°C.

**Note 6:** OUT 1 load = 100Ω in parallel with 13pF.

**Note 7:** To 0.01% for a full-scale change, measured from falling edge of LD1 or LD2.

**Note 8:**  $V_{REF} = 0V$ . DAC register contents changed from all 0s to all 1s or from all 1s to all 0s.

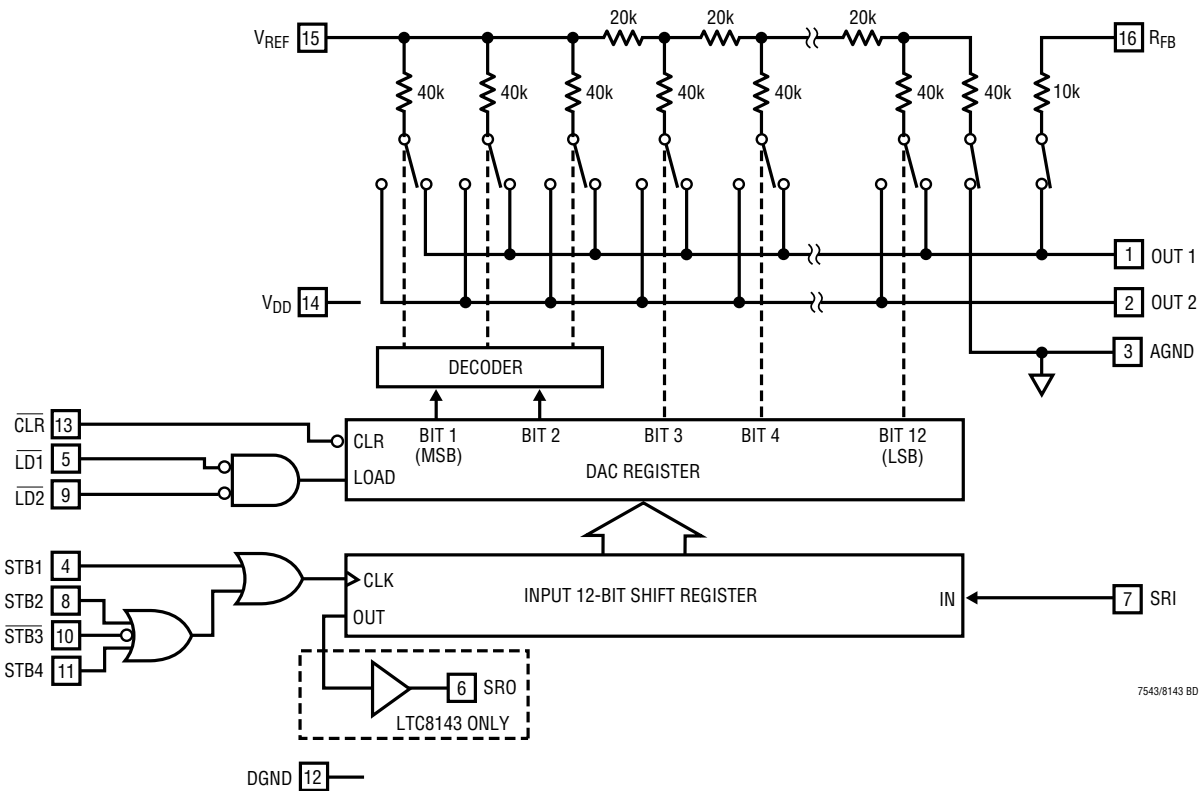
**Note 9:**  $V_{REF} = 6V_{RMS}$  at 1kHz. DAC register loaded with all 1s.

**Note 10:** Calculation from  $e_n = \sqrt{4KTRB}$  where: K = Boltzmann constant (J/K°); R = resistance (Ω); T = resistor temperature (°K); B = bandwidth (Hz).

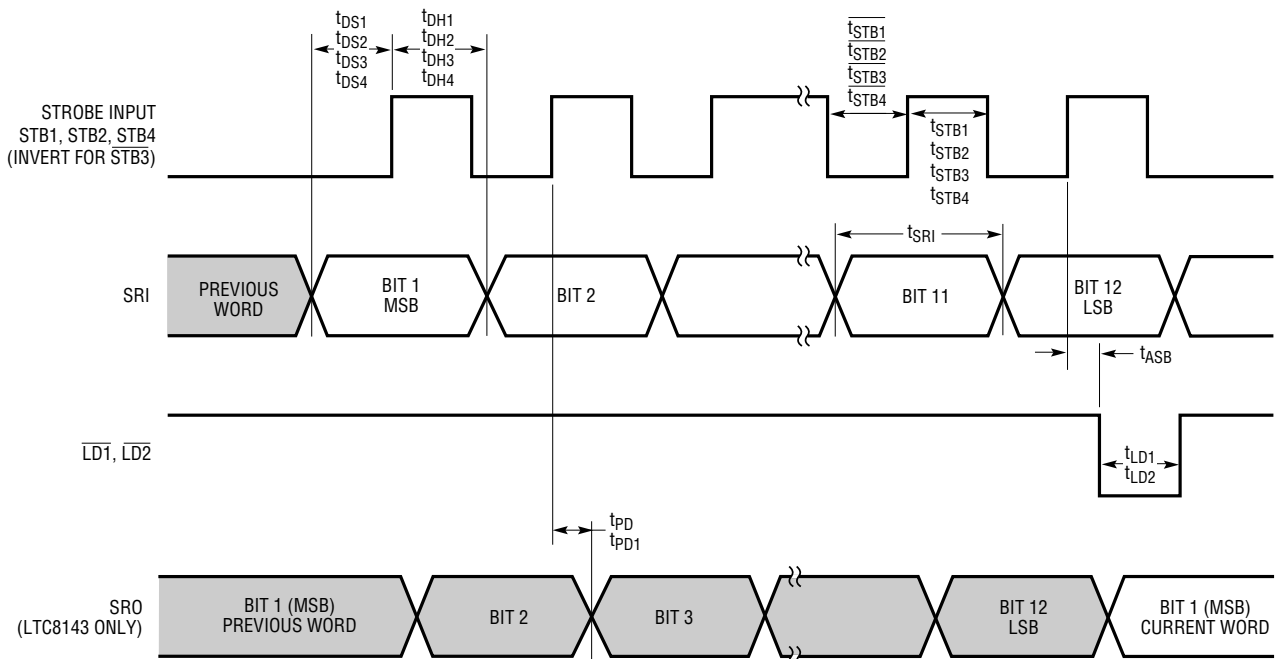
**Note 11:** Minimum high time for STB1, STB2, STB4. Minimum low time for STB3.

**Note 12:** Minimum low time for STB1, STB2, STB4. Minimum high time for STB3.

## BLOCK DIAGRAM



## TIMING DIAGRAM



TRUTH TABLES

Table 1. LTC7543/LTC8143 Input Register

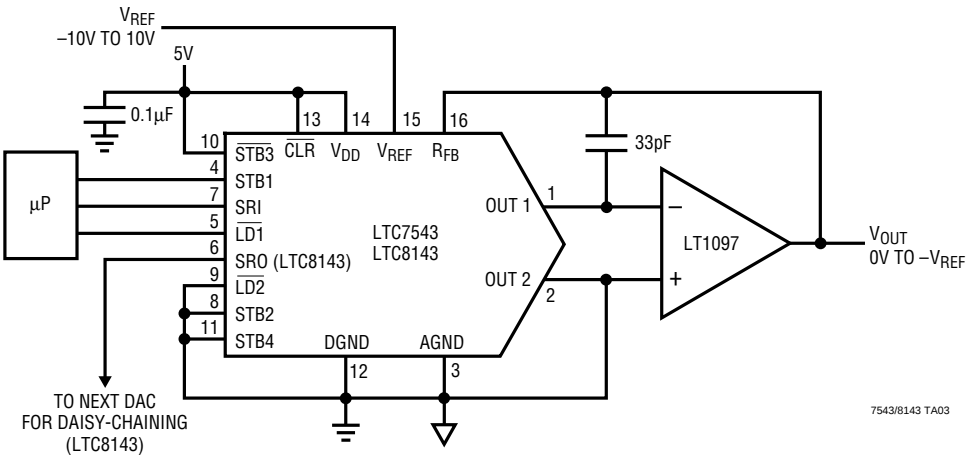
| CONTROL INPUTS        |                       |                       |                       | Input Register Operation<br>(LTC8143: SRO Operation)                                                                                |
|-----------------------|-----------------------|-----------------------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| STB1                  | STB2                  | STB3                  | STB4                  |                                                                                                                                     |
| $\overline{\text{A}}$ | 0                     | 1                     | 0                     | Serial Data Bit on SRI Loaded into Input Register, MSB First<br>(LTC8143: Data Bit or SRI Appears on SRO Pin After 12 Clocked Bits) |
| 0                     | $\overline{\text{A}}$ | 1                     | 0                     |                                                                                                                                     |
| 0                     | 0                     | $\overline{\text{A}}$ | 0                     |                                                                                                                                     |
| 0                     | 0                     | 1                     | $\overline{\text{A}}$ |                                                                                                                                     |
| 1                     | X                     | X                     | X                     | No Input Register Operation<br>(LTC8143: No SRO Operation)                                                                          |
| X                     | 1                     | X                     | X                     |                                                                                                                                     |
| X                     | X                     | 0                     | X                     |                                                                                                                                     |
| X                     | X                     | X                     | 1                     |                                                                                                                                     |

Table 2. LTC7543/LTC8143 DAC Register

| CONTROL INPUTS |     |     | DAC Register Operation                                                             |
|----------------|-----|-----|------------------------------------------------------------------------------------|
| CLR            | LD1 | LD2 |                                                                                    |
| 0              | X   | X   | Reset DAC Register to All 0s (Asynchronous Operation; No Effect on Input Register) |
| 1              | 1   | X   | No DAC Register Operation                                                          |
| 1              | X   | 1   |                                                                                    |
| 1              | 0   | 0   | Load DAC Register with the Contents of Input Register                              |

TYPICAL APPLICATIONS

Unipolar Operation (2-Quadrant Multiplication)

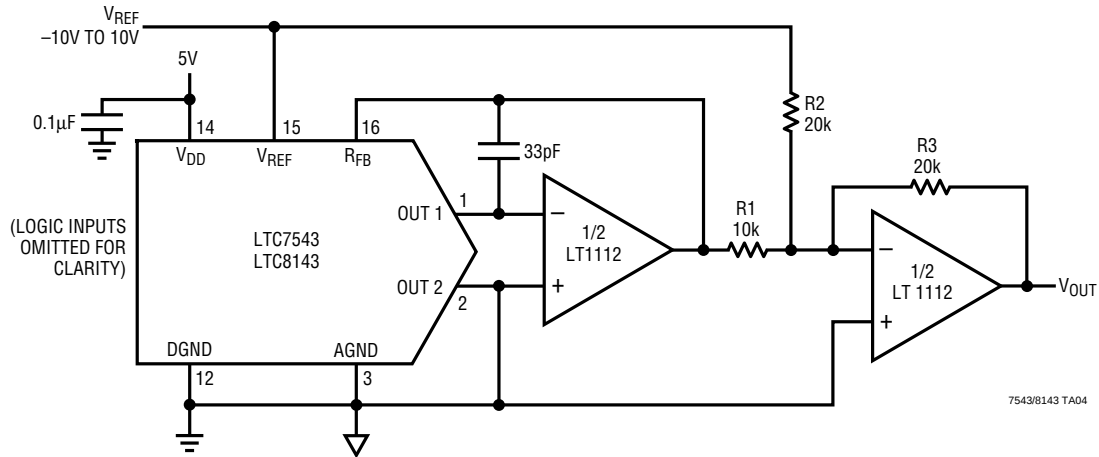


Unipolar Binary Code Table

| DIGITAL INPUT<br>BINARY NUMBER IN<br>DAC REGISTER |      |      | ANALOG OUTPUT<br>$V_{OUT}$            |
|---------------------------------------------------|------|------|---------------------------------------|
| MSB                                               |      | LSB  |                                       |
| 1111                                              | 1111 | 1111 | $-V_{REF}$ (4095/4096)                |
| 1000                                              | 0000 | 0000 | $-V_{REF}$ (2048/4096) = $-V_{REF}/2$ |
| 0000                                              | 0000 | 0001 | $-V_{REF}$ (1/4096)                   |
| 0000                                              | 0000 | 0000 | 0V                                    |

## TYPICAL APPLICATIONS

### Bipolar Operation (4-Quadrant Multiplication)



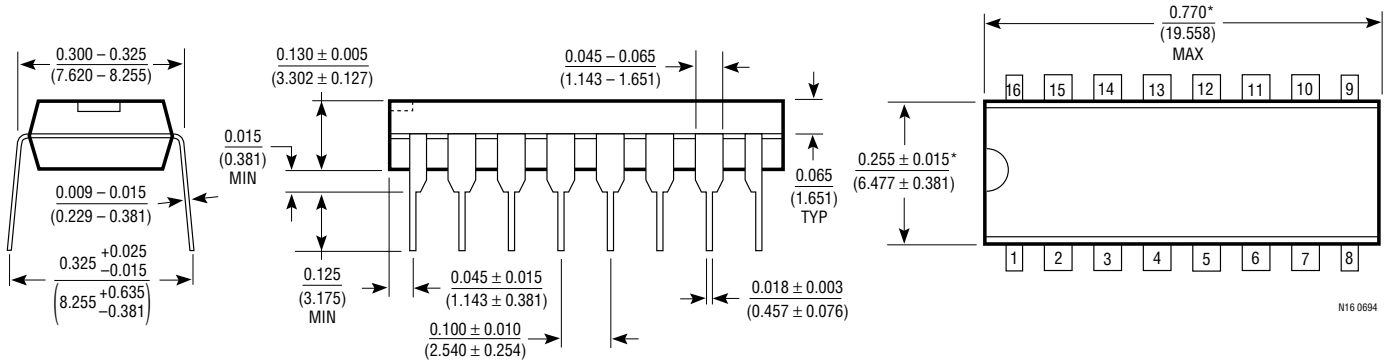
### Bipolar Offset Binary Code Table

| DIGITAL INPUT<br>BINARY NUMBER IN<br>DAC REGISTER |      |      | ANALOG OUTPUT<br>$V_{OUT}$        |
|---------------------------------------------------|------|------|-----------------------------------|
| MSB                                               |      | LSB  |                                   |
| 1111                                              | 1111 | 1111 | $V_{REF} (2047/2048)$             |
| 1000                                              | 0000 | 0001 | $V_{REF} (1/2048)$                |
| 1000                                              | 0000 | 0000 | 0V                                |
| 0111                                              | 1111 | 1111 | $-V_{REF} (1/2048)$               |
| 0000                                              | 0000 | 0000 | $-V_{REF} (2048/2048) = -V_{REF}$ |

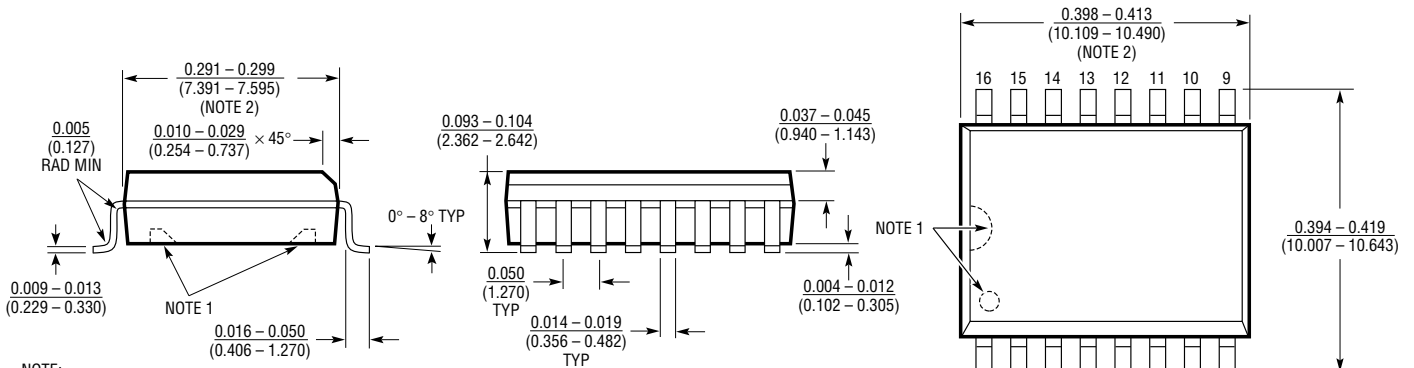
## PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

### N Package 16-Lead Plastic DIP



### S Package 16-Lead Plastic SOL



## RELATED PARTS

| PART NUMBER             | DESCRIPTION                               | COMMENTS                                     |
|-------------------------|-------------------------------------------|----------------------------------------------|
| LTC1257                 | Complete Serial I/O $V_{OUT}$ 12-Bit DAC  | 5V to 15V Single Supply in 8-Pin SO and PDIP |
| LTC1451/LTC1452/LTC1453 | Complete Serial I/O $V_{OUT}$ 12-Bit DACs | 3V/5V Single Supply in 8-Pin SO and PDIP     |
| LTC7541A                | Parallel I/O Multiplying 12-Bit DAC       | 12-Bit Wide Input                            |
| LTC8043                 | Serial Multiplying 12-Bit DAC             | 8-Pin SO and PDIP                            |