ADD-A-PAK Generation VII Power Modules
Thyristor/Thyristor, 75 A

ADD-A-PAK

PRODUCT SUMMARY	
$I_{T(AV)}$	75 A
Type	Modules - Thyristor, Standard

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

RoHS COMPLIANT

- High voltage
- Industrial standard package
- Low thermal resistance
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION

These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS and battery charger.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$	85 °C	75	A
$I_{T(RMS)}$		115	
I_{TSM}	50 Hz	1300	
	60 Hz	1360	
I^2t	50 Hz	8.45	kA^2s
	60 Hz	7.68	
$I^2\sqrt{t}$		84.5	$kA^2\sqrt{s}$
V_{RRM}	Range	400 to 1600	V
T_{Stg}		-40 to 125	°C
T_J		-40 to 125	°C

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ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{RRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	V_{DRM}, MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V	I_{RRM}, I_{DRM} AT 125 °C mA
VSK.71	04	400	500	400	15
	08	800	900	800	
	12	1200	1300	1200	
	16	1600	1700	1600	

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current	$I_{T(AV)}$	180° conduction, half sine wave, T_C = 85 °C			75	A
Maximum continuous RMS on-state current	$I_{T(RMS)}$	DC			115	A
		T_C			80	°C
Maximum peak, one-cycle non-repetitive on-state current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	1300	A
		t = 8.3 ms			1360	
		t = 10 ms	100 % V_{RRM} reapplied		1093	
		t = 8.3 ms			1140	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied	Initial $T_J = T_J$ maximum	8.45	kA^2s
		t = 8.3 ms			7.68	
		t = 10 ms	100 % V_{RRM} reapplied		5.97	
		t = 8.3 ms			5.45	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$ (1)	t = 0.1 ms to 10 ms, no voltage reapplied $T_J = T_J$ maximum			84.5	$kA^2\sqrt{s}$
Maximum value of threshold voltage	$V_{T(TO)}$ (2)	Low level (3)	$T_J = T_J$ maximum		0.96	V
		High level (4)			1.08	
Maximum value of on-state slope resistance	r_t (2)	Low level (3)	$T_J = T_J$ maximum		3.28	mΩ
		High level (4)			2.86	
Maximum on-state voltage drop	V_{TM}	$I_{TM} = \pi \times I_{T(AV)}$	T_J = 25 °C		1.72	V
Maximum non-repetitive rate of rise of turned on current	dI/dt	T_J = 25 °C, from 0.67 V_{DRM}, $I_{TM} = \pi \times I_{T(AV)}$, I_g = 500 mA, t_r < 0.5 µs, t_p > 6 µs			150	A/µs
Maximum holding current	I_H	T_J = 25 °C, anode supply = 6 V, resistive load, gate open circuit			250	mA
Maximum latching current	I_L	T_J = 25 °C, anode supply = 6 V, resistive load			400	

Notes

(1) I^2t for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$

(2) Average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$

(3) 16.7 % x π x I_{AV} < I < π x I_{AV}

(4) I > π x I_{AV}

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TRIGGERING					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**VALUES**	**UNITS**
Maximum peak gate power	P_{GM}			12	W
Maximum average gate power	$P_{G(AV)}$			3.0	
Maximum peak gate current	I_{GM}			3.0	A
Maximum peak negative gate voltage	$-V_{GM}$			10	V
Maximum gate voltage required to trigger	V_{GT}	T_J = - 40 °C	Anode supply = 6 V resistive load	4.0	
		T_J = 25 °C		2.5	
		T_J = 125 °C		1.7	
Maximum gate current required to trigger	I_{GT}	T_J = - 40 °C	Anode supply = 6 V resistive load	270	mA
		T_J = 25 °C		150	
		T_J = 125 °C		80	
Maximum gate voltage that will not trigger	V_{GD}	T_J = 125 °C, rated V_{DRM} applied		0.25	V
Maximum gate current that will not trigger	I_{GD}	T_J = 125 °C, rated V_{DRM} applied		6	mA

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	I_{RRM}, I_{DRM}	T_J = 125 °C, gate open circuit	15	mA
Maximum RMS insulation voltage	V_{INS}	50 Hz	3000 (1 min) 3600 (1 s)	V
Maximum critical rate of rise of off-state voltage	dV/dt	T_J = 125 °C, linear to 0.67 V_{DRM}	1000	V/µs

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER		**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Junction operating and storage temperature range		T_J, T_{Stg}		-40 to 125	°C
Maximum internal thermal resistance, junction to case per leg		R_{thJC}	DC operation	0.29	°C/W
Typical thermal resistance, case to heatsink per module		R_{thCS}	Mounting surface flat, smooth and greased	0.1	
Mounting torque ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	4	Nm
	busbar			3	
Approximate weight				75	g
				2.7	oz.
Case style			JEDEC®	AAP GEN VII (TO-240AA)	

ΔR CONDUCTION PER JUNCTION											
DEVICES	**SINE HALF WAVE CONDUCTION**					**RECTANGULAR WAVE CONDUCTION**					**UNITS**
	180°	**120°**	**90°**	**60°**	**30°**	**180°**	**120°**	**90°**	**60°**	**30°**	
VSK.71..	0.052	0.062	0.079	0.116	0.197	0.037	0.064	0.085	0.121	0.200	°C/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

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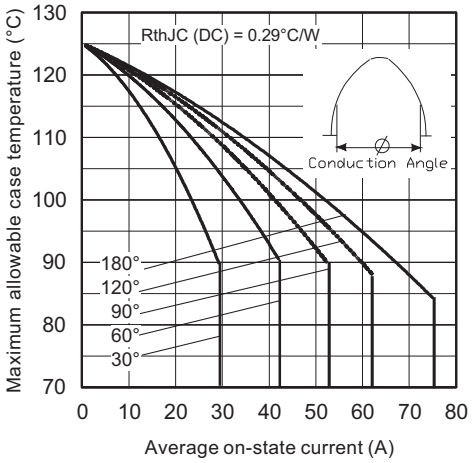

Fig. 1 - Current Ratings Characteristics

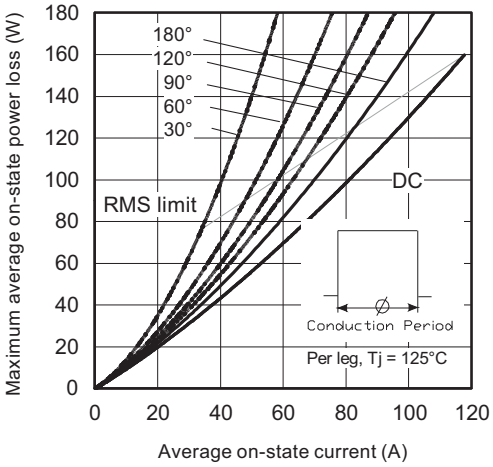

Fig. 4 - On-State Power Loss Characteristics

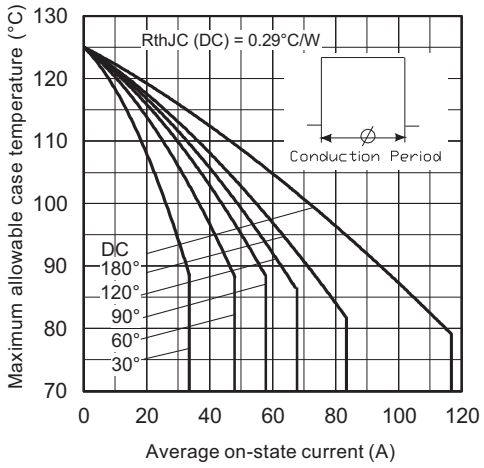

Fig. 2 - Current Ratings Characteristics

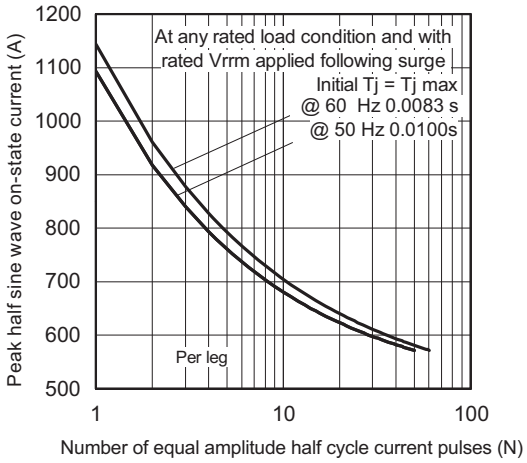

Fig. 5 - Maximum Non-Repetitive Surge Current

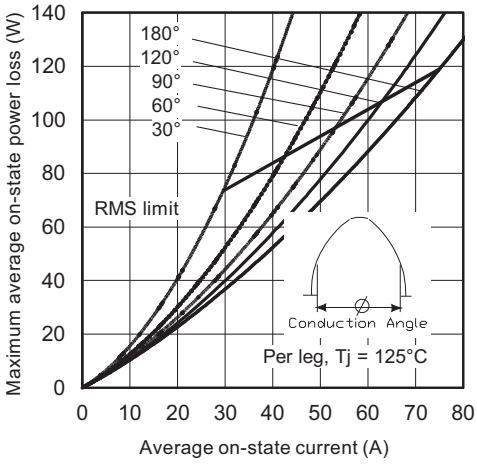

Fig. 3 - On-State Power Loss Characteristics

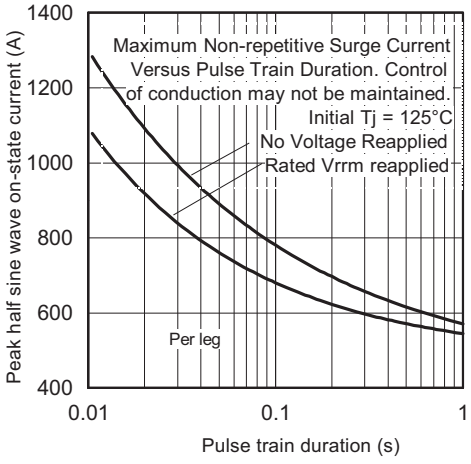

Fig. 6 - Maximum Non-Repetitive Surge Current

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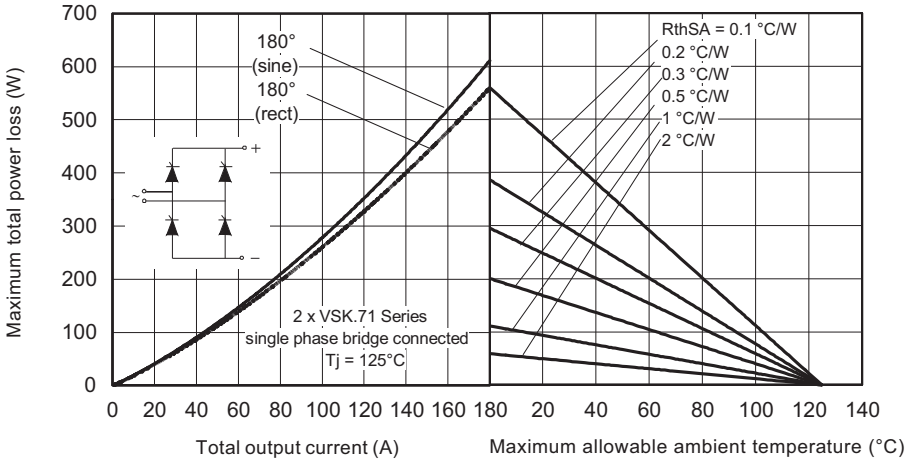

Fig. 7 - On-State Power Loss Characteristics

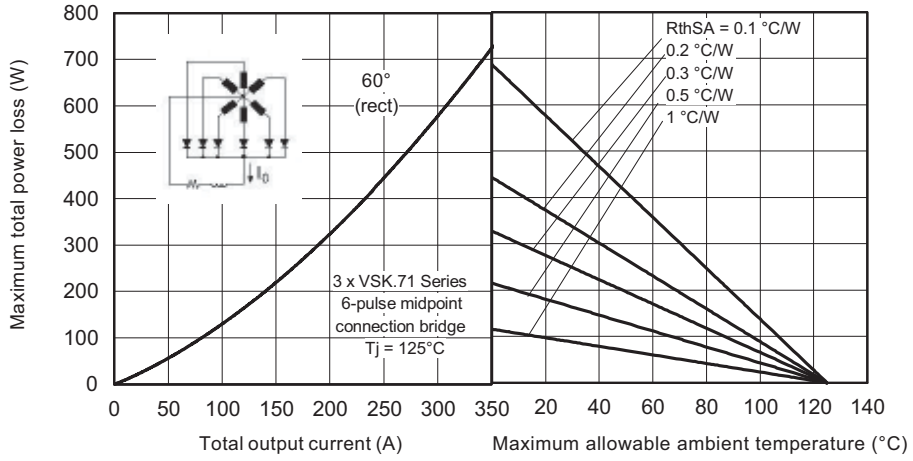

Fig. 8 - On-State Power Loss Characteristics

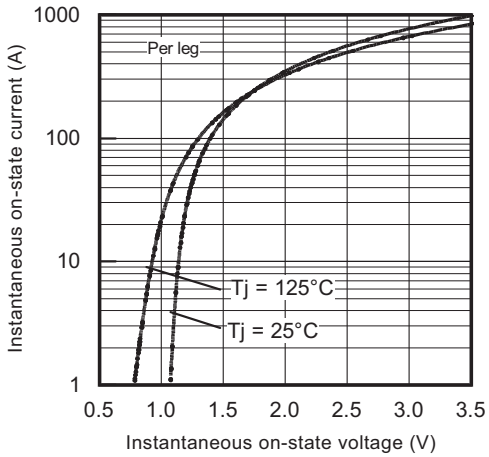

Fig. 9 - On-State Voltage Characteristics

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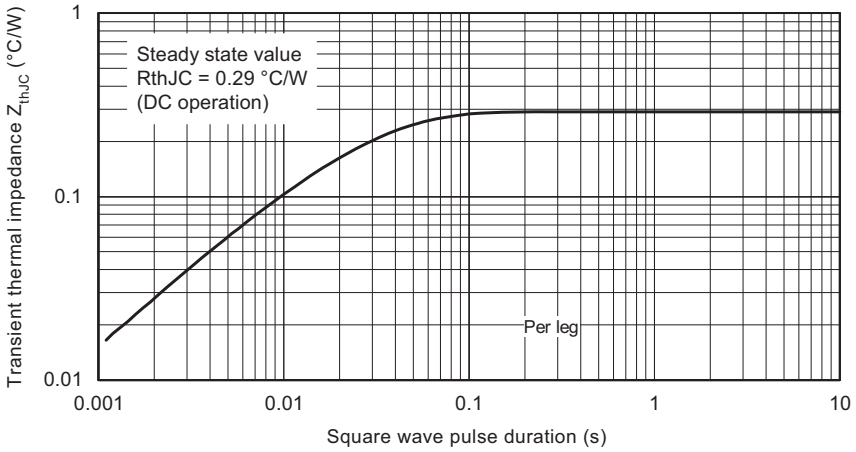

Fig. 10 - Thermal Impedance Z_{thJC} Characteristics

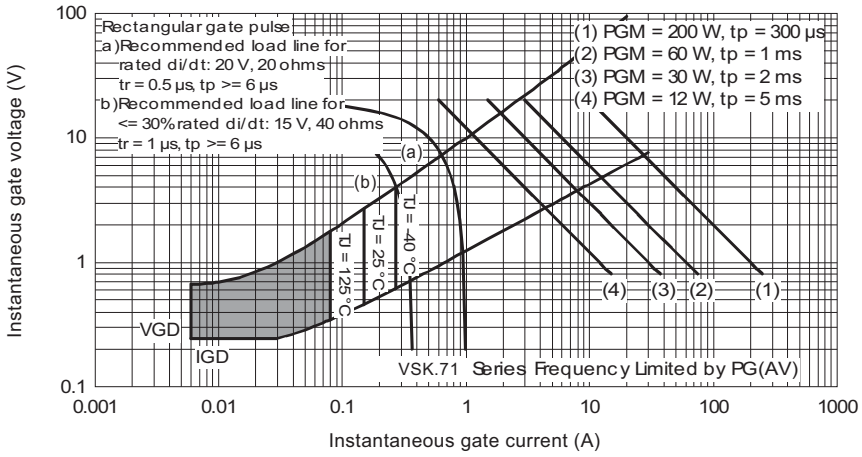

Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

VSK	U	71	/	16
1	2	3		4

- 1 - Module type
- 2 - Circuit configuration (see end of datasheet)
- 3 - Current code (75 A)
- 4 - Voltage code (see Voltage Ratings table)

Note

- To order the optional hardware go to www.vishay.com/doc?95172

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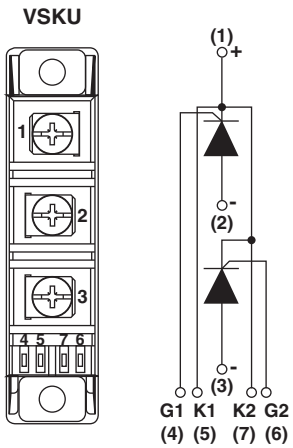
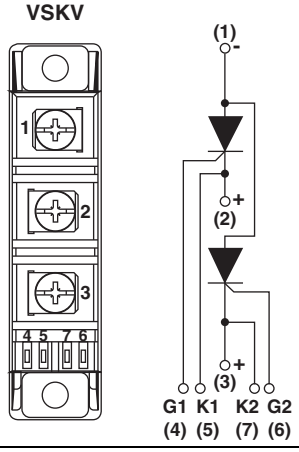
CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Two SCRs common cathodes	U	VSKU 
Two SCRs common anodes	V	VSKV 

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95368

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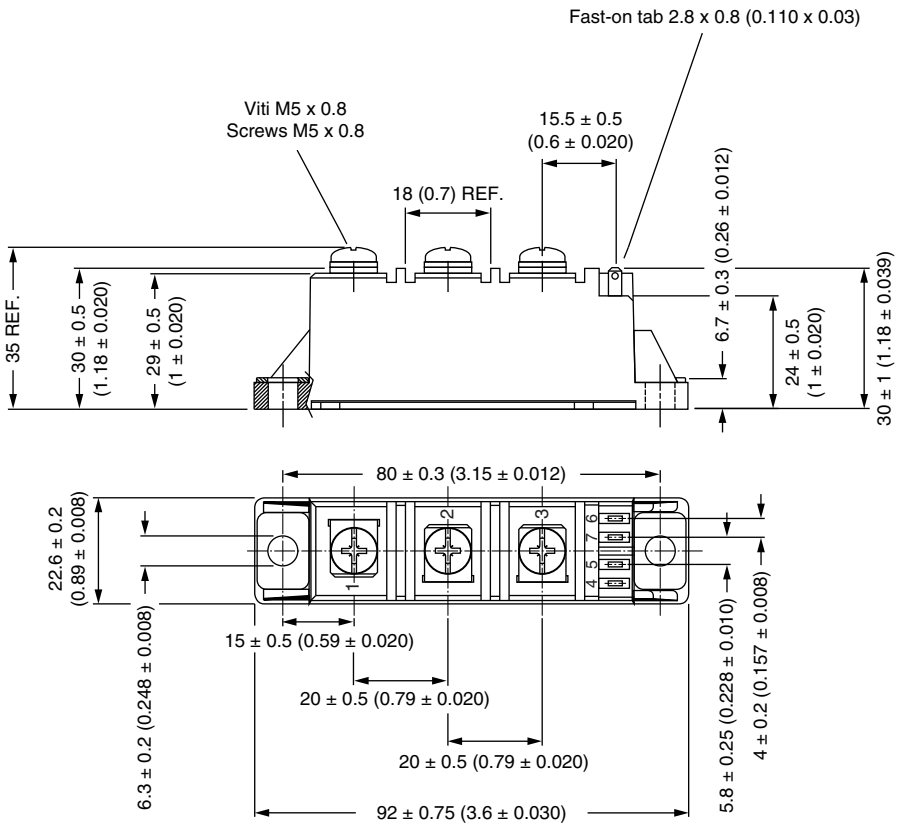
ADD-A-PAK Generation VII - Thyristor

DIMENSIONS in millimeters (inches)



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