CMOS 4-BIT MICROCONTROLLER

TMP47C26N
TMP47C26F

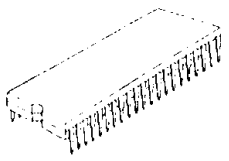
The 47C26 is a high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series with a DTMF generator and a large capacity RAM for repertory dialing applications, and which is suitable for utilization in telephones. The 47C26 is also capable of operation with low voltages such as those supplied by telephone line.

PART No.	ROM	RAM	PACKAGE
TMP47C26N	2048 x 8-bit	384 x 4-bit	SDIP42
TMP47C26F			QFP44

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 33.3μs (at 480KHz)
- ◆Low voltage operation : 2.2V min.
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting: 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (35 pins)
  - Input 2ports 5pins
  - Output 1port 3pins
  - I/O 7ports 27pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurment mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, and leading/trailing edge shift mode
- ◆DTMF (Dual Tone Multi Frequency) output
  - DTMF output with one instruction
  - Single tone output
- ◆RAM for repertory dial : 384 x 4-bit max.
- ◆Hold function
  - Battery/Capacitor back-up
  - Hold function controlled by port K0.
- ◆Real Time Emulator : BM47215A

SDIP42



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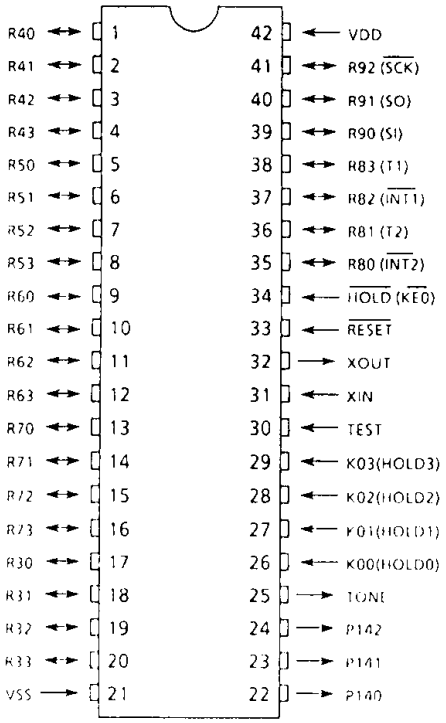
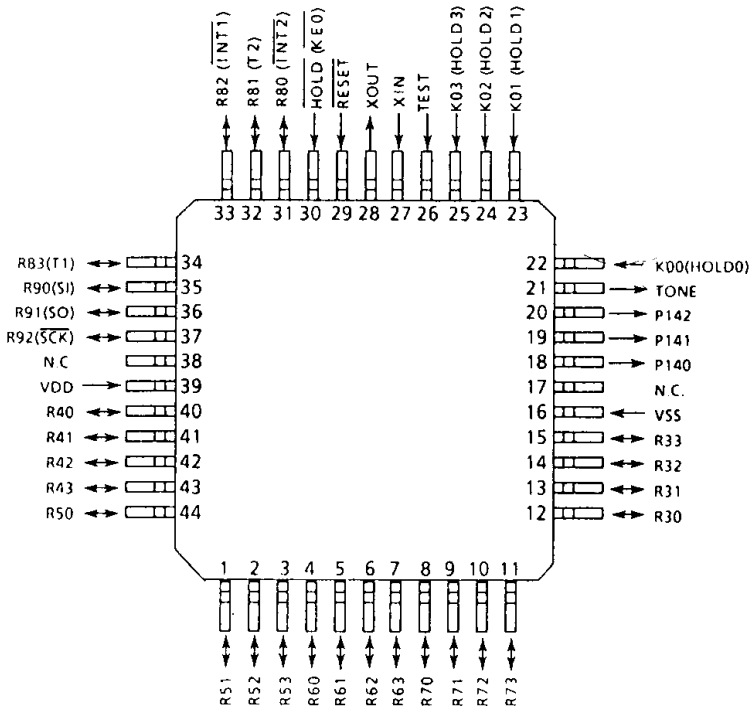
PIN ASSIGNMENT (TOP VIEW)

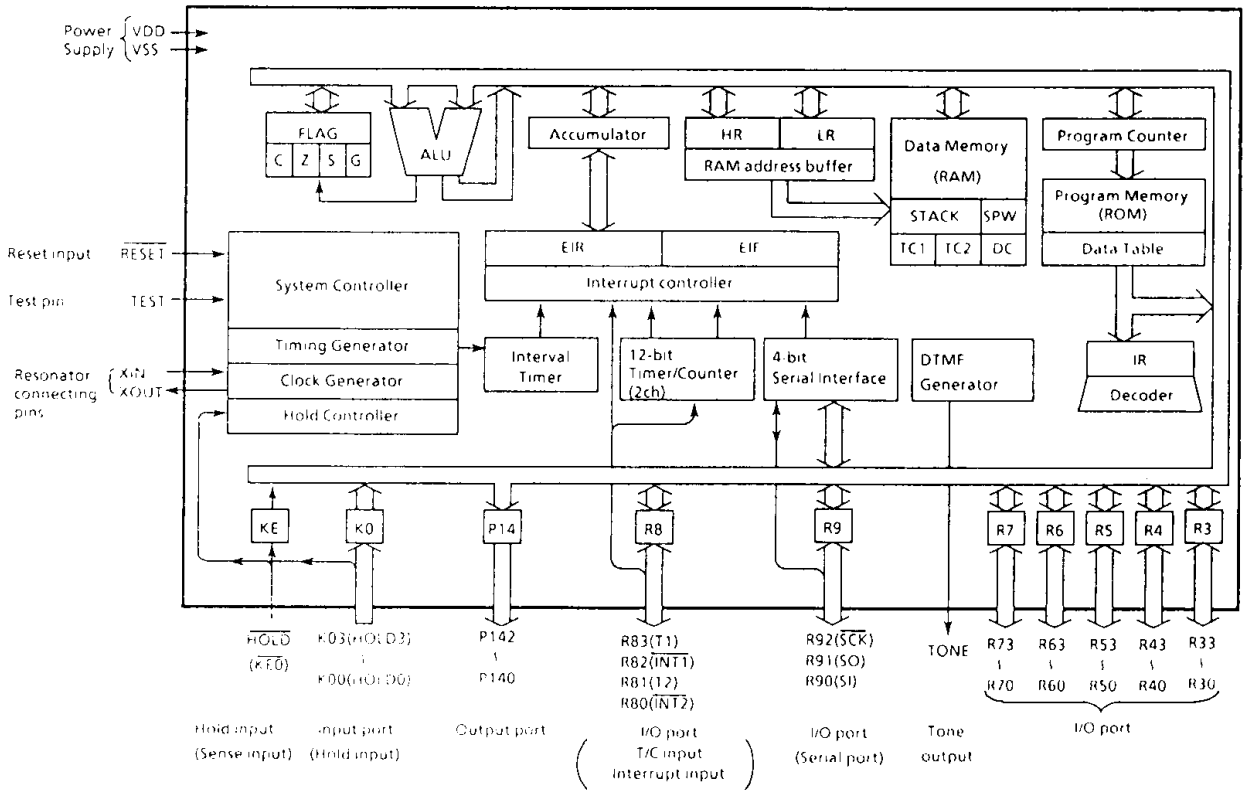
(1) SDIP42



(2) QFP44



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) - K00 (HOLD0)	Input (Input)	4-bit input port	Hold request/release signal input (Active "H")
R33 - R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 - R40			
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P142 - P140	Output	3-bit output port with latch	
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power Supply	+ 2.2V to 4.0V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

As the description is provided with priority on those parts differing from the 47C25.

1. PARTS DIFFERING FROM THE 47C25

(1) P14 (output) port is extended
(2) There is additional to the single tone controlled by TONE command register (OP0D/IP0D)
(3) There is different to the tone output frequency
(4) There is different to the electrical characteristics

(1) P14 (P142-P140)

The 3-bit output port with latch. The latch is initialized to "1" during reset.

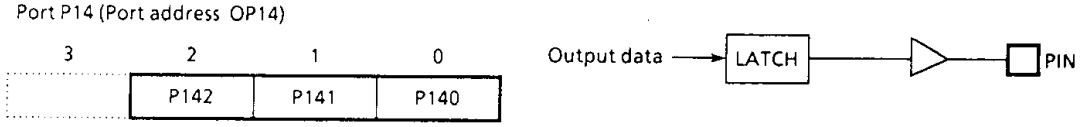


Figure 1. Port P14

(2) Single TONE output

In the enable mode of single tone output operation is as same as the 47C25.

In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted.

At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C26 has no tone output signal.

TONE command register
(Port address : OP0D / IP0D Initial value : 0*00)

3	2	1	0
STE		(R/W)	(CE)

STE	Controls single tone output
0 :	Disable mode of single tone output
1 :	Enable mode of single tone output

Figure 2. TONE Command Register

(3) Tone output frequency

ROW register
(Port address : OP01 / IP01 Initial value : 0000)

Selects ROW tone frequency	
0001 :	Outputs 697.7Hz single tone
0010 :	Outputs 769.2Hz single tone
0100 :	Outputs 857.1Hz single tone
1000 :	Outputs 937.5Hz single tone

COLUMN register
(Port address : OP02 / IP02 Initial value : 0000)

Selects COLUMN tone frequency	
0001 :	Outputs 1212.1Hz single tone
0010 :	Outputs 1333.3Hz single tone
0100 :	Outputs 1481.5Hz single tone
1000 :	Outputs 1621.6Hz single tone

Figure 3. ROW, COLUMN Register

(4) ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Supply Voltage	V_{DD}	In the Normal mode	2.2	–	4.0	V
Supply Current	I_{DD}	Except TONE generating	–	0.1	0.2	mA
	I_{DDT}	TONE generating	–	0.5	1.0	
Clock Frequency	fc		–	480	–	KHz
Instruction Cycle Time	tcy		–	33.3	–	μs
Tone Output Voltage (ROW)	V_{TONE}	$R_L \geq 10K\Omega$, $V_{DD} \approx 2.2V$	130	175	230	mVrms
Frequency Stability	Δf	Except error of osc. frequency	–	–	0.7	%