

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA7280P, TA7281P

5.8W DUAL AUDIO POWER AMPLIFIER.

22W BTL AUDIO POWER AMPLIFIER.

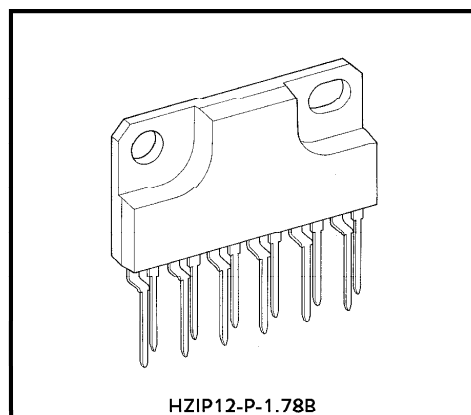
The TA7280P, TA7281P are dual audio power amplifier for consumer applications.

It is designed for high power, low distortion and low noise.

It also contains various kind of protectors.

It is suitable for car-audio power amplifier with high performance.

The kinds of pin configuration are Available : Normal (TA7280P) and Reverse (TA7281P) for easier layout design of PC-board when used in BTL-stereo application.



Weight : 4.04g (Typ.)

FEATURES

- High Power
 - : $P_{OUT}(1) = 22W$ (Typ.)
($V_{CC} = 14.4V$, $f = 1kHz$, $THD = 10\%$, $R_L = 4\Omega$, BTL)
 - $P_{OUT}(2) = 19W$ (Typ.)
($V_{CC} = 13.2V$, $f = 1kHz$, $THD = 10\%$, $R_L = 4\Omega$, BTL)
 - $P_{OUT}(3) = 15W$ (Typ.)
($V_{CC} = 13.2V$, $f = 1kHz$, $THD = 1\%$, $R_L = 4\Omega$, BTL)
 - $P_{OUT}(4) = 5.8W$ (Typ.) / ch
($V_{CC} = 13.2V$, $f = 1kHz$, $THD = 10\%$, $R_L = 4\Omega$, DUAL)
- Low Distortion
 - : $THD(1) = 0.03\%$ (Typ.)
($V_{CC} = 13.2V$, $f = 1kHz$, $P_{OUT} = 4W$, $R_L = 4\Omega$, $G_V = 40dB$, BTL)
 - $THD(2) = 0.06\%$ (Typ.)
($V_{CC} = 13.2V$, $f = 1kHz$, $P_{OUT} = 1W$, $R_L = 4\Omega$, $G_V = 52dB$, DUAL)
- Low Noise
 - : $V_{NO}(1) = 0.14mV_{rms}$ (Typ.)
($V_{CC} = 13.2V$, $R_L = 4\Omega$, $G_V = 40dB$, $R_g = 0$, DIN Noise : DIN45405, BTL)
 - $V_{NO}(2) = 0.7mV_{rms}$ (Typ.)
($V_{CC} = 13.2V$, $R_L = 4\Omega$, $G_V = 52dB$, $R_g = 10k\Omega$, $BW = 20Hz \sim 20kHz$, DUAL)
- Protector Circuit
 - : Thermal Shut Down, Over Voltage Protection, Out- V_{CC} Short, OUT-GND Short and Out-Out Short Protection.
- Operating Supply Voltage Range
 - : $V_{CC}(opr) = 9 \sim 18V$

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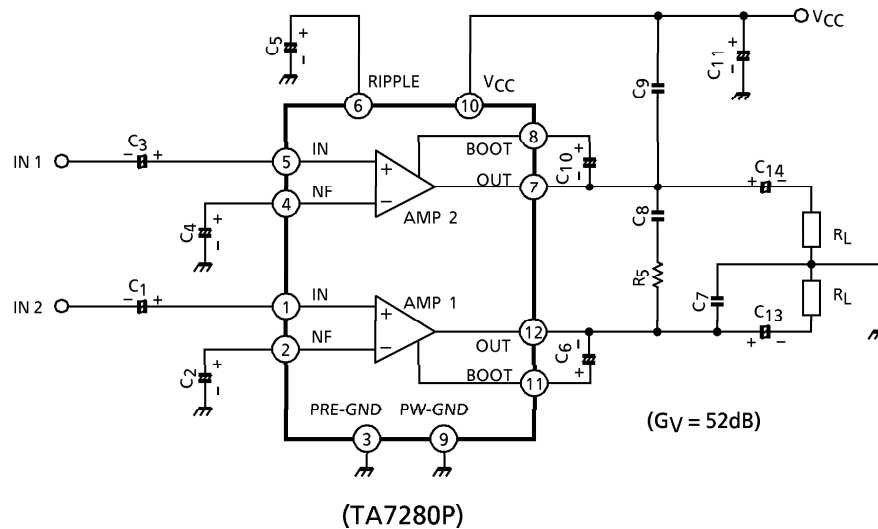
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**BLOCK DIAGRAM
DUAL**



APPLICATION INFORMATION (This explanatory terminal number is for TA7280P)

1. VOLTAGE gain adjustment

(1) DUAL amplifier

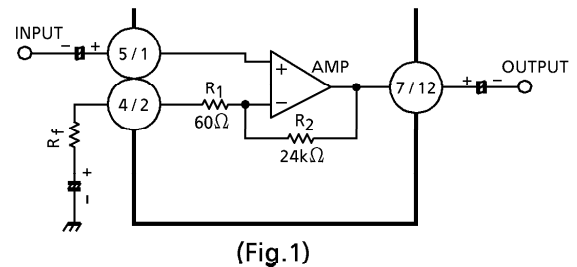
The voltage gain G_V is determined by R_1 , R_2 and R_f in (Fig.1).

$$G_V = 20 \log \frac{R_f + R_1 + R_2}{R_f + R_1} \quad (\text{dB})$$

In case of $R_f = 0$

The voltage gain is set as follows :

$$G_V = 52\text{dB (Typ.)}$$



(2) BTL amplifier

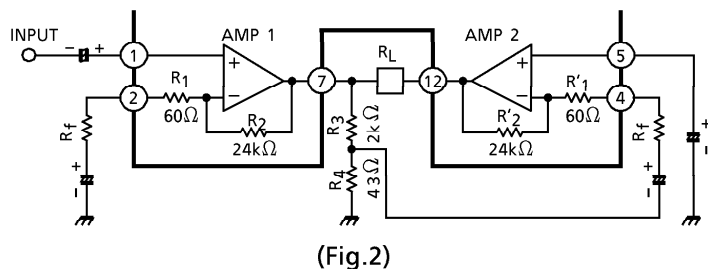
The recommended BTL connection amplifier shown in (Fig.2).

AMP. 1 is noninverting amplifier and AMP. 2 is invert one.

The output voltage is divided by resistors R_3 and R_4 .

The divided voltage is applied to inverting input of AMP. 2. R_3 and R_4 are determined in the following equation.

$$\frac{R_3 + R_4}{R_3} = 20 \log \frac{R_f + R_1 + R_2}{R_f + R_1} \quad (\text{dB}) \quad G_V \text{ in Dual Mode}$$



The voltage gain in this circuit is 6dB higher than that in Dual mode.

$$G_V = 20 \log \frac{R_f + R_1 + R_2}{R_f + R_1} \text{ (dB)}$$

In case of $R_f = 0$

$$G_V = 52 + 6 = 58 \text{ (dB)}$$

In case of $R_f = 430\Omega$

$$G_V = 34 + 6 = 40 \text{ (dB)}$$

Each voltage gain can be set as shown above.

2. Muting

Audio muting can be accomplished by connecting pin⑥ (ripple filter) to GND as shown in (Fig.3). Then, the bias circuits are cut off.

However, caution must be exercised to the following items.

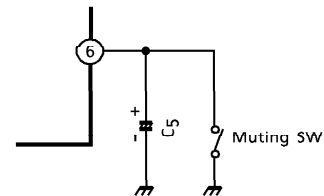
- (1) The recovery time from the muting operation is determined by the capacities of the ripple filter capacitor between pin⑥ and GND, and of the capacitor for NF.
- (2) As this muting system is operated by the short-circuit of ripple filter : C_5 , the ripple rejection ratio becomes worse in the muting condition.

At mute ON, some pop noise of breaking the bias are produced.

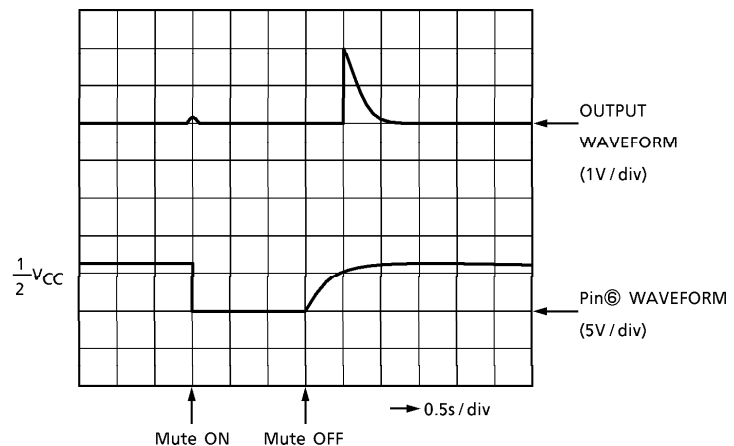
The output waveform at muting ON / OFF during BTL, are shown in (Fig.4).

(Provided $V_{CC} = 13.2V$, $R_L = 4\Omega$, non-signal.)

50dB or more can be obtained for muting amount.



(Fig.3)



$V_{CC} = 13.2V$, $R_L = 4\Omega$, INPUT SHORT, BTL

(Fig.4)

3. Measures against oscillation

C_7, C_8, C_9, C_{12} : The capacitor of polyester film having small variation of the temperature characteristics is recommended as the capacitor for oscillation prevention.

C_{12} : Reduces the gain in the high range frequency (150kHz or over) and increases the oscillation allowance.

R_5 : Increases the oscillation allowance at output clipping of the low range frequency (100Hz or less).

Since the oscillation allowance varies according to the following item, carry out the temperature test to confirm the oscillation allowance.

(1) Gain to be used (G_V setting).

(2) Capacity of capacitor

(3) Kinds of capacitor

(4) Layout of printed board

It is recommended to use the capacitor having the capacity exceeding the oscillation stopping value. At using with the voltage gain G_V lowered or with the high range frequency and the oscillation becomes liable to be produced.

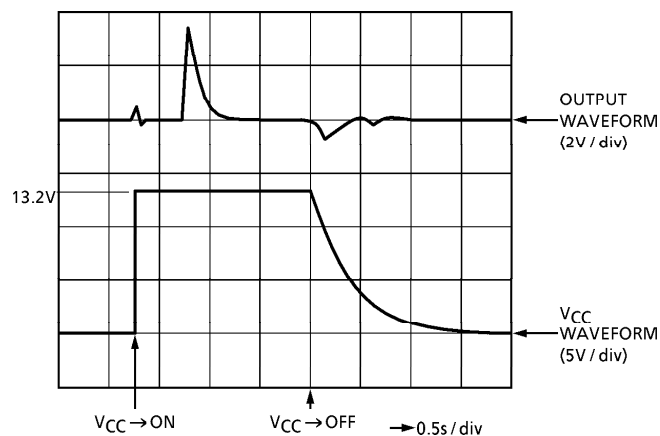
Therefore, application with $G_V = 40\text{dB}$ or over is advisable.

Especially for using with the gain lowered in DUAL operation, insert 1000pF between NF (Pin② and Pin④) and GND.

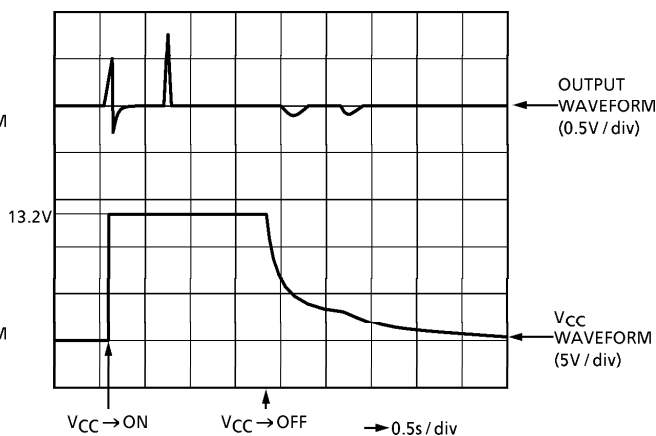
This capacitor reduces the gain of the high range frequency and is effective for oscillation prevention.

4. Output waveform at power supply ON/OFF (Reference)

BTL and dual amplifier DC output waveforms in the condition of $V_{CC} = 13.2\text{V}$, $R_L = 4\Omega$ at non-signal (input short) are shown in (Fig.5) and (Fig.6).



(Fig.5) BTL operation



(Fig.6) DEAL operation

The popping time at power supply ON/OFF varies according to the rise and fall times.

The condition in which the power supply is rapidly and repeatedly made ON/OFF, that is, the condition in which the charge is made on the external capacitor of IC is different from the conditions shown in (Fig.5) and (Fig.6).

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2s)	V _{CC} (surge)	45	V
DC Supply Voltage	V _{CC} (DC)	25	V
Operating Supply Voltage	V _{CC} (opr)	18	V
Output Current (Peak)	I _O (Peak)	4.5	A
Power Dissipation	P _D	25	W
Operating Temperature	T _{opr}	– 30~85	°C
Storage Temperature	T _{stg}	– 55~150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 13.2V, R_L = 4Ω, R_g = 600Ω, f = 1kHz, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current		I _{CCQ}	2	V _{IN} = 0	—	80	145	mA
BLT Connection Mode	Output Power	P _{OUT} (1)	1	THD = 10%, V _{CC} = 14.4V	—	22	—	W
		P _{OUT} (2)	1	THD = 10%	16	19	—	
		P _{OUT} (3)	1	THD = 1%	12	15	—	
	Total Harmonic Distortion	THD (1)	1	P _{OUT} = 4W, G _V = 40dB	—	0.03	0.25	%
	Output Offset Voltage	V _{OFF}	1	V _{IN} = 0	—	0	0.35	V
	Voltage Gain	G _V (1)	1	V _{OUT} = 0.775V _{rms} (0dBm)	—	40	—	dB
	Output Noise Voltage	V _{NO} (1)	1	R _g = 0 DIN45405 noise filter	—	0.14	—	mV _{rms}
DUAL Mod	Ripple Rejection Ratio	R.R. (1)	1	f _{ripple} = 100Hz V _{ripple} = 0.775V _{rms} (0dBm)	—	– 52	– 40	dB
	Output Power	P _{OUT} (4)	2	THD = 10%	5	5.8	—	W
	Total Harmonic Distortion	THD (2)	2	P _{OUT} = 1W	—	0.06	0.30	%
	Voltage Gain	G _V (2)	2	V _{OUT} = 0.775V _{rms} (0dBm)	50	52	54	dB
	Voltage Gain Ratio	ΔG _V	2	V _{OUT} = 0.775V _{rms} (0dBm)	– 1	0	1	dB
	Output Noise Voltage	V _{NO} (2)	2	R _g = 10kΩ BW = 20Hz~20kHz	—	0.7	1.5	mV _{rms}
	Ripple Rejection Ratio	R.R. (2)	2	f _{ripple} = 100Hz V _{ripple} = 0.775V _{rms} (0dBm)	—	– 52	– 40	dB
	Cross Talk	C.T.	2	V _{OUT} = 0.775V _{rms} (0dBm)	—	– 57	—	dB
Input Resistance		R _{IN}	2	f = 1kHz	—	33	—	kΩ

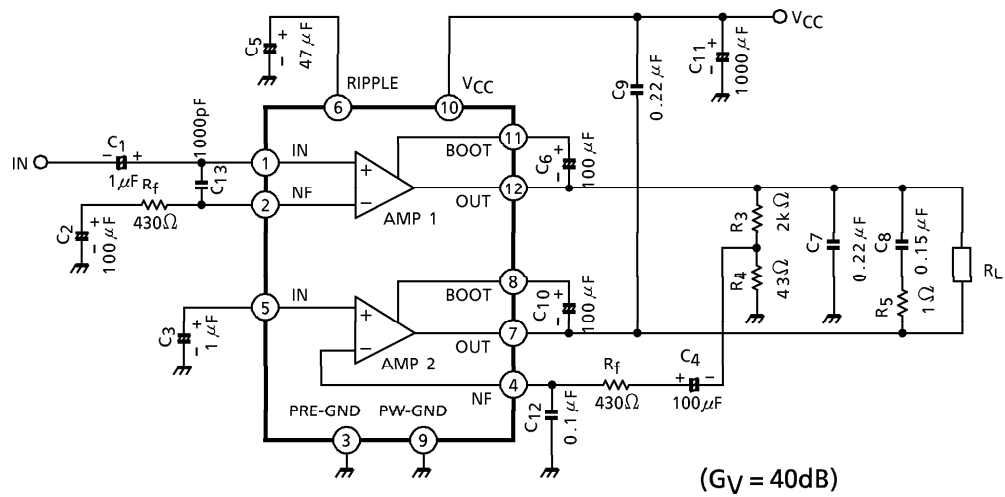
TYP. DC VOLTAGE OF EACH TERMINAL
(V_{CC} = 13.2V, T_a = 25°C, dual mode test circuit)

TERMINAL No.		1	2	3	4	5	6	7	8	9	10	11	12
DC VOLTAGE (V)	TA7280P	1.5	1.5	GND	1.5	1.5	6.4	6.4	12.3	GND	V _{CC}	12.3	6.4
	TA7281P	6.4	12.3	V _{CC}	GND	12.3	6.4	6.4	1.5	1.5	GND	1.5	1.5

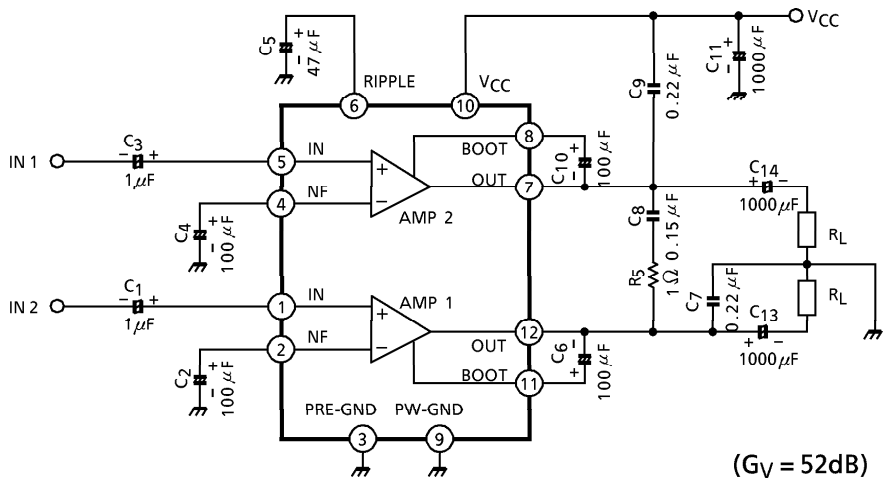
TEST CIRCUIT / APPLICATION CIRCUIT

TA7280P

(1) BTL

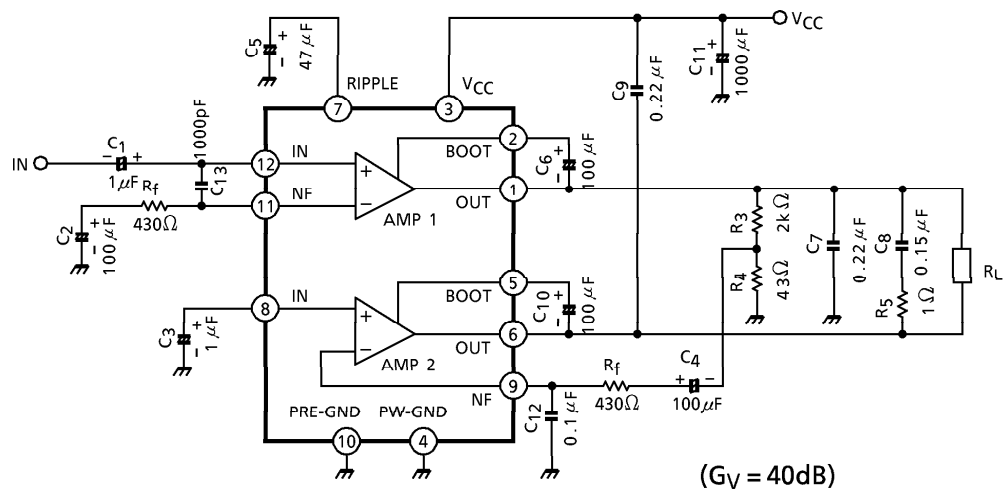


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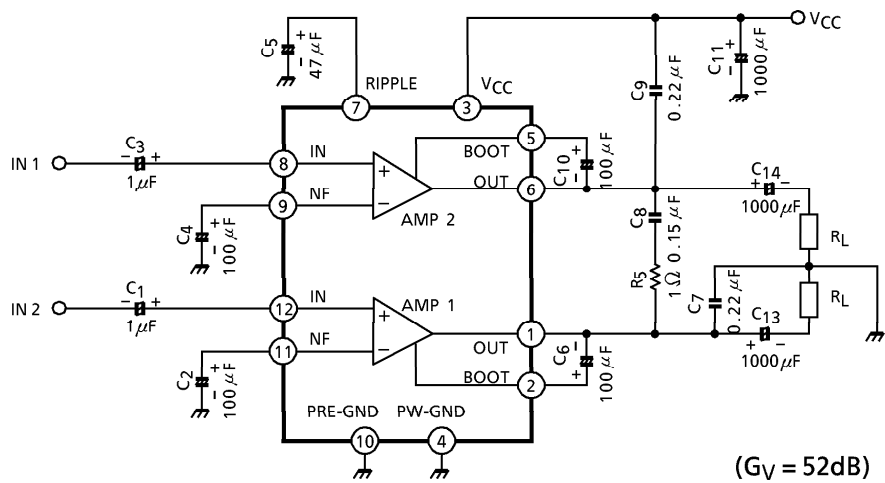


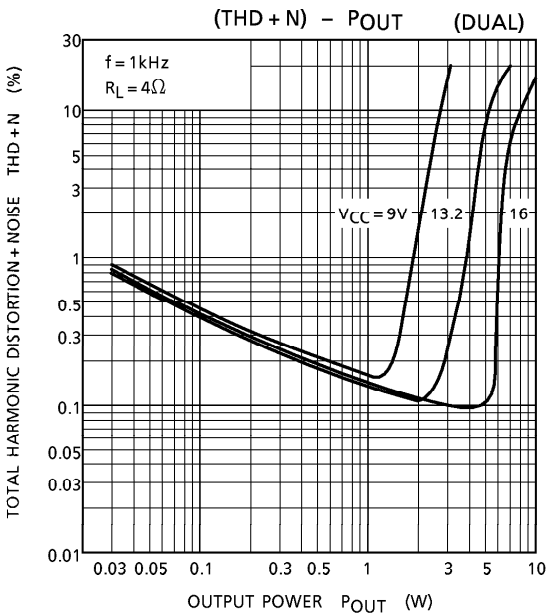
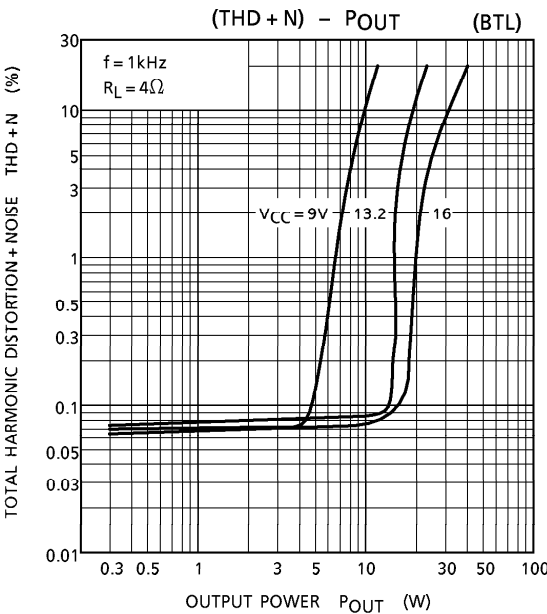
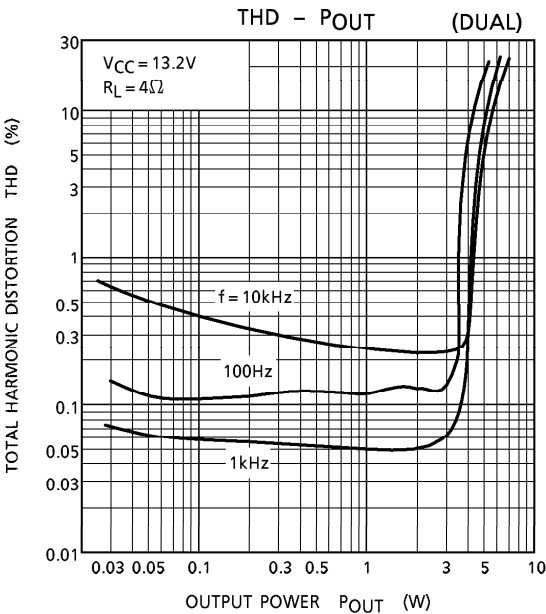
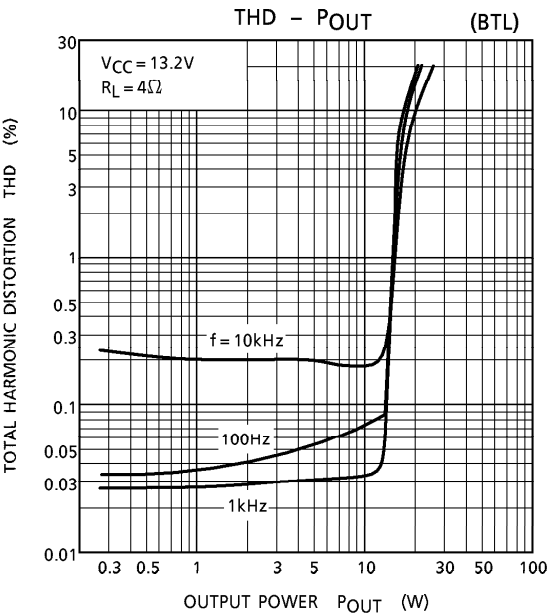
TA7281P

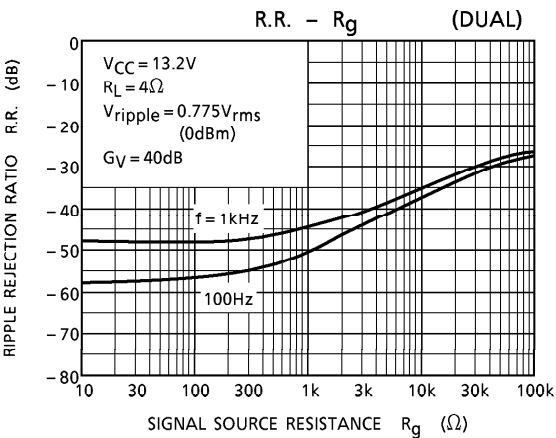
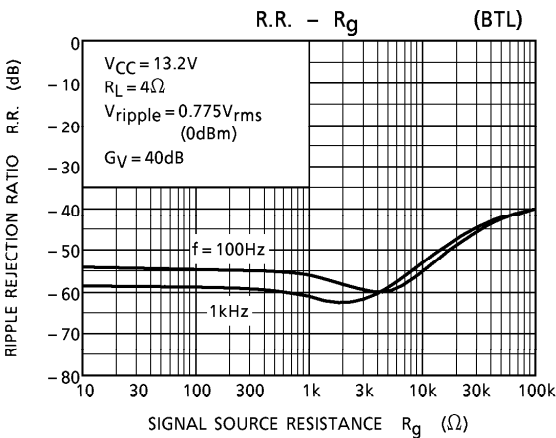
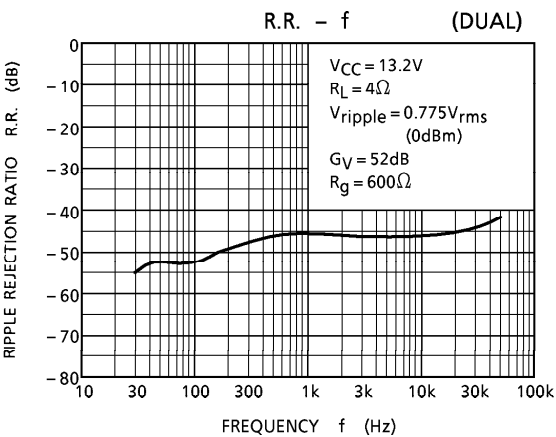
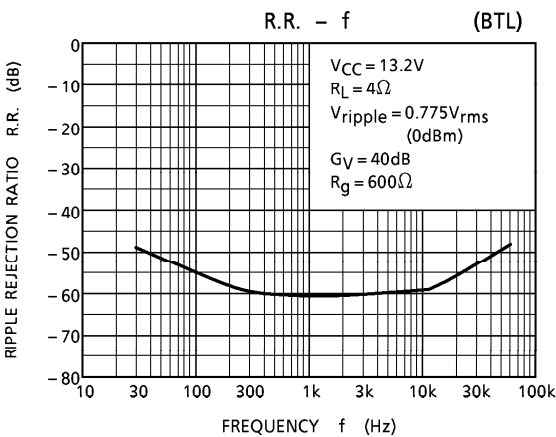
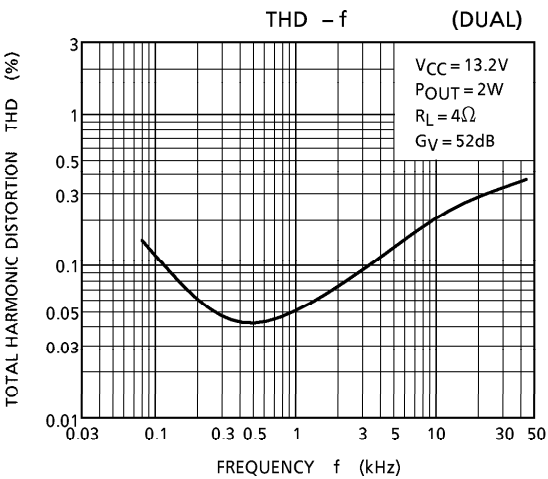
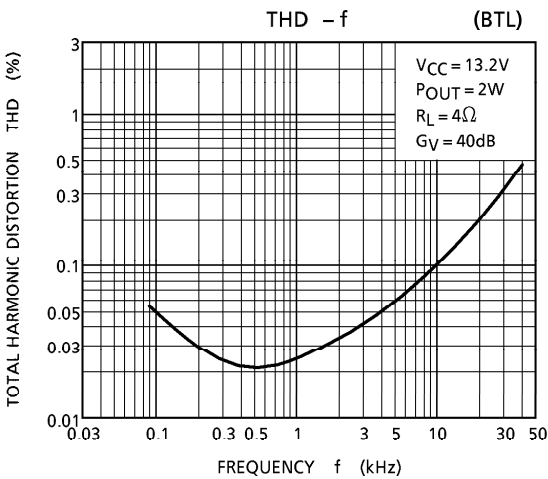
(1) BTL

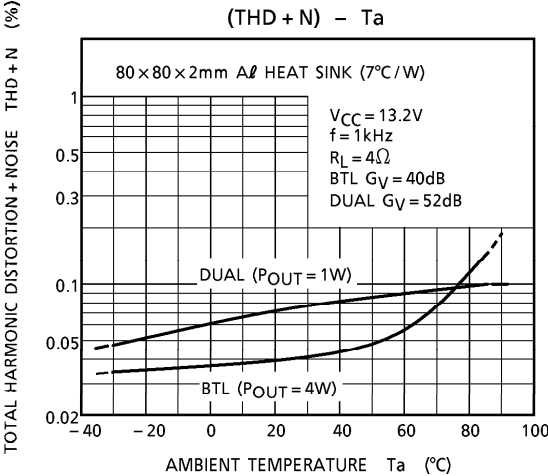
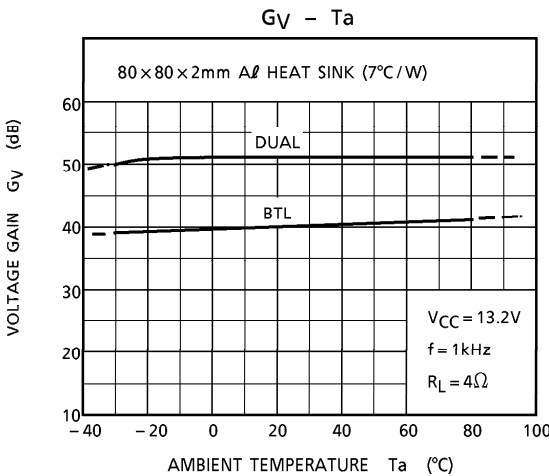
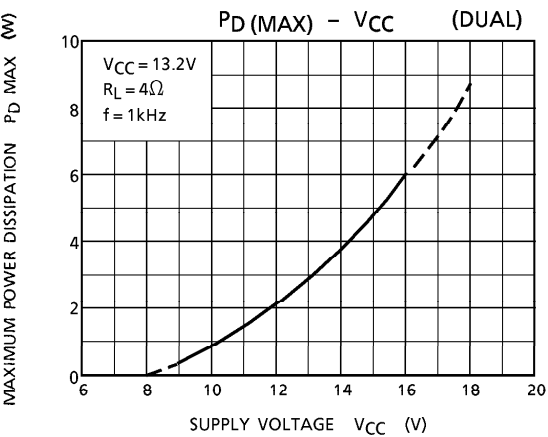
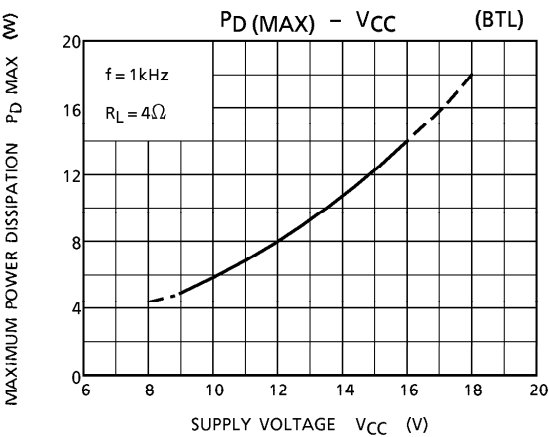
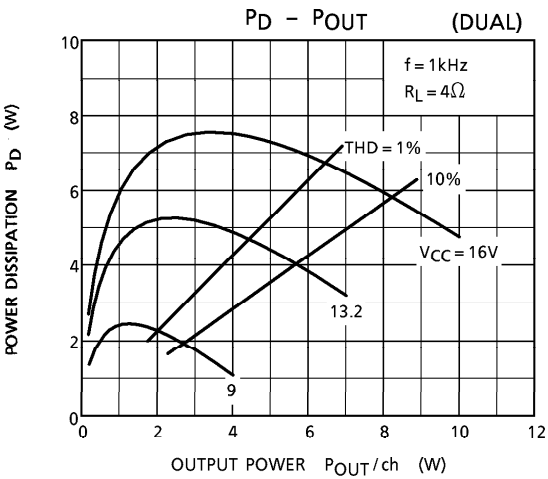
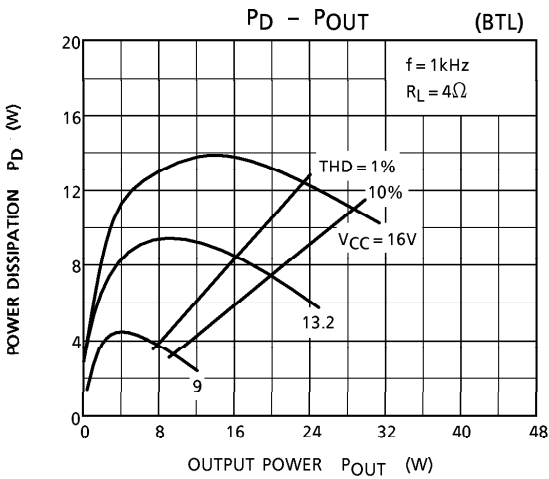


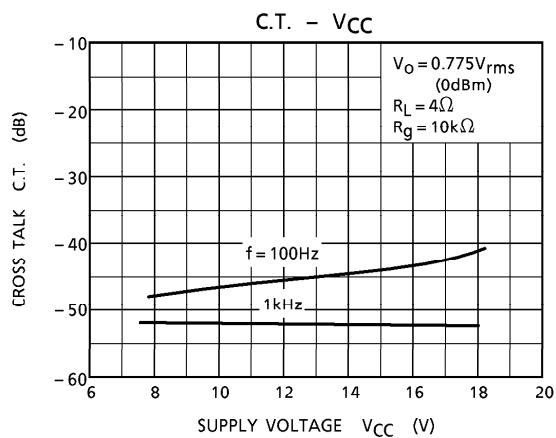
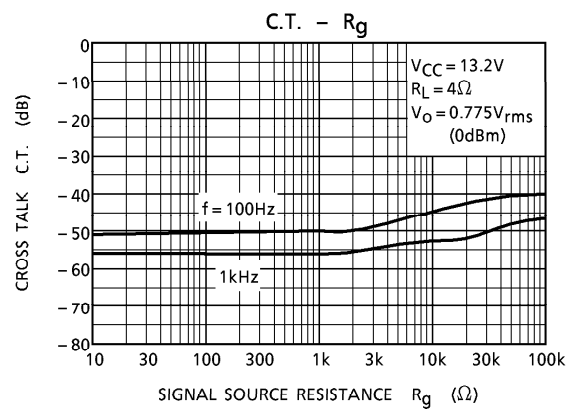
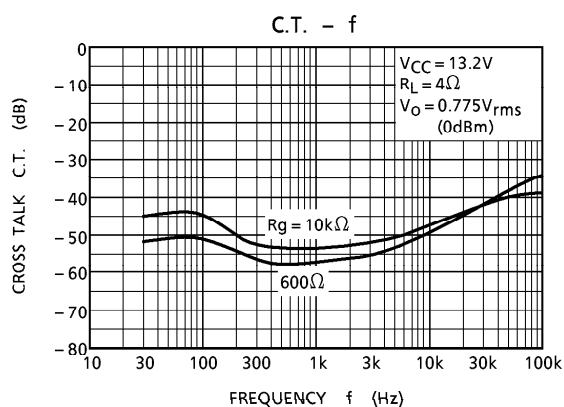
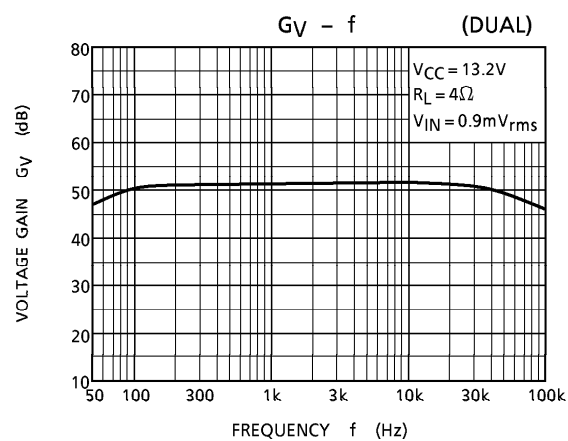
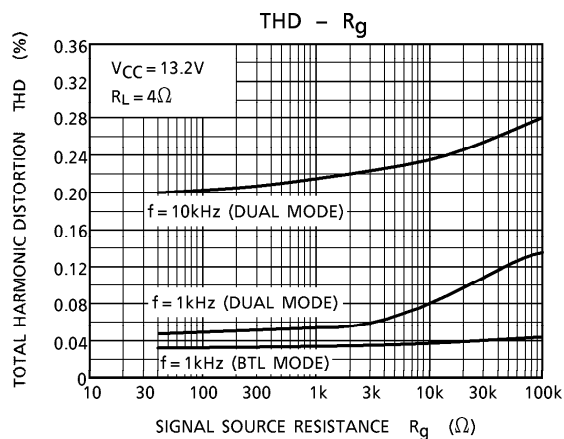
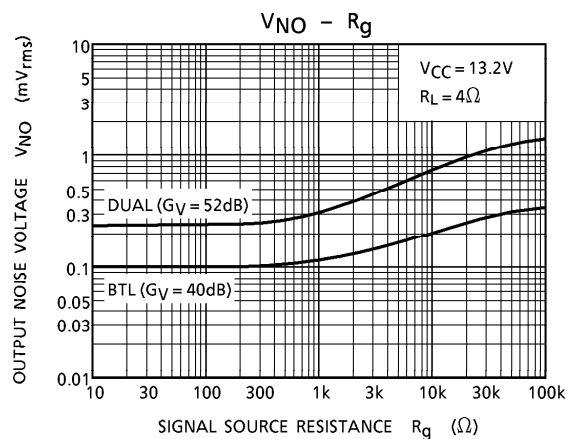
(2) DUAL

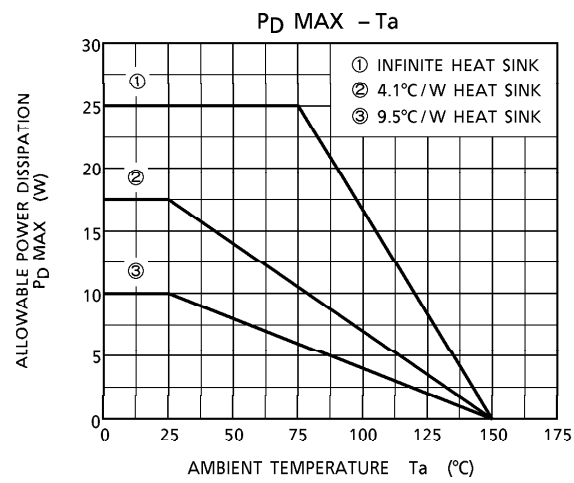
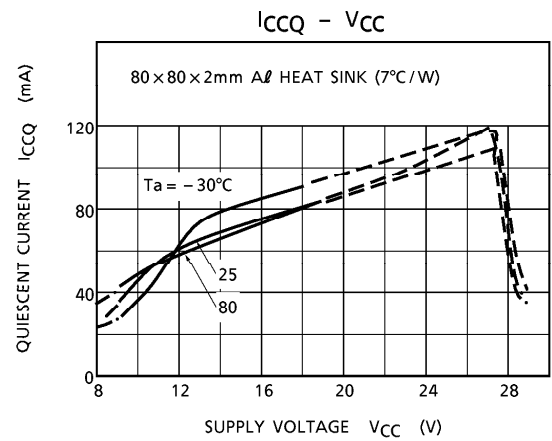
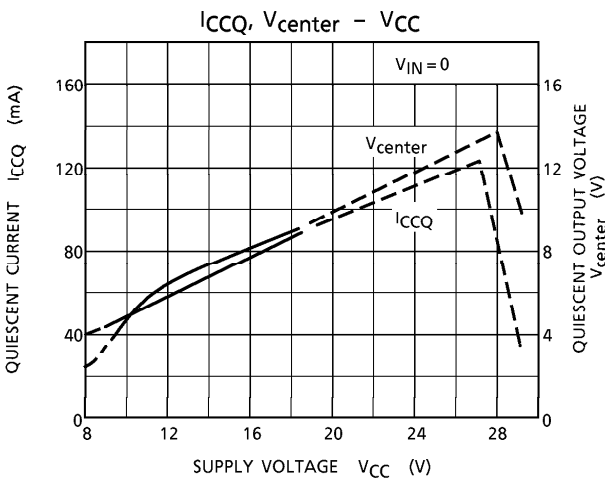












HZIP12-P-1.78B

Figure 1: Dimensions of the connector. The figure includes three views: a top view, a side view, and a bottom view. The top view shows a rectangular component with two circular mounting holes, a width of 15.72 ± 0.2 , a hole diameter of $\varnothing 3.6 \pm 0.2$, and a height of 14.8 ± 0.3 . It features 12 pins with a pitch of 1.778 and a total width of 22.9 MAX . The side view shows a height of 11.31 ± 0.3 and a pin height of 6.5 ± 0.3 . The bottom view shows a width of 22.4 ± 0.2 and a pin diameter of $\varnothing 0.25 (M)$.

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