

NLSX4014

4-Bit 100 Mb/s Configurable Dual-Supply Level Translator

The NLSX4014 is a 4-bit configurable dual-supply bidirectional level translator without a direction control pin. The I/O V_{CC} - and I/O V_L -ports are designed to track two different power supply rails, V_{CC} and V_L respectively. The V_{CC} supply rail is configurable from 1.3 V to 4.5 V while the V_L supply rail is configurable from 0.9 V to ($V_{CC} - 0.4$) V. This allows lower voltage logic signals on the V_L side to be translated into higher voltage logic signals on the V_{CC} side, and vice-versa. Both I/O ports are auto-sensing; thus, no direction pin is required.

The Output Enable (EN) input, when Low, disables both I/O ports by putting them in 3-state. This significantly reduces the supply currents from both V_{CC} and V_L . The EN signal is designed to track V_L .

Features

- Wide High-Side V_{CC} Operating Range: 1.3 V to 4.5 V
Wide Low-Side V_L Operating Range: 0.9 V to ($V_{CC} - 0.4$) V
- Power Supply Isolation
 - ♦ All Outputs are in the High Impedance State if Either V_L or V_{CC} is at Ground
- High-Speed with 100 Mb/s Guaranteed Data Rate for $V_L > 1.6$ V
- Low Bit-to-Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Powerup Sequencing
- Small packaging: 1.7 mm x 2.0 mm UQFN12
- These are Pb-Free Devices

Typical Applications

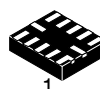
- Mobile Phones, PDAs, Other Portable Devices



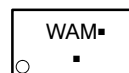
ON Semiconductor®

<http://onsemi.com>

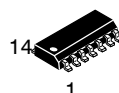
MARKING DIAGRAMS



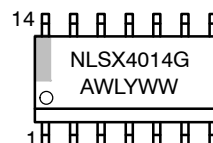
UQFN12
MU SUFFIX
CASE 523AE



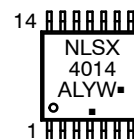
WA = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NLSX4014MUTAG	UQFN12 (Pb-Free)	3000/Tape & Reel
NLSX4014DR2G	SO-14 (Pb-Free)	2500/Tape & Reel
NLSX4014DTR2G	TSSOP14 (Pb-Free)	2500/Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NLSX4014

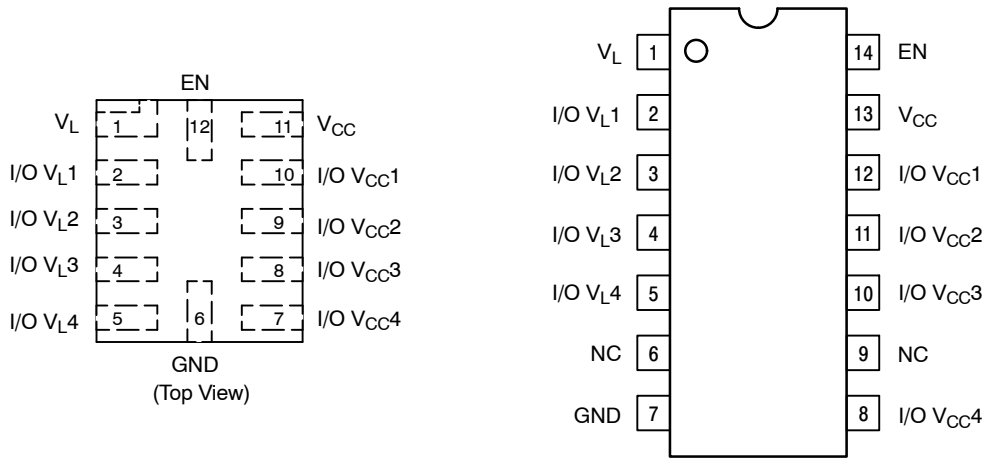


Figure 1. Pin Assignments

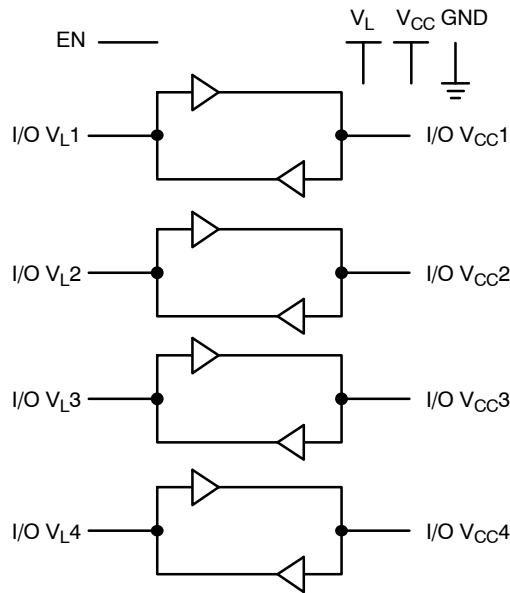


Figure 2. Logic Diagram

PIN ASSIGNMENT

Pins	Description
V _{CC}	V _{CC} Input Voltage
V _L	V _L Input Voltage
GND	Ground
EN	Output Enable
I/O V _{CCn}	I/O Port, Referenced to V _{CC}
I/O V _{Ln}	I/O Port, Referenced to V _L

FUNCTION TABLE

EN	Operating Mode
L	Hi-Z
H	I/O Buses Connected

NLSX4014

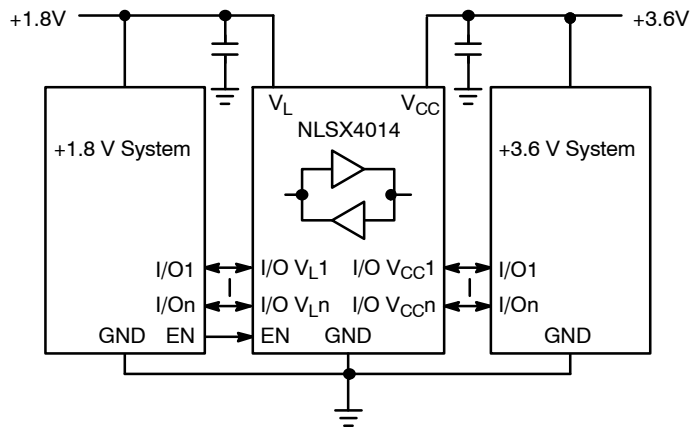


Figure 3. Typical Application Circuit

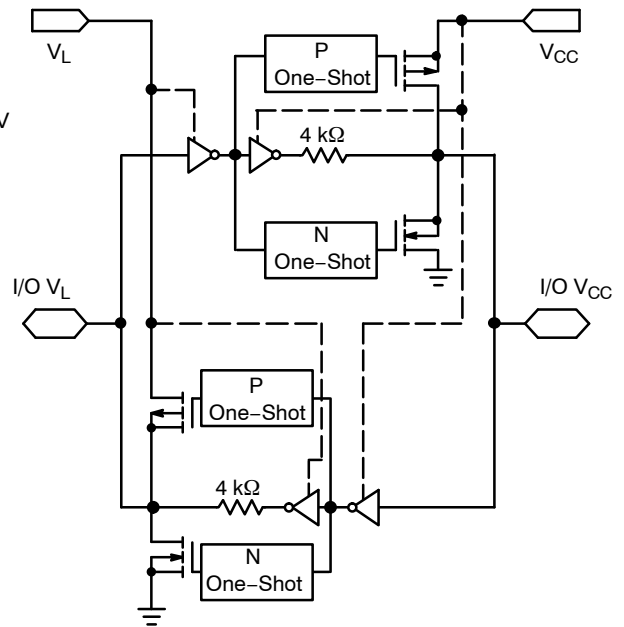


Figure 4. Simplified Functional Diagram (1 I/O Line)
(EN = 1)

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	V _{CC} Supply Voltage	–0.5 to +5.5		V
V _L	V _L Supply Voltage	–0.5 to +5.5		V
I/O V _{CC}	V _{CC} –Referenced DC Input/Output Voltage	–0.5 to (V _{CC} + 0.3)		V
I/O V _L	V _L –Referenced DC Input/Output Voltage	–0.5 to (V _L + 0.3)		V
V _{EN}	Enable Control Pin DC Input Voltage	–0.5 to +5.5		V
I _{IK}	Input Diode Clamp Current	–50	V _I < GND	mA
I _{OK}	Output Diode Clamp Current	–50	V _O < GND	mA
I _{CC}	DC Supply Current Through V _{CC}	± 100		mA
I _L	DC Supply Current Through V _L	± 100		mA
I _{GND}	DC Ground Current Through Ground Pin	± 100		mA
T _{STG}	Storage Temperature	–65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	V _{CC} Supply Voltage	1.3	4.5	V
V _L	V _L Supply Voltage	0.9	V _{CC} – 0.4	V
V _{EN}	Enable Control Pin Voltage	GND	4.5	V
V _{IO}	Bus Input/Output Voltage I/O V _{CC} I/O V _L	GND GND	4.5 4.5	V
T _A	Operating Temperature Range	–40	+85	°C
ΔI/ΔV	Input Transition Rise or Rate V _I , V _{IO} from 30% to 70% of V _{CC} ; V _{CC} = 3.3 V ± 0.3 V	0	10	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 1)	V _{CC} (V) (Note 2)	V _L (V) (Note 3)	-40°C to +85°C			Unit
					Min	Typ (Note 4)	Max	
V _{IHC}	I/O V _{CC} Input HIGH Voltage		1.3 to 4.5	0.9 to (V _{CC} - 0.4)	0.8 * V _{CC}	–	–	V
V _{ILC}	I/O V _{CC} Input LOW Voltage		1.3 to 4.5	0.9 to (V _{CC} - 0.4)	–	–	0.2 * V _{CC}	V
V _{IHL}	I/O V _L Input HIGH Voltage		1.3 to 4.5	0.9 to (V _{CC} - 0.4)	0.8 * V _L	–	–	V
V _{ILL}	I/O V _L Input LOW Voltage		1.3 to 4.5	0.9 to (V _{CC} - 0.4)	–	–	0.2 * V _L	V
V _{IH}	Control Pin Input HIGH Voltage	T _A = +25°C	1.3 to 4.5	0.9 to (V _{CC} - 0.4)	0.8 * V _L	–	–	V
V _{IL}	Control Pin Input LOW Voltage	T _A = +25°C	1.3 to 4.5	0.9 to (V _{CC} - 0.4)	–	–	0.2 * V _L	V
V _{OHC}	I/O V _{CC} Output HIGH Voltage	I/O V _{CC} Source Current = 20 µA	1.3 to 4.5	0.9 to (V _{CC} - 0.4)	0.8 * V _{CC}	–	–	V
V _{OLC}	I/O V _{CC} Output LOW Voltage	I/O V _{CC} Sink Current = 20 µA	1.3 to 4.5	0.9 to (V _{CC} - 0.4)	–	–	0.2 * V _{CC}	V
V _{OHL}	I/O V _L Output HIGH Voltage	I/O V _L Source Current = 20 µA	1.3 to 4.5	0.9 to (V _{CC} - 0.4)	0.8 * V _L	–	–	V
V _{OLL}	I/O V _L Output LOW Voltage	I/O V _L Sink Current = 20 µA	1.3 to 4.5	0.9 to (V _{CC} - 0.4)	–	–	0.2 * V _L	V

1. Normal test conditions are V_{EN} = 0 V, C_{I0VCC} = 15 pF and C_{I0VL} = 15 pF, unless otherwise specified.
2. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.
3. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} - 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} - 0.4) V.
4. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

POWER CONSUMPTION

Symbol	Parameter	Test Conditions (Note 5)	V _{CC} (V) (Note 6)	V _L (V) (Note 7)	-40°C to +85°C			Unit
					Min	Typ	Max	
I _{Q-VCC}	Supply Current from V _{CC}	EN = V _L ; I/O V _{CCn} = 0 V, I/O V _{Ln} = 0 V, I/O V _{CCn} = V _{CC} or I/O V _{Ln} = V _L and I _o = 0	1.3 to 3.6	0.9 to (V _{CC} - 0.4)	–	–	1.0	μA
			0	4.1	–	–	2.0	
			4.5	0	–	–	2.0	
I _{Q-VL}	Supply Current from V _L	EN = V _L ; I/O V _{CCn} = 0 V, I/O V _{Ln} = 0 V, I/O V _{CCn} = V _{CC} or I/O V _{Ln} = V _L and I _o = 0	1.3 to 3.6	0.9 to (V _{CC} - 0.4)	–	–	1.0	μA
				< (V _{CC} - 0.2)				
		EN = V _L ; I/O V _{CCn} = 0 V, I/O V _{Ln} = 0 V, I/O V _{CCn} = V _{CC} or I/O V _{Ln} = (V _{CC} - 0.2 V) and I _o = 0	0	4.1	–	–	2.0	
			4.5	0				
I _{TS-VCC}	V _{CC} Tristate Output Mode Supply Current	EN = 0 V	1.3 to 3.6	0.9 to (V _{CC} - 0.4)	–	–	1.0	μA
I _{TS-VL}	V _L Tristate Output Mode Supply Current	EN = 0 V	1.3 to 3.6	0.9 to (V _{CC} - 0.4)	–	–	0.2	μA
		EN = 0 V		V _{CC} - 0.2	–	–	2.0	
I _{OZ}	I/O Tristate Output Mode Leakage Current	EN = 0 V	1.3 to 3.6	0.9 to (V _{CC} - 0.4)	–	–	0.15	μA
		EN = 0 V		V _{CC} - 0.2	–	–	2.0	
I _{EN}	Output Enable Pin Input Current	–	1.3 to 3.6	0.9 to (V _{CC} - 0.4)	–	–	1.0	μA
I _{OFF}	V _L Port	I/O V _{Ln} = 0 to 4.1 V	0 to 4.5	0	–	–	2.0	μA
	V _{CC} Port	I/O V _{CCn} = 0 to 4.5 V	0	0 to 4.1	–	–	2.0	

5. Normal test conditions are V_{EN} = 0 V, C_{I_{OVCC}} = 15 pF and C_{I_{OV_L}} = 15 pF, unless otherwise specified.

6. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 3.6 V.

7. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} - 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} - 0.4) V.

TIMING CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 8)	V_{CC} (V) (Note 9)	V_L (V) (Note 10)	-40°C to +85°C			Unit
					Min	Typ (Note 11)	Max	
t_{R-VCC}	I/O V_{CC} Rise Time (Output = I/O_ V_{CC})	$C_{IOVCC} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		0.7	2.4	ns
t_{F-VCC}	I/O V_{CC} Falltime (Output = I/O_ V_{CC})	$C_{IOVCC} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		0.5	1.0	ns
t_{R-VL}	I/O V_L Risettime (Output = I/O_ V_L)	$C_{IOVL} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		1.0	3.8	ns
t_{F-VL}	I/O V_L Falltime (Output = I/O_ V_L)	$C_{IOVL} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		0.6	1.2	ns
Z_{O-VCC}	I/O V_{CC} One-Shot Output Impedance		1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		30		Ω
Z_{O-VL}	I/O V_L One-Shot Output Impedance		1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		30		Ω
t_{PD_VL-VCC}	Propagation Delay (Output = I/O_ V_{CC} , t_{PHL} , t_{PLH})	$C_{IOVCC} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		4.5	9.3	ns
t_{PD_VCC-VL}	Propagation Delay (Output = I/O_ V_L , t_{PHL} , t_{PLH})	$C_{IOVL} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		3.0	6.5	ns
t_{SK_VL-VCC}	Channel-to-Channel Skew (Output = I/O_ V_{CC})	$C_{IOVCC} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		0.2	0.3	nS
t_{SK_VCC-VL}	Channel-to-Channel Skew (Output = I/O_ V_L)	$C_{IOVCC} = 15 \text{ pF}$	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		0.2	0.3	nS
MDR	Maximum Data Rate	(Output = I/O_ V_{CC} , $C_{IOVCC} = 15 \text{ pF}$) (Output = I/O_ V_L , $C_{IOVL} = 15 \text{ pF}$)	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)	110			Mb/s
			> 2.2	> 1.8	140			

8. Normal test conditions are $V_{EN} = 0 \text{ V}$, $C_{IOVCC} = 15 \text{ pF}$ and $C_{IOVL} = 15 \text{ pF}$, unless otherwise specified.

9. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.

10. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to ($V_{CC} - 0.4$) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than ($V_{CC} - 0.4$) V.

11. Typical values are for $V_{CC} = +2.8 \text{ V}$, $V_L = +1.8 \text{ V}$ and $T_A = +25^\circ\text{C}$. All units are production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

ENABLE / DISABLE TIME MEASUREMENTS

Symbol	Parameter	Test Conditions (Note 12)	V_{CC} (V) (Note 13)	V_L (V) (Note 14)	-40°C to +85°C			Unit
					Min	Typ (Note 15)	Max	
t_{EN-VCC}	Turn-On Enable Time (Output = I/O V_{CC} , t_{pZH})	$C_{IOVCC} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		130	180	ns
	Turn-On Enable Time (Output = I/O V_{CC} , t_{pZL})	$C_{IOVL} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		100	150	ns
t_{EN-VL}	Turn-On Enable Time (Output = I/O V_L , t_{pZH})	$C_{IOVCC} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		95	185	ns
	Turn-On Enable Time (Output = I/O V_L , t_{pZL})	$C_{IOVL} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		70	110	ns
$t_{DIS-VCC}$	Turn-Off Disable Time (Output = I/O V_{CC} , t_{pHZ})	$C_{IOVCC} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		175	250	ns
	Propagation Delay (Output = I/O V_{CC} , t_{PLZ})	$C_{IOVL} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		150	190	ns
t_{DIS-VL}	Turn-Off Disable Time (Output = I/O V_L , t_{pHZ})	$C_{IOVCC} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		180	250	ns
	Propagation Delay (Output = I/O V_L , t_{PLZ})	$C_{IOVL} = 15$ pF	1.3 to 4.5	0.9 to ($V_{CC} - 0.4$)		160	220	ns

12. Normal test conditions are $V_{EN} = 0$ V, $C_{IOVCC} = 15$ pF and $C_{IOVL} = 15$ pF, unless otherwise specified.

13. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.

14. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to ($V_{CC} - 0.4$) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than ($V_{CC} - 0.4$) V.

15. Typical values are for $V_{CC} = +2.8$ V, $V_L = +1.8$ V and $T_A = +25$ °C. All units are production tested at $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design.

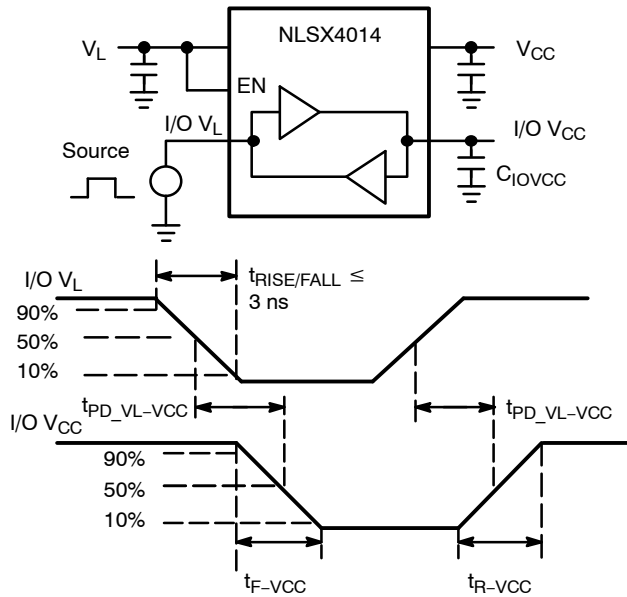


Figure 5. Driving I/O V_L Test Circuit and Timing

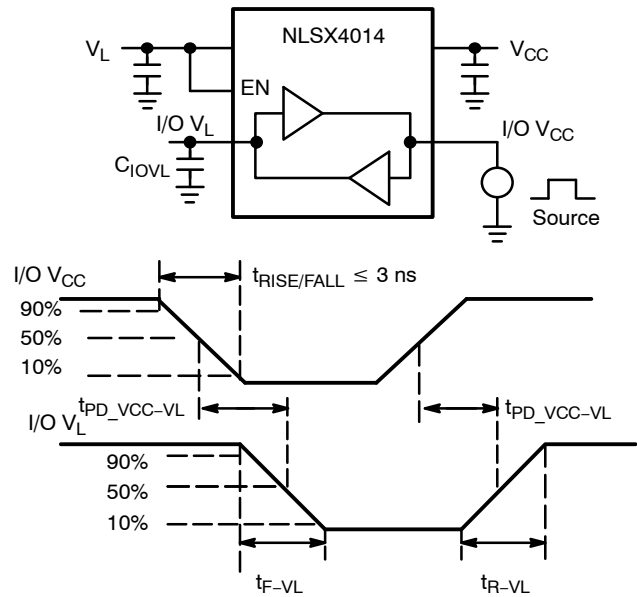
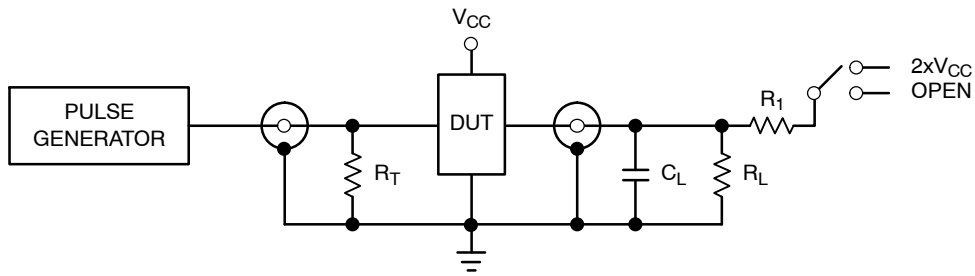


Figure 6. Driving I/O V_{CC} Test Circuit and Timing

NLSX4014



Test	Switch
t_{PZH} , t_{PHZ}	Open
t_{PZL} , t_{PLZ}	$2 \times V_{CC}$

$C_L = 15 \text{ pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 50 \text{ k}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit for Enable/Disable Time Measurement

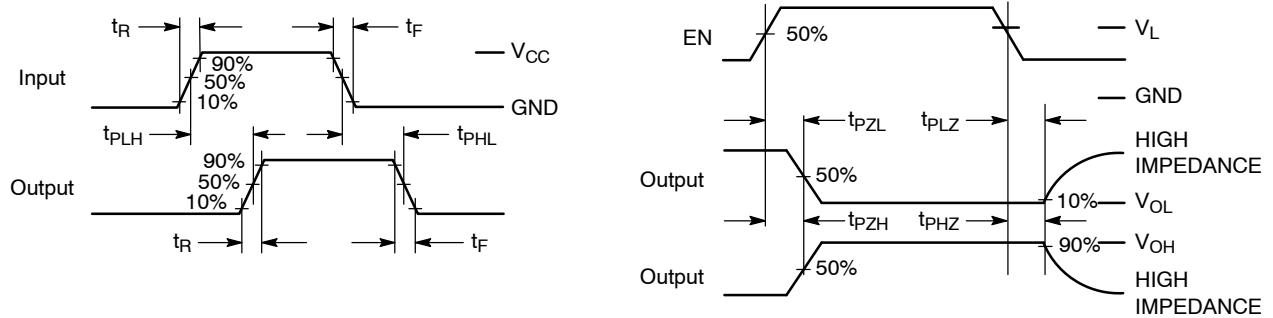


Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement

IMPORTANT APPLICATIONS INFORMATION**Level Translator Architecture**

The NLSX4014 auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC} , which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC} . In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L .

The NLSX4014 consists of four bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions.

Input Driver Requirements

For proper operation, the input driver to the auto sense translator should be capable of driving 2.0 mA of peak output current.

Output Load Requirements

The NLSX4014 is designed to drive CMOS inputs. Resistive pullup or pulldown loads of less than 50 k Ω should not be used with this device. The NLSX3373 or NLSX3378 open-drain auto sense translators are alternate translator options for an application such as the I²C bus that requires pullup resistors.

Enable Input (EN)

The NLSX4014 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Over-Voltage Tolerant (OVT) protection.

Uni-Directional versus Bi-Directional Translation

The NLSX4014 can function as a non-inverting uni-directional translator. One advantage of using the translator as a uni-directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

It is recommended that the V_L supply should be less than or equal to the value of the V_{CC} minus 0.4 V. The sequencing of the power supplies will not damage the device during the power up operation; however, the current consumption of the device will increase if V_L exceeds V_{CC} minus 0.4 V. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0 V.

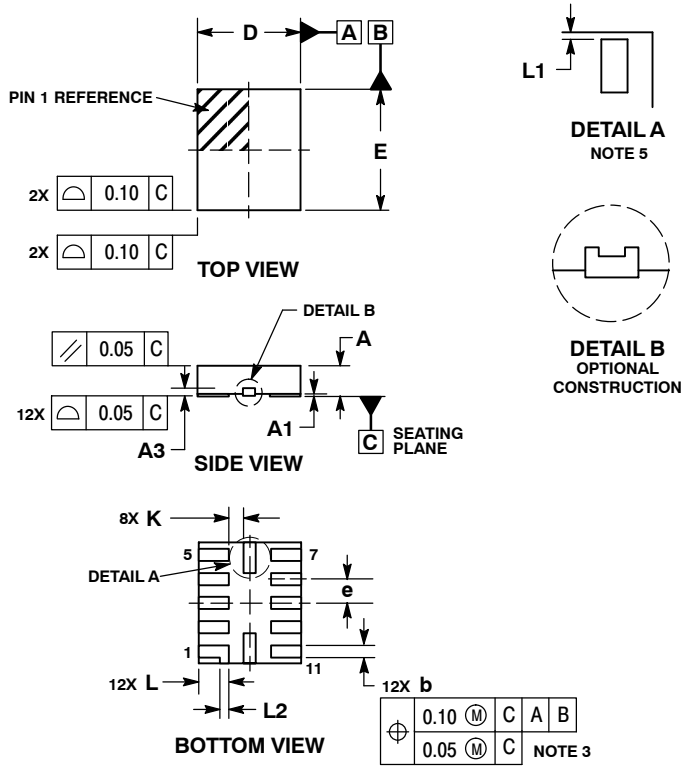
For optimal performance, 0.01 to 0.1 μ F decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the power supply voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

The NLSX4014 provides power supply isolation if either supply voltage V_L or V_{CC} is equal to 0 V. The isolation occurs because the I/O pins are in the high impedance state. It is recommended that pulldown resistors should be used if the V_L or V_{CC} are floated or in a high impedance state. A pulldown resistor connected from the supply voltage to ground ensures that the translator's supply voltage is equal to 0 V.

NLSX4014

PACKAGE DIMENSIONS

UQFN12 1.7x2.0, 0.4P
CASE 523AE-01
ISSUE A

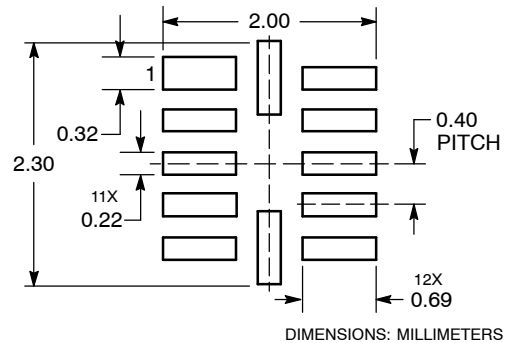


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

MOUNTING FOOTPRINT SOLDERMASK DEFINED

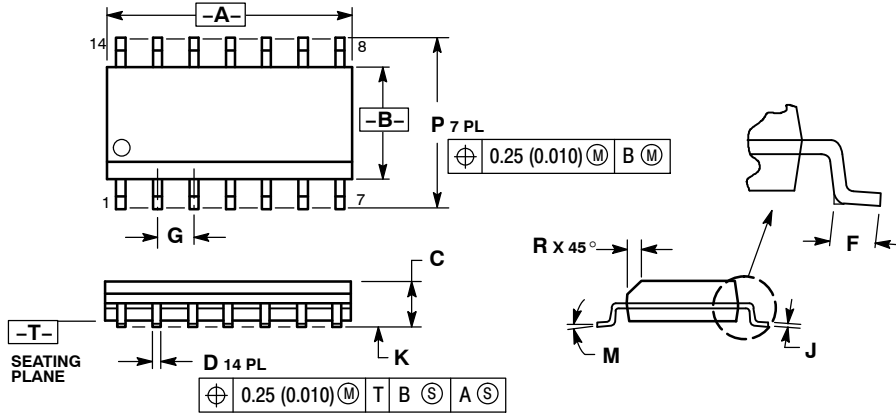


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLSX4014

PACKAGE DIMENSIONS

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE J

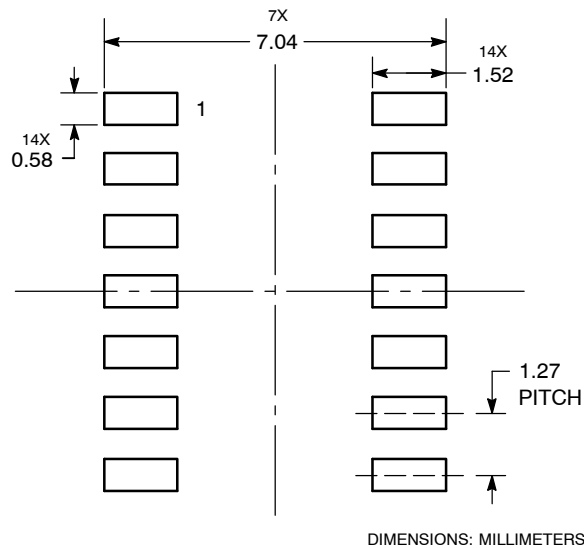


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

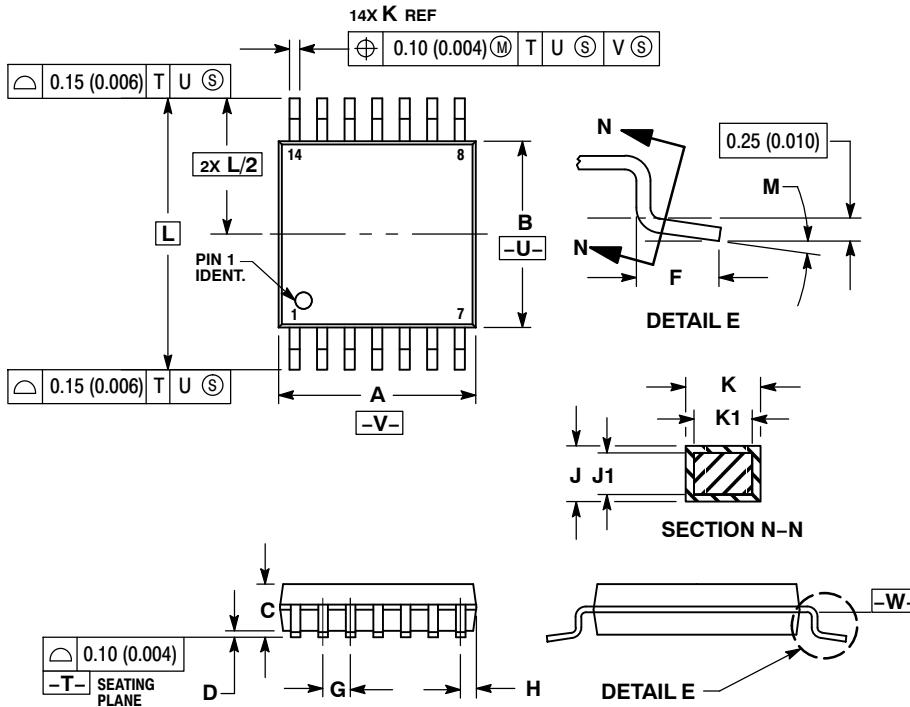
SOLDERING FOOTPRINT



NLSX4014

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE B

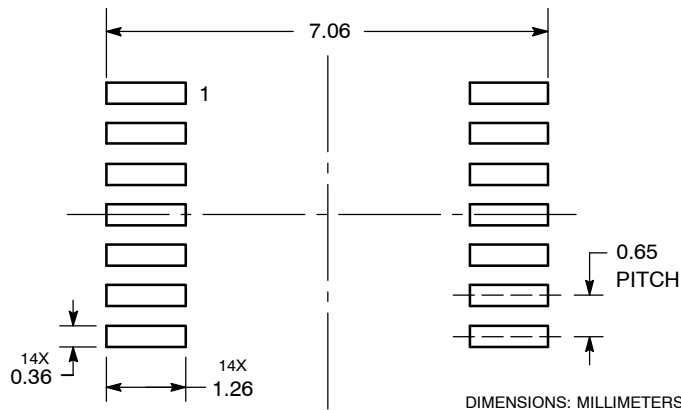


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



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