

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = +25^\circ\text{C}$
-30V	40m Ω @ $V_{GS} = -4.5\text{V}$	-6.5A
	70m Ω @ $V_{GS} = -2.5\text{V}$	-5.0A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

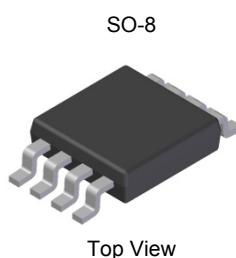
- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

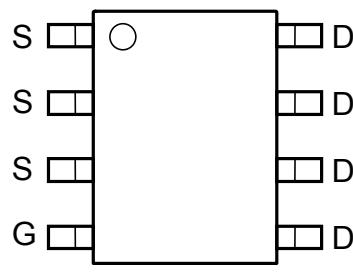
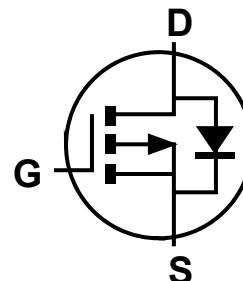
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074g (approximate)



Top View


 Top View
Internal Schematic


Equivalent circuit

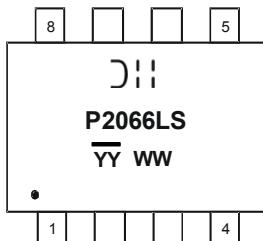
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2066LSS-13	SO-8	2500/Tape & Reel

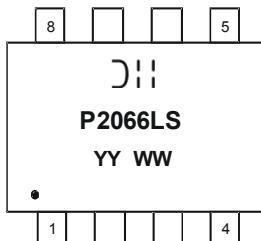
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

DII = Manufacturer's Marking

P2066LS = Product Type Marking Code

YYWW = Date Code Marking

YY or YY = Year (ex: 13 = 2013)

WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	± 12	V
Drain Current (Note 5)	Steady State	I_D	-6.5 -5.2	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)		I_{DM}	-26	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.5	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

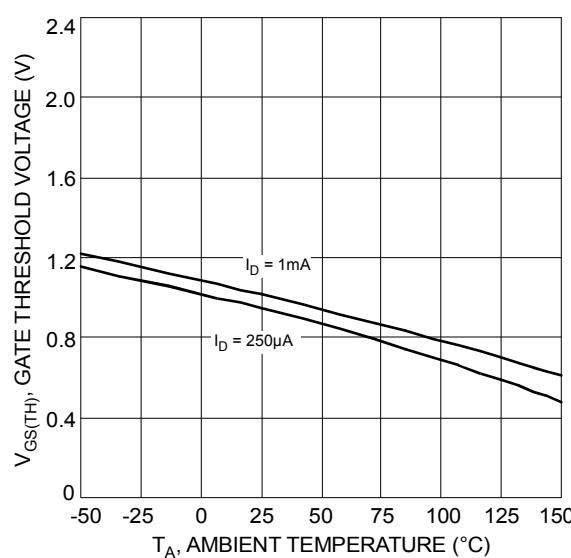
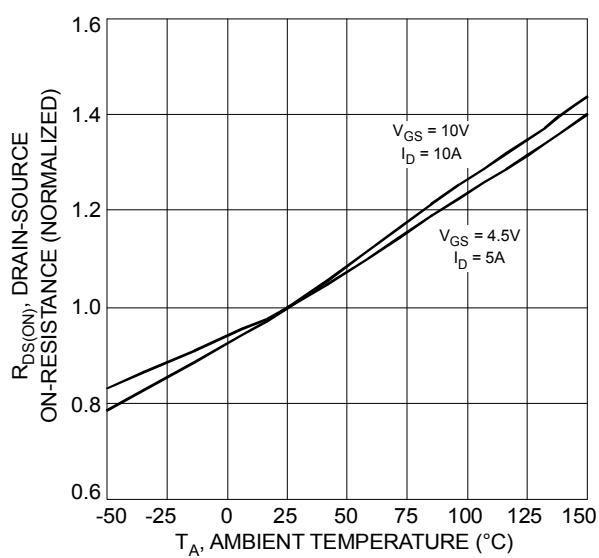
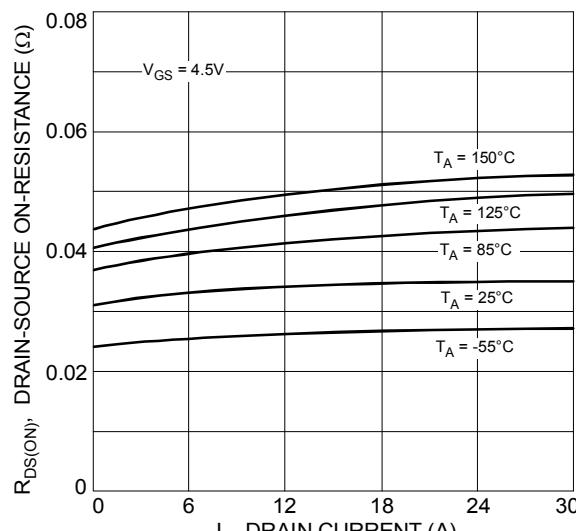
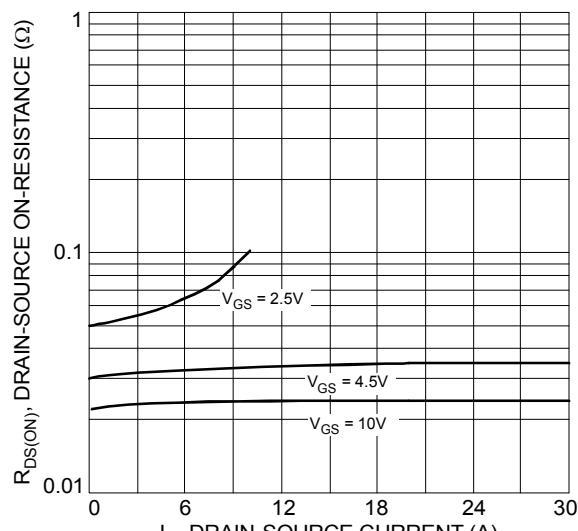
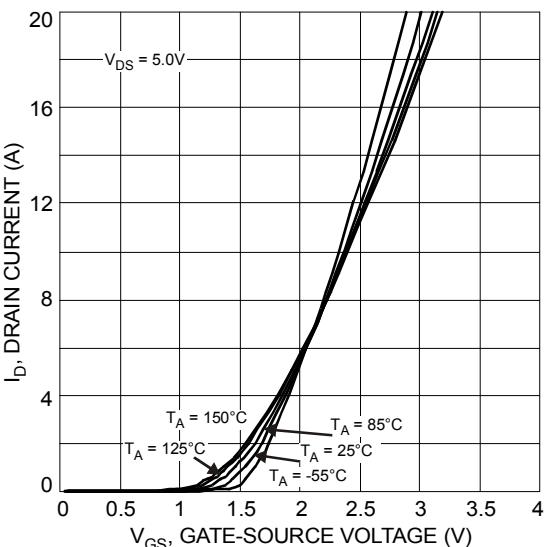
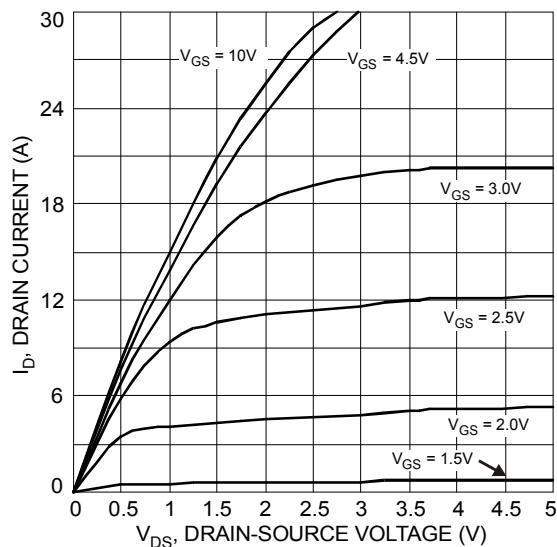
Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(\text{th})}$	-0.6	—	-1.2	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	—	40	$\text{m}\Omega$	$V_{GS} = -4.5\text{V}, I_D = -5.8\text{A}$
		—	—	70		$V_{GS} = -2.5\text{V}, I_D = -3.8\text{A}$
Forward Transconductance	g_{fs}	—	9	—	S	$V_{DS} = -10\text{V}, I_D = -4.6\text{A}$
Diode Forward Voltage	V_{SD}	-0.5	-0.72	-1.4	V	$V_{GS} = 0\text{V}, I_S = -2.1\text{A}$
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	820	—	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	200	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	160	—	pF	
Gate Resistance	R_g	—	10.4	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$
Total Gate Charge	Q_g	—	14.4	—	nC	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V}$ $I_D = -4.5\text{A}$
Gate-Source Charge	Q_{gs}	—	2.6	—		
Gate-Drain Charge	Q_{gd}	—	2.7	—		
Turn-On Delay Time	$t_{D(\text{on})}$	—	13.7	—	ns	$V_{DD} = -10\text{V}, V_{GS} = -4.5\text{V},$ $R_G = 6\Omega, R_L = 10\Omega, I_D = -1\text{A}$
Turn-On Rise Time	t_r	—	14.0	—		
Turn-Off Delay Time	$t_{D(\text{off})}$	—	79.1	—		
Turn-Off Fall Time	t_f	—	35.5	—		

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

6. Short duration pulse test used to minimize self-heating effect.

7. Guaranteed by design. Not subject to product testing.



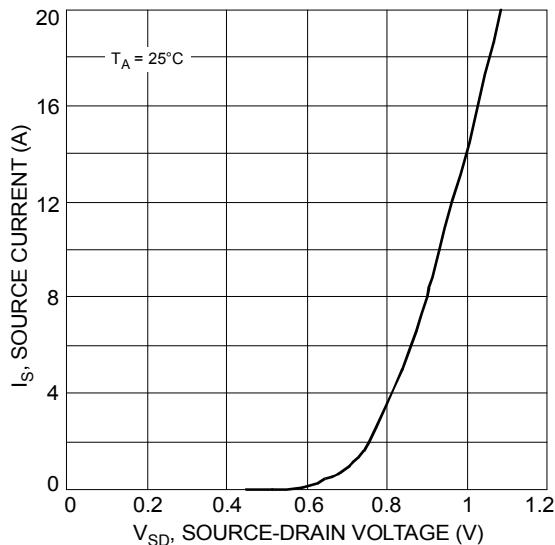


Fig. 7 Diode Forward Voltage vs. Current

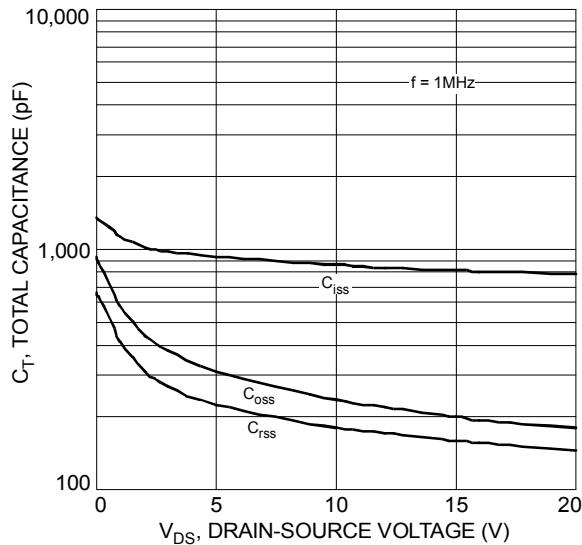


Fig. 8 Typical Total Capacitance

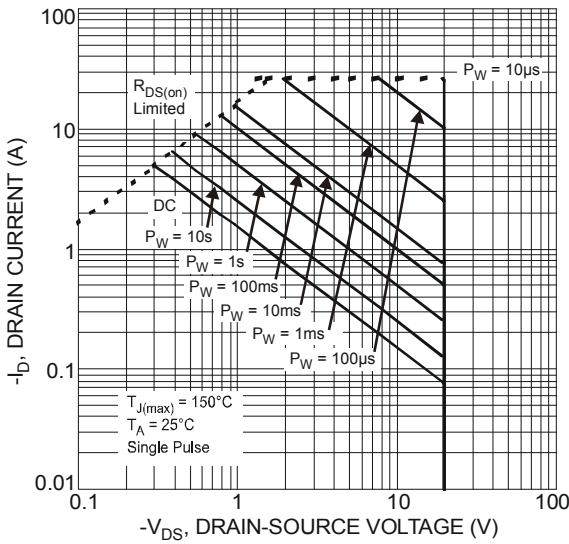
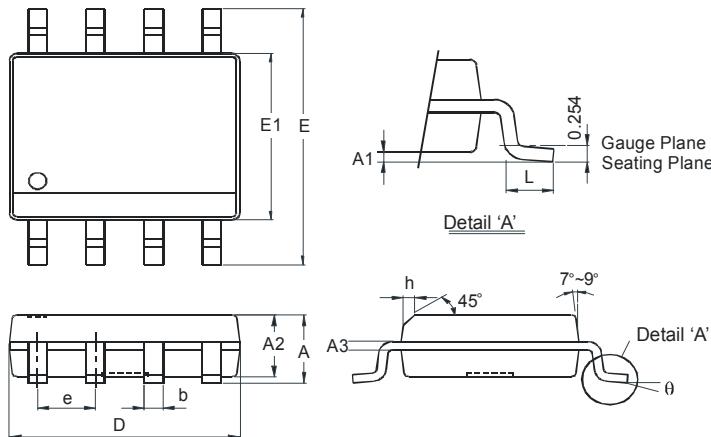


Fig. 9 SOA, Safe Operation Area

Package Outline Dimensions

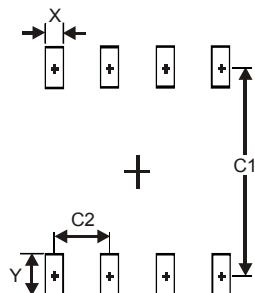
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A_1	0.10	0.20
A_2	1.30	1.50
A_3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E_1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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