Micro Power Systems

MP7581

CMOS
Microprocessor Compatible 8-Bit
8-Channel Data Acquisition System

FEATURES

- 8 Input Channel DAS
- 8-Bit Resolution
- On-Chip 8 x 8 Dual-Port Memory
- Interfaces Directly to 8-Bit µP
- CMOS, TTL Compatible Digital Inputs
- Three-State Outputs
- Ratiometric Capability
- Single +5 V Supply
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to µP
- PDIP & CDIP Packages Available

GENERAL DESCRIPTION

The MP7581 is a microprocessor compatible 8-bit, 8-channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8-bit successive approximation A/D converter, an 8 channel multiplexer, 8 x 8 dual-port RAM, three-state digital outputs (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 x 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs (A0 - A2) with ALE enables the MP7581 to interface with µP systems which feature either shared or separate address and data buses.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7581 is available in Plastic and Ceramic dual-in-line packages.

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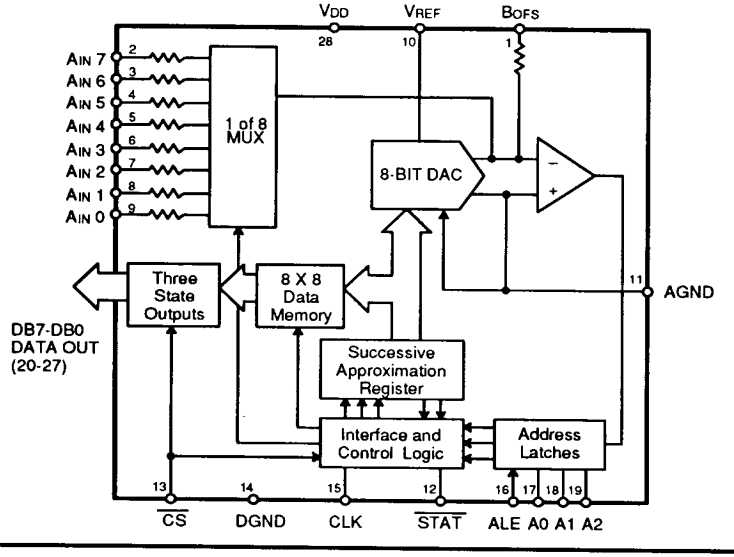
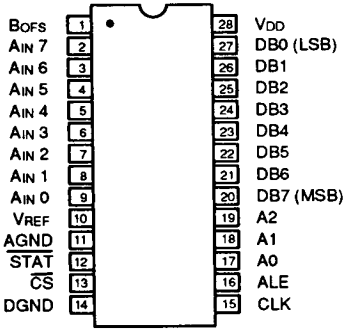
SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (± LSB's)	INL (± LSB's)
Plastic Dip	–40 to +85°C	MP7581JN	1 7/8	1 7/8
Plastic Dip	–40 to +85°C	MP7581KN	7/8	3/4
Plastic Dip	–40 to +85°C	MP7581LN	3/4	1/2
Ceramic Dip	–40 to +85°C	MP7581AD	1 7/8	1 7/8
Ceramic Dip	–40 to +85°C	MP7581BD	7/8	3/4
Ceramic Dip	–40 to +85°C	MP7581CD	3/4	1/2
Ceramic Dip	–55 to +125°C	MP7581SD	1 7/8	1 7/8
Ceramic Dip	–55 to +125°C	MP7581SD/883	1 7/8	1 7/8
Ceramic Dip	–55 to +125°C	MP7581TD	7/8	3/4
Ceramic Dip	–55 to +125°C	MP7581TD/883	7/8	3/4
Ceramic Dip	–55 to +125°C	MP7581UD	3/4	1/2
Ceramic Dip	–55 to +125°C	MP7581UD/883	3/4	1/2

PIN CONFIGURATIONS



28 Pin PDIP & CDIP (0.600")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	BOFS	Bipolar Offset Adjust
2	AIN 7	Analog Input Channel 7
3	AIN 6	Analog Input Channel 6
4	AIN 5	Analog Input Channel 5
5	AIN 4	Analog Input Channel 4
6	AIN 3	Analog Input Channel 3
7	AIN 2	Analog Input Channel 2
8	AIN 1	Analog Input Channel 1
9	AIN 0	Analog Input Channel 0
10	VREF	Negative Voltage Reference Input
11	AGND	Analog Ground
12	$\overline{\text{STAT}}$	Conversion Complete Status Output
13	$\overline{\text{CS}}$	Chip Select Input
14	DGND	Digital Ground

PIN NO.	NAME	DESCRIPTION
15	CLK	Clock Input
16	ALE	Address Latch Enable Input
17	A0	Latch 0 Address Input
18	A1	Latch 1 Address Input
19	A2	Latch 2 Address Input
20	DB7	Data Output Bit 7 (MSB)
21	DB6	Data Output Bit 6
22	DB5	Data Output Bit 5
23	DB4	Data Output Bit 4
24	DB3	Data Output Bit 3
25	DB2	Data Output Bit 2
26	DB1	Data Output Bit 1
27	DB0	Data Output Bit 0 (LSB)
28	VDD	Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = +5 V, V_{REF} = −10 V, Unipolar Operation

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
ACCURACY (JN, AD, SD)								
Differential Non-Linearity	DNL		±1 7/8			±1 7/8	LSB	
Integral Non-Linearity	INL		±1 7/8			±1 7/8	LSB	Best Fit Line
Offset Error			200			200	mV	Adj. to Zero
Gain Error (Worst Channel)			±3			±6	LSB	
Gain Match Between Channels			2			3	LSB	
BOFS Gain Error			−2 1/2				LSB	
ACCURACY (KN, BD, TD)								
Differential Non-Linearity	DNL		±7/8			±7/8	LSB	
Integral Non-Linearity	INL		±3/4			±3/4	LSB	Best Fit Line
Offset Error			80			80	mV	Adj. to Zero
Gain Error (Worst Channel)			±2			±4	LSB	
Gain Match Between Channels			1 1/2			2	LSB	
BOFS Gain Error			−2 1/2				LSB	
ACCURACY (LN, CD, UD)								
Differential Non-Linearity	DNL		±3/4			±3/4	LSB	
Integral Non-Linearity	INL		±1/2			±1/2	LSB	Best Fit Line
Offset Error			50			50	mV	Adj. to Zero
Gain Error (Worst Channel)			±1			±2	LSB	
Gain Match Between Channels			1			1	LSB	
BOFS Gain Error			−2 1/2				LSB	
ANALOG INPUT								
Input Resistance								
At V_{REF} (pin 10)		10	20	30	10	30	kΩ	
At B_{OFS} (pin 1)		10	20	30	10	30	kΩ	
At Any Analog Input (pins 2-9)		10	20	30	10	30	kΩ	
V_{REF} (For Specified Performance			−10				V	±5%
V_{REF} Range (2)		−5		−15	−5	−15	V	
Nominal Analog Input Range (2)								
Unipolar Mode		$-V_{REF}$		$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V	
Bipolar Mode (2)		$-V_{BOFS}$		ρ	$-V_{BOFS}$		V	ρ=|V_{REF}|−V_{BOFS}
DIGITAL INPUTS $\overline{CS}$ (pin 13), ALE (pin 16), A0-A2 (pins 17-19)								
CLK (pin 15)								
V_{INH} Logic HIGH Input Voltage			+2.2		2.4		V	
V_{INL} Logic LOW Input Voltage			+0.4			0.8	V	
I_{IN} Input Current			0.01			1	µA	V_{IN}=0V, V_{DD}
C_{IN} Input Capacitance (2)			4			5	pF	
DIGITAL OUTPUTS $\overline{STAT}$ (pin 12), DB7 to DB0 (pins 20-27)								C_{OUT}=15 pF
V_{OH} Output HIGH Voltage			+4.8		4.5		V	I_{SOURCE}=40µA
V_{OL} Output LOW Voltage			+0.4			0.6	V	I_{SINK}=1.6mA

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ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS CONT'D								
I_{LKG} DB7 to DB0 Floating State Lkg.			0.3			10	µA	
Floating State Output Capacitance (2) (DB7-DB0)			5			10	pF	V_{OUT}=0 to V_{DD}
Output Code								
Unipolar Binary *Figure 8.*								
Complementary Binary								*Figure 10.*
Offset Binary *Figure 10.*								
POWER REQUIREMENTS								
V_{DD}			5			5 (typ)	V	
I_{DD} – Static			3			5	mA	
I_{DD} – Dynamic			3			8	mA	f_{CLK}=1 MHz
AC SPECIFICATIONS (1)								
ALE Pulse Width	t_H		50		80		ns	See "Switching Terminology"
Address Valid to Latch Set-up Time	t_{ALS}		45		70		ns	
Address Valid to Latch Hold Time	t_{ALH}		10		20		ns	
Address Latch to $\overline{CS}$ Set-up Time	t_{LCS}		10		20		ns	
$\overline{CS}$ to Output Prop. Delay	t_{ACC}		200			400	ns	C_L=100pF
$\overline{CS}$ Pulse Width	t_{CW}		250		280		ns	
$\overline{CS}$ to Output Float Prop. Delay	t_{CF}		50			80	ns	
$\overline{CE}$ to Low Impedance Bus	t_{CLZ}		100			150	ns	
Clock Frequency for Stated Accur.	f_{CLK}		1600			1200	kHz	

NOTES
(1) Guaranteed. Not tested.
(2) Typical value only, not guaranteed or production tested.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... +7 V
V_{DD} to DGND ..... +7 V
AGND to DGND ..... GND –0.5 to V_{DD} +0.5 V
Digital Input Voltage to DGND
(pins 13, 16–19) ..... DGND –0.5 to +15 V
Digital Output Voltage to DGND
(pins 12, 20–27) ..... GND –0.5 to V_{DD} +0.5 V
CLK (pin 15) input voltage to DGND . DGND –0.5 to +15 V
V_{REF} (pin 10) to AGND ..... +25 V
V_{BOFS} (pin 1) to AGND ..... +17 V
A_{IN} (0–7) (pin 9–2) ..... +17 V
Storage Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Package Power Dissipation Rating to 50°C
PDIP, ... 1200mW
Derates above 70°C ..... 12mW/°C
CDIP 1000mW
Derates above 50°C ..... 10mW/°C

NOTES:
(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

GENERAL CIRCUIT INFORMATION

Basic Circuit Description

The MP7581 accepts eight analog inputs and sequentially converts each input into an eight-bit binary word using the successive approximation technique. The conversion results are stored in an 8 x 8 but dual-port RAM. The device runs either directly from the microprocessor clock (in 6800 type systems) or from some suitable signal (e.g. ALE in 8085 type systems). Most applications require only a −10 V reference and a +5 V supply. Start-up logic is included on the device to establish the correct sequences on power-up. A maximum of 800 clock pulses are required for this period. The block diagram on page 1 shows the MP7581 functional diagram.

Conversion of a single channel requires 80 input clock periods and a complete scan through all channels requires 640 input clock periods. When a channel conversion is complete, the successive approximation register contents are loaded into the proper channel location of the 8 x 8 RAM. At this time a status signal output, $\overline{STAT}$ (pin 12), gives a short negative going pulse (8 clock periods). This negative going $\overline{STAT}$ pulse is extended to 72 clock periods when channel 1 conversion is complete. An external pulse width detector connected to the status pin can be used to derive conversion-related timing signals for microprocessor interrupts (see Channel Identification *Figure 4.*). Simultaneous with $\overline{STAT}$ going low, the MUX address is decremented. Eight clock periods later the next conversion is started.

Automatic interleaved DMA is provided by on-chip logic to ensure that memory updates take place when the microprocessor is not addressing memory. Memory locations are addressed by A0, A1 and A2. This address may be latched by ALE for systems which feature a multiplexed address/data bus or alternatively, for systems which have separate address and data buses, the address latches can be made transparent by tying ALE (pin 16) HIGH. $\overline{CS}$ (pin 13) activates three-state buffers to place addressed data on the DB0 – DB7 data output pins.

Utilizing a clock frequency of 1200 kHz (max) guarantees conversion time of 66.6 µs per channel, with all 8 channels updated every 532.8 µs.

A/D Circuit Details

In the successive approximation technique, successive bits, starting with the most significant bit (DB7), are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage, A_{IN} (n), using a comparator. If the DAC output is greater than A_{IN} (n), the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than A_{IN} (n), the trial data bit stays in the "1" state, and the next smaller data bit is tried. Each successive bit is tried, compared to A_{IN} (n), and set or reset in this manner until the least significant bit (DB0) decision is made. The successive approximation register now contains a valid digital representation of A_{IN} (n). A_{IN} (n) is assumed to be stable during conversion.

The current weighting D/A converter is a precision multiplying DAC. *Figure 1.* shows the functional diagram of the DAC as used in the MP7581. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted i.e., the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the D/A logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to AGND or to the comparator summing point.

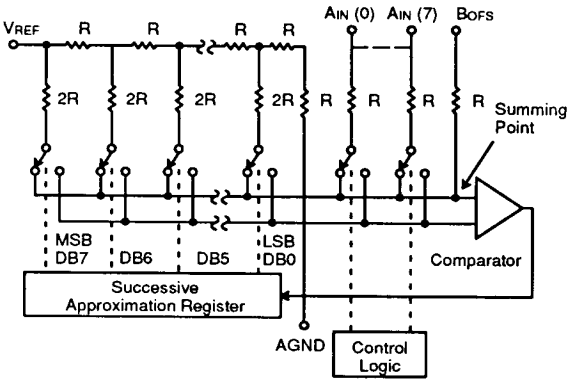


Figure 1. D/A Converter as used in the MP7581

TIMING AND CONTROL OF THE MP7581

Channel Selection

Table 1. shows the truth table for the address inputs. The input address is latched when ALE goes LOW. When ALE is HIGH the address input latch is transparent.

A2	A1	A0	ALE	Channel Data To Be Read
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Table 1. Channel Selection Truth Table

Timing and Control

A typical timing diagram is shown in *Figure 2.* When $\overline{CS}$ is HIGH, the three-state data drivers are in the high-impedance state. When $\overline{CS}$ goes LOW the data drivers switch to the low impedance state (i.e., low impedance to DGND or to V_{DD}). Output data is valid after time t_{ACC}.

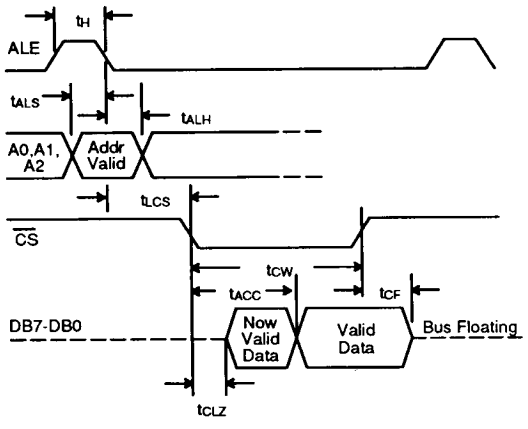


Figure 2. Timing Diagram for the MP7581

Switching Terminology

t_H: ALE pulse width requirement
t_{ALH}: Address Valid to latch hold time
t_{ALS}: Address Valid to latch set–up time
t_{LCS}: Address latch to Chip Select set–up time
t_{CW}: Chip Select pulse width requirement
t_{ACC}: Chip Select to valid data propagation delay
t_{CF}: Chip Select to output data float propagation delay
t_{CLZ}: Chip Select to low impedance data bus

Channel Identification

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The $\overline{STAT}$ output provides an identifying signal by staying low for an additional 64 clock periods over normal (8 clock periods) when channel 0 is active. This is illustrated in *Figure 3.* Memory update takes place on a rising edge of clock pulse. This occurs 6 clock periods before $\overline{STAT}$ goes low.

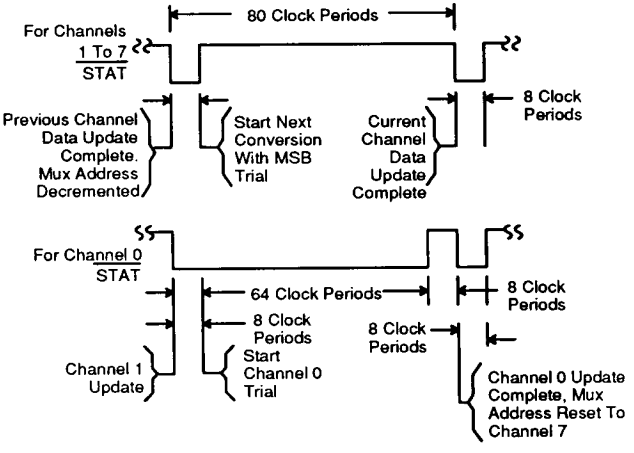


Figure 3. $\overline{STAT}$ Output for Channel Identification

One simple circuit using the $\overline{STAT}$ output is shown in *Figure 4.* The time constant RC is chosen such that X2 ignores the normal $\overline{STAT}$ low pulse width (8 clock periods wide) but responds to the much wider $\overline{STAT}$ low pulse width (72 clock periods wide) occurring during channel 0 conversion. Typically for a 1µs clock period C = 0.022µF, R = 1.8kΩ.

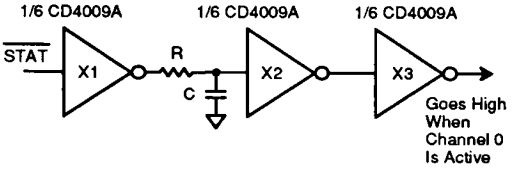


Figure 4. Hardware Channel Identification

Another possibility is to use the microprocessor to interrogate the $\overline{STAT}$ output and hence determine channel identity. A simple routine is shown in *Figure 5.*

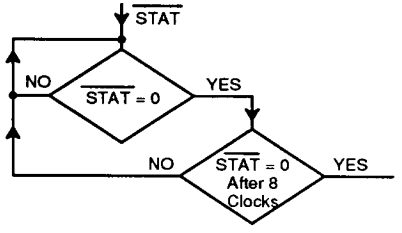


Figure 5. Software Channel Identification

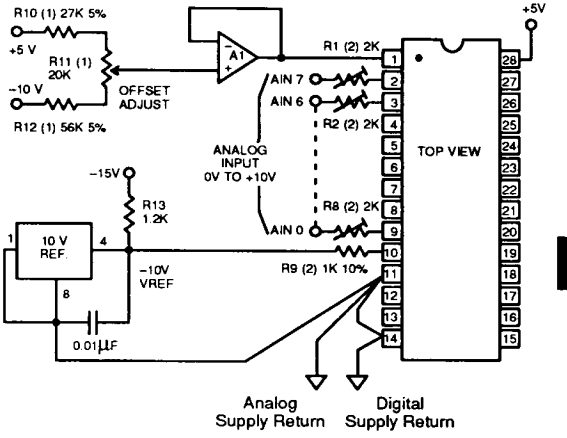
OPERATING THE MP7581

Unipolar Binary Operation

Figure 6.and Figure 7. show the analog circuit connections and typical transfer characteristics for unipolar operation (0 V to +10 V). A 5010 and an op amp are used for the −10 V reference. Calibration is as follows (device clocked i.e., continuous conversions):

OFFSET: Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A0, A1 and A2 LOW and exercise ALE to latch the address.
2. With A_{IN} 0 = 19.5 mV (1/2 LSB) adjust R11, i.e., the offset voltage on B_{OFS} until DB7 – DB1 are LOW and DB0 (LSB) flickers.



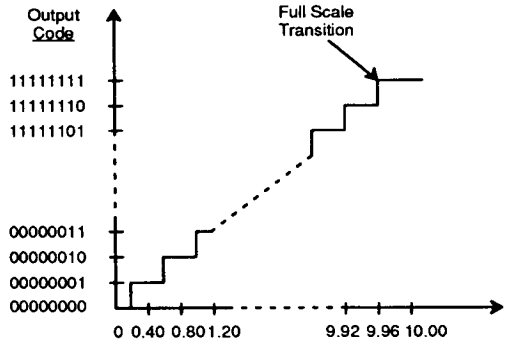
Notes:
(1) A1, R10, R11 and R12 can be omitted if offset trim is not required and BOFS can be tied to AGND.
(2) R1-R8 And R9 can be omitted if gain trim is not required.

Figure 6. MP7581 Unipolar (0 V to +10 V) Operation (Output Code is Straight Binary)

Gain (Full Scale)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply +9.941 V (F_S – 1 1/2 LSB) to all input channels A_{IN} (0–7)
2. Select required channel n via A0, A1, A2 and latch the Address using ALE.
3. Adjust trimmer RN of selected channel until DB7 – DB1 are HIGH and the LSB (DB0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.



Note: Approximate Bit Weights are shown for Illustration. Bit Weight for a –10 V Reference is ~ 39.1mV.

Figure 7. Transfer Characteristic for Unipolar Circuit of Figure 6.

Unipolar (Complementary Binary) Operation

Figure 8. and Figure 9. show the analog circuit connection and typical transfer characteristic for unipolar (complementary binary) operation.

Calibration is as follows (continuous conversions):

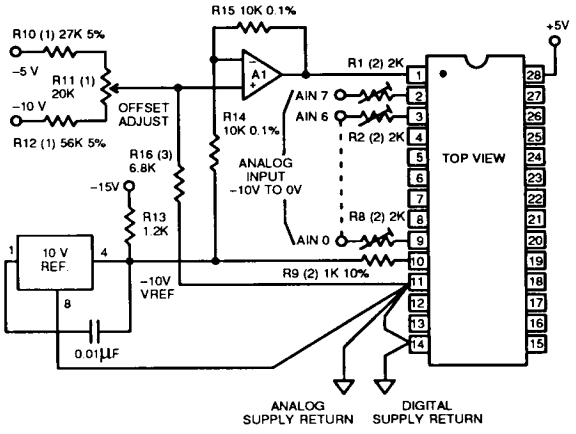
OFFSET: Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A0, A1 and A2 LOW and exercise ALE to latch the address.
2. With A_{IN} 0 = –9.98 V ($-F_S$ + 1/2 LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until DB7 – DB1 are LOW and the LSB (DB0) flickers.

Gain (Full Scale)

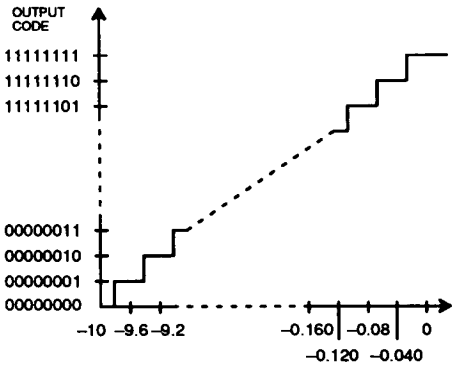
In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply –58.6 mV (1 1 /2 LSB) to all input channels A_{IN} (0–7).
2. Select required channel n via A0, A1, A2 and exercise ALE to latch the address.
3. Adjust trimmer R_N of selected channel until DB7 - DB1 are HIGH and the LSB (DB0) flickers.
4. Select next channel requiring gain trim and repeat step 2 and 3.



NOTES:
(1) R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED.
(2) R1-R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.
(3) R16/R10/R12 = 5KΩ IF R10, R11 AND R12 ARE NOT USED, MAKE R16 = 5KΩ

Figure 8. MP7581 (0 V to –10 V) Operation (Output Code is Complementary Binary)



Input Voltage, Volts (Referred to Analog Ground
Note: Approximate Bit Weights are Shown for Illustration.
Bit Weight for a –10 V Reference is ~ 39.1mv.

Figure 9. Transfer Characteristic for Unipolar Circuit of Figure 8.

Bipolar (Offset Binary) Operation

Figure 10. and Figure 11. illustrate the analog circuitry and transfer characteristic for ±5 V bipolar operation. Output coding is offset binary. Comparator offset correction is again applied to the B_{OFS} pin.

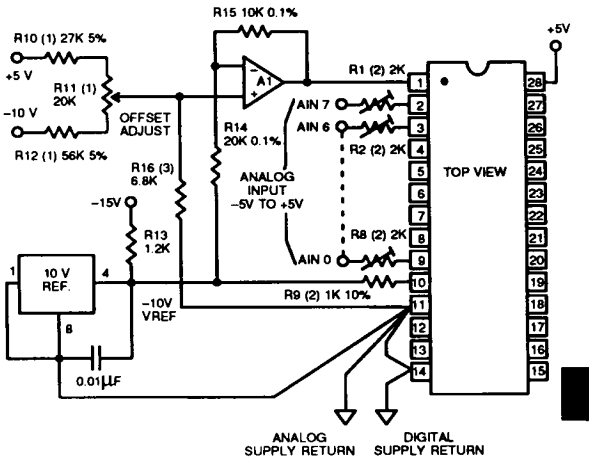
Calibration is as follows (continuous conversions):

OFFSET:

1. Apply –4.980 V (–F.S. + 1/2 LSB) to all input channels, A_{IN} (0-7).
2. Trim R11 of the comparator offset circuit until DB7 - DB1 are LOW and the LSB (DB0) flickers.

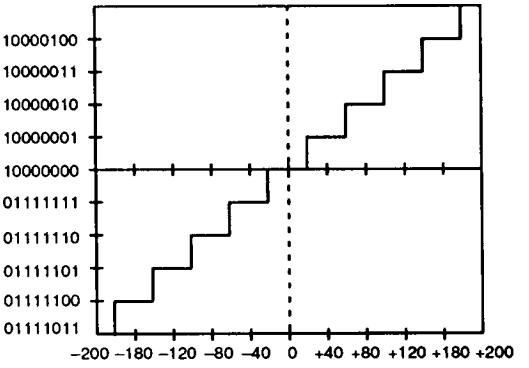
GAIN (FULL SCALE)

1. Apply +4.984 V (+F.S. – 1/2 LSB) to all input channels, A_{IN} (0-7).
2. Select required channel n via A0, A1, A2 and latch the address using ALE.
3. Adjust trimmer RN of selected channel until DB7 - DB1 are HIGH and the LSB (DB0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.
5. Apply 0 V to each gain-trimmed channel. If the ADC output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.



Notes:
(1) R10, R11 And R12 can be omitted if offset trim is not required.
(2) R1-R8 And R9 can be omitted if gain trim is not required.
(3) R16/R10/R12 = 6.8kΩ. If R10, R11 and R12 are not used, make R16 = 6.8kΩ

Figure 10. MP7581 Bipolar (–5 V to +5 V Operation (Output Code Is Offset Binary)



Input Voltage, Millivolts (Referred to Analog Ground)
Note: Approximate Bit Weights are Shown for Illustration.
Bit Weight for a ±5 V Full Scale ~ 39.1mV.

Figure 11. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10.

INTERFACING THE MP7581

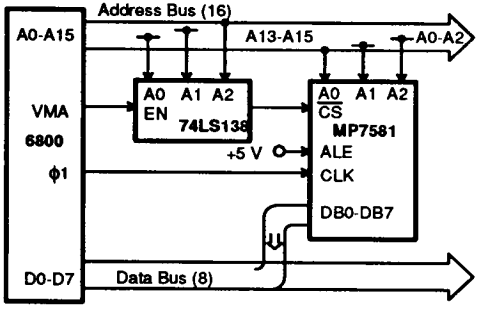


Figure 12. MP7581/6800 Interface

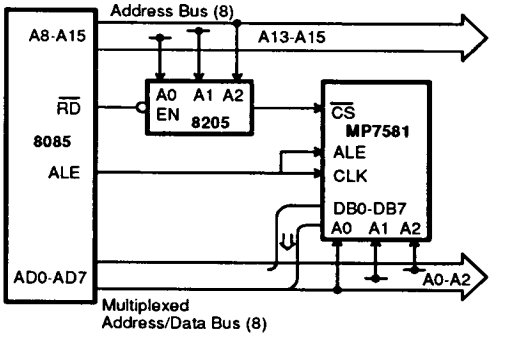


Figure 13. MP7581/8085 Interface

NOTES:

1. ANALOG AND DIGITAL GROUND
   It is recommended that AGND and DGND be connected locally to prevent the possibility of injecting noise into the MP7581. In systems where the AGND – DGND connection is not local, connect back-to-back diodes (IN914 or equivalent) between the MP7581 AGND and DGND pins.

2. LOGIC DEGLITCHING IN μP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address but) can cause glitches at the MP7581 $\overline{CS}$ terminal. These glitches can cause unwanted reads. The best way to avoid glitches is to gate the address decoding logic, e.g., with RD (8080), $\overline{RD}$ (8085) or VMA (6800).