



100mA LDO Linear Regulators with Current-Limiting Switch

MAX4832/MAX4833

General Description

The MAX4832/MAX4833 family of low-dropout (LDO) linear regulators feature an accurate current-limiting switch with an integrated $\overline{\text{FLAG}}$ or $\overline{\text{RESET}}$ function. These devices operate from 2.5V to 5.5V and deliver up to 100mA of load current at a preset output voltage. Preset output voltage levels are 1.8V/2.5V/2.8V/3.0V/3.3V.

The MAX4832/MAX4833 offer a programmable soft-start control function to eliminate false reset during startup. The MAX4832 provides a $\overline{\text{FLAG}}$ function to notify the system when the load current exceeds the limit. The MAX4833 provides a $\overline{\text{RESET}}$ function to notify the system when the output drops below the threshold. Additionally, reverse-current protection prevents current flowing from the output to the input. Other features include a low 90 μ A quiescent current, a 0.1 μ A shutdown current.

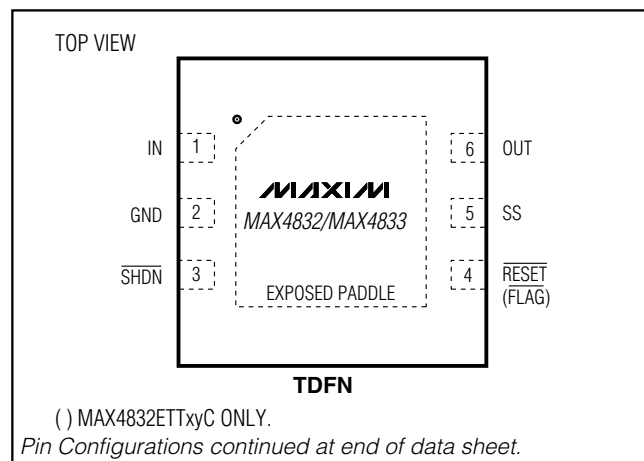
The MAX4832/MAX4833 are available in space-saving 6-pin SOT23 and TDFN packages. Each device is specified over the -40°C to +85°C extended temperature range. Contact factory for other programmed output voltage versions from 1.5V to 3.3V in 100mV increments.

For pin-compatible 250mA versions of this device, refer to the MAX4834/MAX4835. For pin-compatible 500mA versions of this device, refer to the MAX4836/MAX4837.

Applications

SDIO Ports and Devices	Notebook Computers
USB Ports and Devices	Cell Phones
PDA's and Palmtop Devices	GPS Systems

Pin Configurations



Features

- ◆ Guaranteed Minimum 100mA Load Current
- ◆ Accurate Current Limit
- ◆ Preset Output Voltages: 1.8V/2.5V/2.8V/3.0V/3.3V
- ◆ 2.5V to 5.5V Supply Voltage Range
- ◆ Adjustable Soft-Start
- ◆ Low Dropout Voltage
- ◆ Thermal Shutdown
- ◆ Reverse-Current Protection
- ◆ Shutdown Output Discharge (MAX4833)
- ◆ Low 90 μ A Supply Current
- ◆ Ultra-Low 0.1 μ A Shutdown Current
- ◆ $\overline{\text{FLAG}}$ and Latch Off (MAX4832) or $\overline{\text{RESET}}$ (MAX4833)
- ◆ Tiny SOT23 and TDFN Packages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4832EUTxy_-T*	-40°C to +85°C	6 SOT23-6
MAX4832ETTxy_-T	-40°C to +85°C	6 TDFN-6
MAX4833EUTxy_dd-T*	-40°C to +85°C	6 SOT23-6
MAX4833ETTxy_dd-T	-40°C to +85°C	6 TDFN-6

Note: "xy" are placeholders for the output voltage levels of the devices. Insert the values found in Table 1 at the end of this document in the place of "xy". The "_" is a placeholder for either the $\overline{\text{RESET}}$ or the $\overline{\text{FLAG}}$ feature. Insert "B" in the place of "_" for $\overline{\text{RESET}}$ and "C" for $\overline{\text{FLAG}}$. "dd" is a placeholder for the reset timeout period. Insert the values found in Table 2 in the place of "dd." For example, MAX4833EUT18BD2 has a 1.8V output voltage, $\overline{\text{RESET}}$ feature, and a 30ms reset timeout period. Note that "dd" applies only to the devices with $\overline{\text{RESET}}$ option and does not apply to the devices with $\overline{\text{FLAG}}$ option. For devices with the $\overline{\text{FLAG}}$ option, leave dd blank. Standard versions require a minimum order increment of 2.5k units. Nonstandard versions must be ordered in 10k unit increments. Contact factory for availability.

*Future product—contact factory for availability.

Tables 1 and 2 and Selector Guide appear at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

IN, $\overline{\text{SHDN}}$, FLAG, OUT to GND-0.3V to +6V
 RESET to GND-0.3V to ($V_{\text{OUT}} + 0.3\text{V}$)
 SS to GND-0.3V to ($V_{\text{IN}} + 0.3\text{V}$)
 IN to OUT $\pm 6\text{V}$
 OUT Short Circuit to GNDContinuous
 All Pins ESD Handling (Human Body Model)2kV

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 6-Pin SOT23 (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)727mW
 6-Pin TDFN (derate 24.4mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)1951.2mW
 Operating Temperature Range -40°C to $+85^\circ\text{C}$
 Operating Junction Temperature Range -40°C to $+125^\circ\text{C}$
 Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$, $\overline{\text{SHDN}} = \text{IN}$, $C_{\text{OUT}} = 3.3\mu\text{F}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V _{IN}			2.5		5.5	V
Input Undervoltage Lockout Threshold	V _{UVLO}	V _{IN} rising		2.00		2.25	V
Input Undervoltage Lockout Threshold Hysteresis				50			mV
Quiescent Current	I _Q	SHDN = IN, I _{OUT} = 0		90 150			μA
		SHDN = IN, I _{OUT} = 0, V _{UVLO} < V _{IN} < V _{OUT} (nominal)		150			
		SHDN = GND, I _{OUT} = 0		0.1 2			
Dropout Voltage (Note 2)		I _{OUT} = 100mA	T _A = +25°C	75 105		mV	
			T _A = -40°C to +85°C	130			
Output Voltage Accuracy		I _{OUT} = 1mA to 100mA, T _A = +25°C		-1	+1		%V _{NOM}
		I _{OUT} = 1mA to 100mA, T _A = -40°C to +85°C		-2	+2		
Output Current	I _{OUT}			100			mA
Output Current Limit		V _{OUT} = 0V		115	135		mA
Reverse Current at V _{IN}		V _{OUT} = 5.5V, V _{IN} = 0V to V _{OUT}		0.1 2		μA	
Soft-Start Time (Note 3)	t _{SS}	C _{SS} = not connected		0.5	1	2.0	ms
		C _{SS} = 0.01μF		4	10	15	
		C _{SS} = 0.1μF		50	100	150	
Line Regulation (Note 4)		V _{OUT} + 0.5V < V _{IN} < 5.5V, I _{LOAD} = 100μA	T _A = +25°C	-0.04	+0.02	+0.065	%V _{NOM} /V
			T _A = -40°C to +85°C	-0.05	+0.03	+0.08	
Load Regulation		100μA < I _{LOAD} < 100mA, V _{IN} = V _{OUT} + 1V		1.3		%V _{NOM}	
Output Noise		10Hz to 100kHz, C _{SS} = 0.01μF		70		μVRMS	
SHUTDOWN INPUT (SHDN)							
OUT Discharge Resistance in Shutdown (MAX4833)		SHDN = GND		900			Ω
SHDN Input-Voltage High	V _{IH}			1.4			V
SHDN Input-Voltage Low	V _{IL}			0.5			V
SHDN Input Hysteresis				30			mV
SHDN Input Leakage Current		SHDN = IN or GND		-100 +100		nA	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{OUT} + 1V$, $\overline{SHDN} = IN$, $C_{OUT} = 3.3\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET OUTPUT (MAX4833)						
$\overline{RESET}$ Threshold	$V_{\overline{RESET}}$		$0.85 \times V_{OUT}$	$0.875 \times V_{OUT}$	$0.90 \times V_{OUT}$	V
OUT Drop to RESET Delay (Note 5)	t_{OR}			35		μs
$\overline{RESET}$ Timeout Period	$t_{\overline{RESET}}$	D1 timing option	2.5	3.75	5.0	ms
		D2 timing option	20	30	40	
		D3 timing option	150	225	300	
		D4 timing option	1200	1800	2400	
$\overline{RESET}$ Output-Voltage Low		$V_{OUT} \geq 1.0V$, $I_{SINK} = 50\mu A$, $\overline{RESET}$ asserted			0.3	V
		$V_{OUT} \geq 1.5V$, $I_{SINK} = 3.2mA$, $\overline{RESET}$ asserted			0.4	
$\overline{RESET}$ Output-Voltage High		$V_{OUT} \geq 2.0V$, $I_{SOURCE} \leq 500\mu A$, $\overline{RESET}$ deasserted	$0.8 \times V_{OUT}$			V
FLAG OUTPUT (MAX4832)						
Blanking Time (Note 6)	t_{BLANK}	$V_{OUT} + 1V \leq V_{IN} \leq 5.5V$, $OUT = GND$	5	10	17	ms
Open-Drain $\overline{FLAG}$ Output-Voltage Low		$I_{SINK} = 3.2mA$, $\overline{FLAG}$ asserted, $V_{OUT} \geq 1.5V$			0.4	V
Open-Drain $\overline{FLAG}$ Leakage Current		$V_{\overline{FLAG}} = 5.5V$		0.01	1	μA
THERMAL PROTECTION						
Thermal-Shutdown Temperature		Junction temperature rising		+165		$^\circ C$
Thermal-Shutdown Hysteresis				15		$^\circ C$

Note 1: Parts are 100% tested at $+25^\circ C$. Limits across the full temperature range are guaranteed by design and correlation over the specified temperature range.

Note 2: The dropout voltage is measured from V_{IN} to V_{OUT} when V_{OUT} is 2% below its nominal value. The nominal output voltage is measured from V_{OUT} to GND when V_{IN} is 1V greater than V_{OUT} . Defined only for $V_{OUT} \geq 2.5V$.

Note 3: Soft-start time is defined as the time required for the output to rise from 10% of its nominal value to 90% of its nominal value.

Note 4: For $V_{OUT} < 2V$, V_{IN} must be above 2.5V.

Note 5: This is the maximum time OUT can be out of tolerance before a reset is issued. It is implemented to ensure that momentary output glitches do not trigger a reset condition.

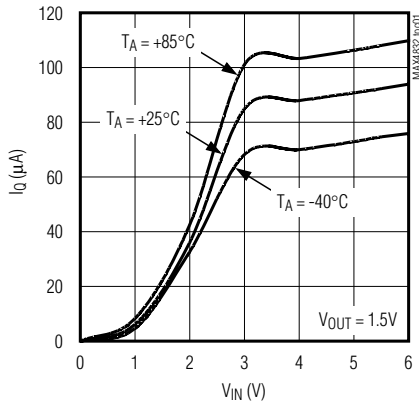
Note 6: In startup mode, the blanking time counter is not started until the soft-start time has elapsed. The total time from startup to $\overline{FLAG}$ issued is $t_{SS} + t_{BLANK}$.

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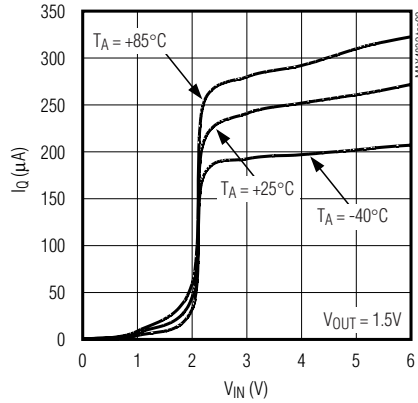
Typical Operating Characteristics

($V_{IN} = V_{OUT} + 1V$, $\overline{SHDN} = IN$, $C_{OUT} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

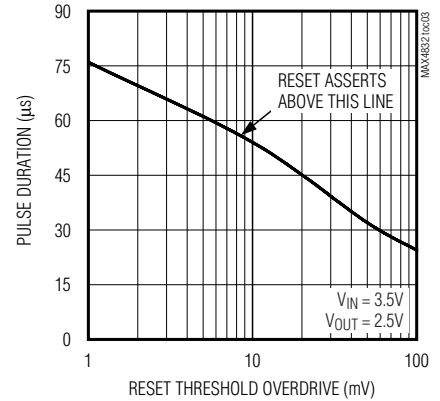
**QUIESCENT CURRENT vs. INPUT VOLTAGE
(NO LOAD)**



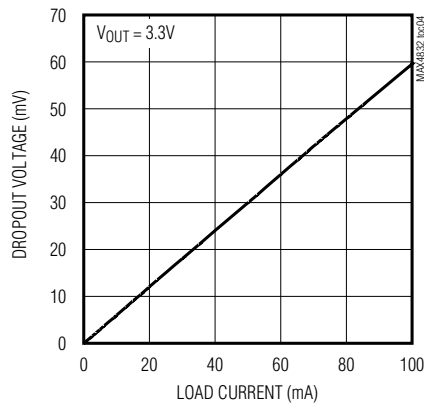
**QUIESCENT CURRENT vs. INPUT VOLTAGE
(100mA LOAD)**



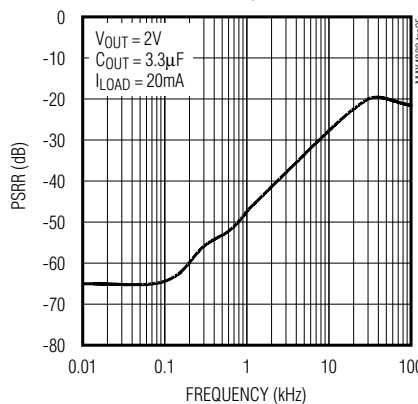
**MAXIMUM TRANSIENT DURATION
vs. RESET THRESHOLD OVERDRIVE**



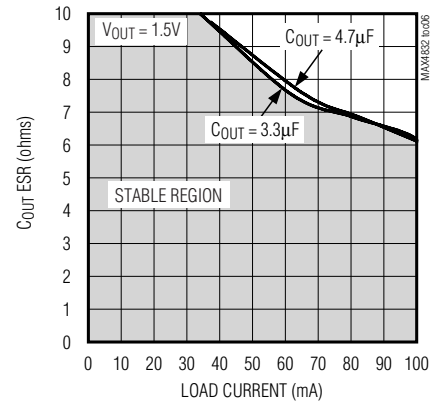
DROPOUT VOLTAGE vs. LOAD CURRENT



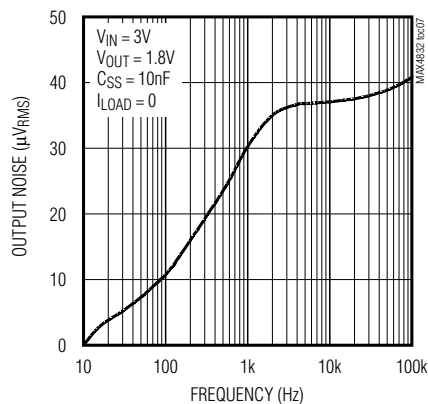
**POWER-SUPPLY REJECTION RATIO
vs. FREQUENCY**



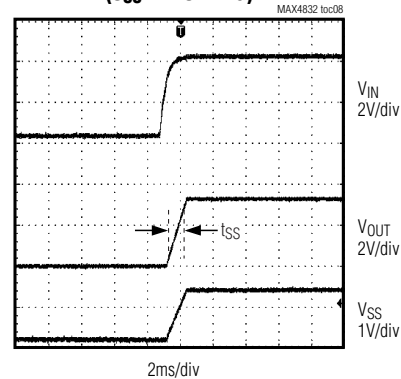
**REGION OF STABLE COUT ESR
vs. LOAD CURRENT**



OUTPUT NOISE vs. FREQUENCY



**SOFT-START RESPONSE
(CSS = FLOATING)**



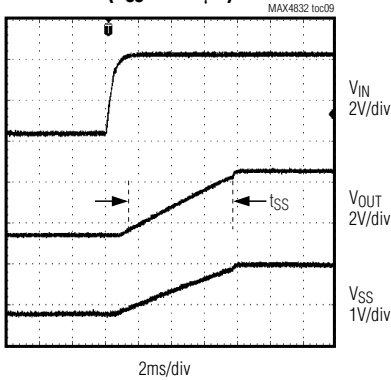
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Typical Operating Characteristics (continued)

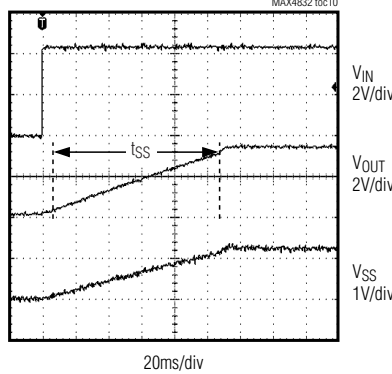
($V_{IN} = V_{OUT} + 1V$, $\overline{SHDN} = IN$, $C_{OUT} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

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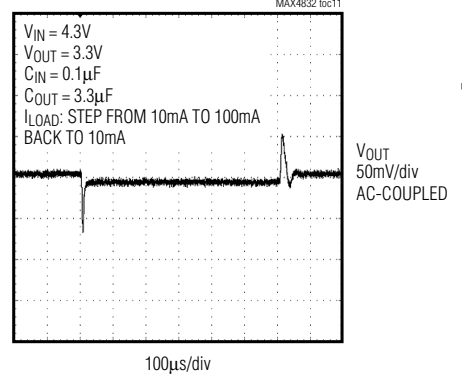
SOFT-START RESPONSE
($C_{SS} = 0.01\mu F$)



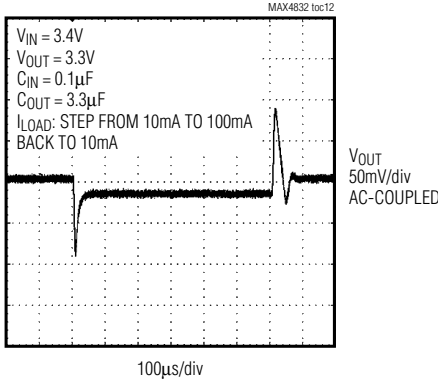
SOFT-START RESPONSE
($C_{SS} = 0.1\mu F$)



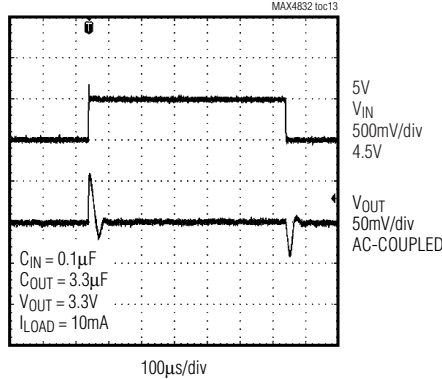
LOAD-TRANSIENT RESPONSE



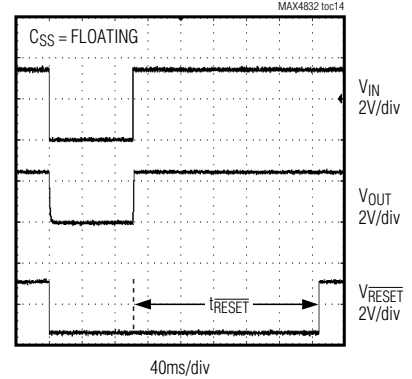
LOAD-TRANSIENT RESPONSE
NEAR DROPOUT



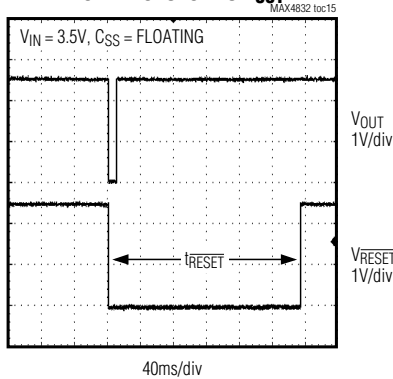
LINE-TRANSIENT RESPONSE



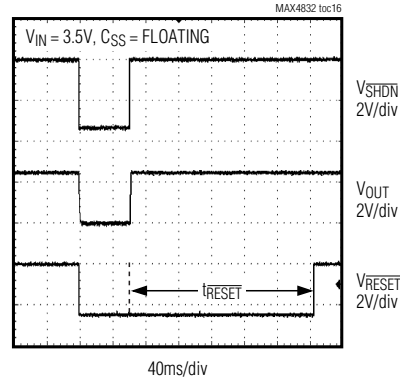
$\overline{RESET}$ RESPONSE TO V_{IN}



$\overline{RESET}$ RESPONSE TO V_{OUT}



$\overline{RESET}$ RESPONSE TO SHUTDOWN

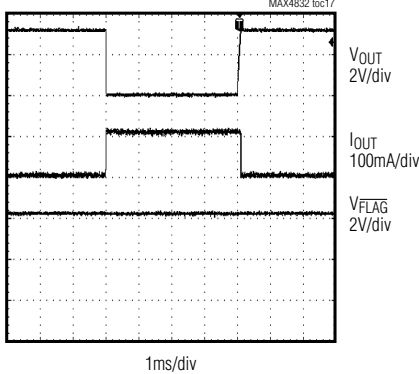


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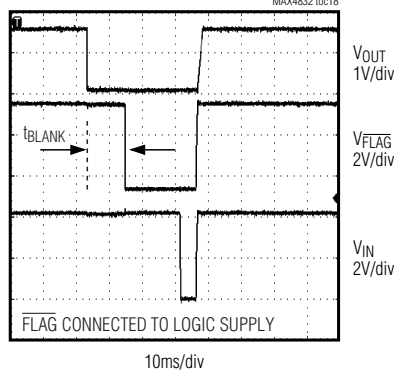
Typical Operating Characteristics (continued)

($V_{IN} = V_{OUT} + 1V$, $\overline{SHDN} = IN$, $C_{OUT} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

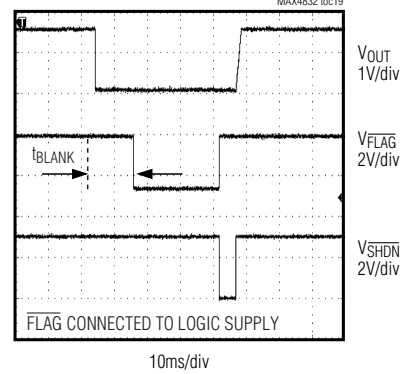
FLAG RESPONSE WHEN OUT IS SHORTED TO GND < BLANKING TIME



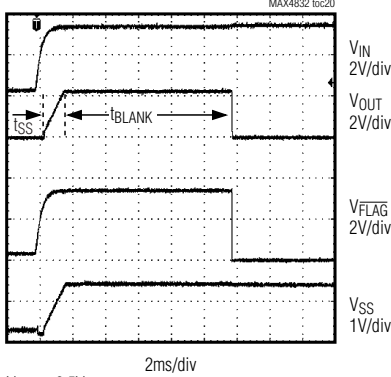
FLAG RESPONSE WHEN OUT IS SHORTED TO GND > BLANKING TIME (IN IS TOGGLED)



FLAG RESPONSE WHEN OUT IS SHORTED TO GND > BLANKING TIME (SHDN IS TOGGLED)

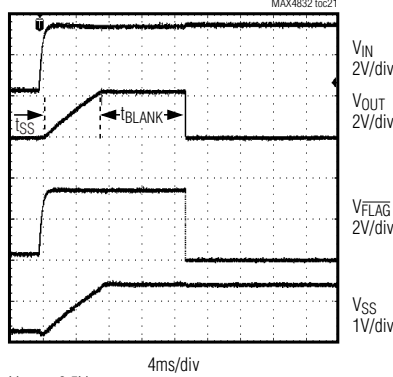


STARTUP IN AN OVERLOAD CONDITION (CSS NOT CONNECTED)



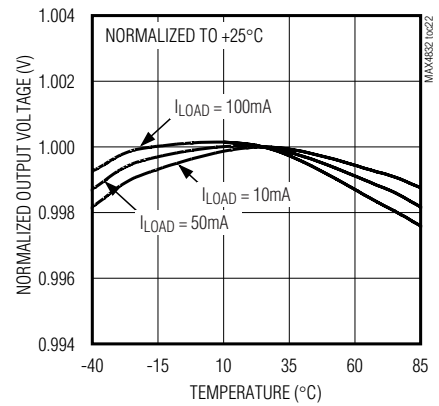
$V_{OUT} = 2.5V$
 $I_{LOAD} = I_{LIMIT\ MAXIMUM}$
 FLAG CONNECTED TO IN

STARTUP IN AN OVERLOAD CONDITION (CSS = 0.01μF)



$V_{OUT} = 2.5V$
 $I_{LOAD} = I_{LIMIT\ MAXIMUM}$
 FLAG CONNECTED TO IN

NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



100mA LDO Linear Regulators with Current-Limiting Switch

Pin Description

PIN		NAME	FUNCTION
SOT23	TDFN		
1	1	IN	Regulator Power Input. Bypass IN to GND with a 0.1μF ceramic capacitor. Install the bypass capacitor as close to the device as possible.
2	2	GND	Ground
3	3	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Drive $\overline{\text{SHDN}}$ low to shutdown the regulator. Drive $\overline{\text{SHDN}}$ high or connect to IN for normal operation.
4	4	$\overline{\text{FLAG}}$ (MAX4832)	Overcurrent Flag. Open-drain $\overline{\text{FLAG}}$ goes low when the device senses sustained current exceeding the current-limit threshold for a duration longer than the blanking time. $\overline{\text{FLAG}}$ is high when $\overline{\text{SHDN}}$ is low or the device is in thermal shutdown.
		$\overline{\text{RESET}}$ (MAX4833)	Active-Low Reset Output. Push-pull $\overline{\text{RESET}}$ goes low when the voltage at OUT is below the reset threshold or when the voltage at OUT is greater than IN. $\overline{\text{RESET}}$ is low when $\overline{\text{SHDN}}$ is low or the device is in thermal shutdown. After the reset condition terminates, $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period.
5	5	SS	Soft-Start Control. Connect a capacitor, C _{SS} , from SS to GND to program the output rise time at startup. No capacitor from SS to GND gives 1ms output rise time at startup. See the soft-start response time plots in the <i>Typical Operating Characteristics</i> .
6	6	OUT	Regulator Output. Bypass OUT to GND with a 3.3μF or larger ceramic capacitor. The capacitor's ESR should be less than 0.2Ω for stable operation.
—	EP	EP	Exposed Pad. EP is internally connected to GND. Externally connect EP to GND to provide a low thermal resistance path from the IC junction to the PC board.

Detailed Description

The MAX4832/MAX4833 are ultra-low quiescent current, low-dropout linear regulators with an integrated current limiter. These devices guarantee up to 100mA drive capabilities and regulate the preset output voltage.

The MAX4832 has a flag output that asserts low when the load current exceeds the current limit for more than the blanking time (t_{BLANK}). The MAX4833 has a reset output that asserts low when the regulator output voltage is below the reset threshold voltage (V_{RESET}). V_{RESET} is 87.5% of the nominal output voltage. Figure 1 shows the simplified functional diagram and Figure 2 shows the typical application circuits.

$\overline{\text{FLAG}}$ Output (MAX4832)

The open-drain $\overline{\text{FLAG}}$ output goes low and the LDO's pass transistor is latched off when the current in the pass transistor is at its output current limit for more than the blanking time (t_{BLANK}). Cycling IN, or $\overline{\text{SHDN}}$ (high to low to high) brings the device out of its latched-off state and back into normal operation.

$\overline{\text{RESET}}$ Output (MAX4833)

The $\overline{\text{RESET}}$ output asserts when one of the following conditions occurs:

- The input voltage (V_{IN}) is below the input undervoltage lockout threshold (V_{UVLO}).
- The output voltage (V_{OUT}) is below the reset threshold (V_{RESET}).
- $\overline{\text{SHDN}}$ is pulled low.
- The device is in thermal shutdown.
- When $V_{\text{OUT}} > V_{\text{IN}}$.

$\overline{\text{RESET}}$ remains low for the reset timeout period (t_{RESET}) after reset conditions are terminated. There are four $\overline{\text{RESET}}$ timeout periods available as shown in the *Electrical Characteristics* table. $\overline{\text{RESET}}$ is available in a push-pull configuration as shown in the *Selector Guide*.

Shutdown

Pull $\overline{\text{SHDN}}$ low to shut down the LDO and reduce the quiescent current consumption of the device from 90μA to 0.1μA. In shutdown mode, the pass transistor, control circuit, and reference circuit are turned off. Connect $\overline{\text{SHDN}}$ to a supply voltage greater than V_{IH} to turn on the LDO.

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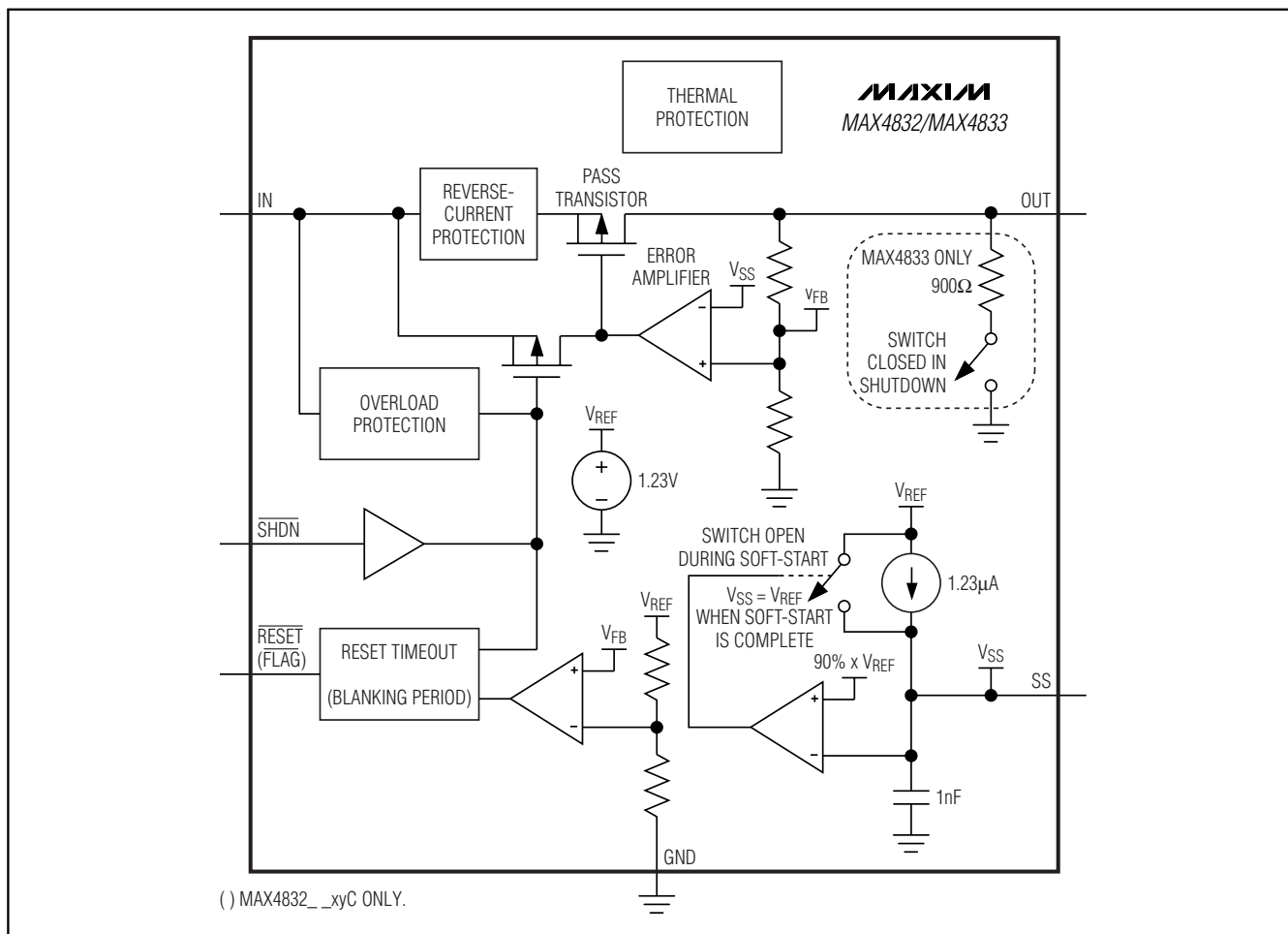


Figure 1. Functional Diagram

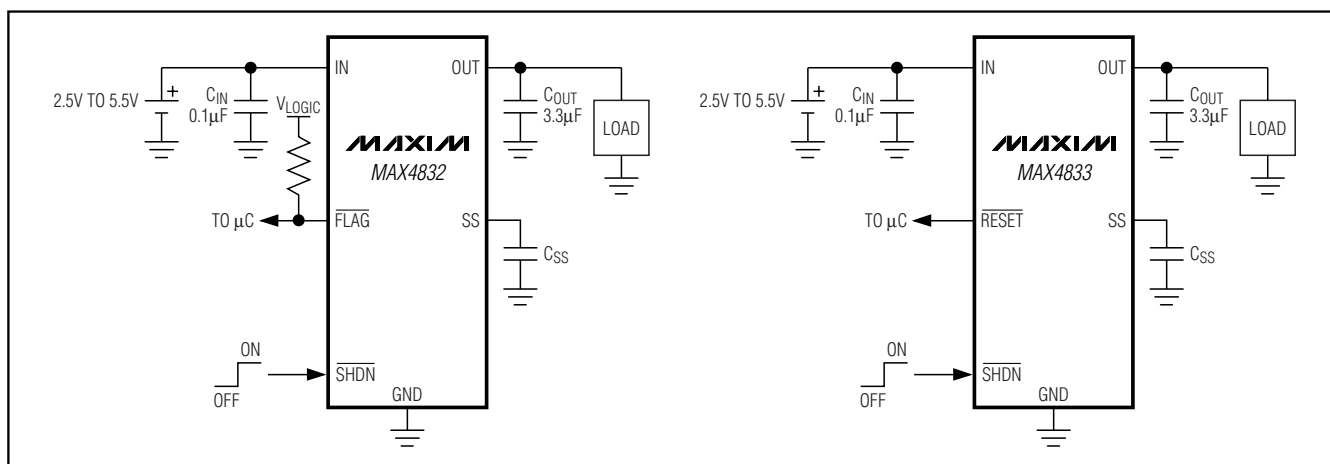


Figure 2. Typical Application Circuits

100mA LDO Linear Regulators with Current-Limiting Switch

Shutdown Discharge (MAX4833)

OUT discharges through a 900Ω internal resistor during shutdown mode.

Reverse OUT to IN Current

When the output voltage is greater than the input voltage, the internal pass transistor turns off. To avoid reverse-charging the input source, the current at IN is guaranteed to be below 3μA when $V_{OUT} \geq V_{IN}$.

Current Limit

The MAX4832/MAX4833 include an accurate internal current-limiting circuit. OUT can be shorted to ground indefinitely without damaging the part.

The MAX4832 latches off if the load current exceeds the current limit for more than the blanking time (see the *FLAG Output* section). During soft-start, the device does not latch off to an overload condition. During an overload condition, the MAX4833 holds the current at current limit until the thermal limit is reached. Once the junction temperature reaches +165°C, thermal shutdown occurs.

Thermal Shutdown

When the junction temperature (T_J) exceeds +165°C, the LDO's pass transistor turns off allowing the junction to cool. The LDO's pass transistor turns on again after the IC's junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

Soft-Start

During power-up, the soft-start ensures that the output ramps up slowly reducing inrush current peaks. See the soft-start response time plots in the *Typical Operating Characteristics*. The soft-start time (t_{SS}) is given by the following equation:

$$t_{SS} = C_{SS} \text{ (ms)}$$

where C_{SS} is in nF.

A soft-start capacitor (C_{SS}) of 10nF gives a 10ms t_{SS} . A 1ms minimum soft-start time is fixed internally to ensure that the output rises slowly even without any external capacitor at SS pin to ground. The device is in soft-start mode when either the voltage at IN or $\overline{SHDN}$ is cycled high to low to high.

Applications Information

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 100mA, use a 3.3μF (min) ceramic output capacitor with an ESR <0.2Ω. To reduce noise and improve load transient response, stability, and power-supply rejection, use larger output capacitor values such as 10μF (note that some ceramic capacitors exhibit large capacitance and ESR variation with temperature). X7R capacitors provide good performance over the -40°C to +85°C operating temperature range.

To improve power-supply rejection and transient response, use a 0.1μF capacitor between IN and GND. The MAX4832/MAX4833 remain stable with purely resistive loads or current loads up to 100mA.

15kV Operational ESD Protection

A 3.3μF or higher value ceramic capacitor from OUT to GND provides a 15kV (Human Body Model) protection at OUT. The ESR value of the capacitor should be less than 0.2Ω.

Reset Transient Immunity

The reset circuit is relatively immune to short duration, falling V_{OUT} transients. The *Typical Operating Characteristics* show a graph of the Maximum Transient Duration vs. Reset Threshold Overdrive for which reset is not asserted. The graph was produced using falling V_{OUT} transients starting at V_{OUT} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a falling V_{OUT} transient can typically have without triggering the reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{OUT} transient that goes only 10mV below the reset threshold and lasts up to 54μs does not trigger a reset pulse.

Layout

When using the TDFN package, connect its exposed paddle to GND to provide a low thermal resistance path for heat transfer from the IC junction to the printed circuit board.

100mA LDO Linear Regulators with Current-Limiting Switch

Selector Guide

PART	PIN-PACKAGE	OUTPUT CURRENT (mA)	RESET OUTPUT CONFIGURATION	RESET (FLAG)	SHUTDOWN DISCHARGE	LATCH OFF
MAX4832EUTxyC	6 SOT23-6	100	Open-Drain	FLAG	No	Yes
MAX4832ETTxyC	6 TDFN-6	100	Open-Drain	FLAG	No	Yes
MAX4833EUTxyBdd	6 SOT23-6	100	Push-Pull	RESET	Yes	No
MAX4833ETTxyBdd	6 TDFN-6	100	Push-Pull	RESET	Yes	No

Suffix 'xy' in the part number stands for nominal output voltage. 1.8V, 2.5V, 2.8V, 3.0V, 3.3V are the standard options. For other voltages between 1.5V to 3.3V, contact factory.

Table 1. Standard Output Voltage Suffix Guide

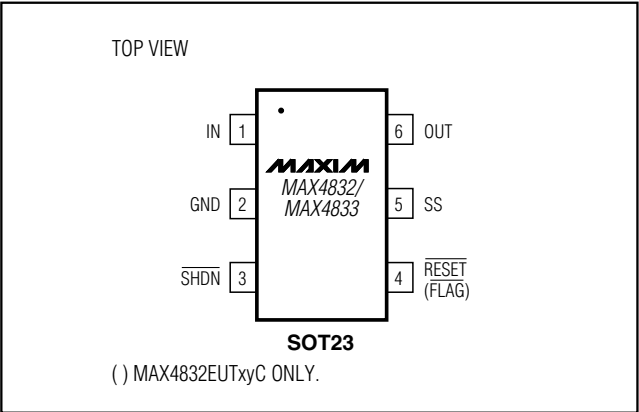
xy	OUTPUT VOLTAGE (V)
18	1.8
25	2.5
28	2.8
30	3.0
33	3.3

Nonstandard output voltages from 1.5V to 3.3V are available in 100mV increments. Contact factory for availability.

Table 2. RESET Timeout Period Suffix Guide

dd	RESET TIMEOUT (ms)
D1	3.75
D2	30
D3	225
D4	1800

Pin Configurations (continued)



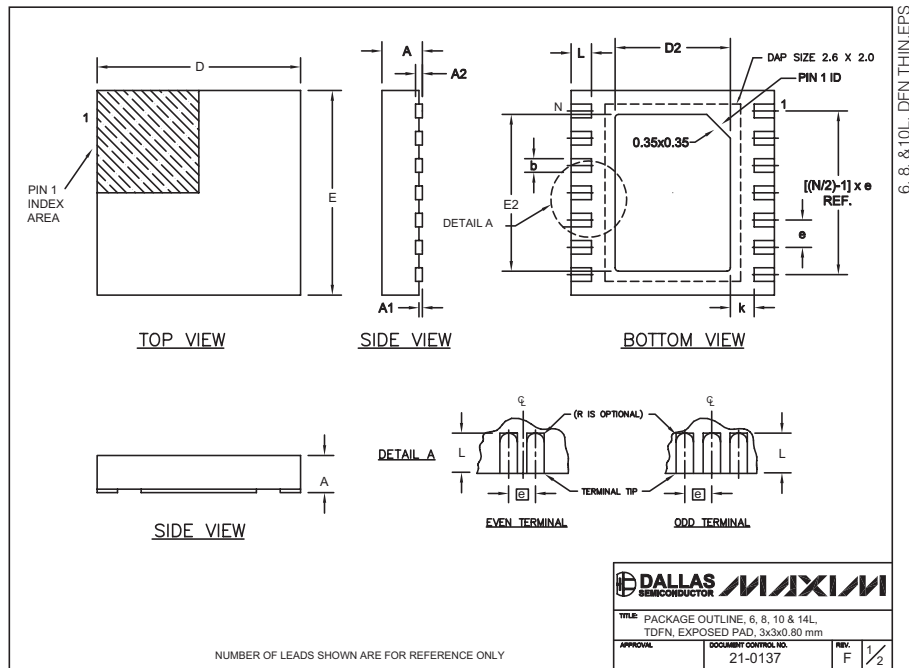
Chip Information

TRANSISTOR COUNT: 1575
 PROCESS: BiCMOS
 TDFN Exposed Pad: Connected to GND

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.03	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.03	2.40 REF

NOTES:

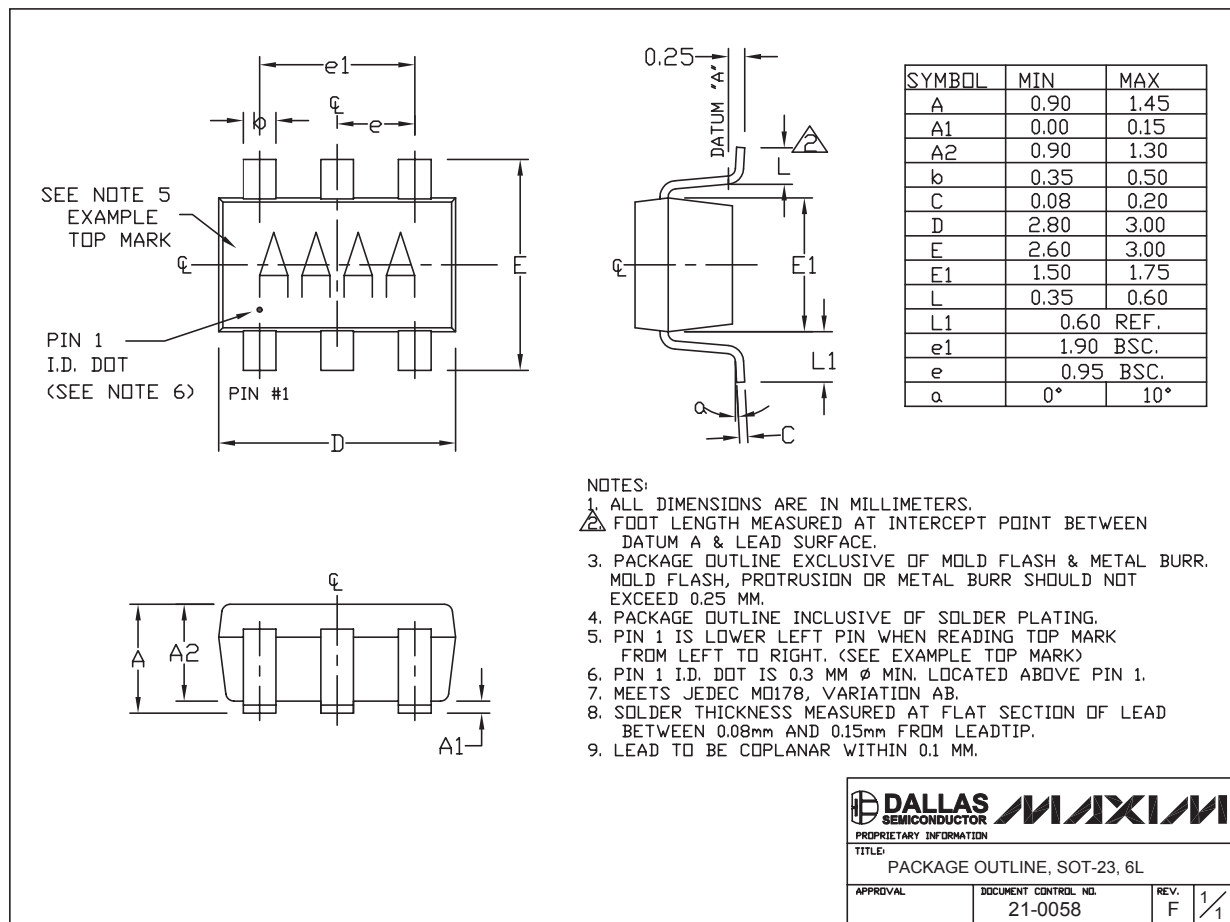
- ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
- COPLANARITY SHALL NOT EXCEED 0.08 mm.
- WARPAGE SHALL NOT EXCEED 0.10 mm.
- PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
- DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
- "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM		
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm		
APPROVAL:	DOCUMENT CONTROL NO. 21-0137	REV. F 2/2

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Package Information (continued)

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6LSOTEPs

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