

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

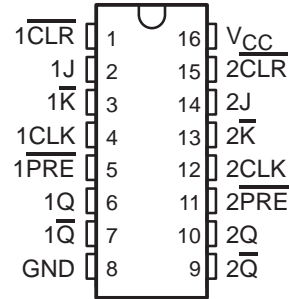
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS109A	50	6
'AS109A	129	29

## description

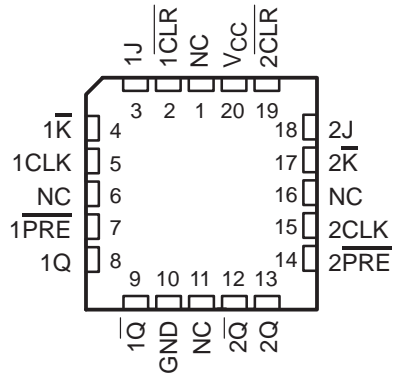
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the J and  $\overline{\text{K}}$  inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and  $\overline{\text{K}}$  inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\overline{\text{K}}$  and tying J high. They also can perform as D-type flip-flops if J and  $\overline{\text{K}}$  are tied together.

The SN54ALS109A and SN54AS109A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS109A and SN74AS109A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS109A, SN54AS109A ... J PACKAGE  
SN74ALS109A, SN74AS109A ... D OR N PACKAGE  
(TOP VIEW)



SN54ALS109A, SN54AS109A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{\text{Q}}0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{\text{Q}}0$

<sup>†</sup> The output levels in this configuration are not specified to meet the minimum levels for  $V_{OH}$  if the lows at  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

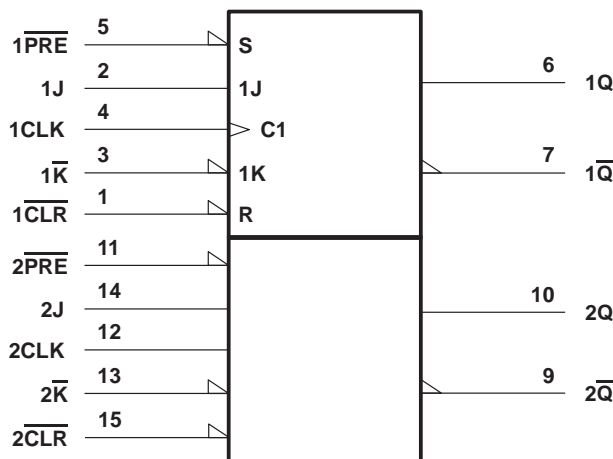
# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS109A	–55°C to 125°C
SN74ALS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V
I <sub>OH</sub>	High-level output current		−0.4			−0.4			mA
I <sub>OL</sub>	Low-level output current		4			8			mA
f <sub>clock</sub>	Clock frequency		0	30		0	34		MHz
t <sub>w</sub>	Pulse duration	PRE or CLR low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t <sub>su</sub>	Setup time before CLK↑	Data	15			15			ns
		PRE or CLR inactive	10			10			
t <sub>h</sub>	Hold time after CLK↑	Data	0			0			ns
T <sub>A</sub>	Operating free-air temperature		−55	125		0	70		°C



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS109A		SN74ALS109A		UNIT
			MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA	−1.5		−1.5		V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −0.4 mA	V <sub>CC</sub> − 2		V <sub>CC</sub> − 2		V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA		0.25 0.4		V
			I <sub>OL</sub> = 8 mA		0.35 0.5		
I <sub>I</sub>	CLK, J, or $\overline{K}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V	0.1		0.1		mA
	$\overline{PRE}$ or $\overline{CLR}$		0.2		0.2		
I <sub>IH</sub>	CLK, J, or $\overline{K}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20		20		μA
	$\overline{PRE}$ or $\overline{CLR}$		40		40		
I <sub>IL</sub>	CLK, J, or $\overline{K}$	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	−0.2		−0.2		mA
	$\overline{PRE}$ or $\overline{CLR}$		−0.4		−0.4		
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	−20	−112	−30	−112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, See Note 1	2.4	4	2.4	4	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J,  $\overline{K}$ , CLK, and  $\overline{PRE}$  grounded, then with J,  $\overline{K}$ , CLK, and  $\overline{CLR}$  grounded.

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			30		34		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	3	17	3	13	ns
t <sub>PHL</sub>			5	17	5	15	
t <sub>PLH</sub>	CLK	Q or Q̄	5	21	5	16	ns
t <sub>PHL</sub>			5	20	5	18	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS109A	–55°C to 125°C
SN74AS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54AS109A			SN74AS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V
I <sub>OH</sub>	High-level output current		−2			−2			mA
I <sub>OL</sub>	Low-level output current		20			20			mA
f <sub>clock</sub> *	Clock frequency		0	90		0	105		MHz
t <sub>w</sub> *	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t <sub>su</sub> *	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2			2			
t <sub>h</sub> *	Hold time after CLK↑	Data	0			0			ns
T <sub>A</sub>	Operating free-air temperature		−55	125		0	70		°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109A			SN74AS109A			UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				–1.2			–1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$			0.25	0.5		0.25	0.5	V
$I_I$		$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$				0.1			0.1	mA
$I_{IH}$	CLK, J, or $\overline{K}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$				20			20	$\mu\text{A}$
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$					40			40	
$I_{IL}$	CLK, J, or $\overline{K}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$				–0.5			–0.5	mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$					–1.8			–1.8	
$I_{O\text{§}}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$		–30		–112	–30		–112	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , See Note 1			11.5	17		11.5	17	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J,  $\overline{K}$ , CLK, and  $\overline{\text{PRE}}$  grounded, then with J, K, CLK, and  $\overline{\text{CLR}}$  grounded.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS109A		SN74AS109A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			90		105		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	2	9	2	8	ns
t <sub>PHL</sub>			3.5	11.5	3.5	10.5	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	2.5	10	2.5	9	ns
t <sub>PHL</sub>			3.5	10.5	3.5	9	

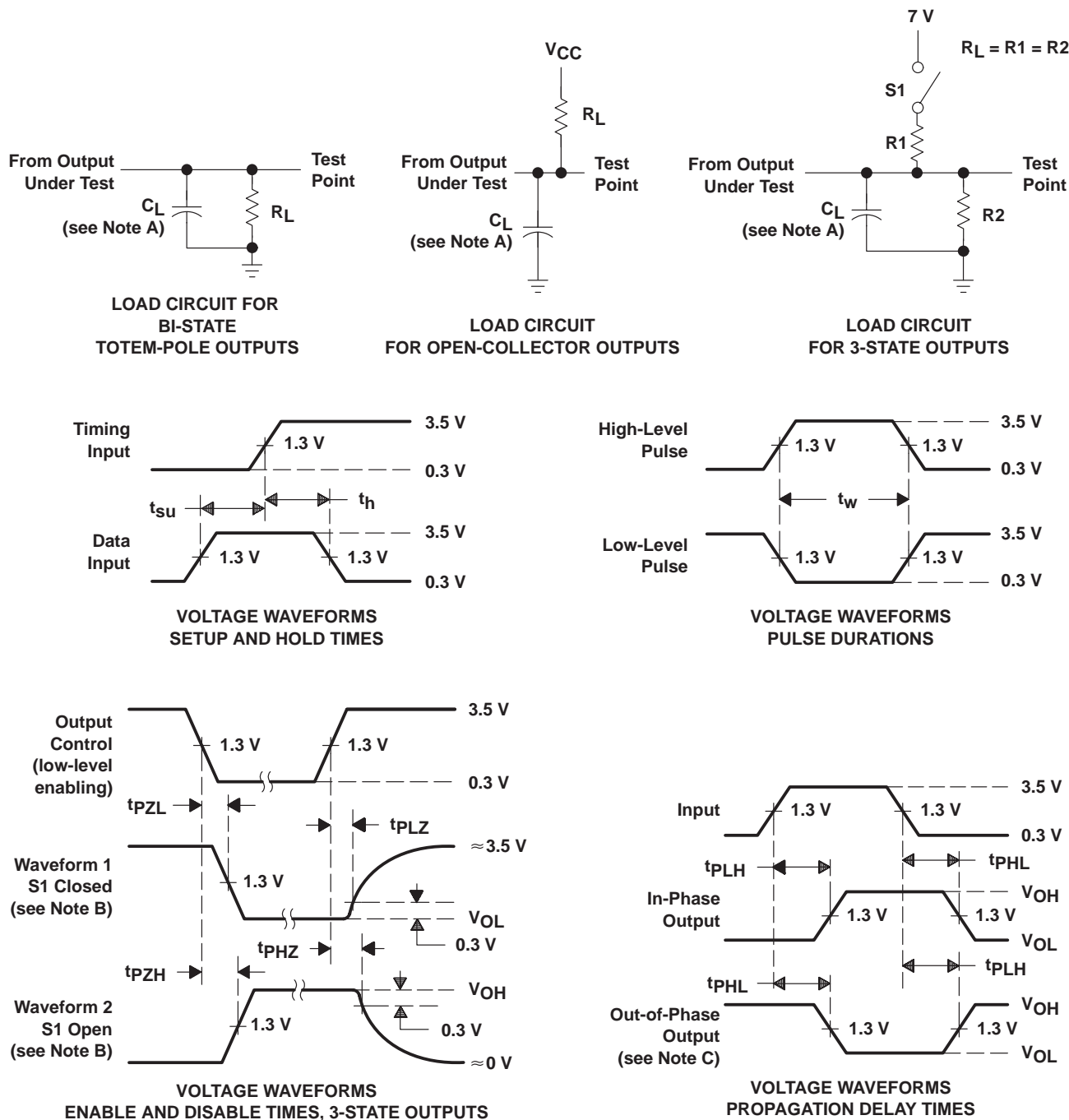
\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
84000012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8400001EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
8400001FA	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
JM38510/37102B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/37102BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SN54ALS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SN54AS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SN74ALS109AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS109AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74ALS109ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS109ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS109ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS109ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS109AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54ALS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS109AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

---

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

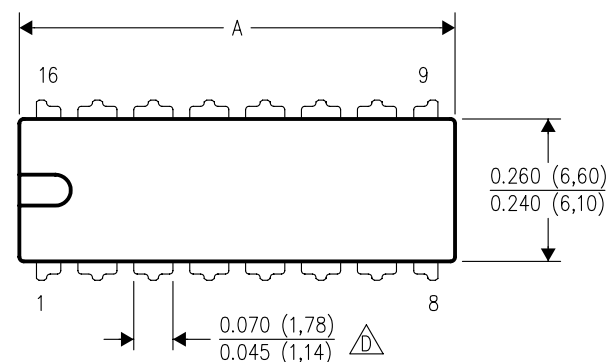


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

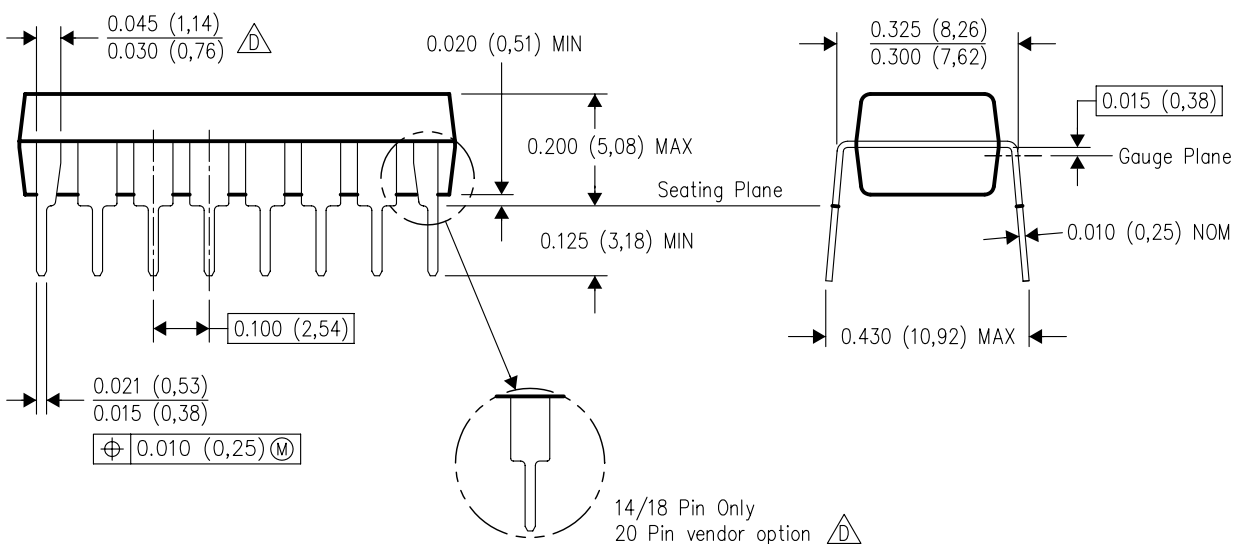
N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated