

SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B - APRIL 1982 - REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS109A	50	6
'AS109A	129	29

description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and \overline{K} inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and \overline{K} inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding \overline{K} and tying J high. They also can perform as D-type flip-flops if J and \overline{K} are tied together.

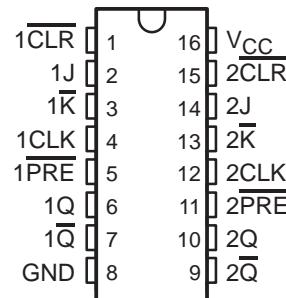
The SN54ALS109A and SN54AS109A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS109A and SN74AS109A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

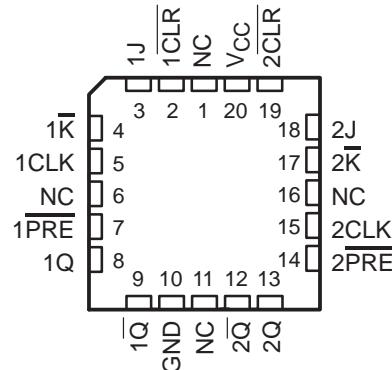
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	\overline{K}	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^{\dagger}	H^{\dagger}
H	H	\uparrow	L	L	L	H
H	H	\uparrow	H	L	Toggle	
H	H	\uparrow	L	H	Q0	\overline{Q}_0
H	H	\uparrow	H	H	H	L
H	H	L	X	X	Q0	\overline{Q}_0

[†]The output levels in this configuration are not specified to meet the minimum levels for V_{OH} if the lows at PRE and CLR are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.

SN54ALS109A, SN54AS109A . . . J PACKAGE
SN74ALS109A, SN74AS109A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS109A, SN54AS109A . . . FK PACKAGE
(TOP VIEW)

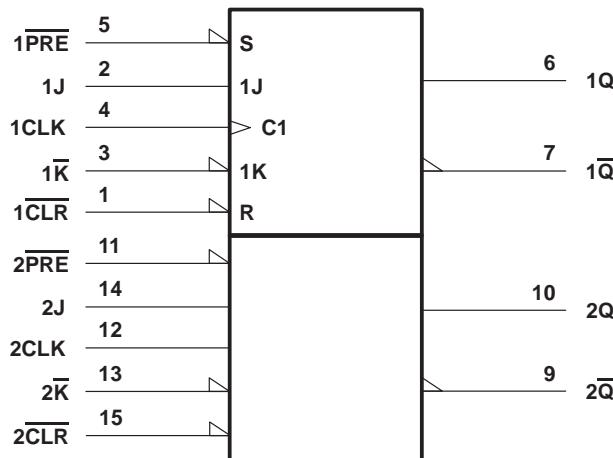


NC – No internal connection

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
I _{OH}	High-level output current				-0.4			-0.4	mA
I _{OL}	Low-level output current				4			8	mA
f _{clock}	Clock frequency		0	30	0	0	34	MHz	
t _W	Pulse duration	PRE or CLR low	15		15				ns
		CLK high	16.5		14.5				
		CLK low	16.5		14.5				
t _{su}	Setup time before CLK↑	Data	15		15				ns
		PRE or CLR inactive	10		10				
t _h	Hold time after CLK↑	Data	0		0				ns
T _A	Operating free-air temperature		-55	125	0	0	70	°C	

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS109A			SN74ALS109A			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _J = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA		0.25	0.4	0.25	0.4	V
		I _{OL} = 8 mA				0.35	0.5	
I _I	CLK, J, or \bar{K} PRE or CLR	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
				0.2		0.2		
I _{IH}	CLK, J, or \bar{K} PRE or CLR	V _{CC} = 5.5 V, V _I = 2.7 V		20		20		μ A
				40		40		
I _{IL}	CLK, J, or \bar{K} PRE or CLR	V _{CC} = 5.5 V, V _I = 0.4 V		-0.2		-0.2		mA
				-0.4		-0.4		
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-30	-112			mA
I _{CC}	V _{CC} = 5.5 V, See Note 1		2.4	4	2.4	4		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω , T _A = MIN to MAX§				UNIT	
			SN54ALS109A		SN74ALS109A			
			MIN	MAX	MIN	MAX		
f _{max}			30		34		MHz	
t _{PLH}	PRE or CLR	Q or \bar{Q}	3	17	3	13	ns	
			5	17	5	15		
t _{PHL}	CLK	Q or \bar{Q}	5	21	5	16	ns	
			5	20	5	18		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS109A			SN74AS109A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-2			-2	mA
I _{OL}	Low-level output current			20			20	mA
f _{clock} *	Clock frequency	0	90	0	105		105	MHz
t _w *	Pulse duration	PRE or CLR low	4		4			ns
		CLK high	4		4			
		CLK low	5.5		5.5			
t _{su} *	Setup time before CLK↑	Data	5.5		5.5			ns
		PRE or CLR inactive	2		2			
t _h *	Hold time after CLK↑	Data	0		0			ns
T _A	Operating free-air temperature	-55	125	0	70		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS109A			SN74AS109A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1	mA
I _{IH}	CLK, J, or \bar{K}			20			20	μ A
	PRE or CLR	V _{CC} = 5.5 V, V _I = 2.7 V		40			40	
I _{IL}	CLK, J, or \bar{K}			-0.5			-0.5	mA
	PRE or CLR	V _{CC} = 5.5 V, V _I = 0.4 V		-1.8			-1.8	
I _O §	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	V _{CC} = 5.5 V, See Note 1		11.5	17		11.5	17	mA

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54AS109A		SN74AS109A			
			MIN	MAX	MIN	MAX		
f_{max}^*			90	105			MHz	
t_{PLH}	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	2	9	2	8	ns	
t_{PHL}			3.5	11.5	3.5	10.5		
t_{PLH}	CLK	Q or \overline{Q}	2.5	10	2.5	9	ns	
t_{PHL}			3.5	10.5	3.5	9		

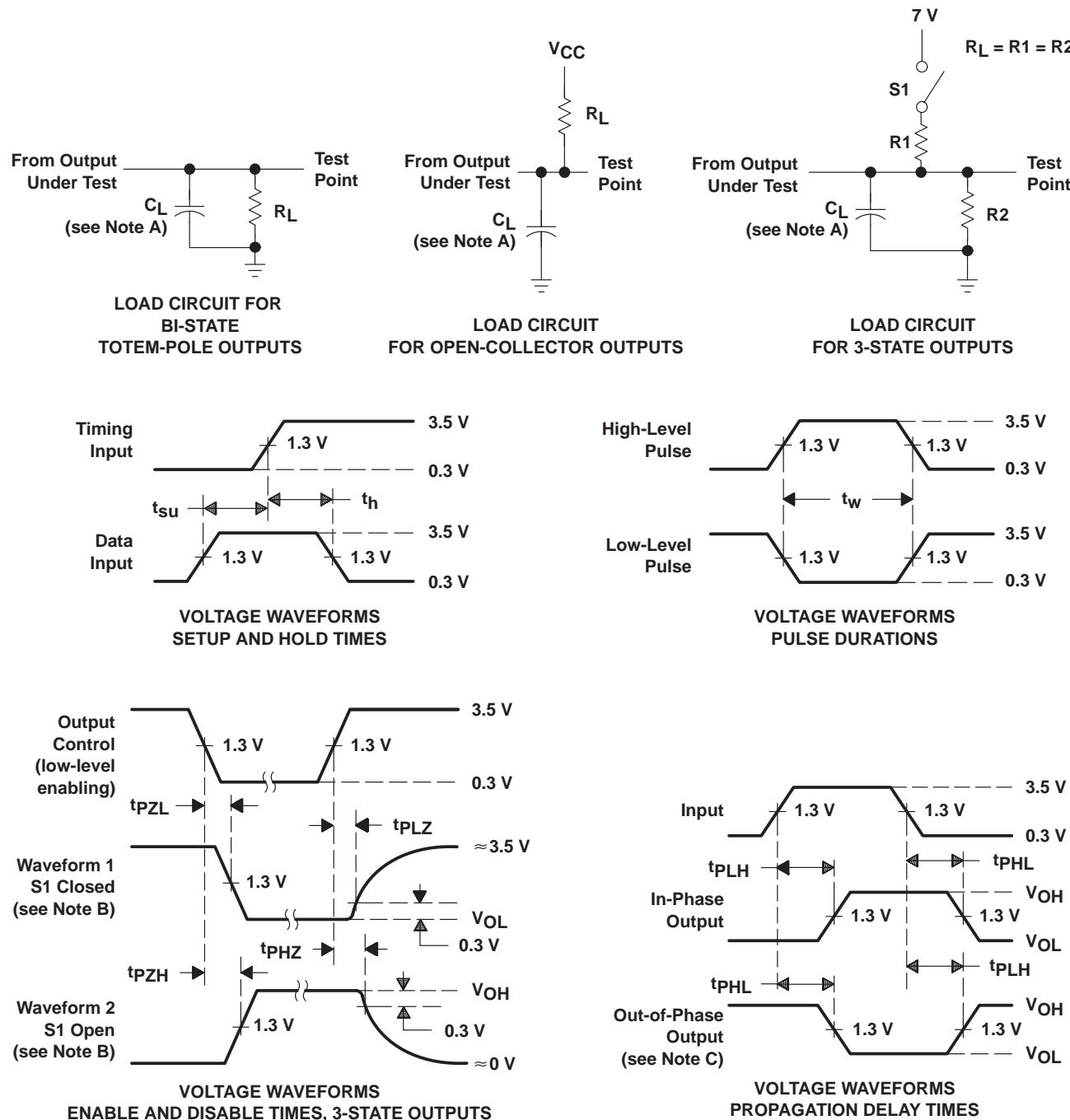
* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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WITH CLEAR AND PRESET**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
84000012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8400001EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
8400001FA	OBsolete	CFP	W	16		TBD	Call TI	Call TI
JM38510/37102B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/37102BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SN54ALS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SN54AS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SN74ALS109AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS109AN3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74ALS109ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS109ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS109ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS109ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS109ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS109ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS109AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54ALS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS109AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS109AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

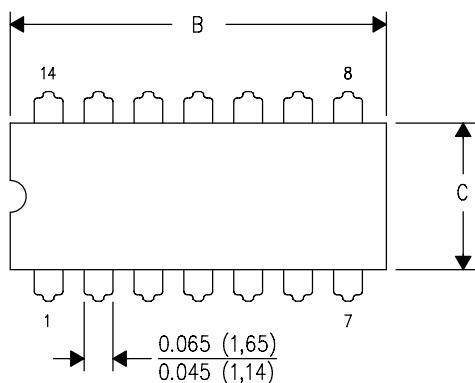
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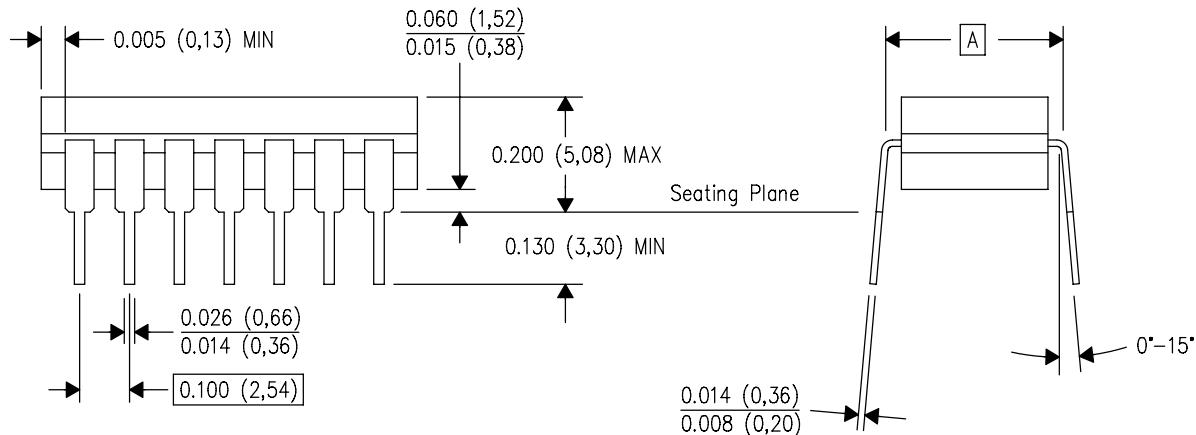
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

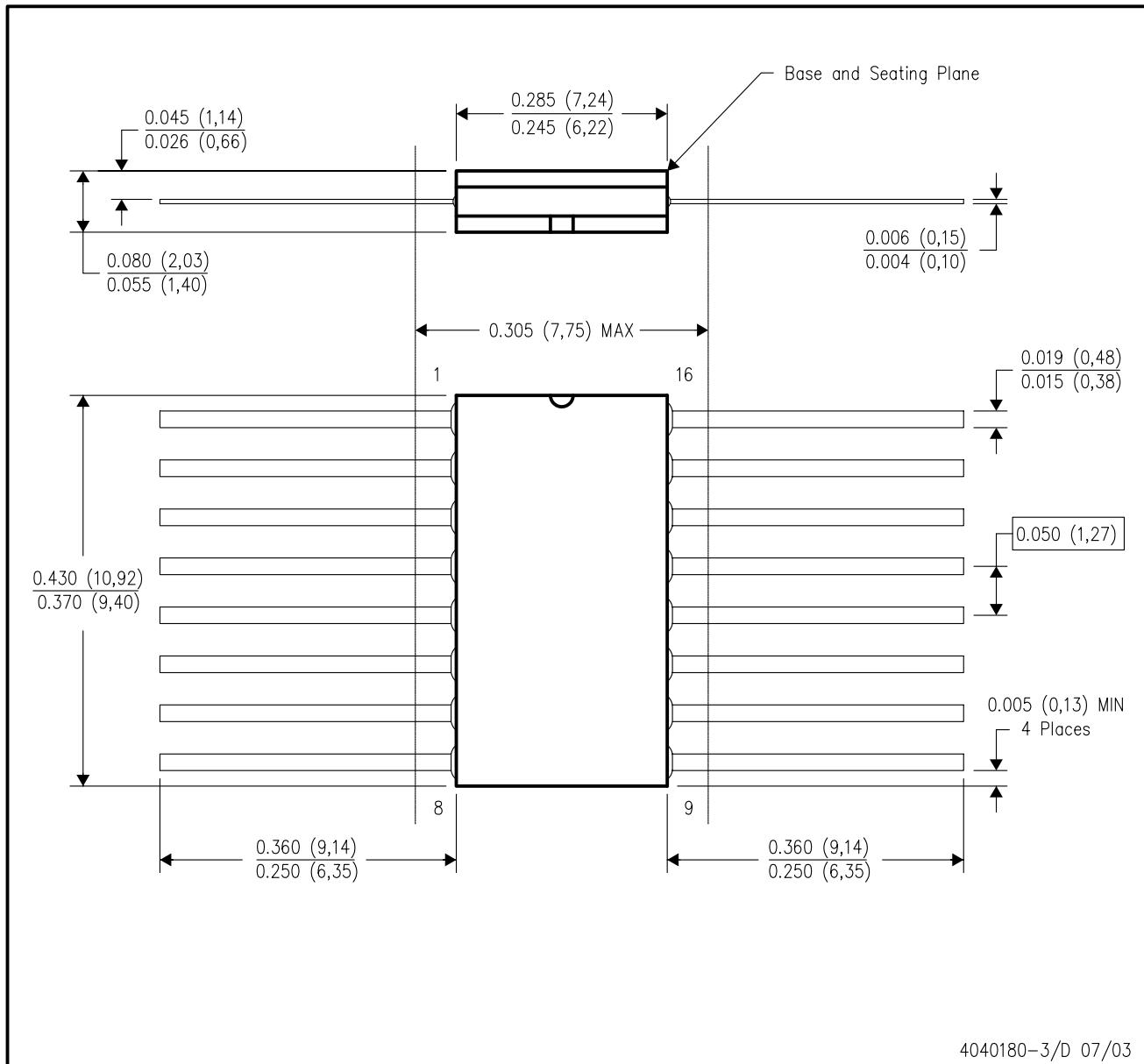


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



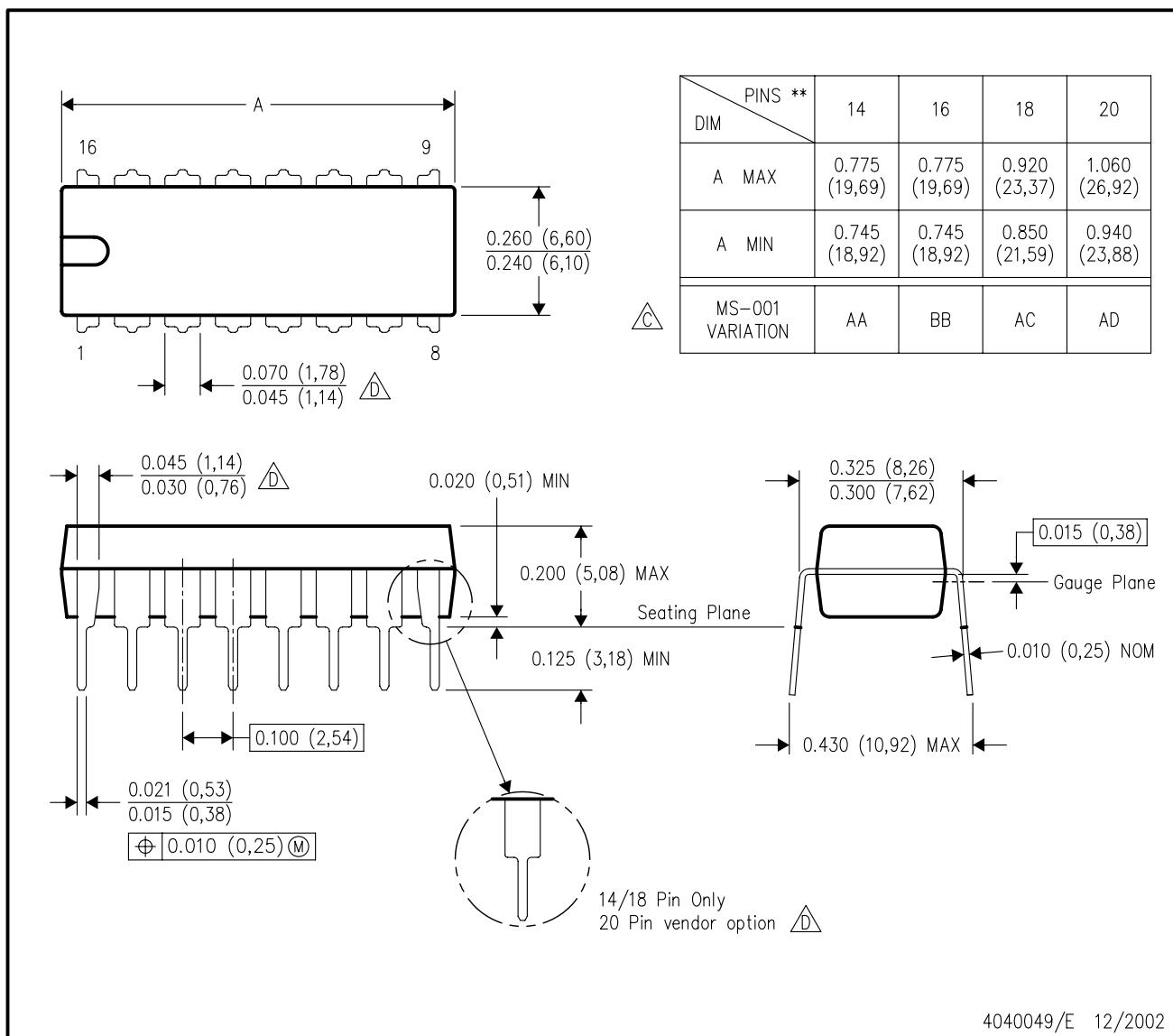
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MS-004

N (R-PDIP-T**)

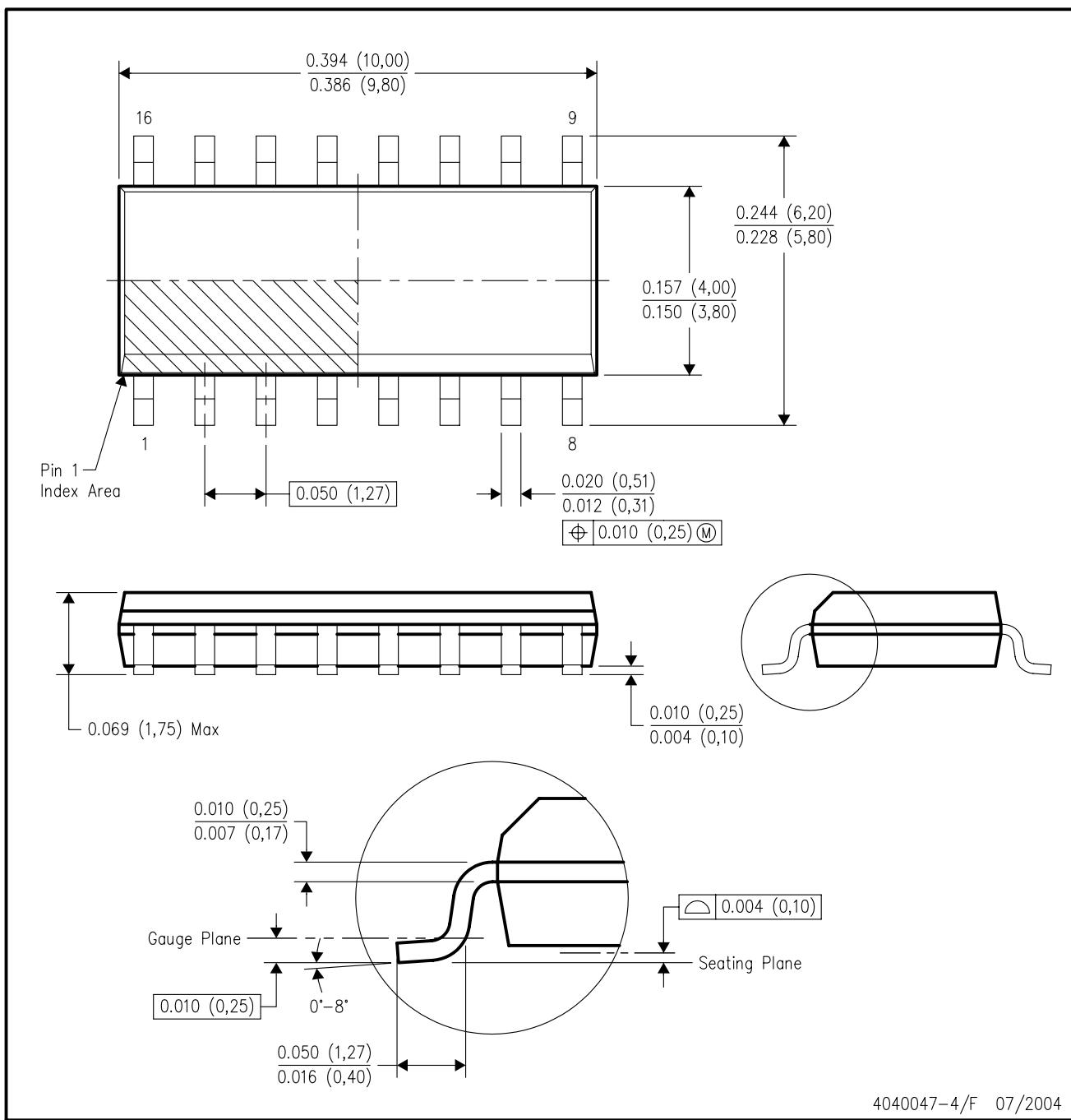
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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