iPOWIR™ TECHNOLOGY

High Frequency Synchronous Buck Optimized LGA Power Stage

Integrated Power Semiconductors, Driver IC, & Passives

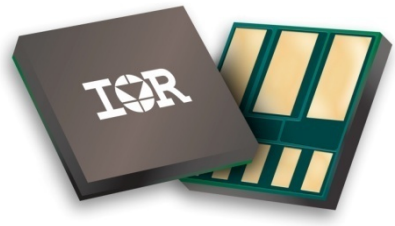
Features

- 40A Multiphase building block
- No de-rating up to T_{PCB} = 95ºC
- Optimized for low power loss
- Optimized for low EMI
- Bias supply range of 4.5V to 7.0V
- Operation up to 1.5MHz
- Bi-directional Current flow
- Under Voltage Lockout
- LGA interface
- 7.65mm x 7.65mm outline

Applications

- High Frequency, Low Profile DC-DC
- Multi-phase Architectures
- Low Duty Cycle, High Current solutions
- Microprocessor Power Supplies
- General DC/DC Converters

Package Description	Interface Connection	Standard Quantity	T & R Orientation
iP2005APbF	LGA	10	N/A
iP2005ATRPbF	LGA	2000	Figure 15

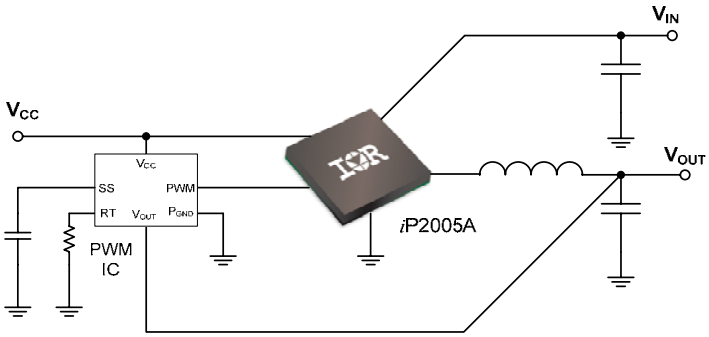


Description

The iP2005A is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 7.65mm x 7.65mm x 1.66mm power block. The additional components required for a complete multiphase converter are a PWM controller, the output inductors, and the input and output capacitors.

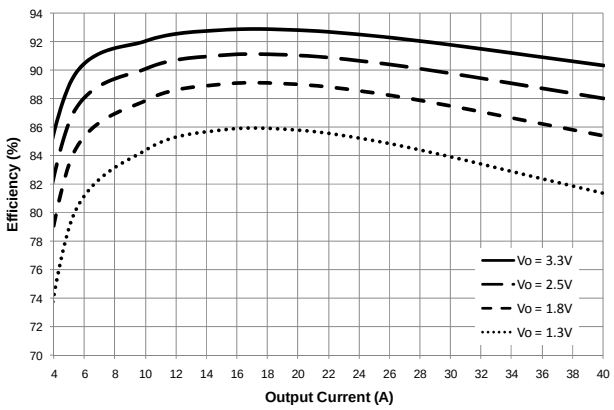
iPOWIR Technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer, and component selection.

Typical Application



iP2005A Product Efficiency

V_{IN} = 12V, F_{SW} = 1MHz, & T_{BLK} = 125ºC



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to P_{GND})

V_{IN} to P_{GND} ……..-0.5V to 16.5V
V_{DD} to P_{GND} ……-0.5V to 7.5V
CV_{CC} to P_{GND} ……...-0.5V to 7.5V
PWM to P_{GND} ……-0.5V to VDD + 0.5V (Note 1)
ENABLE to P_{GND} ……-0.5V to VDD + 0.5V (Note 1)
Storage Temperature ……..-60ºC to 150ºC
Block Temperature ……-40ºC to 150ºC (Note 2)
ESD Rating……...JEDEC, JESD22-A114 (HBM[4KV], Class 3A)
……JEDEC, JESD22-A115 (MM[400V], Class C)
MSL Rating……..……..3
Reflow Temperature ……..260ºC Peak

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those listed in the "Recommended Operating Conditions" section of this specification is not implied.

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Voltage (V_{DD})	4.5	-	7.0	V	
Input Voltage (V_{IN})	6.5	-	13.2	V	
Output Voltage (V_{OUT})	-	-	5.5	V	
Output Current (I_{OUT})	-	-	40	A	
Switching Frequency	250	-	1500	kHz	
On Time Duty Cycle	-	-	85	%	
Minimum V_{SW} On Time	60	-	-	ns	V_{DD} = 5.0V, V_{IN} = 12V
Block Temperature (T_{BLK})	-40	-	125	ºC	(Note 2)

Electrical Specifications

These specifications apply for T_{BLK} = 0ºC to 125ºC and V_{DD} = 5.0V unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
P_{Loss}					
Power Block Losses	-	9.3	11.1	W	V_{IN} = 12V, V_{DD} = 5.0V, V_{OUT} = 1.3V, I_{OUT} = 40A, F_{SW} = 1MHz, L_{OUT} = 0.3uH, T_{BLK} = 25ºC (Note 3)
V_{DD}					
Supply Current (Stand By) (I_{Q-VDD})	-	2.2	3	mA	V_{DD} = 5.0, ENABLE = 0V
Supply Current (Operating)	-	50	65	mA	V_{IN} = 12V, ENABLE = V_{DD} = 5V, F_{SW} = 1MHz, 10% DC
CV_{CC} (LDO Output)					
Output Voltage	5.5	6.0	6.75	V	
Output Current	80	-	-	mA	
Output Capacitor	1.0	-	-	µF	Ceramic, X5R, 16V
Power-On Reset (POR)					
V_{DD} Rising	3.7	4.1	4.5	V	
Hysteresis	140	185	230	mV	V_{DD} Rising & Falling
CVCC Rising	4.2	4.6	5.0	V	
Hysteresis	165	220	275	mV	CV_{CC} Rising & Falling
ENABLE INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	Schmitt Trigger Input V_{DD} = POR to 7.0V
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull-down Impedance	-	100	-	kΩ	
Rising Propagation Delay (T_{PDH})	-	40	-	ns	
Falling Propagation Delay (T_{PDL})	-	75	-	ns	

Electrical Specifications (continued)

These specifications apply for T_{BLK} = 0ºC to 125ºC and V_{DD} = 5.0V unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
PWM INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	Schmitt Trigger Input V_{DD} = POR to 7.0V (Note 4)
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull-down impedance	-	100	-	kΩ	
Rising Propagation Delay (T_{PDH})	-	60	-	ns	
Falling Propagation Delay (T_{PDL})	-	30	-	ns	

Notes:

1. Must not exceed 7.5V
2. Block Temperature (T_{BLK}) is defined as any Die temperature within the package
3. Measurement made with six 10µF (TDK C3225X5R1C106KT or equivalent) ceramic capacitors placed across VIN to PGND pins (see Figure 8)
4. Not associated with rise and fall times. Does not affect Power Loss

Power Loss Curve

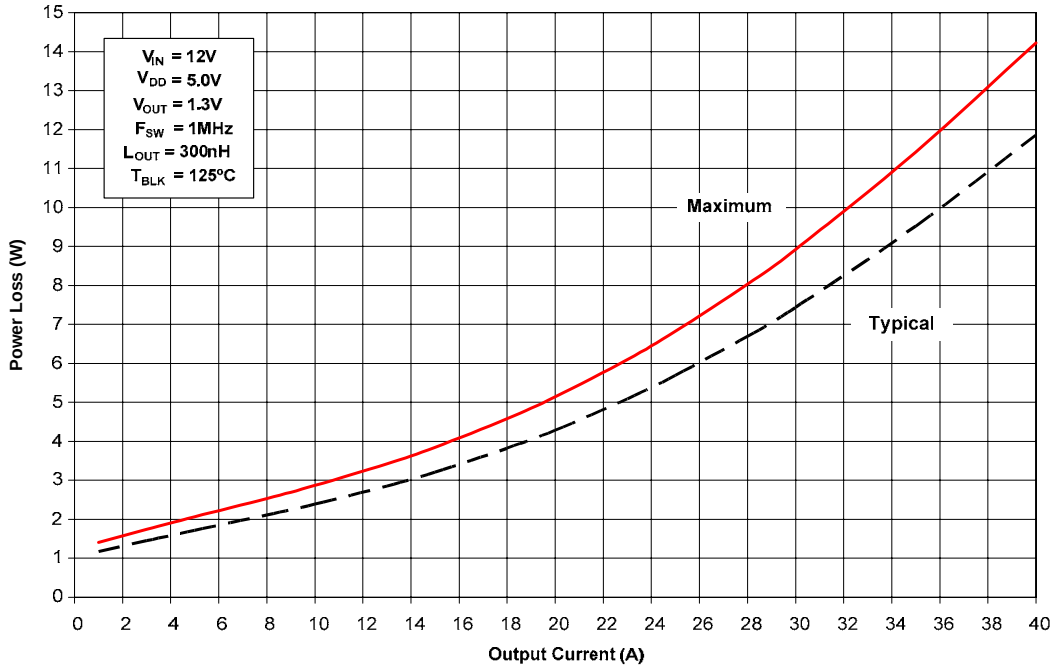


Figure 1 Power Loss Curve

SOA Curve

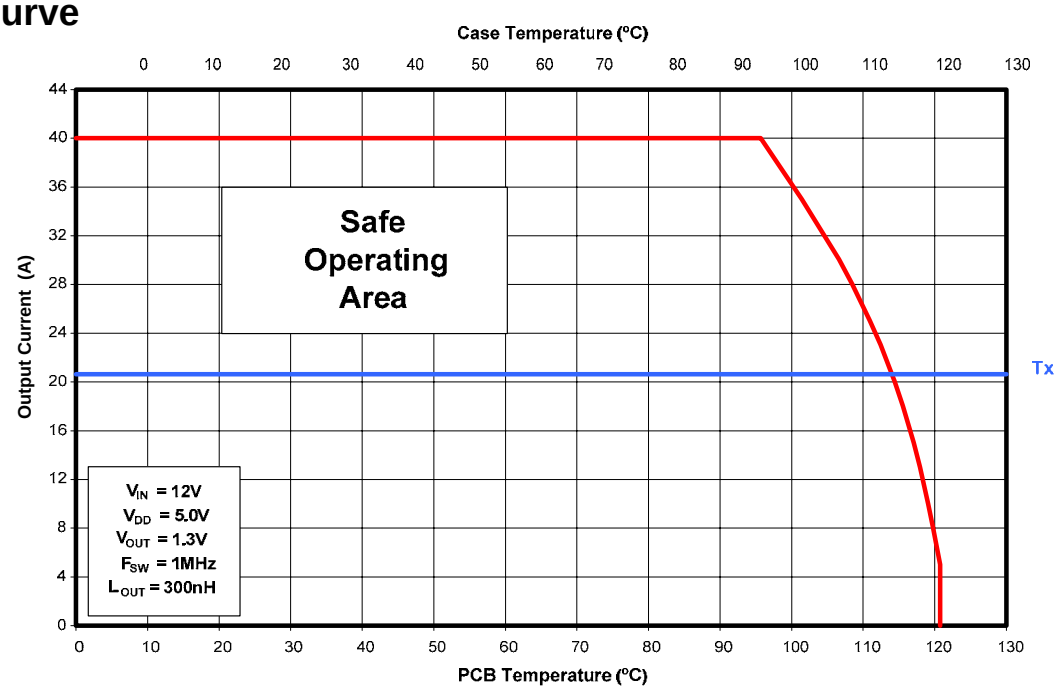


Figure 2 Safe Operating Area Curve

Typical Performance Curves

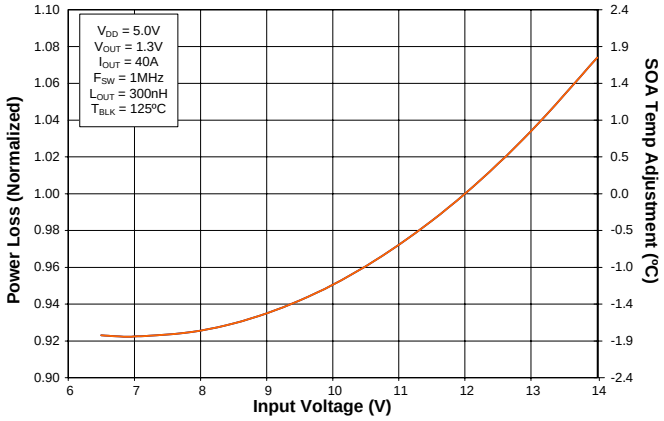


Figure 3 Normalized Power Loss vs. Input Voltage

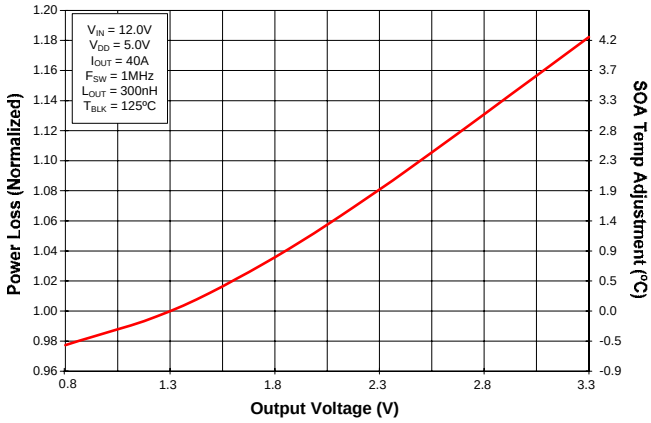


Figure 4 Normalized Power Loss vs. Output Voltage

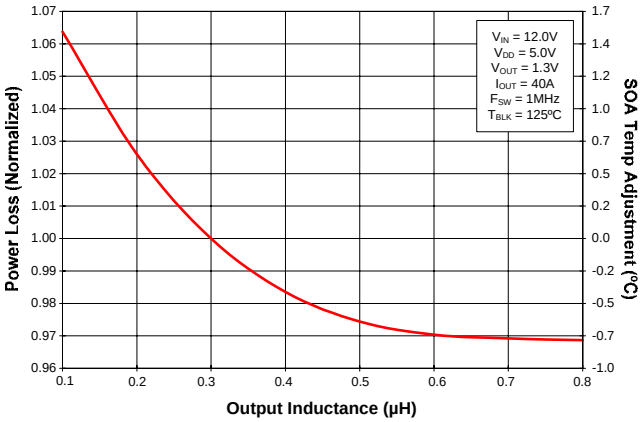


Figure 5 Normalized Power Loss vs. Inductance

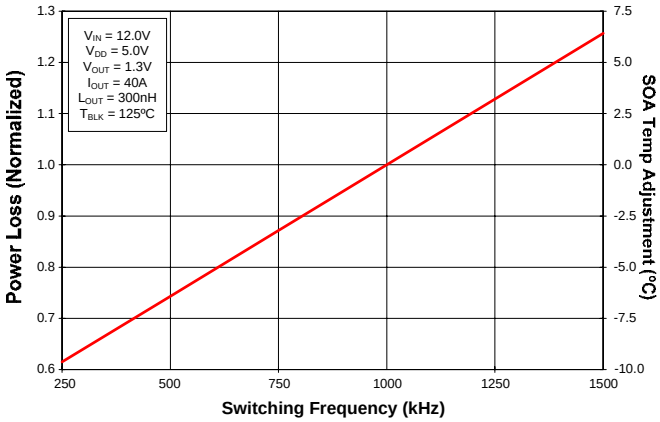


Figure 6 Normalized Power Loss vs. Switching Frequency

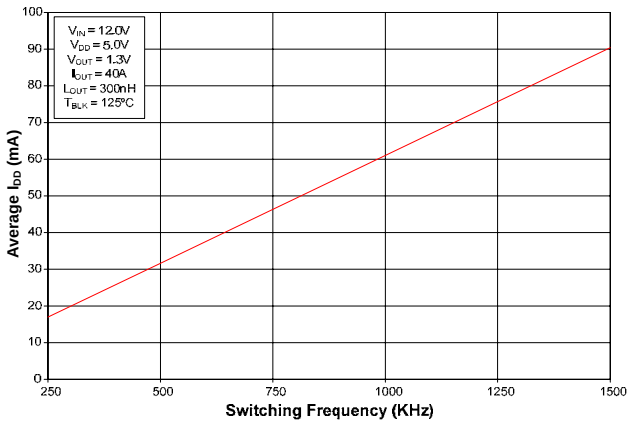


Figure 7 V_{DD} Supply Current vs. Switching Frequency

$P_{IN} = V_{IN}$ Average **x** I_{IN} Average

$P_{DD} = V_{DD}$ Average **x** I_{DD} Average

$P_{OUT} = V_{OUT}$ Average **x** I_{OUT} Average

$P_{LOSS} = (P_{IN} + P_{DD}) - P_{OUT}$

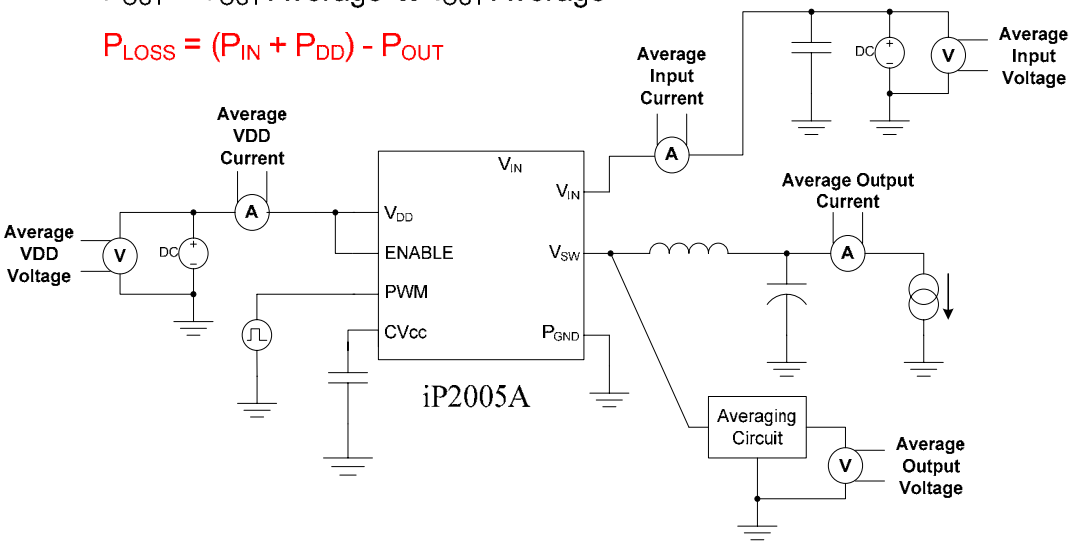


Figure 8 Power Loss Test Circuit

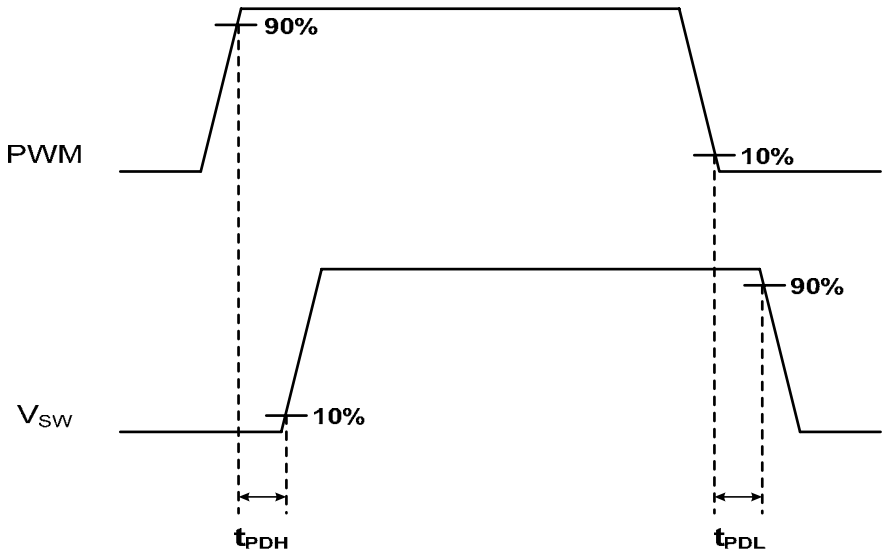


Figure 9 Timing Diagram

Applying the Safe Operating Area (SOA) Curve

The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case. Please refer to International Rectifier Application Note AN1047 for further details on using this SOA curve in your thermal environment.

Procedure

1. Calculate (based on estimated Power Loss) or measure the Case temperature on the device and the Board temperature near the device (1mm from the edge).
2. Draw a line from Case Temperature axis to the PCB Temperature axis.
3. Draw a vertical line from the T_X axis intercept to the SOA curve.
4. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.

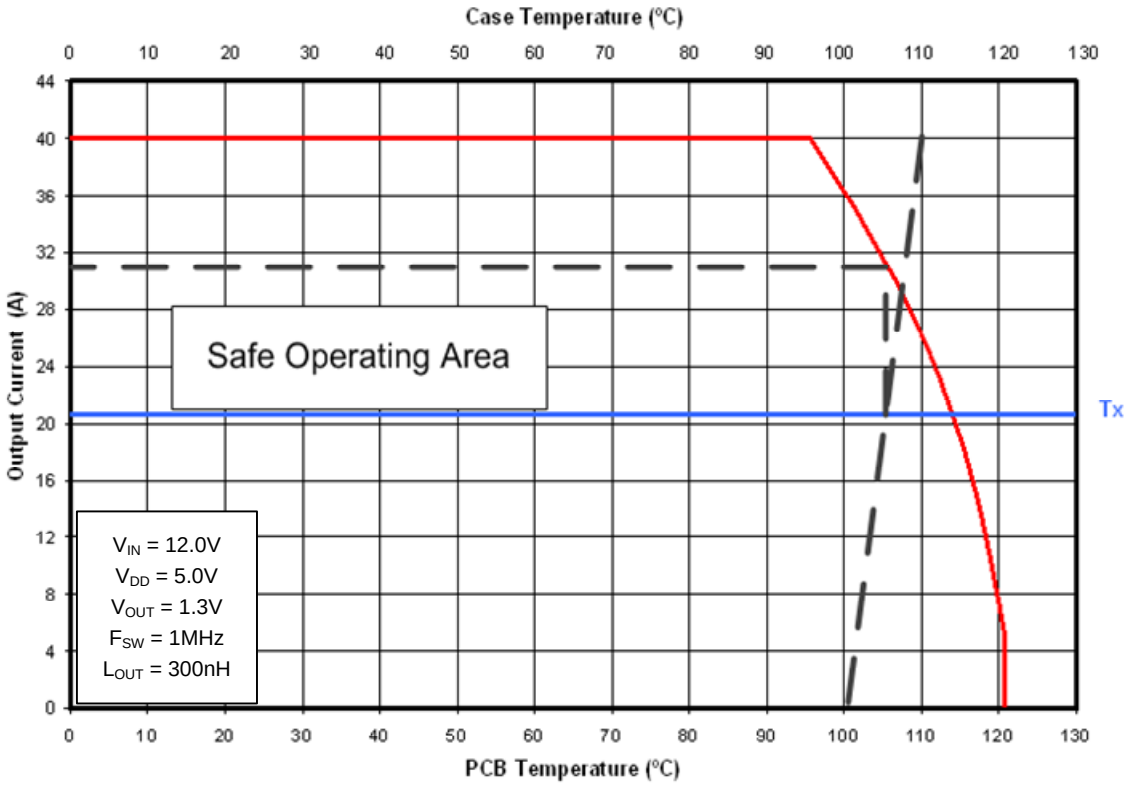


Figure 10 SOA Example, Continuous current ≈ 31A for T_{PCB} = 100ºC & T_{CASE} = 110ºC

Calculating Power Loss and SOA for Different Operating Conditions

To calculate Power Loss for a given set of operation conditions, the following procedure should be followed:

Power Loss Procedure

1.Determine the maximum current for each iP2005A and obtain the maximum power loss from Figure 1
2.Use the normalized curves to obtain power loss values that match the operating conditions in the application
3.The maximum power loss under the application conditions is then the product of the power loss from Figure 1 and the normalized values.

To calculate the Safe Operating Area (SOA) for a given set of operating conditions, the following procedure should be followed:

SOA Procedure

1.Determine the maximum PCB and CASE temperature at the maximum operating current for each iP2005A
2.Use the normalized curves to obtain SOA temperature adjustments that match the operating conditions in the application
3.Then, add the sum of the SOA temperature adjustments to the T_X axis intercept in Figure 2

Design Example

Operating Conditions:

Output Current = 30A	Input Voltage = 10V	Output Voltage = 1.3V
Switching Freq = 750kHz	Inductor = 0.2µH	Drive Voltage (V_{DD}) = 5V

Calculating Maximum Power Loss:

(Figure 1)	Maximum power loss = 9.0W
(Figure 3)	Normalized power loss for input voltage ≈ 0.95
(Figure 4)	Normalized power loss for output voltage ≈ 1.0
(Figure 5)	Normalized power loss for output inductor ≈ 1.026
(Figure 6)	Normalized power loss for switch frequency ≈ 0.87

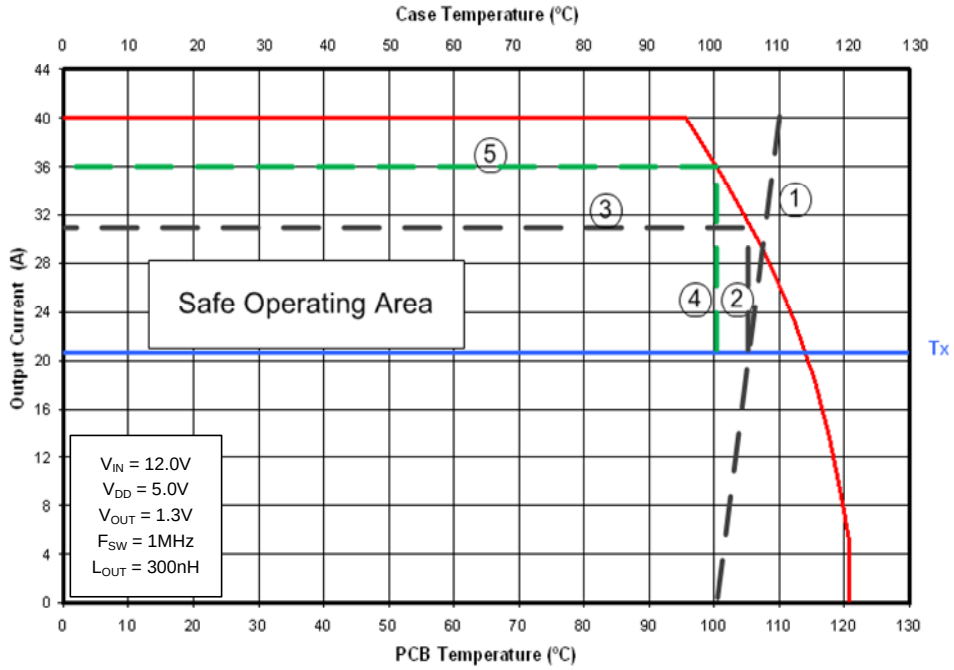
Calculated Maximum Power Loss ≈ 9.0W x 0.95 x 1.0 x 1.026 x 0.87 ≈ 7.63W

Calculating SOA Temperature:

(Figure 3) SOA temperature adjustment for input voltage ≈ -1.2ºC
(Figure 4) SOA temperature adjustment for output voltage ≈ 0.0ºC
(Figure 5) SOA temperature adjustment for output inductor ≈ 0.6 ºC
(Figure 6) SOA temperature adjustment for switch frequency ≈ -3.5 ºC

T_X axis intercept adjustment ≈ -1.2 ºC + 0.0 ºC + 0.6 ºC – 3.5 ºC ≈ -4.1 ºC

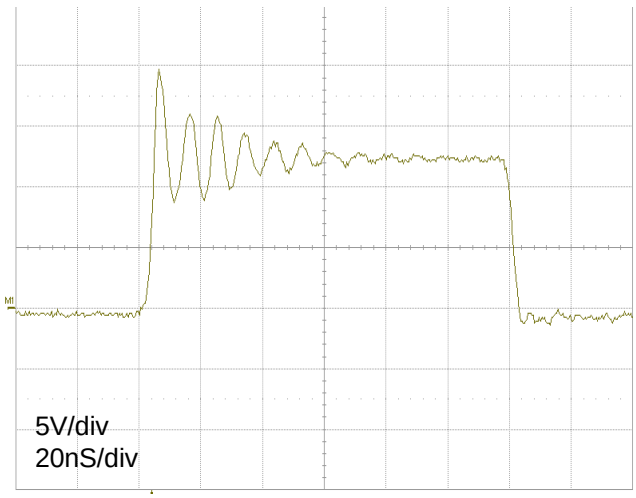
Assuming T_{PCB} = 100ºC & T_{CASE} = 110ºC
The following example shows how the SOA current is adjusted for T_X decrease of 4.1ºC



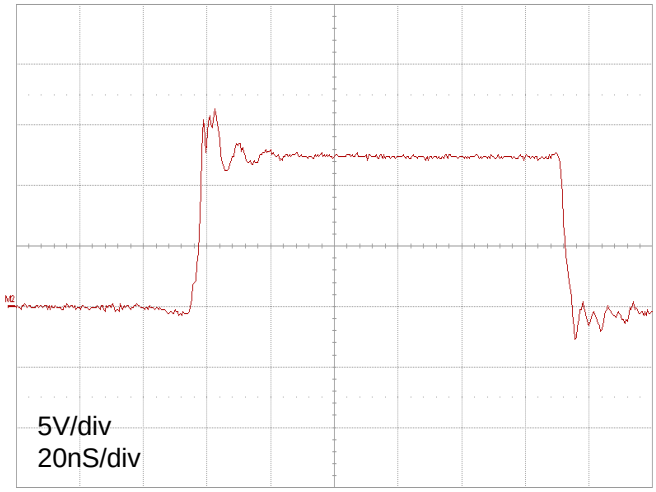
1. Draw a line from Case Temperature axis to the PCB Temperature axis.
2. Draw a vertical line from the T_X axis intercept to the SOA curve.
3. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.
4. Draw a new vertical line from the T_X axis by adding or subtracting the SOA adjustment temperature from the original T_X intercept point.
5. Draw a horizontal line from the intersection of the new vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the new SOA continuous current.

The SOA adjustment indicates the part is still allowed to run at a continuous current of 36A.

Optimized EMI Feature



Vsw of iP2003A



Vsw of iP2005A

The iP2005A is designed for low Electromagnetic Interference (EMI) which minimizes power loss and space, and simplifies system design by eliminating the need for external snubber circuits. These benefits are achieved by optimizing the internal component layout, integrating bypass filters and implementing active clamp circuitry as a means of reducing switching node voltage ringing; which is one of main sources of EMI. The figures above show waveform comparisons of switching node voltages of the previous generation iP2003A product and iP2005A under equivalent operation conditions.

Internal Block Diagram

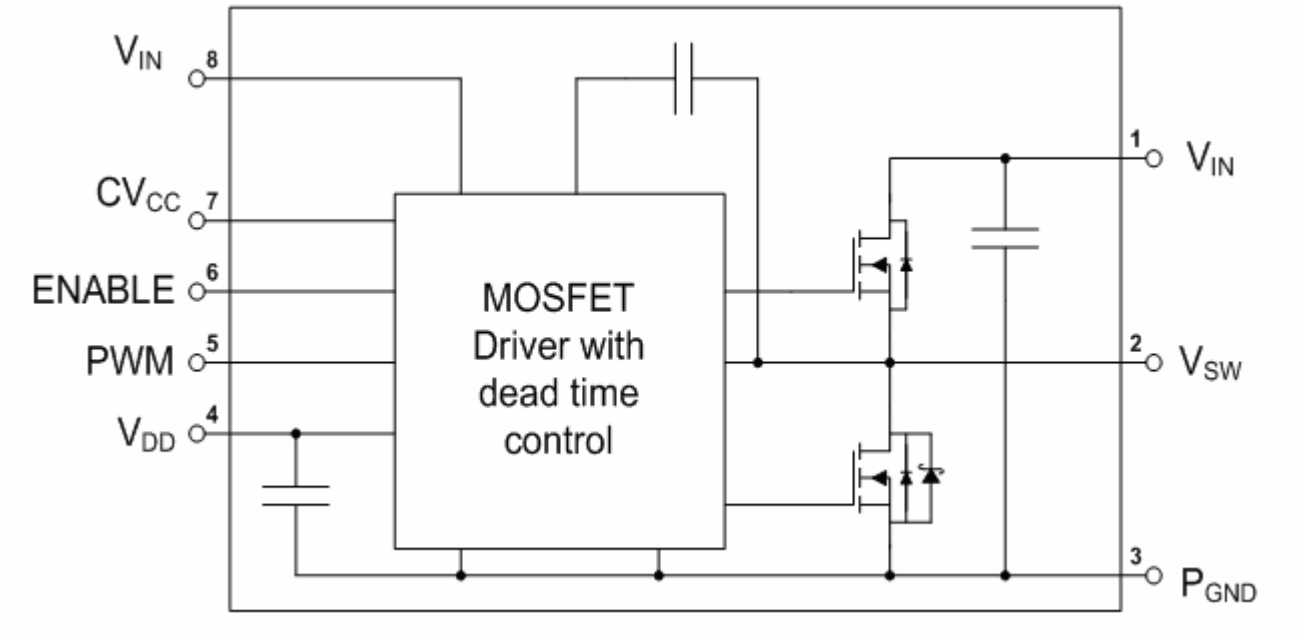


Figure 11 Internal Block Diagram

Pin Description

Pin Number	Pin Name	Description
1, 8	V_{IN}	Input voltage pin. Connect input capacitors close to this pin.
2	Vsw	Voltage Switching Node – pin connection to the output inductor.
3	P_{GND}	Power Ground
4	V_{DD}	Supply voltage to internal circuitry.
5	PWM	TTL level input to MOSFET drivers. When PWM is HIGH, the Control FET is on and the Sync FET is off. When PWM is LOW, the Sync FET is on and the Control FET is off.
6	ENABLE	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the Control and Synchronous FETs are turned off.
7	CV_{CC}	Output of internal regulator. Attached a minimum of 1.0µF capacitance from this pin to PGND. Recommended to use 16V, X5R, Ceramic type capacitor.

Recommended PCB Layout

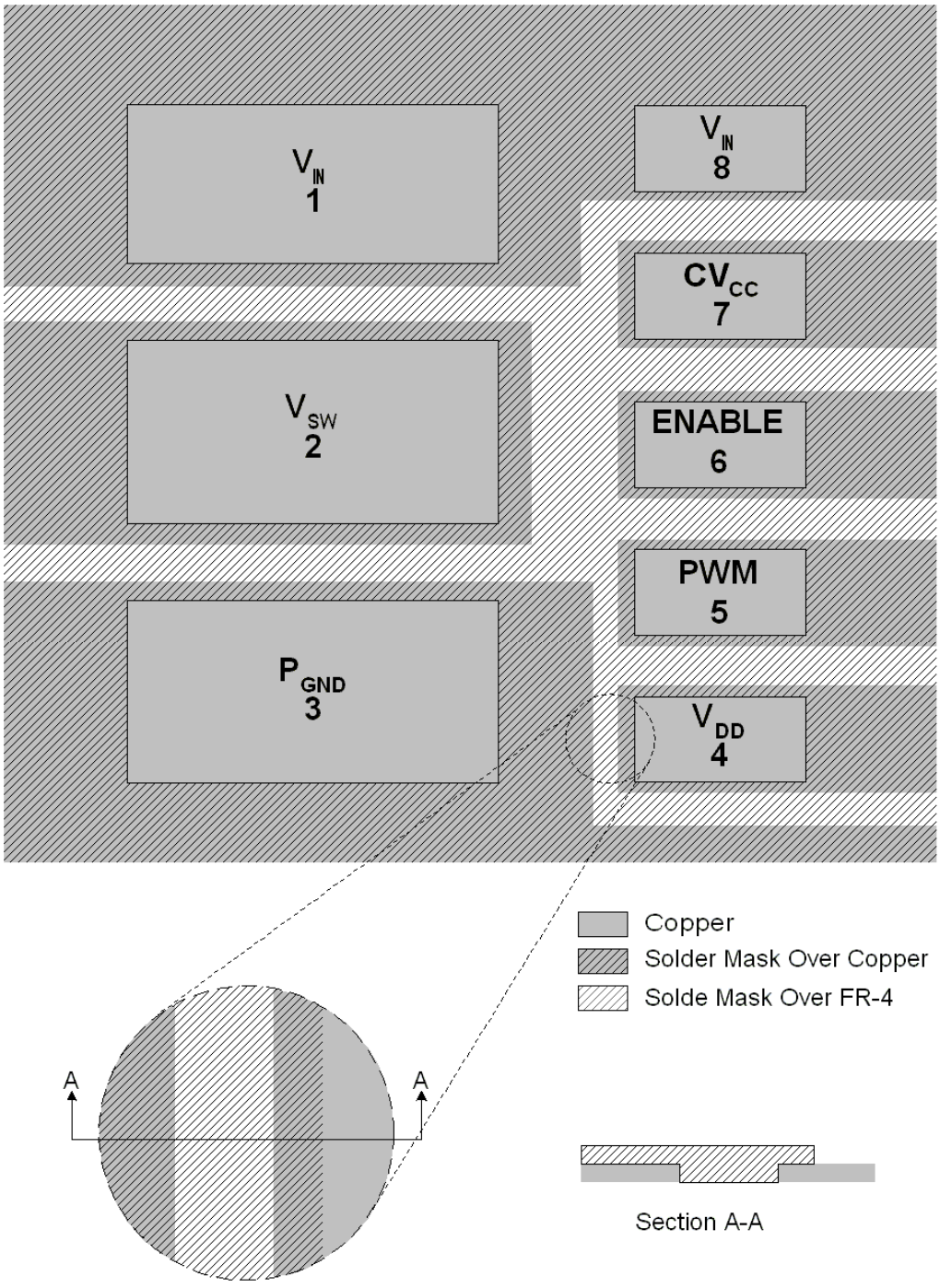


Figure 12 Top copper and Solder-mask layer of PCB layout

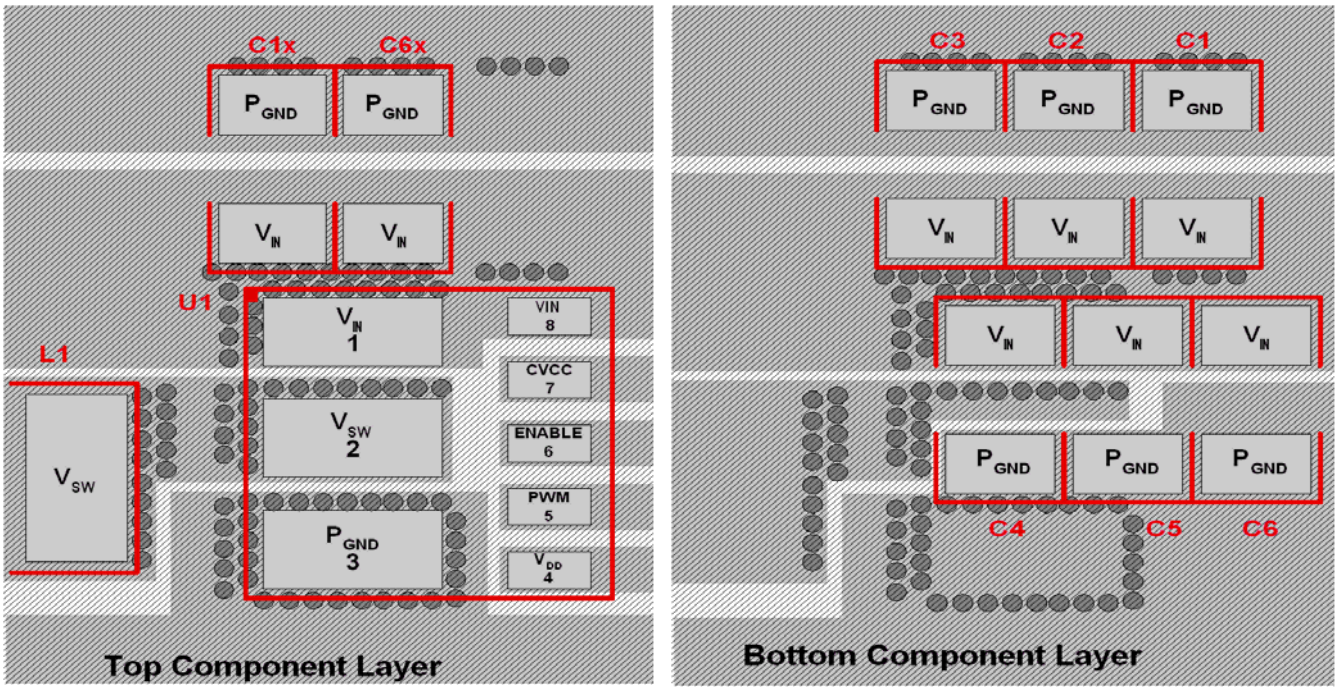


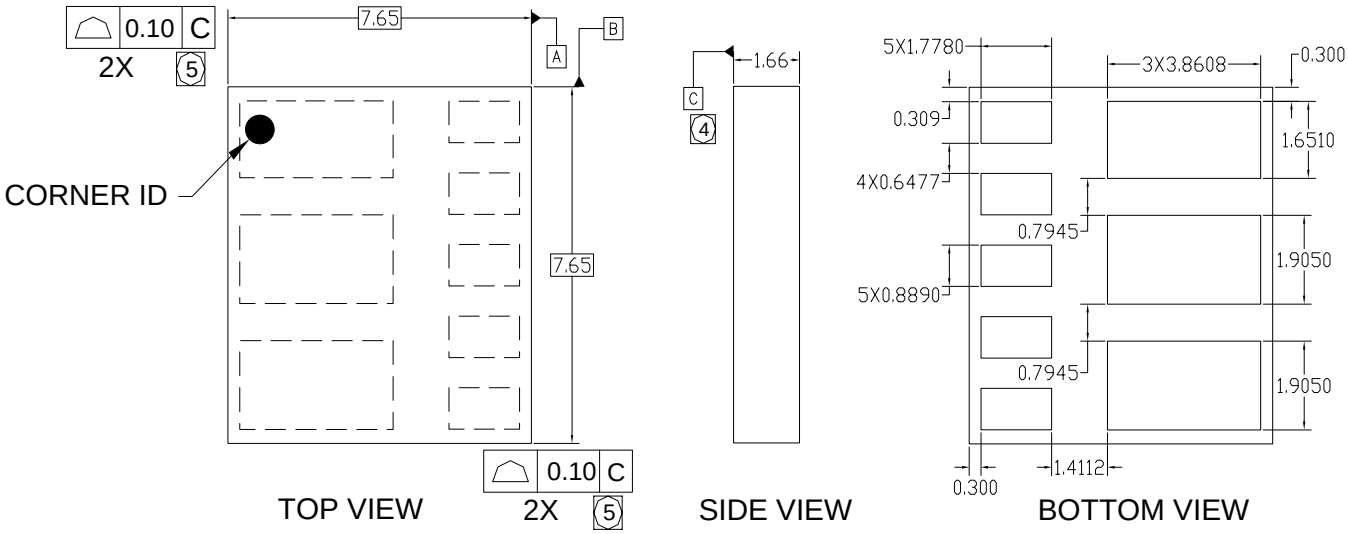
Figure 13 Top & Bottom Component and Via Placement (Topside, Transparent view down)

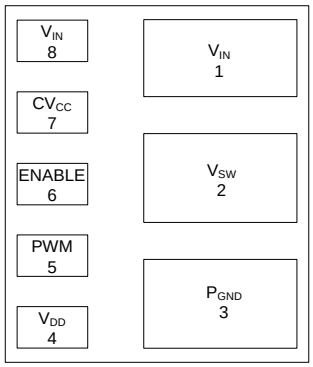
PCB Layout Guidelines

The following guidelines are recommended to reduce the parasitic values and optimize overall performance.

- All pads on the iP2005A footprint design need to be Solder-mask defined (see Figure 12). Also refer to International Rectifier application notes AN1028 and AN1029 for further footprint design guidance.
- Place as many vias around the Power pads (V_{IN}, V_{SW}, and P_{GND}) for both electrical and optimal thermal performance.
- A minimum of six 10µF, X5R, 16V ceramic capacitors per iP2005A are needed for greater than 30A operation. This will result in the lowest loss due to input capacitor ESR.
- Placement of the ceramic input capacitors is critical to optimize switching performance. In cases where there is a heatsink on the case of iP2005A, place all six ceramic capacitors right underneath the iP2005A footprint (see Figure 13 Bottom Component Layer). In cases where there is not heatsink, C1 and C6 on the bottom layer may be moved to the C1x and C6x locations (respectively) on the top component layer (see Figure 13 Top Component Layer). In both cases, C2 – C5 need to be placed right underneath the iP2005A PCB footprint.
- Dedicate at least two layer to for P_{GND} only
- Duplicate the Power Nodes on multiple layers (refer to AN1029).

Mechanical Outline Drawing





BOTTOM VIEW
ELECTRICAL I/O

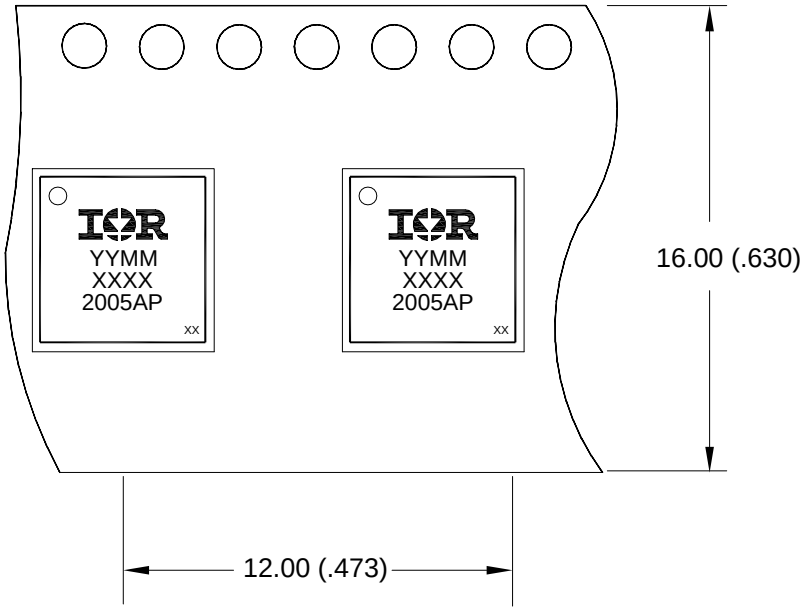
Notes:
1. Dimensions & Tolerances per ASME Y14.5M – 1994
2. Dimensions are shown in Millimeters
3. Tolerances are:
   .XX = +/- 0.1
   .XXX = +/- 0.025
   .XXXX = +/- 0.01

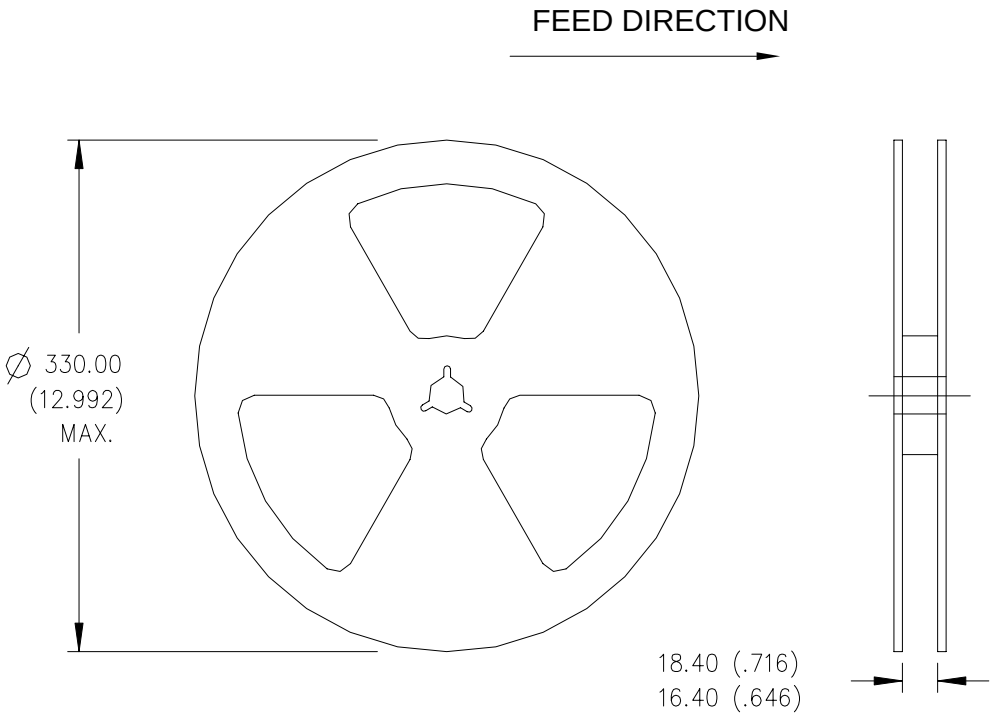
④ Primary datum C is seating plane
⑤ Bilateral tolerance zone is applied to each side of package body

Layout Notes:
1. Land patterns on user's PCB should be an identical mirror image of the pattern shown in bottom view
2. Lands should be solder mask defined
3. All I/O pads on this product are metal finish with flash gold

Figure 14 Mechanical Outline Drawing

Tape and Reel Information



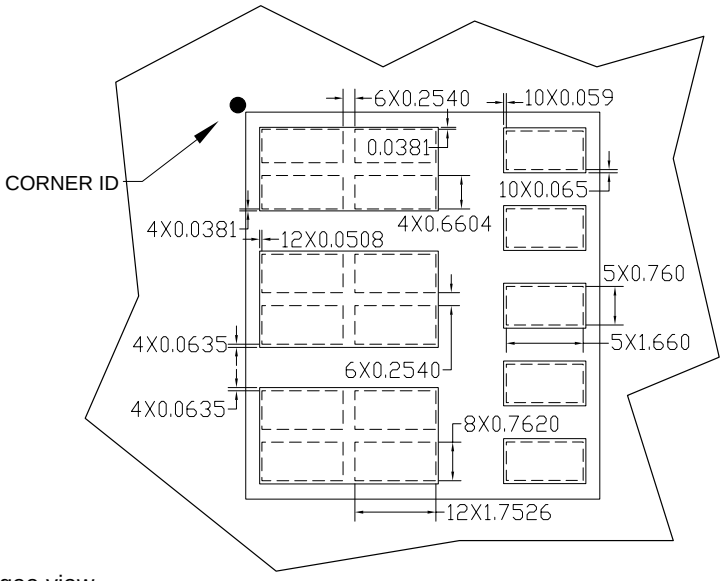


NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Figure 15 Tape and Reel Information

Recommended Solder Paste Stencil Design



Notes:
1.This view is stencil squeegee view
2.Dimensions are shown in millimeters
3.This opening is based on using 150 micron thick stencil. If using a different thickness stencil, this opening needs to be adjusted accordingly.
4.Dashed lines show stencil openings. Solid lines show PCB pad openings.
5.The recommended reflow peak temperature is 260ºC. The total furnace time is approximately 5 minutes with approximately 10 seconds at peak temperature.

Figure 16 Solder Paste Stencil Design

Part Marking

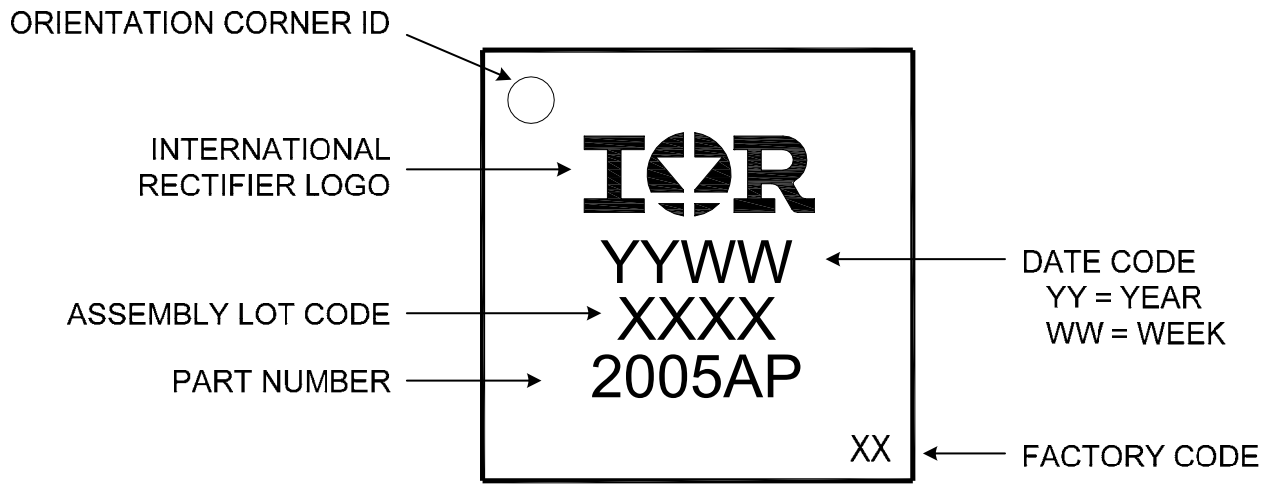


Figure 17 Part Marking

International
IOR Rectifier

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TAC Fax: (310) 252-7903

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