# LatticeECP2/M Family Data Sheet

DS1006 Version 04.1, September 2013

# LatticeECP2/M Family Data Sheet Introduction

July 2012 Data Sheet DS1006

## Features

- **High Logic Density for System Integration**
  - 6K to 95K LUTs
  - 90 to 583 I/Os
- **Embedded SERDES (LatticeECP2M Only)**
  - Data Rates 250 Mbps to 3.125 Gbps
  - Up to 16 channels per device
    PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.
- **sysDSP™ Block**
  - 3 to 42 blocks for high performance multiply and accumulate
  - Each block supports
    - One 36x36, four 18x18 or eight 9x9 multipliers
- **Flexible Memory Resources**
  - 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
    - 18Kbit block
    - Single, pseudo dual and true dual port
    - Byte Enable Mode support
  - 12K to 202Kbits distributed RAM
    - Single port and pseudo dual port
- **sysCLOCK Analog PLLs and DLLs**
  - Two GPLLs and up to six SPLLs per device
    - Clock multiply, divide, phase & delay adjust
    - Dynamic PLL adjustment
  - Two general purpose DLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - Source synchronous standards support
    - SPI4.2, SFI4 (DDR Mode), XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR and DDR2 memory support
    - DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
  - Dedicated DQS support
- **Programmable sysI/O™ Buffer Supports Wide Range Of Interfaces**
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 3/2/18 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL
- **Flexible Device Configuration**
  - 1149.1 Boundary Scan compliant
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual boot images supported
  - TransFR™ I/O for simple field updates
  - Soft Error Detect macro embedded
- **Optional Bitstream Encryption (LatticeECP2/M "S" Versions Only)**
- **System Level Support**
  - ispTRACY™ internal logic analyzer capability
  - On-chip oscillator for initialization & general use
  - 1.2V power supply

*Table 1-1. LatticeECP2 (Including "S-Series") Family Selection*

| Device | ECP2-6 | ECP2-12 | ECP2-20 | ECP2-35 | ECP2-50 | ECP2-70 |
|---|---|---|---|---|---|---|
| LUTs (K) | 6 | 12 | 21 | 32 | 48 | 68 |
| Distributed RAM (Kbits) | 12 | 24 | 42 | 64 | 96 | 136 |
| EBR SRAM (Kbits) | 55 | 221 | 276 | 332 | 387 | 1032 |
| EBR SRAM Blocks | 3 | 12 | 15 | 18 | 21 | 60 |
| sysDSP Blocks | 3 | 6 | 7 | 8 | 18 | 22 |
| 18x18 Multipliers | 12 | 24 | 28 | 32 | 72 | 88 |
| GPLL + SPLL + DLL | 2+0+2 | 2+0+2 | 2+0+2 | 2+0+2 | 2+2+2 | 2+4+2 |
| Maximum Available I/O | 190 | 297 | 402 | 450 | 500 | 583 |
| **Packages and I/O Combinations** | | | | | | |
| 144-pin TQFP (20 x 20 mm) | 90 | 93 | | | | |
| 208-pin PQFP (28 x 28 mm) | | 131 | 131 | | | |
| 256-ball fpBGA (17 x 17 mm) | 190 | 193 | 193 | | | |
| 484-ball fpBGA (23 x 23 mm) | | 297 | 331 | 331 | 339 | |
| 672-ball fpBGA (27 x 27 mm) | | | 402 | 450 | 500 | 500 |
| 900-ball fpBGA (31 x 31 mm) | | | | | | 583 |

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*Table 1-2. LatticeECP2M (Including "S-Series") Family Selection*

| Device | ECP2M20 | ECP2M35 | ECP2M50 | ECP2M70 | ECP2M100 |
|---|---|---|---|---|---|
| LUTs (K) | 19 | 34 | 48 | 67 | 95 |
| sysMEM Blocks (18kb) | 66 | 114 | 225 | 246 | 288 |
| Embedded Memory (Kbits) | 1217 | 2101 | 4147 | 4534 | 5308 |
| Distributed Memory (Kbits) | 41 | 71 | 101 | 145 | 202 |
| sysDSP Blocks | 6 | 8 | 22 | 24 | 42 |
| 18x18 Multipliers | 24 | 32 | 88 | 96 | 168 |
| GPLL+SPLL+DLL | 2+6+2 | 2+6+2 | 2+6+2 | 2+6+2 | 2+6+2 |
| Maximum Available I/O | 304 | 410 | 410 | 436 | 520 |
| **Packages and SERDES / I/O Combinations** | | | | | |
| 256-ball fpBGA (17 x 17 mm) | 4 / 140 | 4 / 140 | | | |
| 484-ball fpBGA (23 x 23 mm) | 4 / 304 | 4 / 303 | 4 / 270 | | |
| 672-ball fpBGA (27 x 27 mm) | | 4 / 410 | 8 / 372 | | |
| 900-ball fpBGA (31 x 31 mm) | | | 8 / 410 | 16 / 416 | 16 / 416 |
| 1152-ball fpBGA (35 x 35 mm) | | | | 16 / 436 | 16 / 520 |

## Introduction

The LatticeECP2/M family of FPGA devices is optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption ("S" versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LatticeECP2/M FPGA family. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The Diamond design tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP2/M family. By using these IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

# LatticeECP2/M Family Data Sheet Architecture

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## Architecture Overview

Each LatticeECP2/M device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing blocks, as shown in Figure 2-1. In addition, the LatticeECP2M family contains SERDES Quads in one or more of the corners. Figure 2-2 shows the block diagram of ECP2M20 with one quad.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2/M devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeECP2/M devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP2M devices feature up to 16 embedded 3.125Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS Quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed by a soft IP interface, referred to as the SERDES Client Interface (SCI). These quads (up to four) are located at the corners of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP2/M devices are arranged in eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as SPI4.2, along with memory interfaces including DDR2.

The LatticeECP2/M registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2/M architecture provides two General PLLs (GPLL) and up to six Standard PLLs (SPLL) per device. In addition, each LatticeECP2/M family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block is located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual boot support is located toward the center of this EBR row. The Ball Grid Array (BGA) package devices in the LatticeECP2/M family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator. The LatticeECP2/M devices use 1.2V as their core voltage.

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*Figure 2-1. Simplified Block Diagram, ECP2-6 Device (Top Level)*

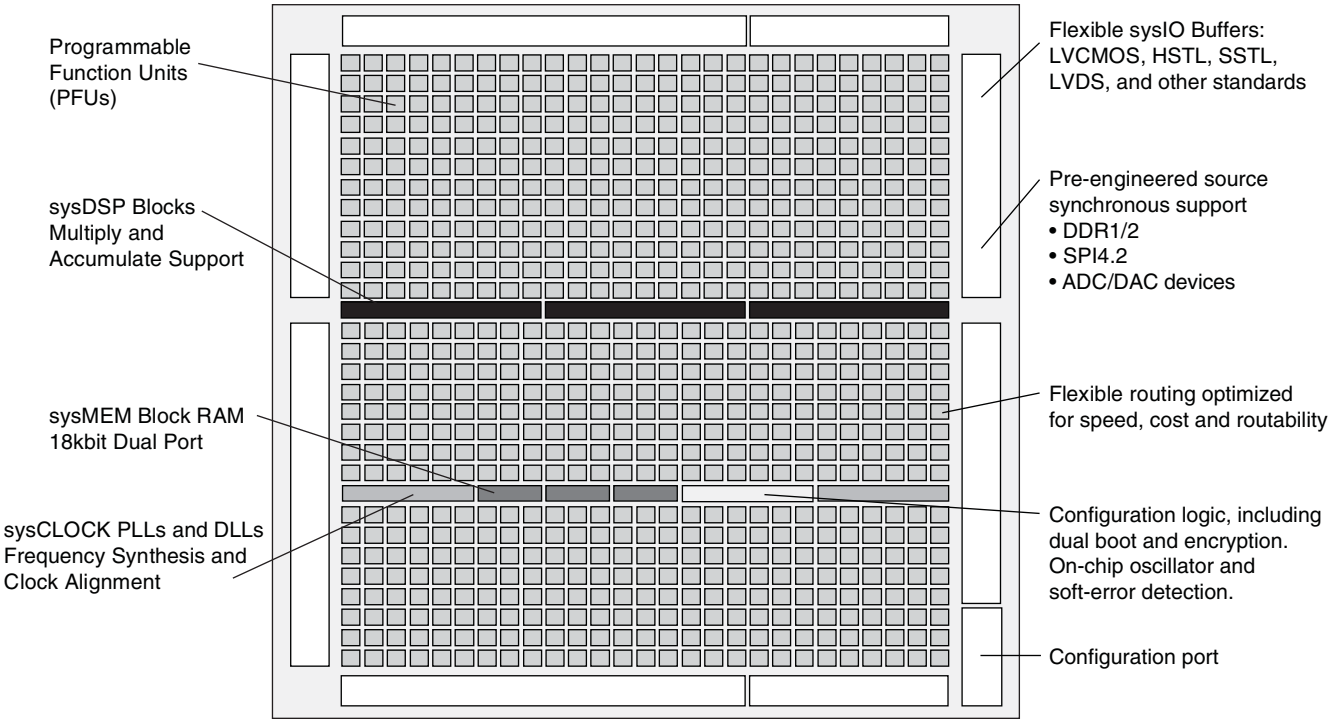
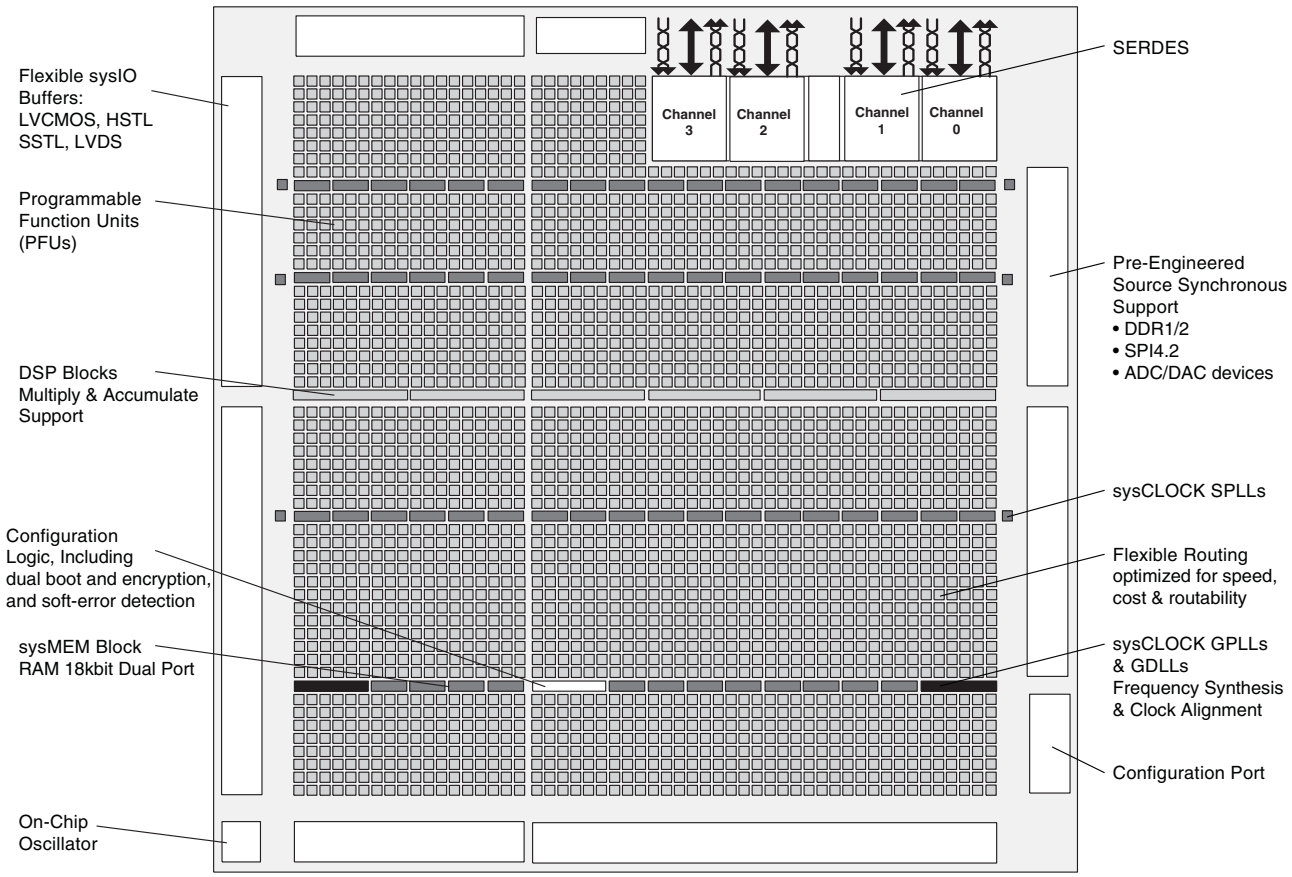



*Figure 2-2. Simplified Block Diagram, ECP2M20 Device (Top Level)*

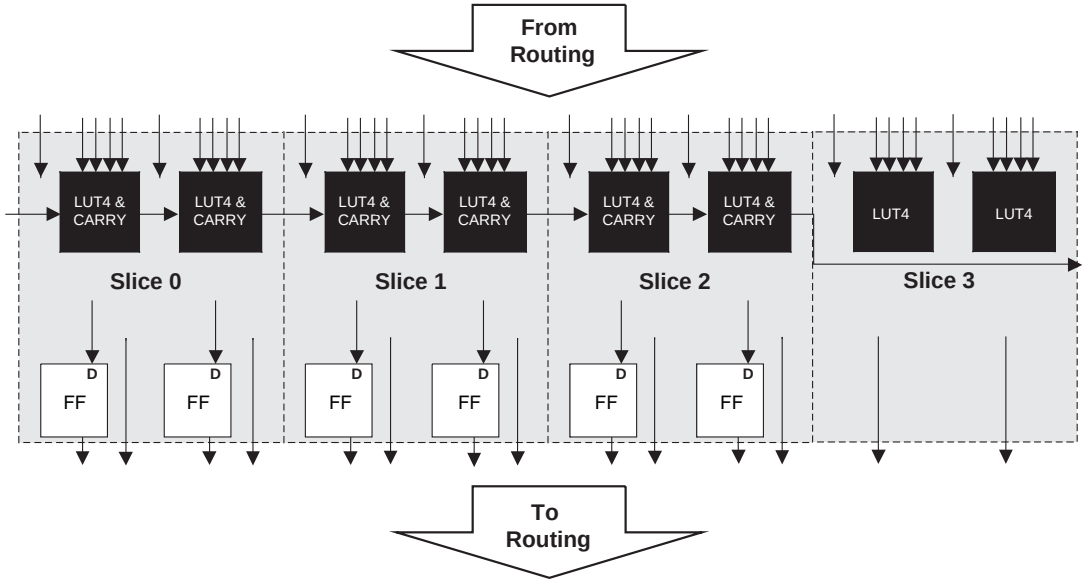


## PFU Blocks

The core of the LatticeECP2/M device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

***Figure 2-3. PFU Diagram***




## Slice

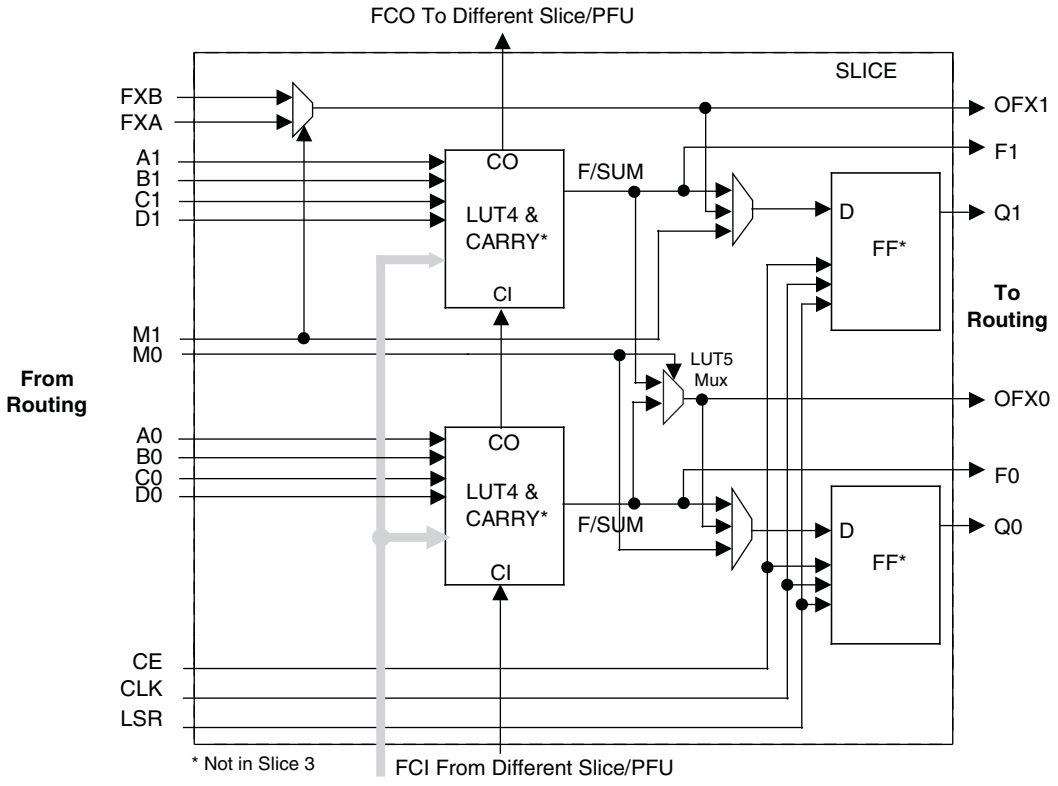
Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains some logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

***Table 2-1. Resources and Modes Available per Slice***

| Slice | PFU BLock | | PFF Block | |
|---|---|---|---|---|
| | Resources | Modes | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 3 | 2 LUT4s | Logic, ROM | 2 LUT4s | Logic, ROM |

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

*Figure 2-4. Slice Diagram*




For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

*Table 2-2. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FC | Fast Carry-in[1] |
| Input | Inter-slice signal | FXA | Intermediate signal to generate LUT6 and LUT7 |
| Input | Inter-slice signal | FXB | Intermediate signal to generate LUT6 and LUT7 |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Slice 2 of each PFU is the fast carry chain output[1] |

1. See Figure 2-4 for connection details.
2. Requires two PFUs.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with Async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP2/M devices, please see the list of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required to Implement Distributed RAM***

| | SPR 16X4 | PDPR 16X4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

**ROM Mode**
ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

## Routing

There are many resources provided in the LatticeECP2/M devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, allowing the routing of both short and long connections between PFUs.

The LatticeECP2/M family has an enhanced routing architecture that produces a compact design. The Diamond design software takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## sysCLOCK Phase Locked Loops (GPLL/SPLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP2/M family support two General Purpose PLLs (GPLLs) which are full-featured PLLs. In addition, some of the larger devices have two to six Standard PLLs (SPLLs) that have a subset of GPLL functionality.

### General Purpose PLL (GPLL)

The architecture of the GPLL is shown in Figure 2-5. A description of the GPLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP or from a user clock PIN/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

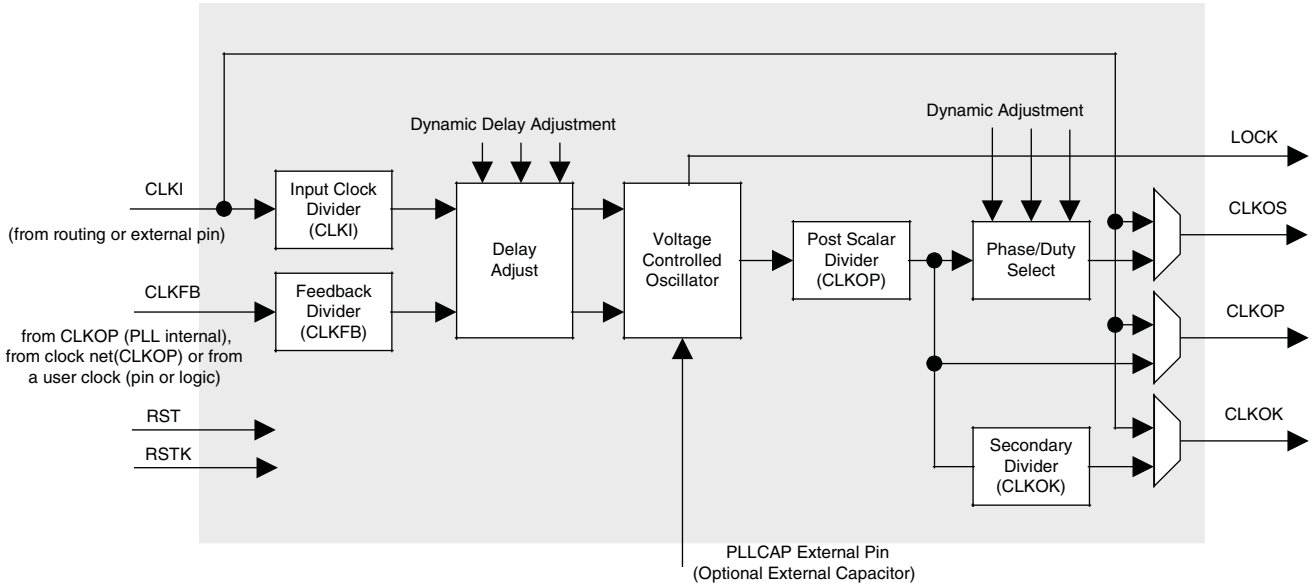
The Delay Adjust Block adjusts either the delays of the reference or feedback signals. The Delay Adjust Block can either be programmed during configuration or can be adjusted dynamically. The setup, hold or clock-to-out times of the device can be improved by programming a delay in the feedback or input path of the PLL, which will advance or delay the output clock with reference to the input clock.

Following the Delay Adjust Block, both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. LatticeECP2/M devices have two dedicated pins on the left and right edges of the device for connecting optional external capacitors to the VCO. This allows the PLLs to operate at a lower frequency. This is a shared resource that can only be used by one PLL (GPLL or SPLL) per side.

The output of the VCO then enters the post-scalar divider. The post-scalar divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. A secondary divider takes the CLKOP signal and uses it to derive lower frequency outputs (CLKOK). The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOP signal and generates the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The primary output from the post scalar divider CLKOP along with the outputs from the secondary divider (CLKOK) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

*Figure 2-5. General Purpose PLL (GPLL) Diagram*




## Standard PLL (SPLL)

Some of the larger devices have two to six Standard PLLs (SPLLs). SPLLs have the same features as GPLLs but without delay adjustment capability. SPLLs also provide different parametric specifications. For more information, please see the list of additional technical documentation at the end of this data sheet.

Table 2-4 provides a description of the signals in the GPLL and SPLL blocks.

*Table 2-4. GPLL and SPLL Blocks Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | “1” to reset PLL counters, VCO, charge pumps and M-dividers |
| RSTK | I | “1” to reset K-divider |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (no phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | “1” indicates PLL LOCK to CLKI |
| DDAMODE[1] | I | Dynamic Delay Enable. “1”: Pin control (dynamic), “0”: Fuse Control (static) |
| DDAIZR[1] | I | Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on |
| DDAILAG[1] | I | Dynamic Delay Lag/Lead. “1”: Lead, “0”: Lag |
| DDAIDEL[2:0][1] | I | Dynamic Delay Input |
| DPA MODES | I | DPA (Dynamic Phase Adjust/Duty Cycle Select) mode |
| DPHASE [3:0] | I | DPA Phase Adjust inputs |
| DDDUTY [3:0] | — | DPA Duty Cycle Select inputs |

1. These signals are not available in SPLL.

## Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP2/M family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Frequency Detector (PFD) input mux. The reference signal for the PFD can also be generated from the Delay Chain and CLKFB signals. The feedback input to the PFD is generated from the CLKFB pin, CLKI or from tapped signal from the Delay chain.

The PFD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. This binary output of the PFD is fed into a Arithmetic Logic Unit (ALU). Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated DLLDELA delay block. The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-6 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions. For more information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

***Figure 2-6. Delay Locked Loop Diagram (DLL)***

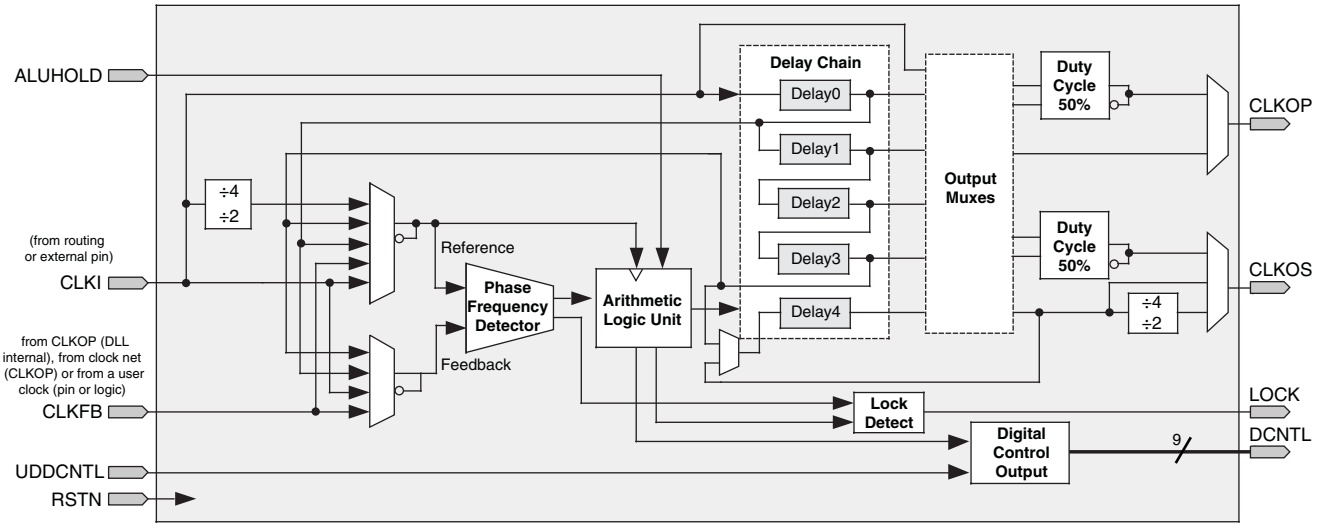


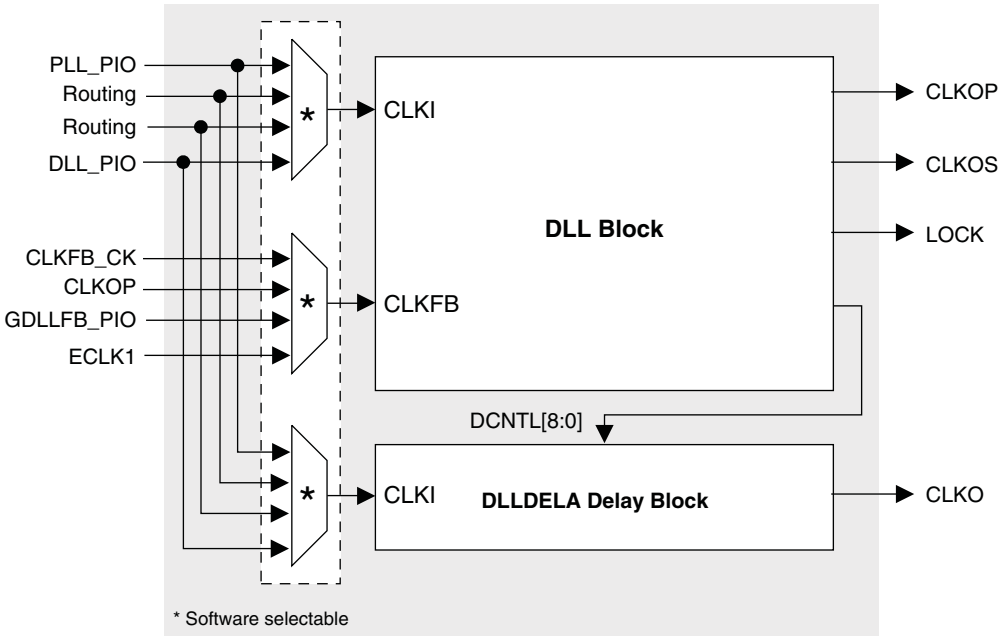
*Table 2-5. DLL Signals*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | DLL feed input from DLL output, clock net, routing or external pin |
| RSTN | I | Active low synchronous reset |
| ALUHOLD | I | Active high freezes the ALU |
| UDDCNTL | I | Synchronous enable signal (hold high for two cycles) from routing |
| DCNTL[8:0] | O | Encoded digital control signals for PIC INDEL and slave delay calibration |
| CLKOP | O | The primary clock output |
| CLKOS | O | The secondary clock output with fine phase shift and/or division by 2 or by 4 |
| LOCK | O | Active high phase lock indicator |

## DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

*Figure 2-7. DLLDELA Delay Block*




## PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

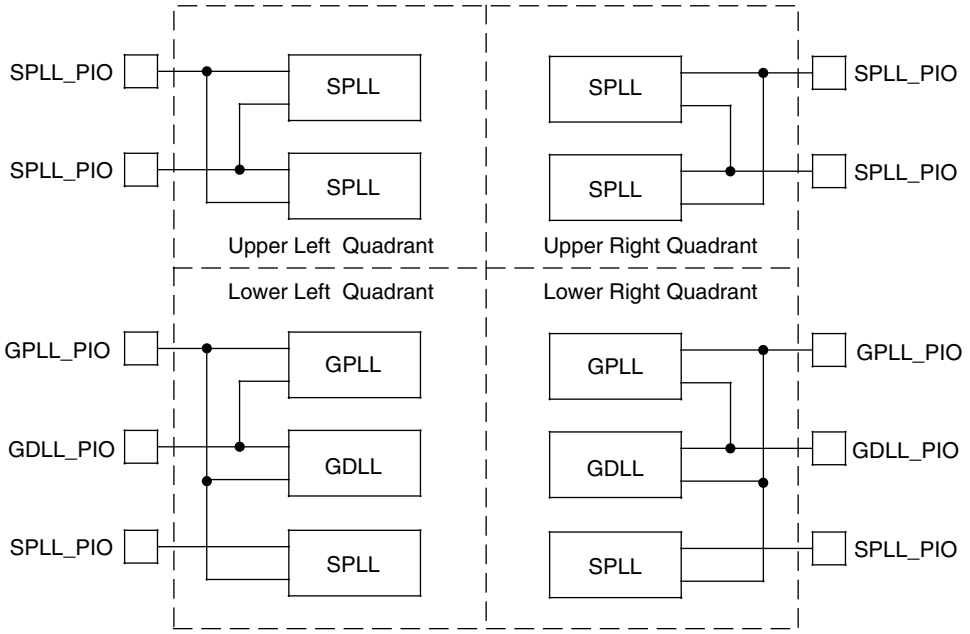
The DLLs in the LatticeECP2/M are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

## GPLL/SPLL/GDLL PIO Input Pin Connections (LatticeECP2M Family Only)

All LatticeECP2M devices contain two GDLLs, two GPLLs and six SPLLs, arranged in quadrants as shown in Figure 2-8. In the LatticeECP2M devices GPLLs, SPLLs and GDLLs share their input pins. Figure 2-8 shows the sharing of SPLLs input pin connections in the upper two quadrants and the sharing of GDLL, GPLL and SPLL input pin connections in the lower two quadrants.

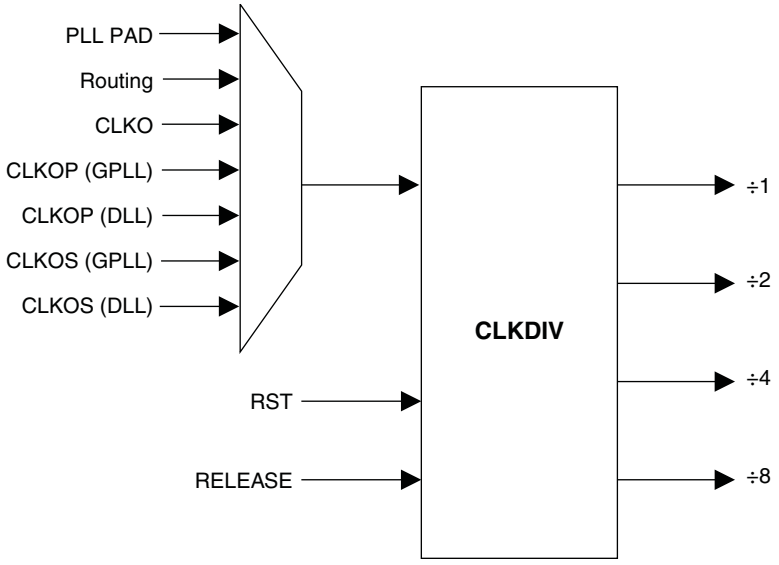
***Figure 2-8. Sharing of PIO Pins by GPLL, SPLL and GDLL in LatticeECP2M Devices***




## Clock Dividers

LatticeECP2/M devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, DLL-DELA delay blocks, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and synchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information about clock dividers, please see the list of additional technical documentation at the end of this data sheet. Figure 2-9 shows the clock divider connections.

*Figure 2-9. Clock Divider Connections*



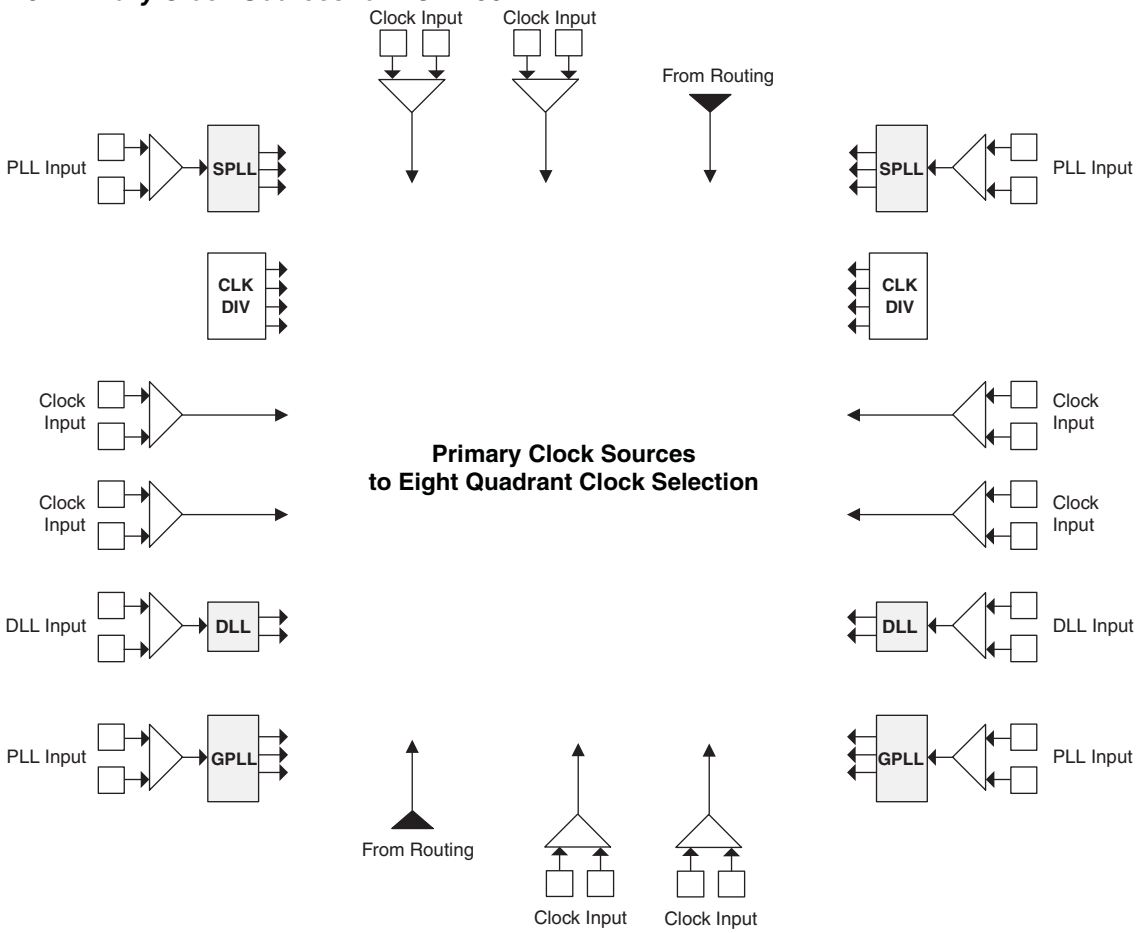

## Clock Distribution Network

LatticeECP2/M devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

### Primary Clock Sources

LatticeECP2/M devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2/M devices have two to eight sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device, with the exception of the LatticeECP2M 256-fpBGA package devices which have six dedicated clock inputs on the device. Figure 2-10 shows the primary clock sources.

*Figure 2-10. Primary Clock Sources for ECP2-50*

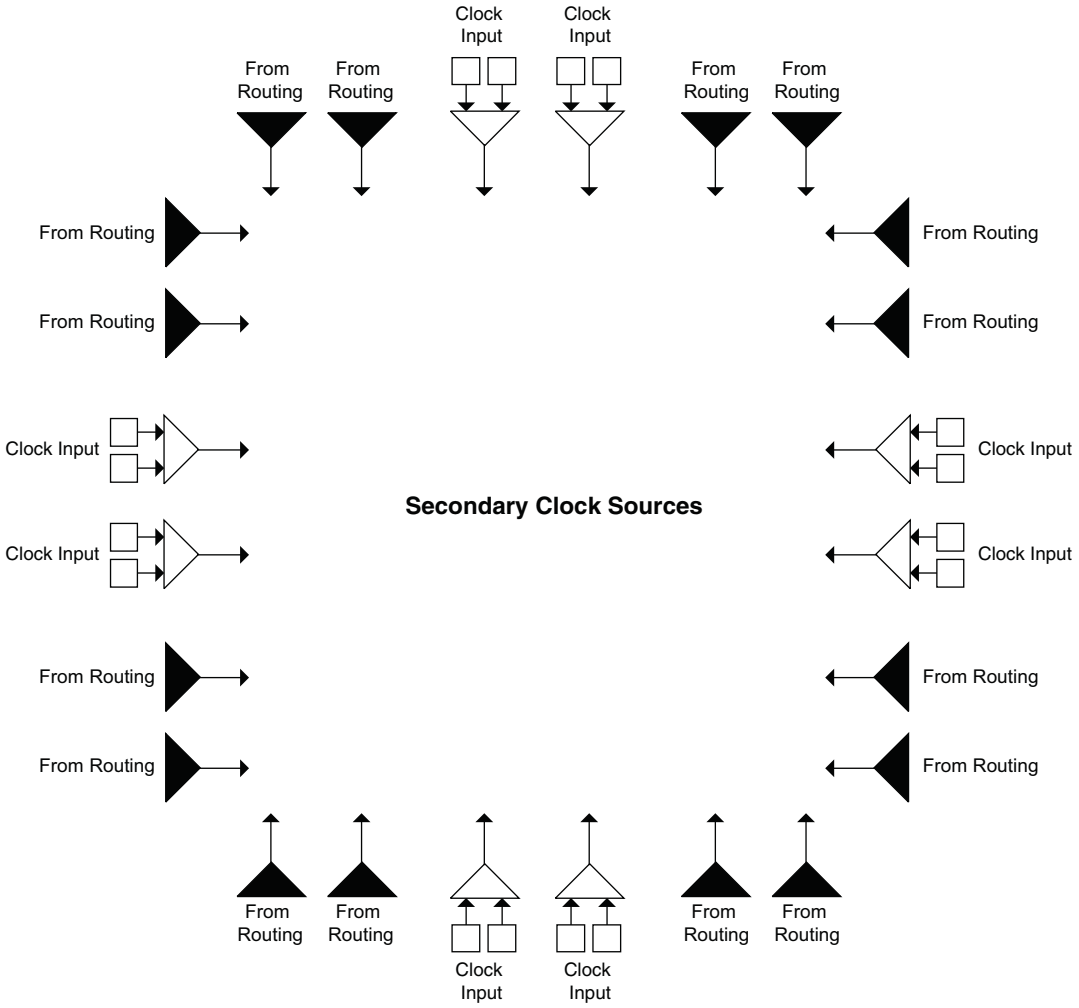



Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

## Secondary Clock/Control Sources

LatticeECP2/M devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-11 shows the secondary clock sources.

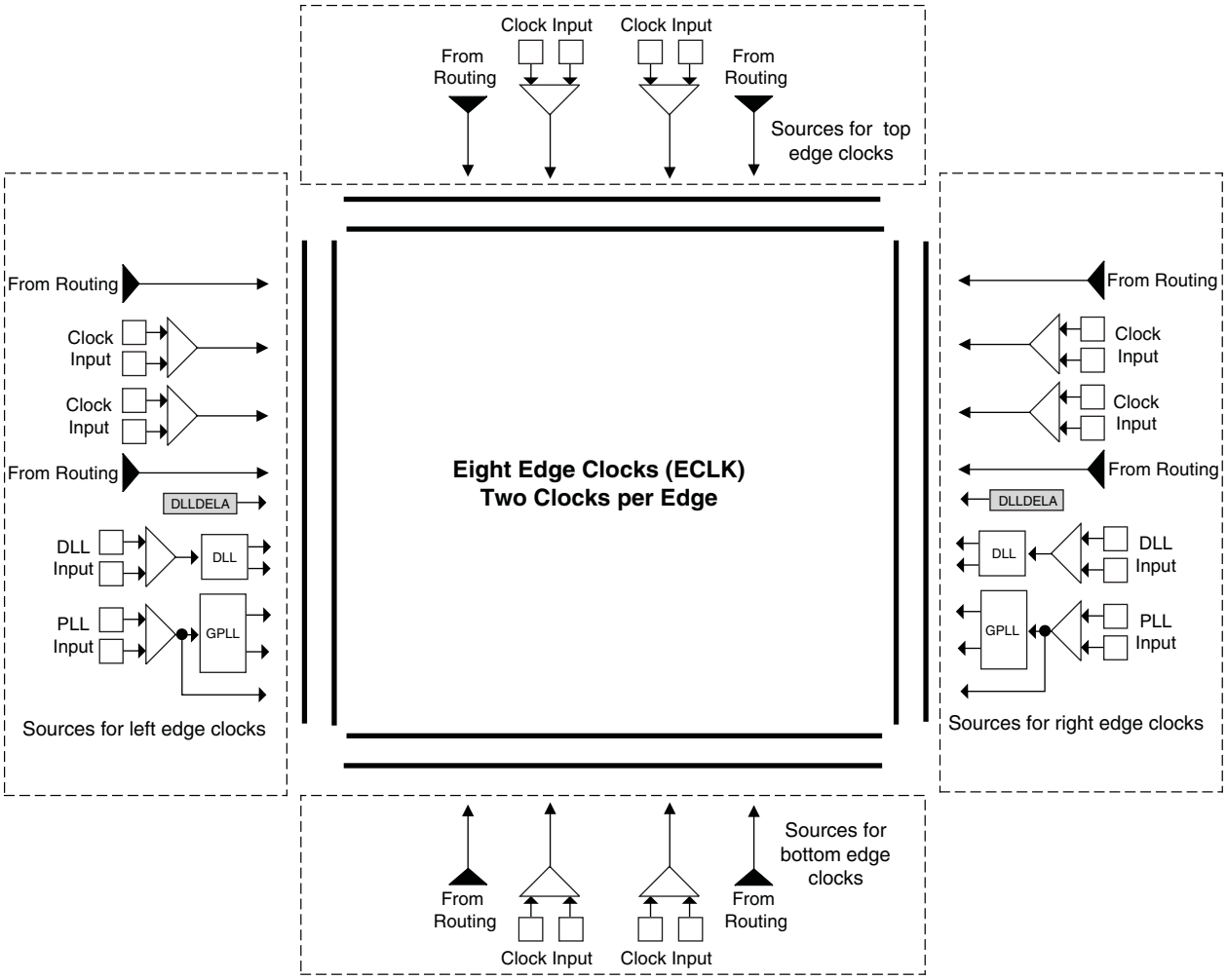
***Figure 2-11. Secondary Clock Sources***



## Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

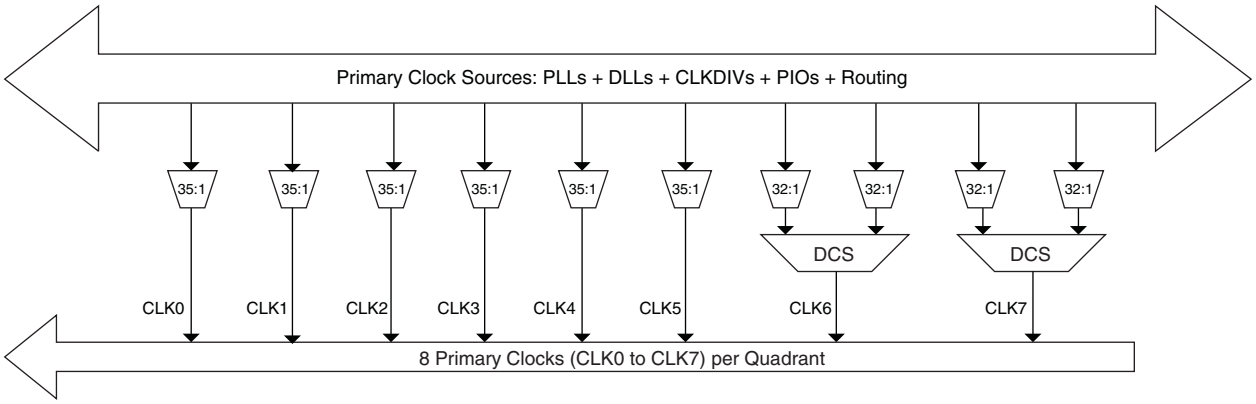
***Figure 2-12. Edge Clock Sources***



## Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

***Figure 2-13. Per Quadrant Primary Clock Selection***

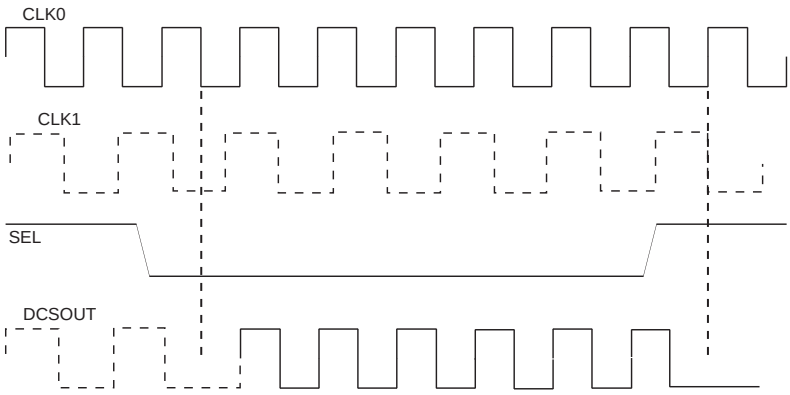



## Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

***Figure 2-14. DCS Waveforms***




## Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distrubed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

***Figure 2-15. Secondary Clock Regions ECP2-50***

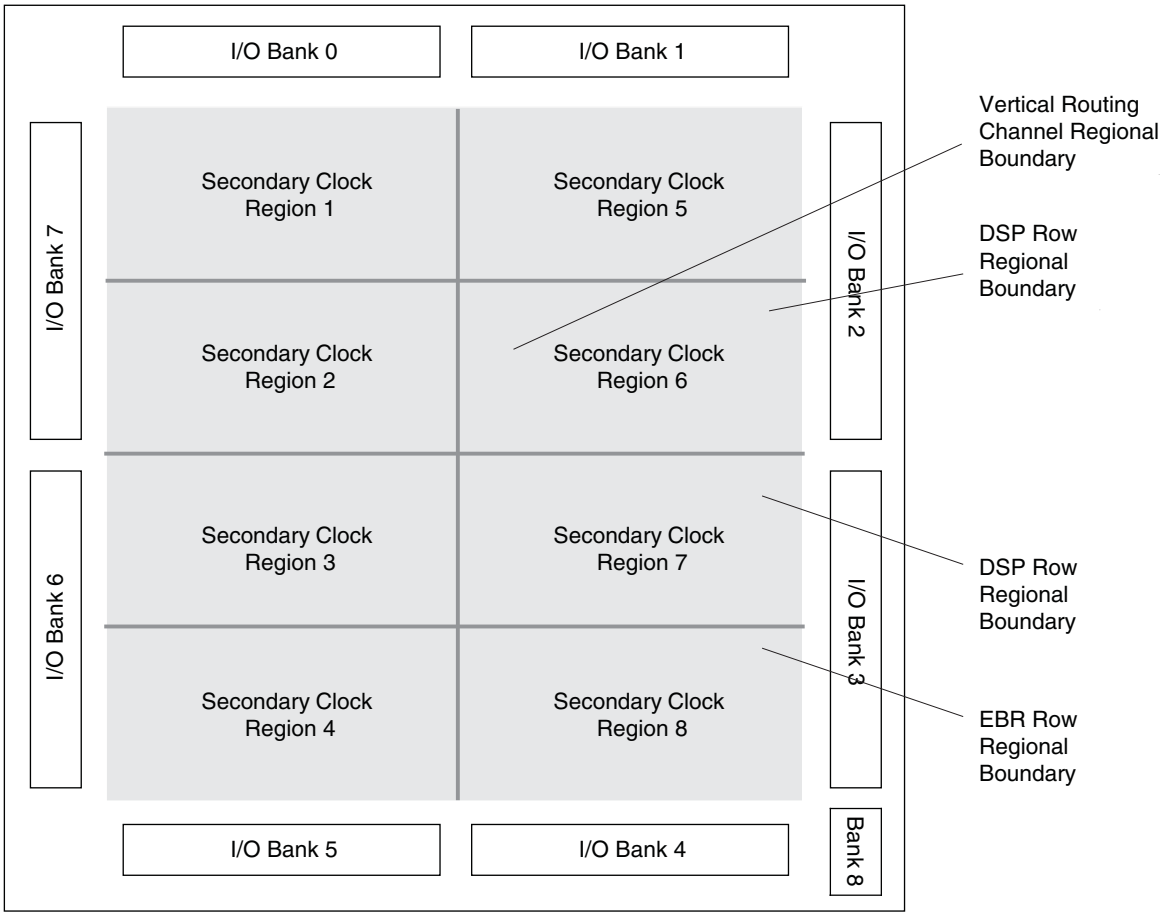
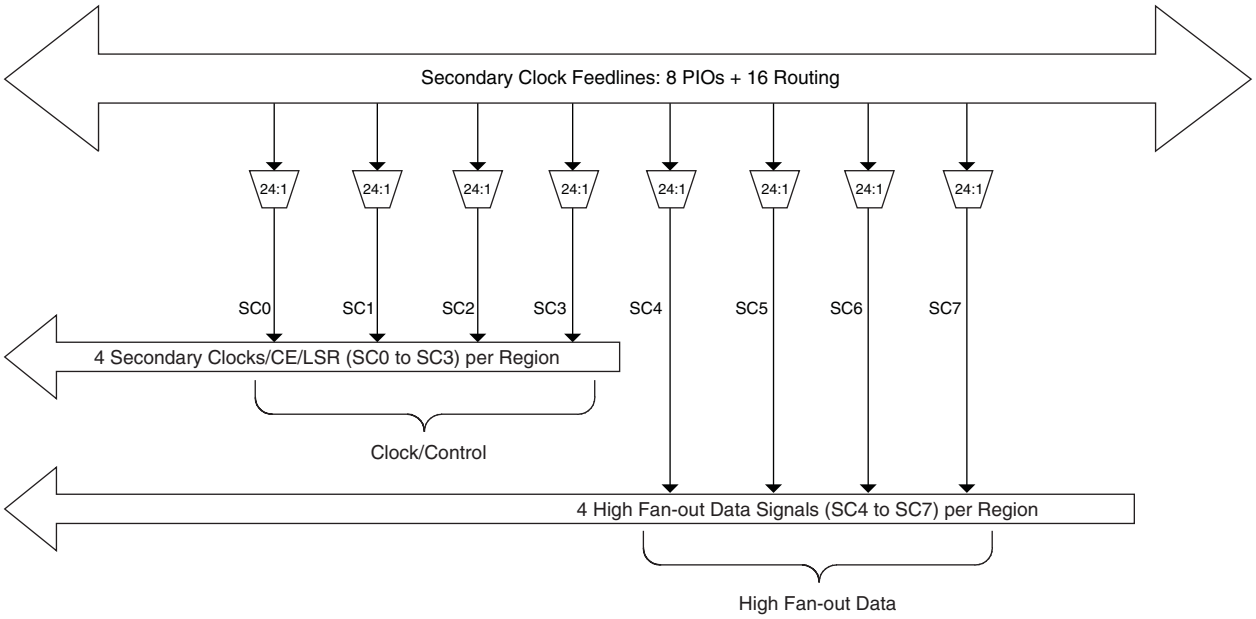


*Figure 2-16. Secondary Clock Selection*




## Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

*Figure 2-17. Slice0 through Slice2 Clock Selection*

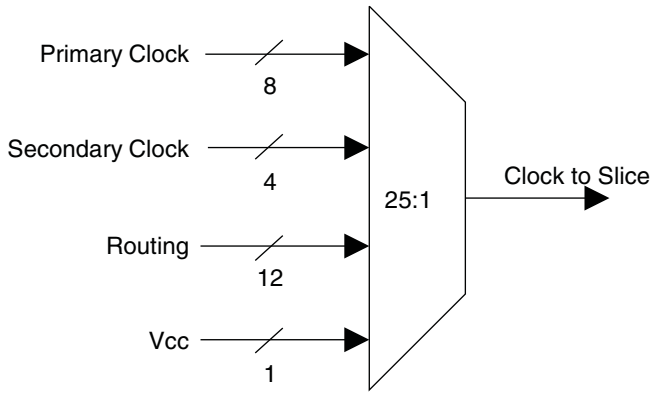
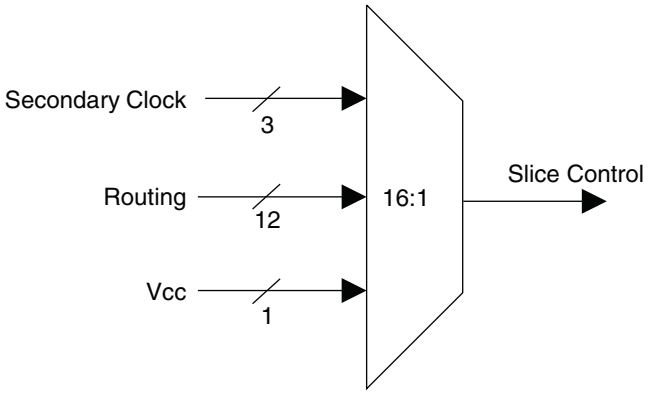


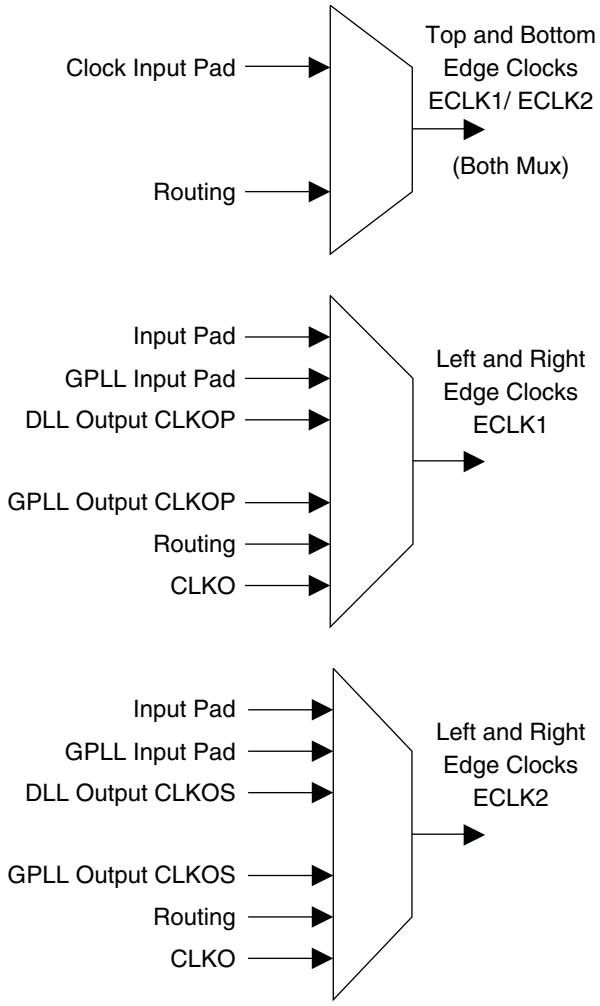
*Figure 2-18. Slice0 through Slice2 Control Selection*




## Edge Clock Routing

LatticeECP2/M devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per device: two edge clocks per edge. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKO signal (generated from the DLLDELA block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-19 shows the selection muxes for these clocks.

*Figure 2-19. Edge Clock Mux Connections*



# sysMEM Memory

LatticeECP2/M devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

## sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

***Table 2-6. sysMEM Block Configurations***

| Memory Mode | Configurations |
|---|---|
| Single Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18<br>512 x 36 |
| True Dual Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18 |
| Pseudo Dual Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18<br>512 x 36 |

## Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

## RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

## Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

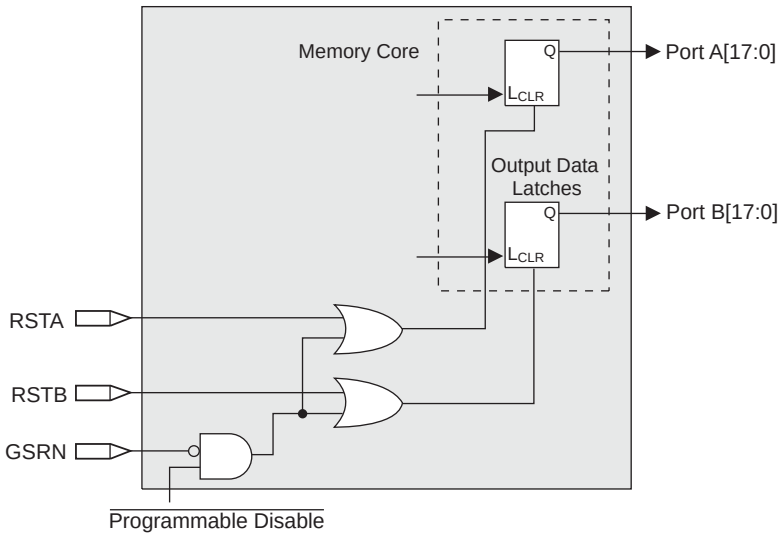
1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

***Figure 2-20. Memory Core Reset***

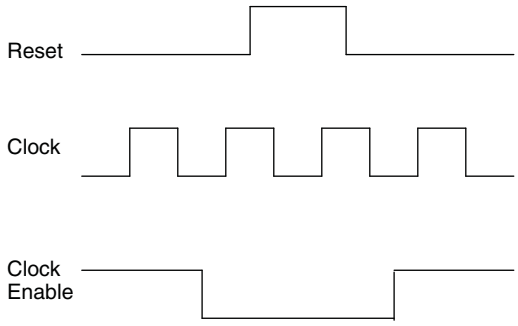



For further information about the sysMEM EBR block, please see the the list of additional technical documentation at the end of this data sheet.

## EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

***Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram***




If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

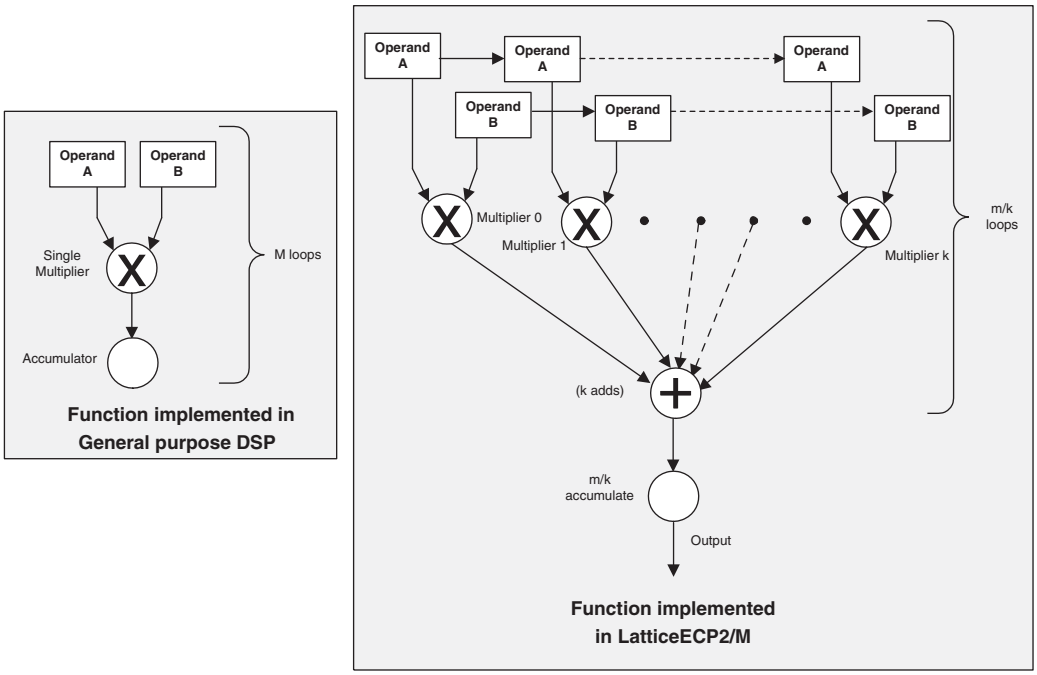
# sysDSP™ Block

The LatticeECP2/M family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

## sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP2/M, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-22 compares the fully serial and the mixed parallel and serial implementations.

***Figure 2-22. Comparison of General DSP and LatticeECP2/M Approaches***




## sysDSP Block Capabilities

The sysDSP block in the LatticeECP2/M family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP2/M family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. In the LatticeECP2/M family the DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available on each block depends in the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-7 shows the capabilities of the block.

***Table 2-7. Maximum Number of Elements in a Block***

| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 8 | 4 | 1 |
| MAC | 2 | 2 | — |
| MULTADDSUB | 4 | 2 | — |
| MULTADDSUBSUM | 2 | 1 | — |

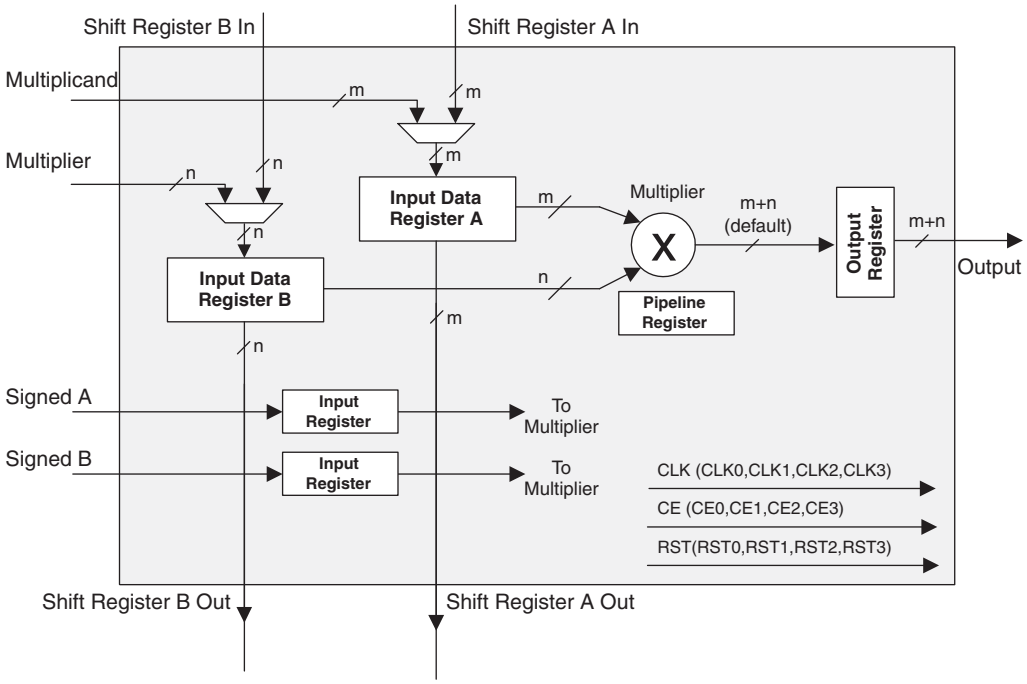
Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle.
- In the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

## MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-23 shows the MULT sysDSP element.

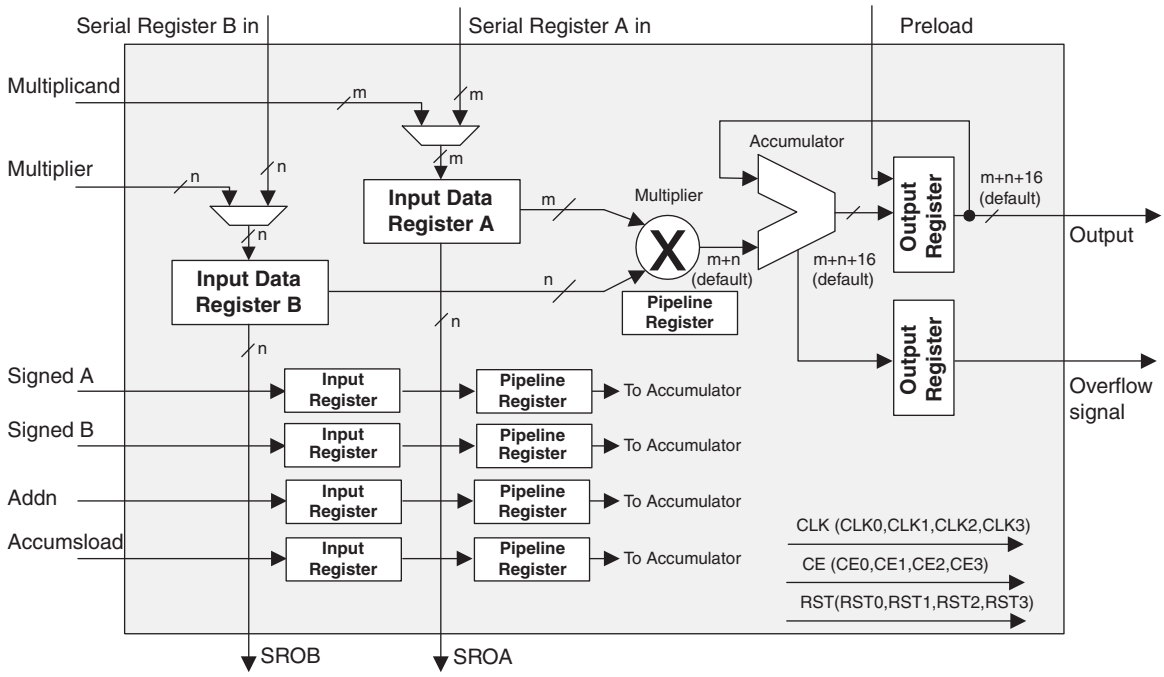
***Figure 2-23. MULT sysDSP Element***



## MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in the LatticeECP2/M family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-24 shows the MAC sysDSP element.

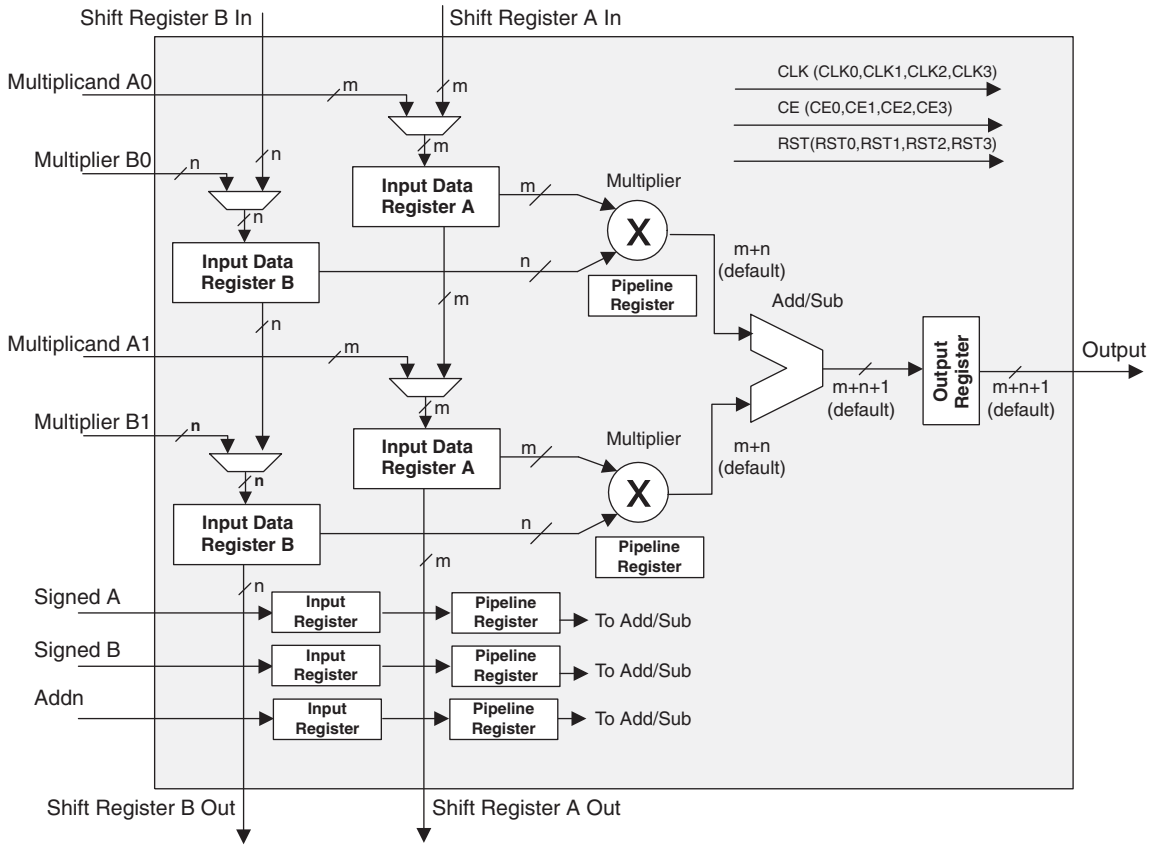
***Figure 2-24. MAC sysDSP***



## MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

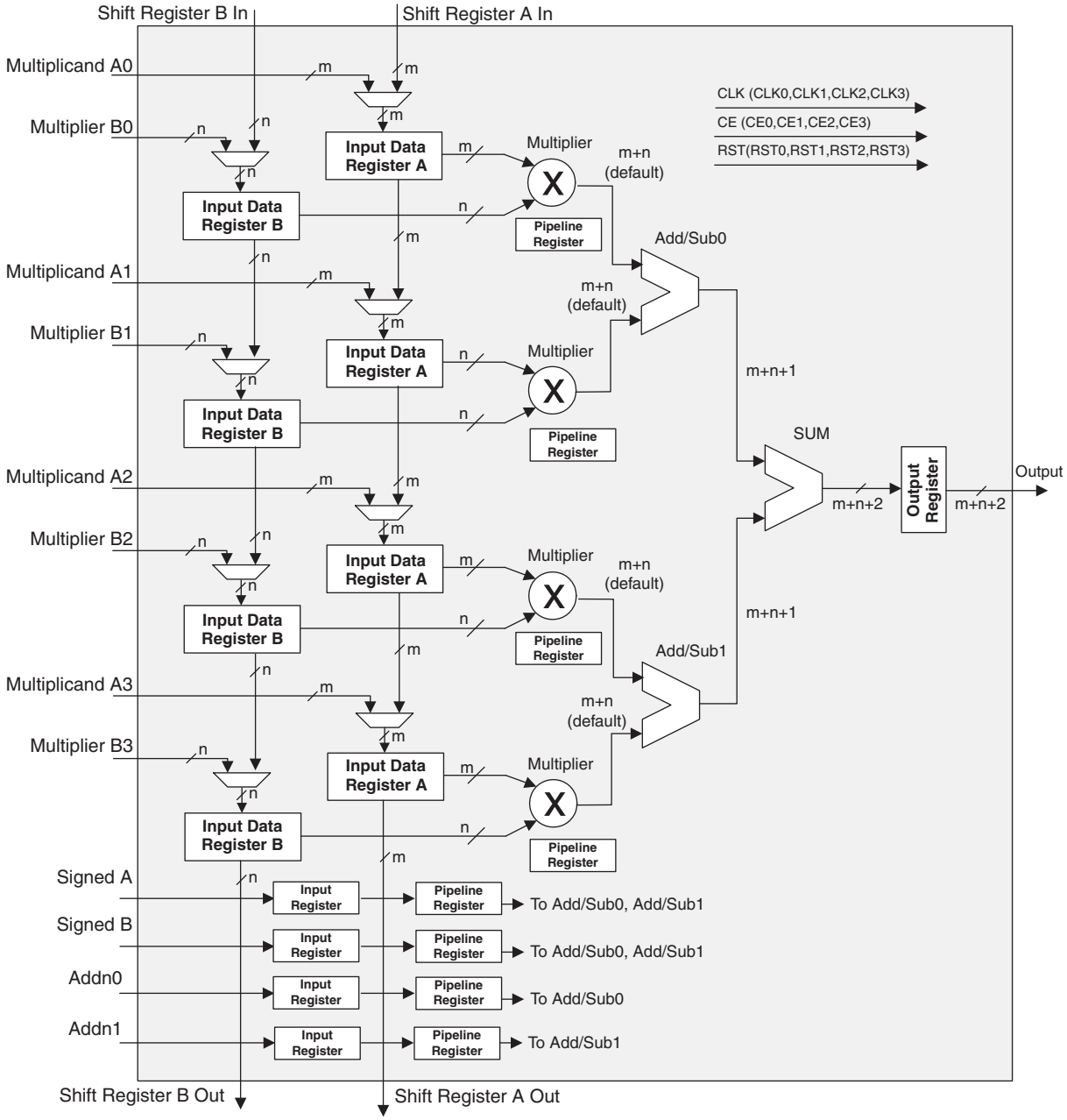
***Figure 2-25. MULTADDSUB***



## MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

***Figure 2-26. MULTADDSUBSUM***




## Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3)

one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

## Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

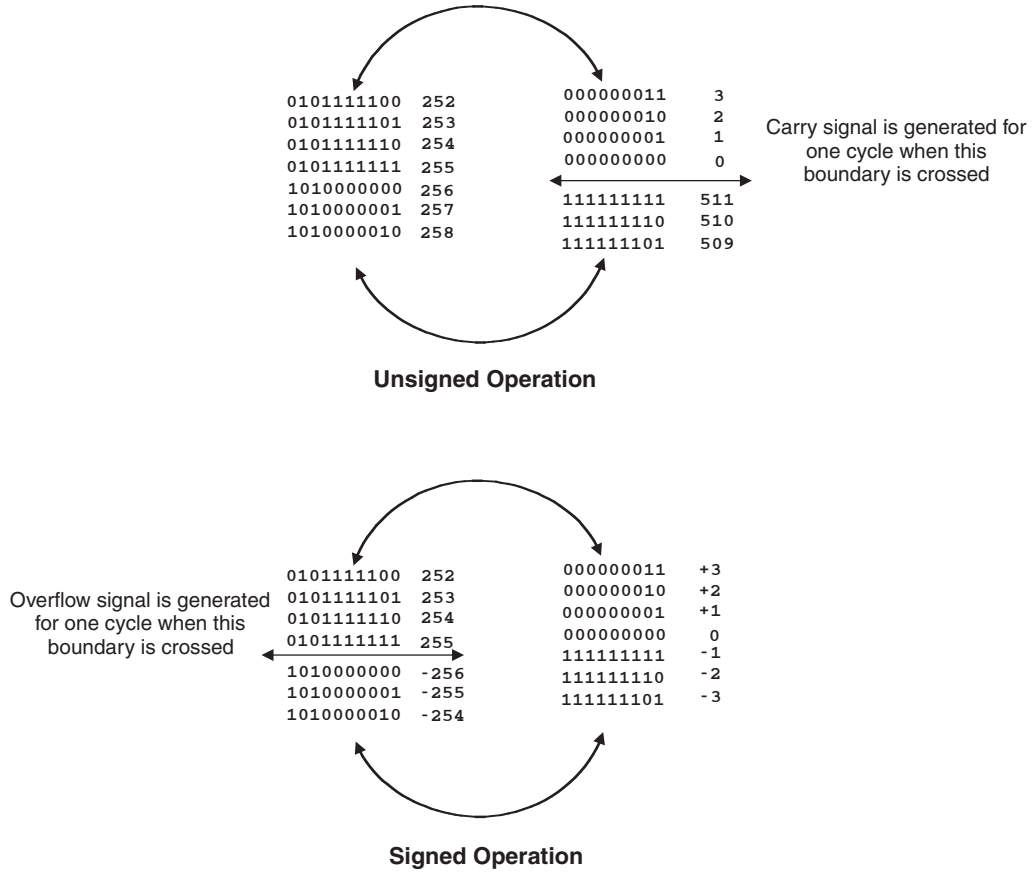
***Table 2-8. Sign Extension Example***

| Number | Unsigned | Unsigned 9-bit | Unsigned 18-bit | Signed | Two's Complement Signed 9 Bits | Two's Complement Signed 18 Bits |
|---|---|---|---|---|---|---|
| +5 | 0101 | 000000101 | 000000000000000101 | 0101 | 000000101 | 000000000000000101 |
| -6 | N/A | N/A | N/A | 1010 | 111111010 | 111111111111111010 |

## OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number than the accumulator, "roll-over" is said to have occurred and an overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-27.

***Figure 2-27. Accumulator Overflow/Underflow***



### IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

## Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

### Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

***Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family***

| Device | DSP Block | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|---|---|---|---|---|
| ECP2-6 | 3 | 24 | 12 | 3 |
| ECP2-12 | 6 | 48 | 24 | 6 |
| ECP2-20 | 7 | 56 | 28 | 7 |
| ECP2-35 | 8 | 64 | 32 | 8 |
| ECP2-50 | 18 | 144 | 72 | 18 |
| ECP2-70 | 22 | 176 | 88 | 22 |
| ECP2M20 | 6 | 48 | 24 | 6 |
| ECP2M35 | 8 | 64 | 32 | 8 |
| ECP2M50 | 22 | 176 | 88 | 22 |
| ECP2M70 | 24 | 192 | 96 | 24 |
| ECP2M100 | 42 | 336 | 168 | 42 |

***Table 2-10. Embedded SRAM in the LatticeECP2/M Family***

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) |
|---|---|---|
| ECP2-6 | 3 | 55 |
| ECP2-12 | 12 | 221 |
| ECP2-20 | 15 | 277 |
| ECP2-35 | 18 | 332 |
| ECP2-50 | 21 | 387 |
| ECP2-70 | 60 | 1106 |
| ECP2M20 | 66 | 1217 |
| ECP2M35 | 114 | 2101 |
| ECP2M50 | 225 | 4147 |
| ECP2M70 | 246 | 4534 |
| ECP2M100 | 288 | 5308 |

## LatticeECP2/M DSP Performance

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP2/M family.

***Table 2-11. DSP Performance***

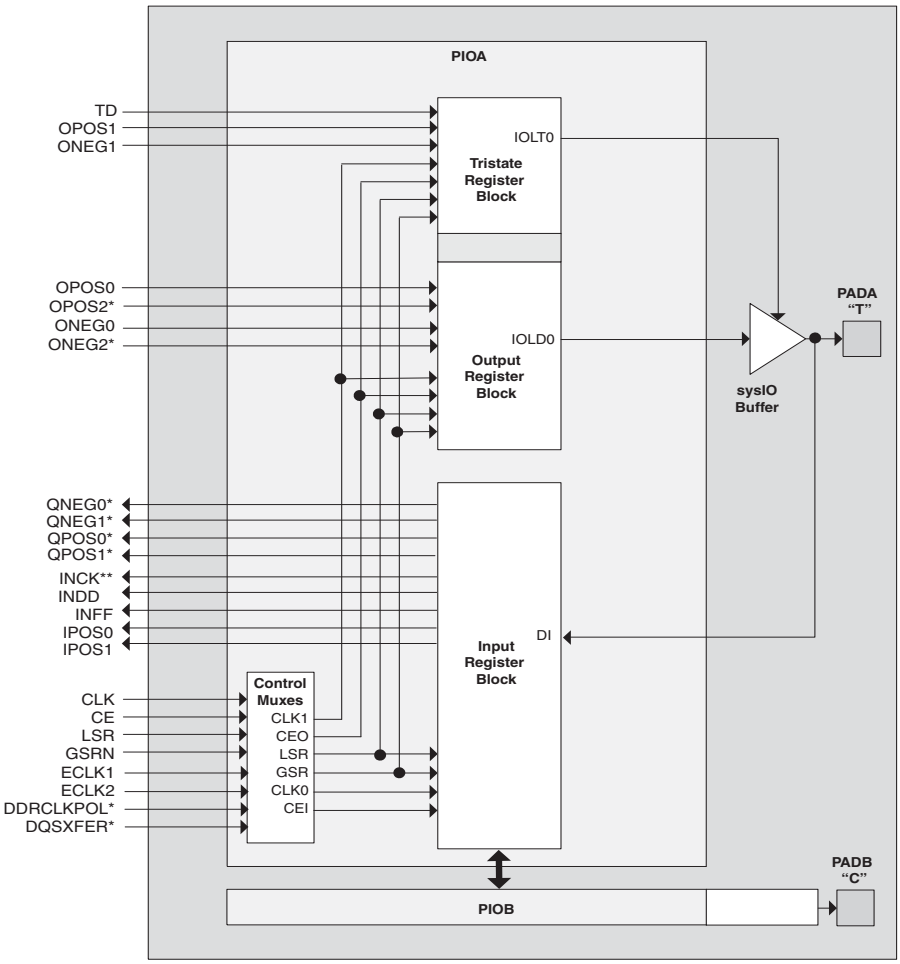
| Device | DSP Block | DSP Performance GMAC |
|---|---|---|
| ECP2-6 | 3 | 3.9 |
| ECP2-12 | 6 | 7.8 |
| ECP2-20 | 7 | 9.1 |
| ECP2-35 | 8 | 10.4 |
| ECP2-50 | 18 | 23.4 |
| ECP2-70 | 22 | 28.6 |
| ECP2M20 | 6 | 7.8 |
| ECP2M35 | 8 | 10.4 |
| ECP2M50 | 22 | 28.6 |
| ECP2M70 | 24 | 31.2 |
| ECP2M100 | 42 | 54.6 |

For further information about the sysDSP block, please see the list of additional technical information at the end of this data sheet.

# Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-28. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-12 provides the PIO signal list.

*Figure 2-28. PIC Diagram*




*Signals are available on left/right/bottom edges only.
** Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-28. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

*Table 2-12. PIO Signals List*

| Name | Type | Description |
|---|---|---|
| CE0, CE1 | Control from the core | Clock enables for input and output block flip-flops |
| CLK0, CLK1 | Control from the core | System clocks for input and output blocks |
| ECLK1, ECLK2 | Control from the core | Fast edge clocks |
| LSR | Control from the core | Local Set/Reset |
| GSRN | Control from routing | Global Set/Reset (active low) |
| INCK[2] | Input to the core | Input to Primary Clock Network or PLL reference inputs |
| DQS | Input to PIO | DQS signal from logic (routing) to PIO |
| INDD | Input to the core | Unregistered data input to core |
| INFF | Input to the core | Registered input on positive edge of the clock (CLK0) |
| IPOS0, IPOS1 | Input to the core | Double data rate registered inputs to the core |
| QPOS0[1], QPOS1[1] | Input to the core | Gearbox pipelined inputs to the core |
| QNEG0[1], QNEG1[1] | Input to the core | Gearbox pipelined inputs to the core |
| OPOS0, ONEG0, OPOS2, ONEG2 | Output data from the core | Output signals from the core for SDR and DDR operation |
| OPOS1 ONEG1 | Tristate control from the core | Signals to Tristate Register block for DDR operation |
| DEL[3:0] | Control from the core | Dynamic input delay control bits |
| TD | Tristate control from the core | Tristate signal from the core used in SDR operation |
| DDRCLKPOL | Control from clock polarity bus | Controls the polarity of the clock (CLK0) that feed the DDR input block |
| DQSXFER | Control from core | Controls signal to the Output block |

1. Signals available on left/right/bottom only.
2. Selected I/O.

# PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

## Input Register Block

The input register blocks for PIOs in left, right and bottom edges contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-29 shows the diagram of the input register block for left, right and bottom edges. The input register block for the top edge contains one memory element to register the input signal as shown in Figure 2-30. The following description applies to the input register block for PIOs in the left, right and bottom edges of the device.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In DDR Mode, two registers are used to sample the data on the positive and negative edges of the DQS signal, creating two data streams, D0 and D1. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

***Figure 2-29. Input Register Block for Left, Right and Bottom Edges***

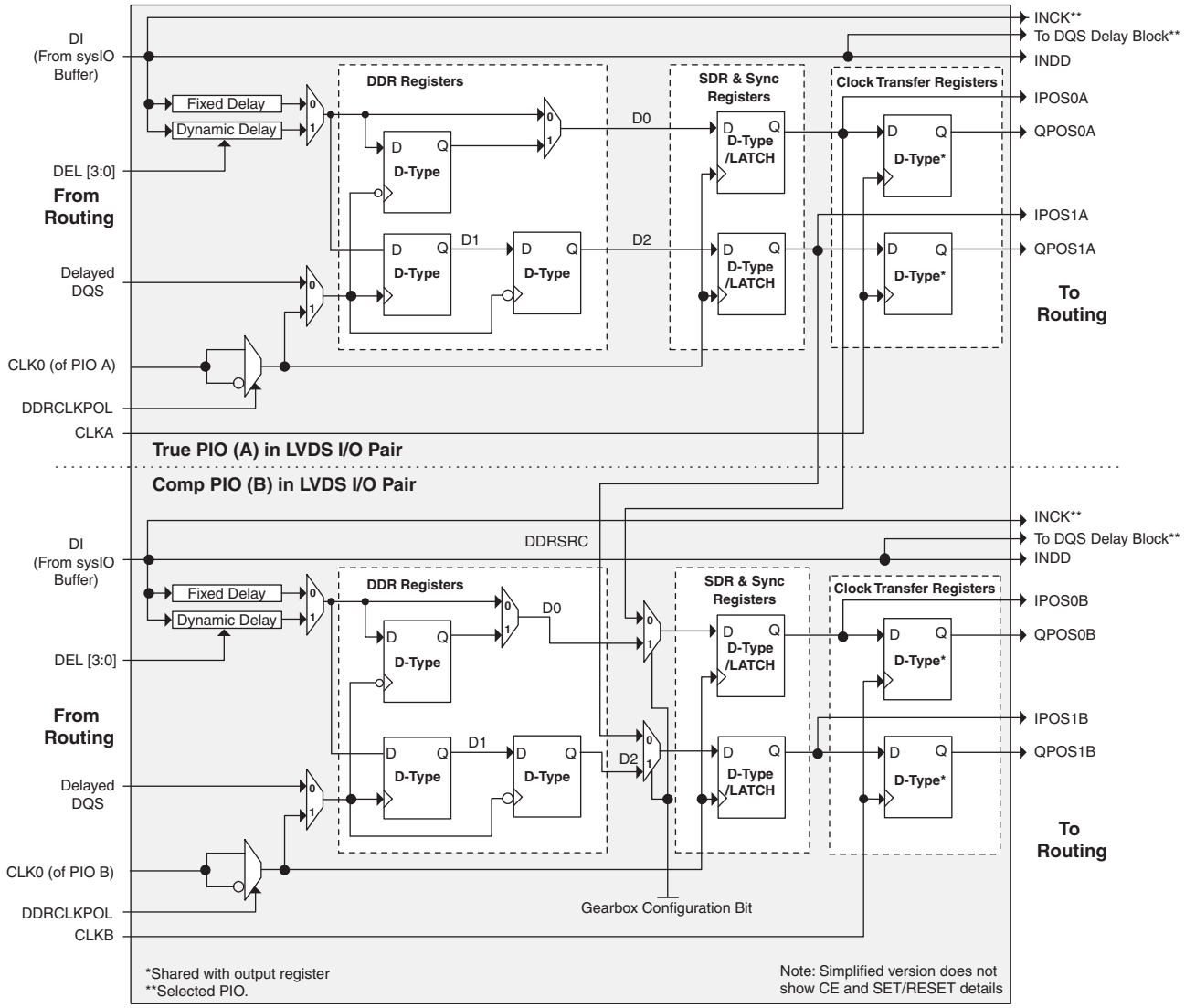
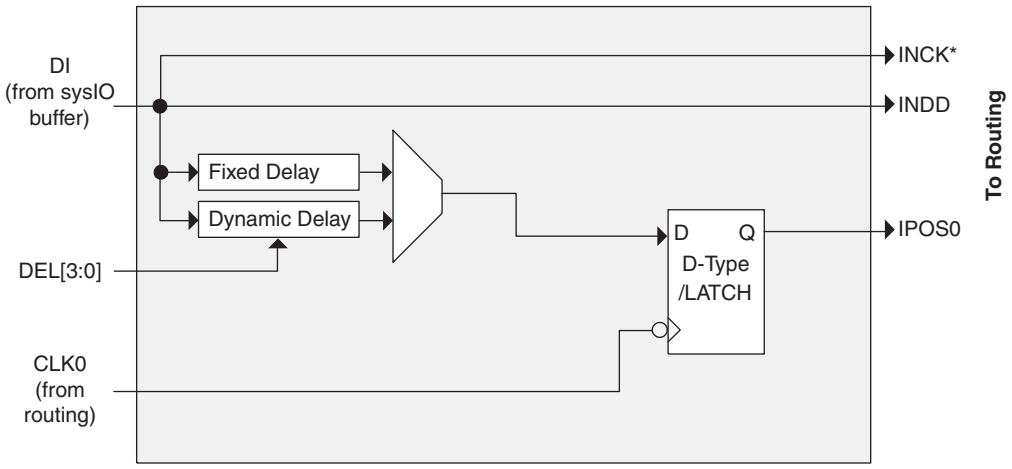


*Figure 2-30. Input Register Block Top Edge*




Note: Simplified version does not show CE and SET/RESET details.
*On selected blocks.

## Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the PIOs on the left, right and bottom contain a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-31 shows the diagram of the Output Register Block for PIOs on the left, right and the bottom edges. Figure 2-32 shows the diagram of the Output Register Block for PIOs on the top edge of the device.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. Then at the next clock cycle this registered OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

By combining the output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, that takes four data streams: ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-32 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

*Figure 2-31. Output and Tristate Block for Left, Right and Bottom Edges*

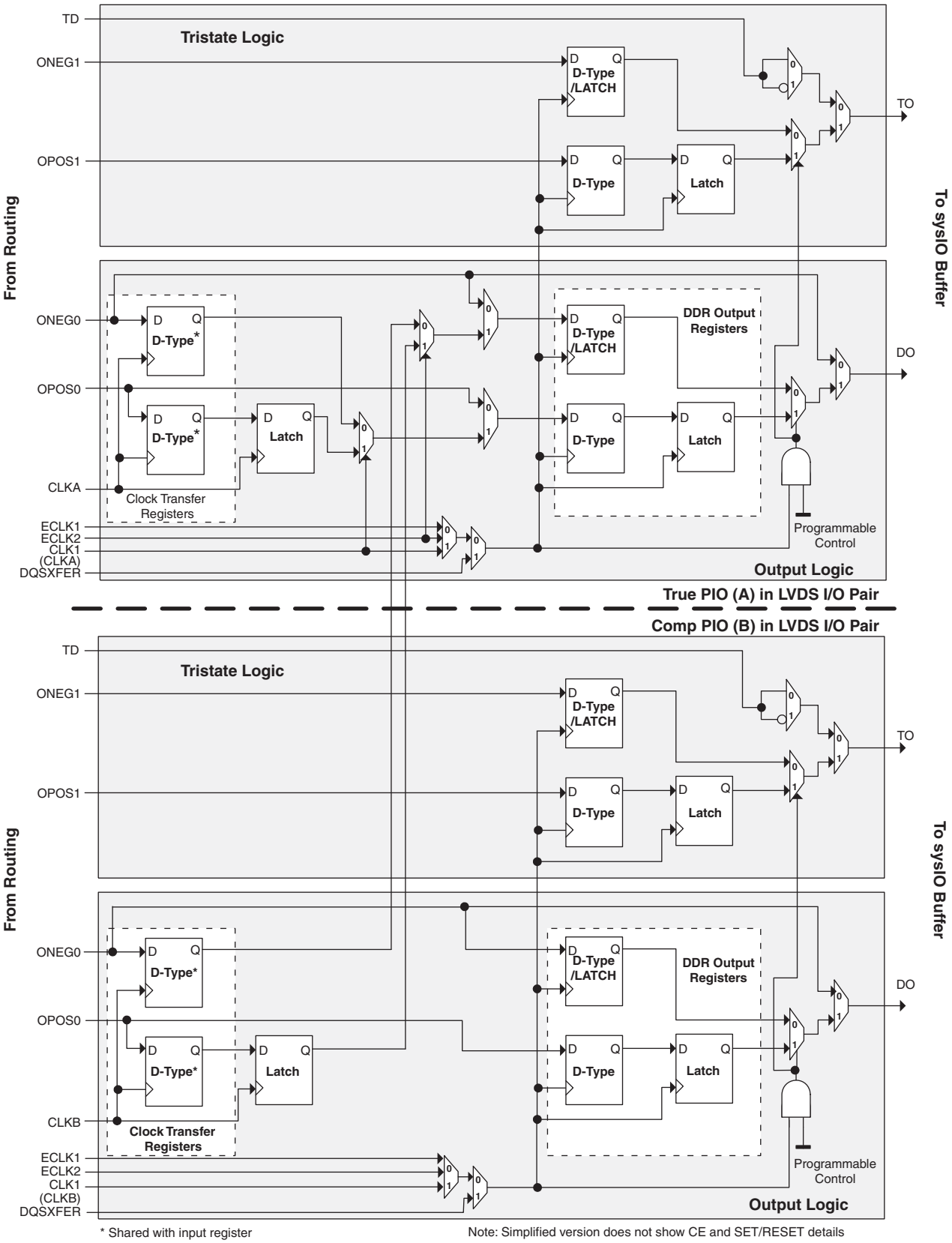
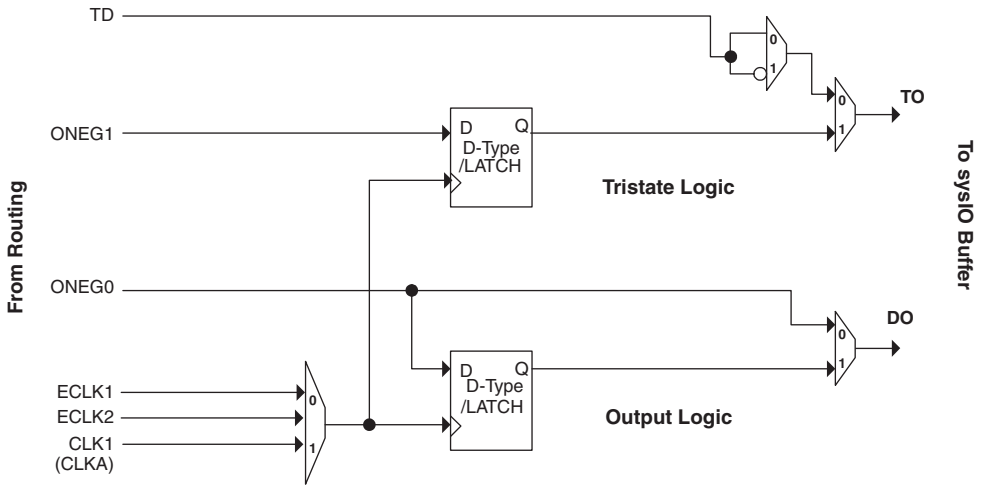


*Figure 2-32. Output and Tristate Block, Top Edge*




Note: Simplified version does not show CE and SET/RESET details.

### Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-32 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

### Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

## DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by the edge of the device as detailed below.

### Left and Right Edges

PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 16 PIOs. Figure 2-33 shows the assignment of DQS pins in each set of 16 PIOs.

### Bottom Edge

PICs on the bottom edge have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-34 shows the assignment of DQS pins in each set of 18 PIOs.

## Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

***Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device***

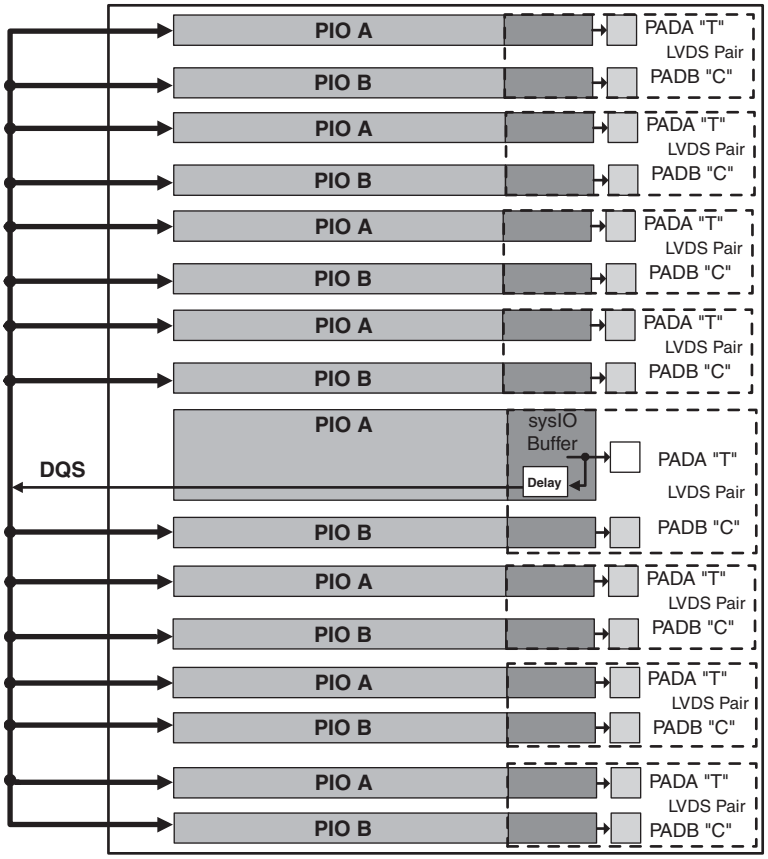
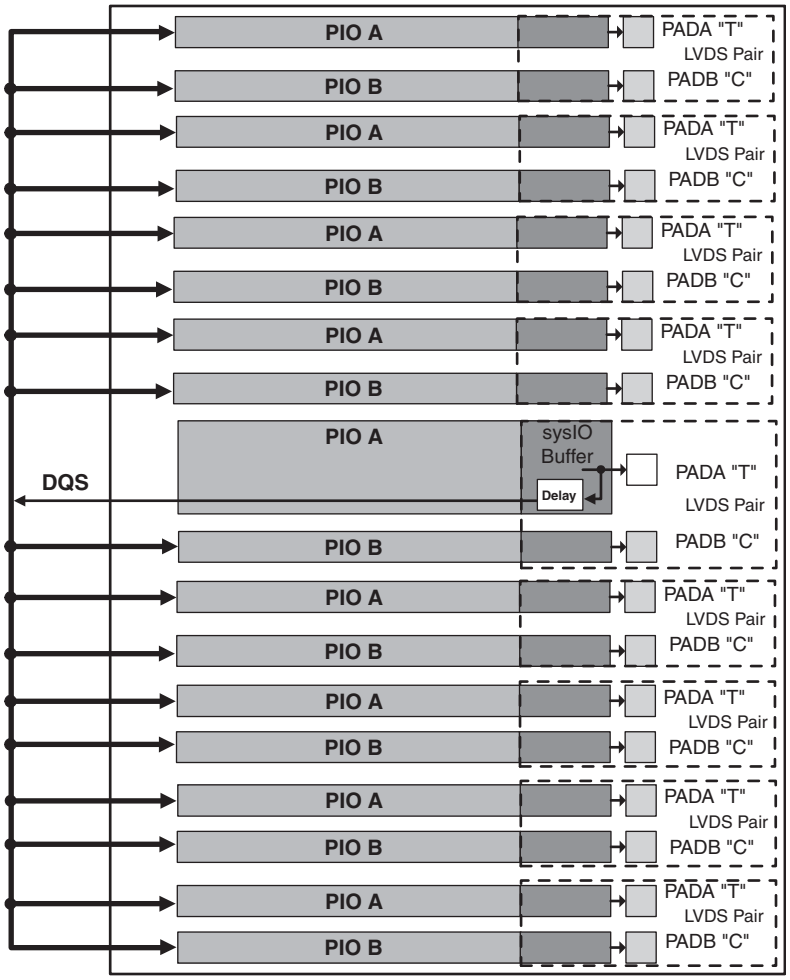


*Figure 2-34. DQS Input Routing for the Bottom Edge of the Device*



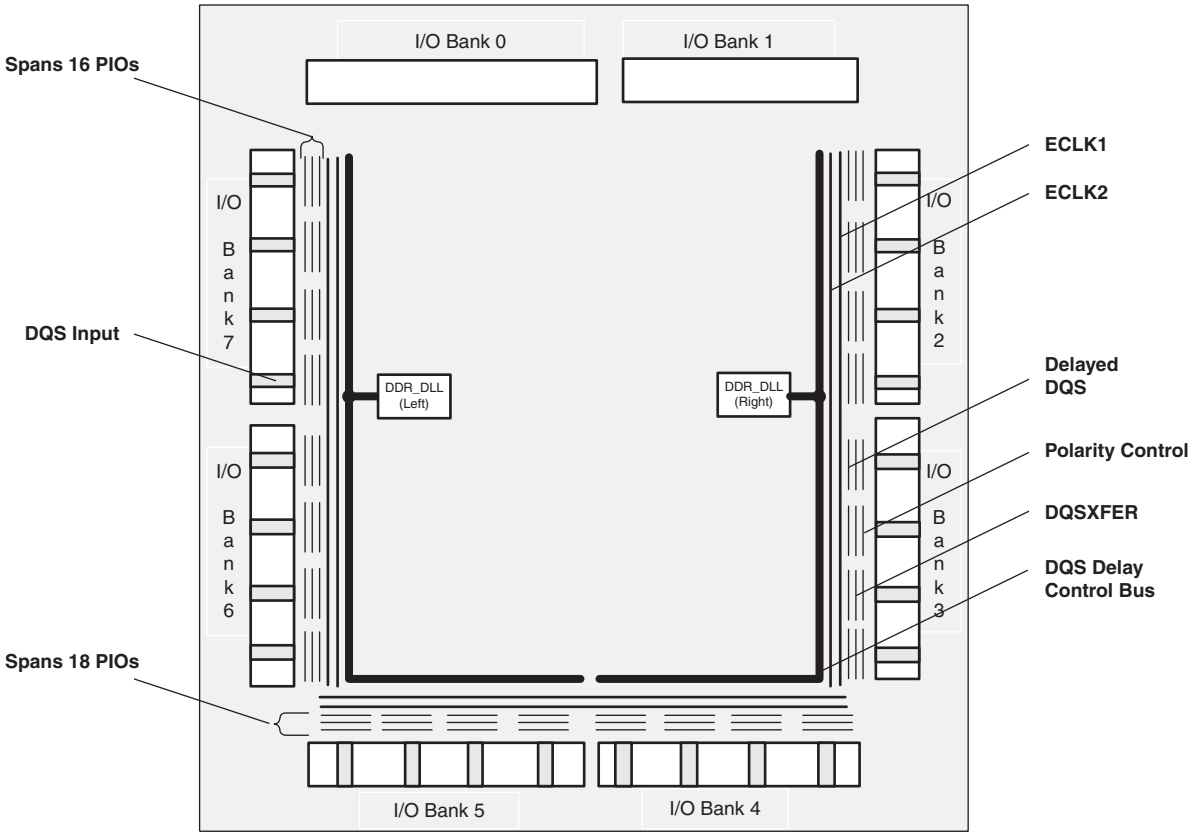

## DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-35 and Figure 2-36 show how the DQS transition signals are routed to the PIOs.

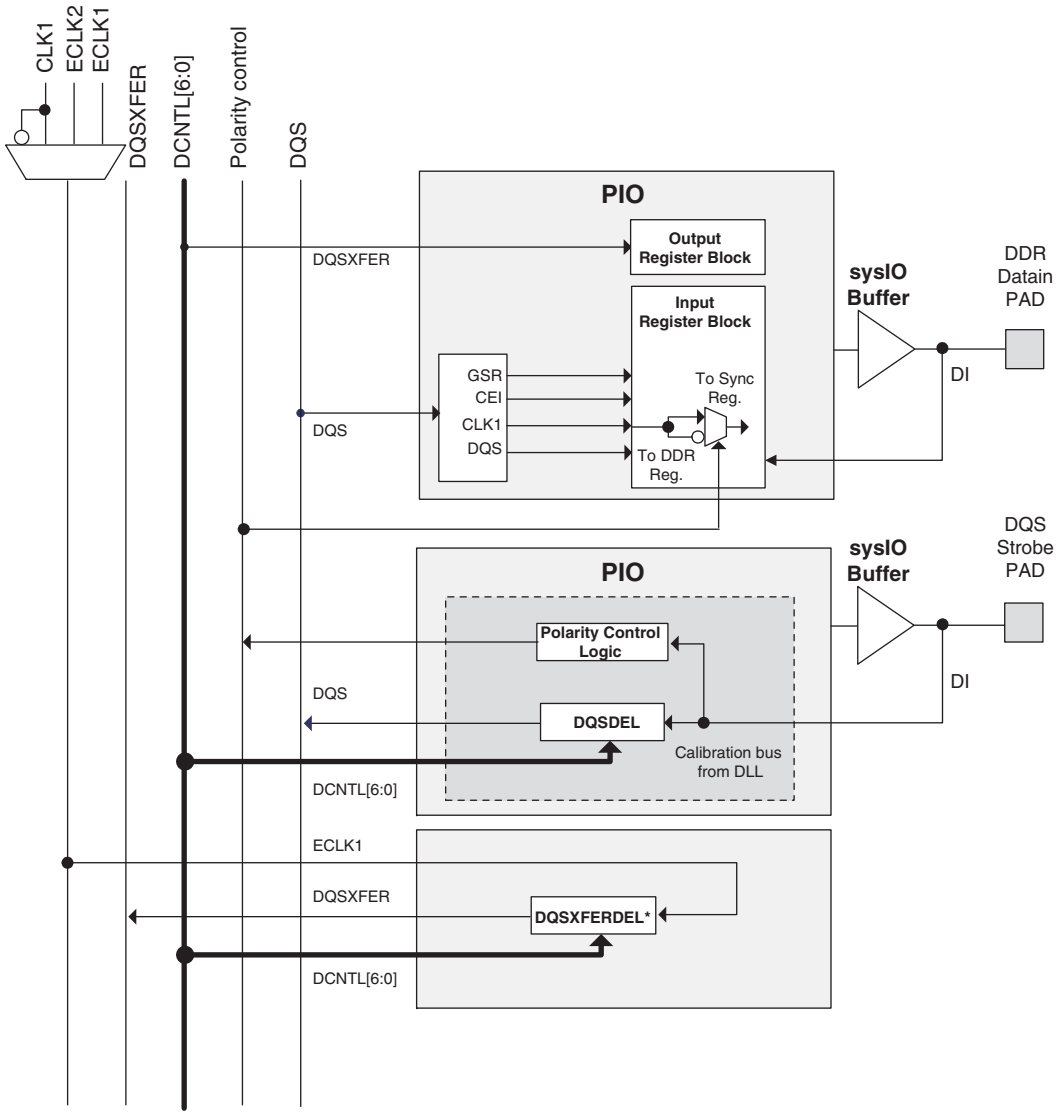
The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-35. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

*Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution*




Note: Bank 8 is not shown.

*Figure 2-36. DQS Local Bus*




*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

### DQSXFER

LatticeECP2/M devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

## sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

### sysI/O Buffer Banks

LatticeECP2/M devices have nine sysI/O buffer banks: eight banks for user I/Os arranged two per side. The ninth sysI/O buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage ($V_{CCIO}$). In addition, each bank, except Bank 8, has voltage references, $V_{REF1}$ and $V_{REF2}$, which allow it to be completely independent from the others. Bank 8 shares two voltage references, $V_{REF1}$ and $V_{REF2}$, with Bank 3. Figure 2-37 shows the nine banks and their associated supplies.

In LatticeECP2/M devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using $V_{CCIO}$. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of $V_{CCIO}$.

Each bank can support up to two separate $V_{REF}$ voltages, $V_{REF1}$ and $V_{REF2}$, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

*Figure 2-37. LatticeECP2 Banks*

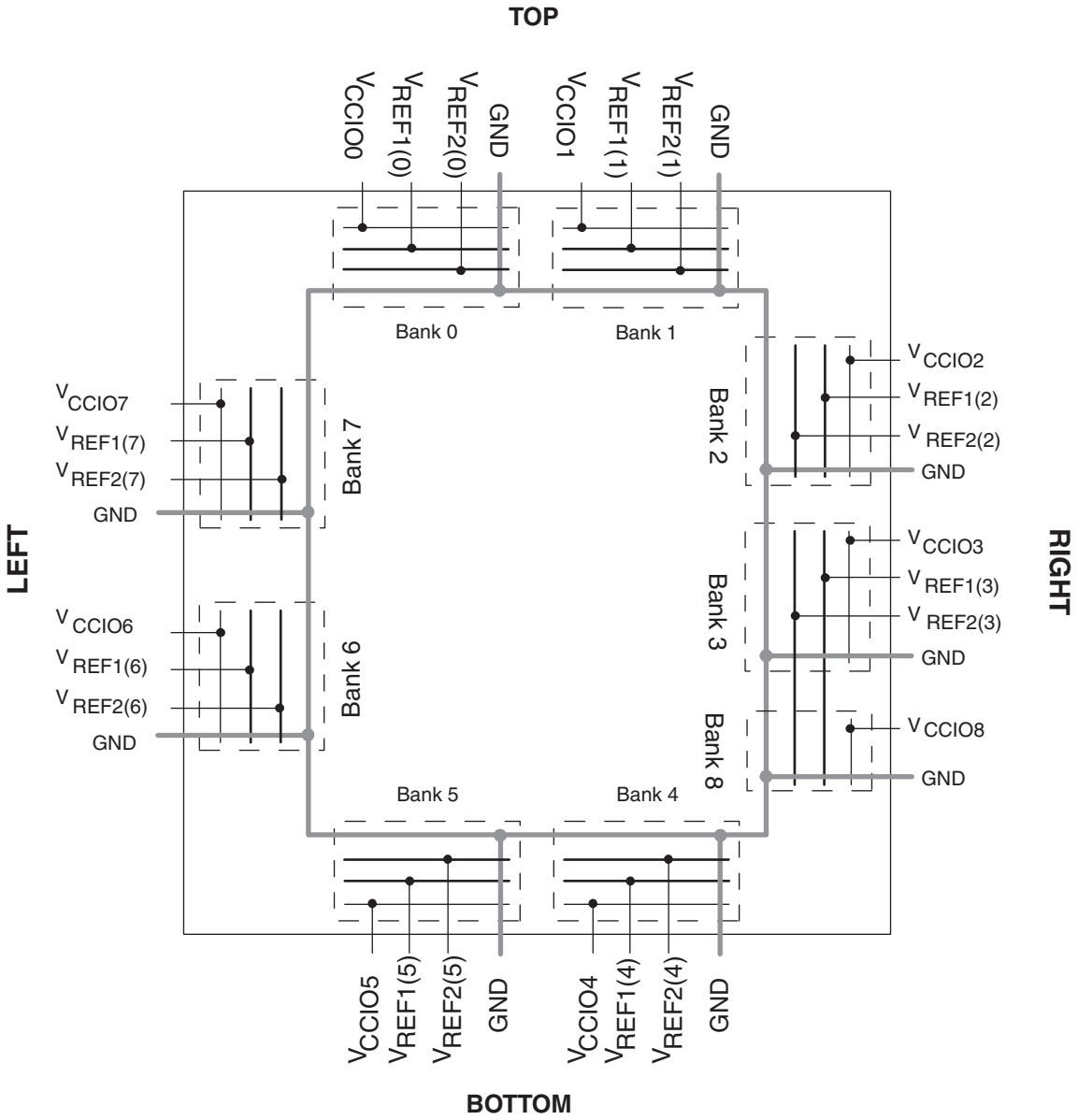
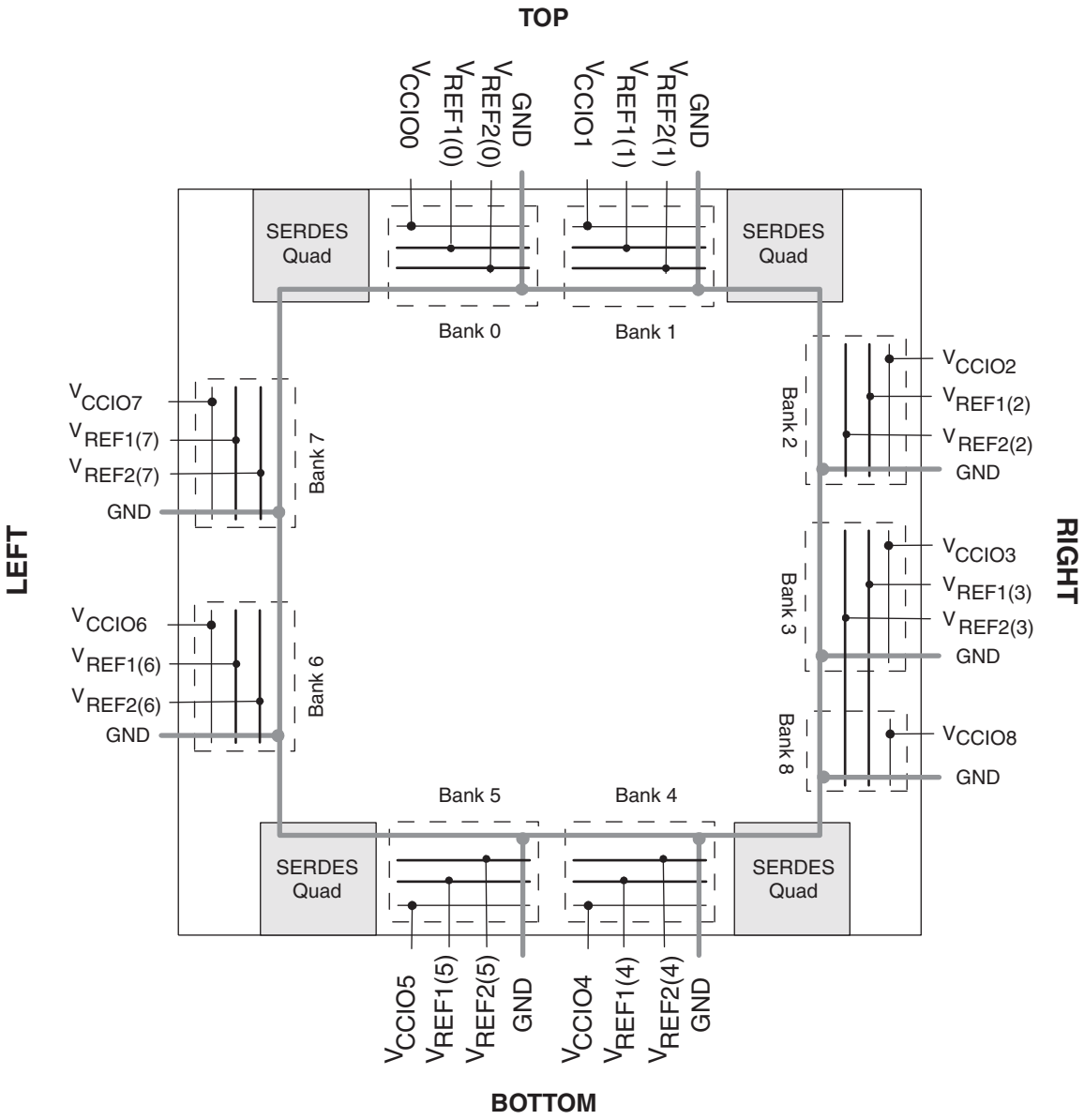


*Figure 2-38. LatticeECP2M Banks*




LatticeECP2/M devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Bottom (Bank 4 and Bank 5) sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the bottom banks of the device consist of two single-ended output drivers and two

sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

3. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

4. **Bank 8 sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in Bank 8 consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

In LatticeECP2 devices, only the I/Os on the bottom banks have programmable PCI clamps. In LatticeECP2M devices, the I/Os on the left and bottom banks have programmable PCI clamps.

## Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, $V_{CCIO8}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP2/M devices, see the list of additional technical documentation at the end of this data sheet.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered-up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

Prior to and throughout programming of the FPGA, the I/O of the device have a weak-pullup resistor to $V_{CCIO}$ on the input buffer and the output buffer is tri-stated. A pullup to $V_{CCIO}$ is present on the input until the user programs the input differently in the FPGA design. See the DC Electrical Characteristics table of this data sheet. The pullup value will be between 20-30K ohms based on the $V_{CCIO}$ voltage supplied on the board. This pullup will also remain active if the design does not use a particular I/O.

## Supported sysI/O Standards

The LatticeECP2/M sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/

O standards (together with their supply and reference voltages) supported by LatticeECP2/M devices. For further information about utilizing the sysI/O buffer to support a variety of standards please see the the list of additional technical information at the end of this data sheet.

***Table 2-13. Supported Input Standards***

| Input Standard | $V_{REF}$ (Nom.) | $V_{CCIO}$[1] (Nom.) |
|---|---|---|
| **Single Ended Interfaces** | | |
| LVTTL | — | — |
| LVCMOS33 | — | — |
| LVCMOS25 | — | — |
| LVCMOS18 | — | 1.8 |
| LVCMOS15 | — | 1.5 |
| LVCMOS12 | — | — |
| PCI 33 | — | 3.3 |
| HSTL18 Class I, II | 0.9 | — |
| HSTL15 Class I | 0.75 | — |
| SSTL3 Class I, II | 1.5 | — |
| SSTL2 Class I, II | 1.25 | — |
| SSTL18 Class I, II | 0.9 | — |
| **Differential Interfaces** | | |
| Differential SSTL18 Class I, II | — | — |
| Differential SSTL2 Class I, II | — | — |
| Differential SSTL3 Class I, II | — | — |
| Differential HSTL15 Class I | — | — |
| Differential HSTL18 Class I, II | — | — |
| LVDS, MLVDS, LVPECL, BLVDS, RSDS | — | — |

1 When not specified, $V_{CCIO}$ can be set anywhere in the valid operating range (page 3-1).

*Table 2-14. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA, 16mA, 20mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA, 16mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA, 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II | N/A | 1.8 |
| HSTL15 Class I | N/A | 1.5 |
| SSTL3 Class I, II | N/A | 3.3 |
| SSTL2 Class I, II | N/A | 2.5 |
| SSTL18 Class I, II | N/A | 1.8 |
| **Differential Interfaces** | | |
| Differential SSTL3, Class I, II | N/A | 3.3 |
| Differential SSTL2, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL15, Class I | N/A | 1.5 |
| LVDS | N/A | 2.5 |
| MLVDS[1] | N/A | 2.5 |
| BLVDS[1] | N/A | 2.5 |
| LVPECL[1] | N/A | 3.3 |
| RSDS[1] | N/A | 2.5 |
| LVCMOS33D[1] | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |

1. Emulated with external resistors. For more detail, please see information regarding additional technical documentation at the end of this data sheet.

## Hot Socketing

LatticeECP2/M devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeECP2/M ideal for many multiple power supply and hot-swap applications.

## SERDES and PCS (Physical Coding Sublayer)

LatticeECP2M devices feature up to 16 channels of embedded SERDES arranged in quads at the corners of the devices. Figure 2-39 shows the position of the quad blocks in relation to the PFU array for LatticeECP2M70 and LatticeECP2M100 devices. Table 2-15 shows the location of Quads for all the devices.

Each quad contains four dedicated SERDES (Ch0 to Ch3) for high-speed, full-duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains digital logic to support an array of popular data protocols. PCS also contains logic to the interface to FPGA core.

***Figure 2-39. SERDES Quads (LatticeECP2M70/LatticeECP2M100)***

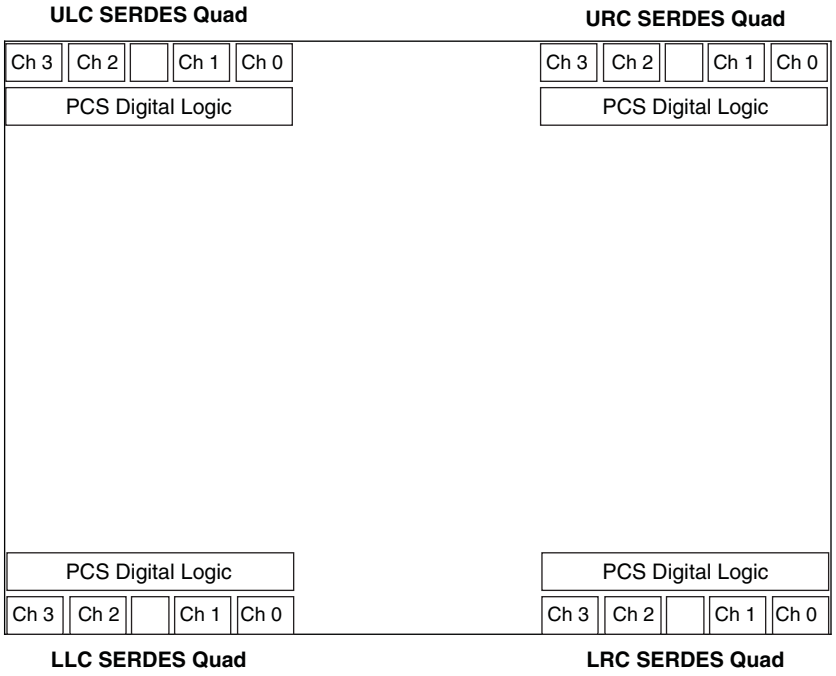



***Table 2-15. Available SERDES Quads per LatticeECP2M Devices***

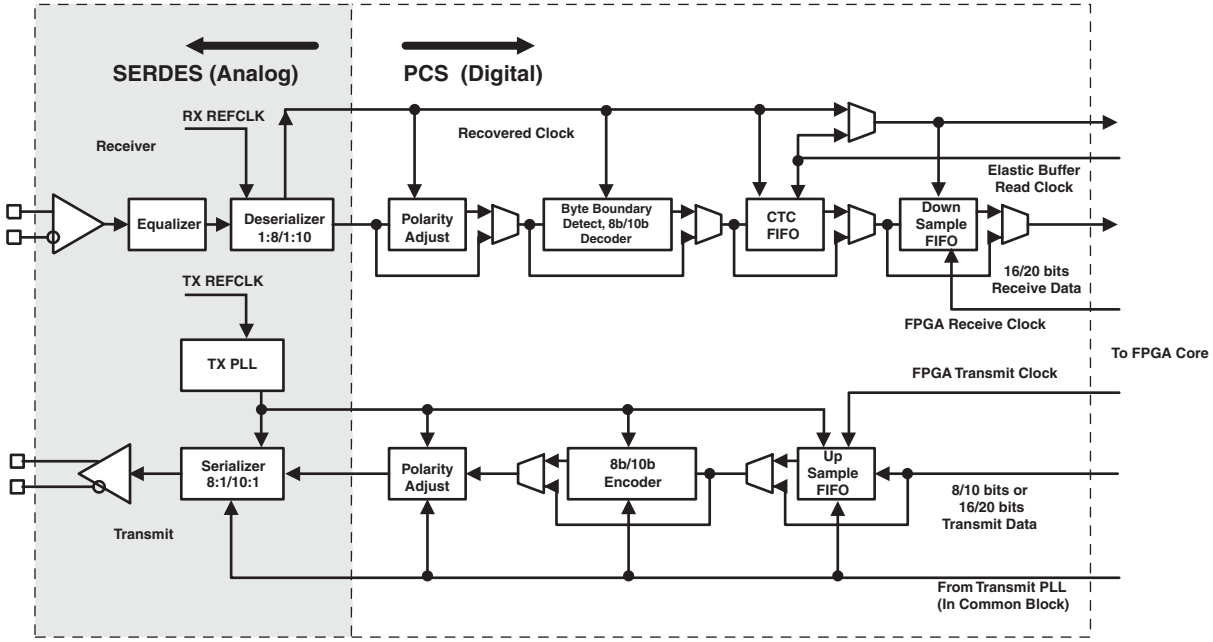
| Device | URC Quad | ULC Quad | LRC Quad | LLC Quad |
|---|---|---|---|---|
| ECP2M20 | Available | — | — | — |
| ECP2M35 | Available | — | — | — |
| ECP2M50 | Available | — | Available | — |
| ECP2M70 | Available | Available | Available | Available |
| ECP2M100 | Available | Available | Available | Available |

### SERDES Block

A differential receiver receives the serial encoded data stream, equalizes the signal, extracts the buried clock and de-serializes the data-stream before passing the 8- or 10-bit data to the PCS logic. The transmit channel receives the parallel (8- or 10-bit) encoded data, serializes the data and transmits the serial bit stream through the differential buffers. There is a single transmit clock per quad. Figure 2-40 shows a single channel SERDES and its interface to the PCS logic. Each SERDES receiver channel provides a recovered clock to the PCS block and to the FPGA core logic.

Each Transmit and Receive channel has its independent power supplies. The Output and Input buffers of each channel also have their own independent power supplies. In addition, there are separate power supplies for PLL, terminating resistor per quad.

***Figure 2-40. Simplified Channel Block Diagram for SERDES and PCS***




## PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer receivers and adjusts the polarity, detects, byte boundary, decodes (8b/10b) and provides Clock Tolerance Compensation (CTC) FIFO for changing the clock domain from receiver clock to the FPGA Clock.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, adjusts the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

## SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is a soft IP interface that allow the SERDES/PCS Quad block to be controlled by registers as opposed to the configuration memory cells. It is a simple register configuration interface.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With Diamond, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet and x4 PCI-Express and 4x Serial RapidIO can be implemented using IP (provided by Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

For further information about SERDES, please see the list of additional technical documentation at the end of this data sheet.

## IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP2/M devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage $V_{CCJ}$ and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

## Device Configuration

All LatticeECP2/M devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support both byte-wide and serial configuration, including the standard SPI Flash interface. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In- System Configuration specification. The sysCONFIG port is a 20-pin interface with six I/Os used as dedicated pins with the remainder used as dual-use pins. See TN1108, LatticeECP2/M sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

### Enhanced Configuration Option

LatticeECP2/M devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual boot image support.

1. **Decryption Support**
   LatticeECP2/M devices provide on-chip, One Time Programmable (OTP) non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM® command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology, for details.

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP2/M can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP2/M device can revert back to the original backup configuration and try again. This all can be done without power cycling the system.

For more information about device configuration, please see the list of additional technical documentation at the end of this data sheet.

### Soft Error Detect (SED) Support

LatticeECP2/M devices have dedicated logic to perform CRC checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP2 device can also be programmed

for checking soft errors (SED) in SRAM. SED can be run on a programmed device when the user logic is not active. If a soft error occurs, during user mode (normal operation) the device can be programmed to either reload from a known good boot image or generate an error signal.

For further information about Soft Error Detect (SED) support, please see the list of additional technical documentation at the end of this data sheet.

### External Resistor

LatticeECP2/M devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

### On-Chip Oscillator

Every LatticeECP2/M device has an internal CMOS oscillator which is used to derive a Master Clock for configuration. The oscillator and the Master Clock run continuously and are available to user logic after configuration is completed. The software default value of the Master Clock is 2.5MHz. Table 2-16 lists all the available Master Configuration Clock frequencies for normal non-encrypted mode and encrypted mode. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the Master Clock frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information about the use of this oscillator for configuration or user mode, please see the list of additional technical documentation at the end of this data sheet.

***Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration***

| Non-Encrypted Mode CCLK (MHz) | | | Encrypted Mode CCLK (MHz) |
|---|---|---|---|
| 2.5[1] | 13.0 | 45.0 | 2.5[1] |
| 4.3 | 15.0 | 55.0 | 5.4 |
| 5.4 | 20.0 | 60.0 | 10.0 |
| 6.9 | 26.0 | — | — |
| 8.1 | 30.0 | — | — |
| 9.2 | 34.0 | — | — |
| 10.0 | 41.0 | 130.0 | — |

1. Software default frequency.

## Density Shifting

The LatticeECP2/M family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. Design migration between LatticeECP2 and LatticeECP2M families is not possible. For specific requirements relating to sysCONFIG pins of the ECP2M50, M70 and M100, see the Logic Signal Connections tables.

# LatticeECP2/M Family Data Sheet DC and Switching Characteristics

September 2013 Data Sheet DS1006

## Absolute Maximum Ratings[1, 2, 3]

Supply Voltage $V_{CC}$ . . . . . -0.5 to 1.32V

Supply Voltage $V_{CCAUX}$ . . . . . -0.5 to 3.75V

Supply Voltage $V_{CCJ}$ . . . . . -0.5 to 3.75V

Output Supply Voltage $V_{CCIO}$ . . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[4]. . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature (Tj) . . . . . +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions[7]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$[1, 4, 5] | Core Supply Voltage | 1.14 | 1.26 | V |
| $V_{CCAUX}$[1, 3, 4, 5] | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCPLL}$ | PLL Supply Voltage | 1.14 | 1.26 | V |
| $V_{CCIO}$[1, 2, 4] | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| $V_{CCJ}$[1] | Supply Voltage for IEEE 1149.1 Test Access Port | 1.14 | 3.465 | V |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | 0 | 85 | °C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | -40 | 100 | °C |
| **SERDES External Power Supply (For LatticeECP2M Family Only)** | | | | |
| $V_{CCIB}$ | Input Buffer Power Supply (1.2V) | 1.14 | 1.26 | V |
| | Input Buffer Power Supply (1.5V) | 1.425 | 1.575 | V |
| $V_{CCOB}$ | Output Buffer Power Supply (1.2V) | 1.14 | 1.26 | V |
| | Output Buffer Power Supply (1.5V) | 1.425 | 1.575 | V |
| $V_{CCAUX33}$ | Termination Resistor Switching Power Supply | 3.135 | 3.465 | V |
| $V_{CCRX}$[6] | Receive Power Supply | 1.14 | 1.26 | V |
| $V_{CCTX}$[6] | Transmit Power Supply | 1.14 | 1.26 | V |

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| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CCP}$[6] | PLL and Reference Clock Buffer Power | 1.14 | 1.26 | V |

1. If $V_{CCIO}$ or $V_{CCJ}$ is set to 1.2V, they must be connected to the same power supply as $V_{CC}$. If $V_{CCIO}$ or $V_{CCJ}$ is set to 3.3V, they must be connected to the same power supply as $V_{CCAUX}$. $V_{CCPLL}$ must be connected to the same power supply as $V_{CC}$ through careful filtering and decoupling.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCAUX}$ ramp rate must not exceed 30mV/µs during power-up when transitioning between 0V and 3.3V.
4. For proper power-up configuration, users must ensure that the configuration control signals such as the CFGx, INITN, PROGRAMN and DONE pins are driven to the proper logic levels when the device powers up. The device power-up is triggered by the last of $V_{CC}$, $V_{CCAUX}$ or $V_{CCIO8}$ supplies that reaches its minimum valid levels. Alternatively, if the configuration control signals are pulled up by $V_{CCIO8}$, the $V_{CCIO8}$ (configuration I/O bank) voltage must be powered up prior to or at the same time as the last of VCC or VCCAUX reaches its minimum levels.
5. For power-up, $V_{CC}$ must reach its valid minimum value before powering up $V_{CCAUX}$ (LatticeECP2/M “S” version devices only).
6. $V_{CCRX}$,$V_{CCTX}$ and $V_{CCP}$ must be tied together in each quad and all quads need to be powered up.
7. For more power supply design recommendations, refer to TN1114 Electrical Recommendations for Lattice SERDES.

## Hot Socketing Specifications[1, 2, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DK}$ | Input or I/O leakage current | $0 \le V_{IN} \le V_{IH}$ (MAX.) | — | — | +/-1000 | µA |
| $I_{HDIN}$[5] | SERDES average input current when device is powered down and inputs are driven | | — | — | 4 | mA |

1. $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ should rise/fall monotonically. $V_{CC}$ and $V_{CCPLL}$ must be connected to the same power supply (applies to ECP2-6, ECP2-12 and ECP2-20 only).
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.
5. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed $V_{CCIB}$ of 1.575V, 8b10b data and internal AC coupling.

## ESD Performance

Please refer to LatticeECP2/M Product Family Qualification Summary for complete qualification data, including ESD performance.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2] | Input or I/O Low Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| $I_{IH}$[1, 3] | Input or I/O High Leakage | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 150 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -210 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 210 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 210 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | -210 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1[4] | I/O Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 8 | pf |
| C2[4] | Dedicated Input Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 6 | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. When used as $V_{REF}$, maximum leakage = 25uA
3. Applicable to general purpose I/Os in top and bottom banks.
4. $T_A$ 25°C, f = 1.0MHz.

## LatticeECP2 Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | ECP2-6 | 10 | mA |
| | | ECP2-12 | 20 | mA |
| | | ECP2-20 | 30 | mA |
| | | ECP2-35 | 50 | mA |
| | | ECP2-50 | 70 | mA |
| | | ECP2-70 | 100 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP2-6 | 24 | mA |
| | | ECP2-12 | 24 | mA |
| | | ECP2-20 | 24 | mA |
| | | ECP2-35 | 24 | mA |
| | | ECP2-50 | 24 | mA |
| | | ECP2-70 | 24 | mA |
| $I_{CCGPLL}$ | GPLL Power Supply Current (per GPLL) | ECP2-35, -50, -70 Only | 0.5 | mA |
| $I_{CCSPLL}$ | GPLL Power Supply Current (per SPLL) | ECP2-35, -50, -70 Only | 0.5 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP2-6 | 2 | mA |
| | | ECP2-12 | 2 | mA |
| | | ECP2-20 | 2 | mA |
| | | ECP2-35 | 2 | mA |
| | | ECP2-50 | 2 | mA |
| | | ECP2-70 | 2 | mA |
| $I_{CCJ}$ | VCCJ Power Supply Current | All Devices | 3 | mA |

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 25°C, power supplies at normal voltage.

## LatticeECP2M Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | ECP2M20 | 25 | mA |
| | | ECP2M35 | 50 | mA |
| | | ECP2M50 | 85 | mA |
| | | ECP2M70 | 100 | mA |
| | | ECP2M100 | 100 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP2M20 | 24 | mA |
| | | ECP2M35 | 24 | mA |
| | | ECP2M50 | 24 | mA |
| | | ECP2M70 | 24 | mA |
| | | ECP2M100 | 24 | mA |
| $I_{CCGPLL}$ | GPLL Power Supply Current (per GPLL) | All Devices | 0.5 | mA |
| $I_{CCSPLL}$ | GPLL Power Supply Current (per SPLL) | All Devices | 0.5 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP2M20 | 2 | mA |
| | | ECP2M35 | 2 | mA |
| | | ECP2M50 | 2 | mA |
| | | ECP2M70 | 2 | mA |
| | | ECP2M100 | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply Current | All Devices | 3 | mA |

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 25°C, power supplies at normal voltage.

## LatticeECP2 Initialization Supply Current[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5, 6, 7] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | ECP2-6 | 34 | mA |
| | | ECP2-12 | 54 | mA |
| | | ECP2-20 | 82 | mA |
| | | ECP2-35 | 135 | mA |
| | | ECP2-50 | 187 | mA |
| | | ECP2-70 | 267 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP2-6 | 30 | mA |
| | | ECP2-12 | 30 | mA |
| | | ECP2-20 | 30 | mA |
| | | ECP2-35 | 30 | mA |
| | | ECP2-50 | 30 | mA |
| | | ECP2-70 | 30 | mA |
| $I_{CCGPLL}$ | GPLL Power Supply Current (per GPLL) | ECP2-35, -50, -70 Only | 0.5 | mA |
| $I_{CCSPLL}$ | SPLL Power Supply Current (per SPLL) | ECP2-35, -50, -70 Only | 0.5 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (per Bank) | All Devices | 3 | mA |
| $I_{CCJ}$ | VCCJ Power Supply Current | All Devices | 4 | mA |

1. Until DONE signal is active.
2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
4. Frequency 0MHz.
5. $T_J$ = 25°C, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

## LatticeECP2M Initialization Supply Current[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5, 6, 7] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | ECP2M20 | 41 | mA |
| | | ECP2M35 | 107 | mA |
| | | ECP2M50 | 169 | mA |
| | | ECP2M70 | 254 | mA |
| | | ECP2M100 | 378 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP2M20 | 30 | mA |
| | | ECP2M35 | 30 | mA |
| | | ECP2M50 | 30 | mA |
| | | ECP2M70 | 30 | mA |
| | | ECP2M100 | 30 | mA |
| $I_{CCGPLL}$ | GPLL Power Supply Current (per GPLL) | All Devices | 0.5 | mA |
| $I_{CCSPLL}$ | SPLL Power Supply Current (per SPLL) | All Devices | 0.5 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (per Bank) | All Devices | 3 | mA |
| $I_{CCJ}$ | VCCJ Power Supply Current | All Devices | 4 | mA |

1. Until DONE signal is active.
2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
4. Frequency 0MHz.
5. $T_J$ = 25ºC, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

## SERDES Power Supply Requirements (LatticeECP2M Family Only)[1]

**Over Recommended Operating Conditions**

| Symbol | Description | Typ.[2] | Units |
|---|---|---|---|
| **Standby (Power Down)** | | | |
| $I_{CCTX-SB}$ | $V_{CCTX}$ current (per channel) | 10 | µA |
| $I_{CCRX-SB}$ | $V_{CCRX}$ current (per channel) | 75 | µA |
| $I_{CCIB-SB}$ | Input buffer current (per channel) | 0 | µA |
| $I_{CCOB-SB}$ | Output buffer current (per channel) | 0 | µA |
| $I_{CCP-SB}$ | SERDES PLL current (per quad) | 30 | µA |
| $I_{CCAX33-SB}$ | SERDES termination current (per quad) | 10 | µA |
| **Operating (Data Rate = 3.125 Gbps)** | | | |
| $I_{CCTX-OP}$ | $V_{CCTX}$ current (per channel) | 19 | mA |
| $I_{CCRX-OP}$ | $V_{CCRX}$ current (per channel) | 34 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 4 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 13 | mA |
| $I_{CCP-OP}$ | SERDES PLL current (per quad) | 26 | mA |
| $I_{CCAX33-OP}$ | SERDES termination current (per quad) | 0.01 | mA |

1. Equalization enabled, pre-emphasis disabled.
2. $T_J$ = 25°C, power supplies at nominal voltage.

## SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

***Table 3-1. SERDES Power[1]***

| Symbol | Description | Typ.[2] | Units |
|---|---|---|---|
| $P_{S-1CH-31}$ | SERDES power (one channel @ 3.125 Gbps) | 90 | mW |
| $P_{S-1CH-25}$ | SERDES power (one channel @ 2.5 Gbps) | 87 | mW |
| $P_{S-1CH-12}$ | SERDES power (one channel @ 1.25 Gbps) | 86 | mW |
| $P_{S-1CH-02}$ | SERDES power (one channel @ 250 Mbps) | 76 | mW |

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
2. Typical values measured at 25ºC and 1.2V.

## sysI/O Recommended Operating Conditions

| Standard | $V_{CCIO}$ | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| LVCMOS 2.5[2] | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 1.2[2] | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI | 3.135 | 3.3 | 3.465 | — | — | — |
| SSTL18[2] Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL2[2] Class I, II | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL3[2] Class I, II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL[2] 15 Class I | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL[2] 18 Class I, II | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| LVDS[2] | 2.375 | 2.5 | 2.625 | — | — | — |
| MLVDS25[1] | 2.375 | 2.5 | 2.625 | — | — | — |
| LVPECL33[1, 2] | 3.135 | 3.3 | 3.465 | — | — | — |
| BLVDS25[1, 2] | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS[1, 2] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL18D_I[2], II[2] | 1.71 | 1.8 | 1.89 | — | — | — |
| SSTL25D_ I[2], II[2] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL33D_ I[2], II[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| HSTL15D_ I[2] | 1.425 | 1.5 | 1.575 | — | — | — |
| HSTL18D_ I[2], II[2] | 1.71 | 1.8 | 1.89 | — | — | — |

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of $V_{CCIO}$.

## sysI/O Single-Ended DC Electrical Characteristics

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.5 | -0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8, 4 | -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 | -0.3 | 0.35 $V_{CC}$ | 0.65 $V_{CC}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| PCI | -0.3 | 0.3 $V_{CCIO}$ | 0.5 $V_{CCIO}$ | 3.6 | 0.1 $V_{CCIO}$ | 0.9 $V_{CCIO}$ | 1.5 | -0.5 |
| SSTL3 Class I | -0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.7 | $V_{CCIO}$ - 1.1 | 8 | -8 |
| SSTL3 Class II | -0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.5 | $V_{CCIO}$ - 0.9 | 16 | -16 |
| SSTL2 Class I | -0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.54 | $V_{CCIO}$ - 0.62 | 7.6 | -7.6 |
| | | | | | | | 12 | -12 |
| SSTL2 Class II | -0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.35 | $V_{CCIO}$ - 0.43 | 15.2 | -15.2 |
| | | | | | | | 20 | -20 |
| SSTL18 Class I | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6.7 | -6.7 |
| SSTL18 Class II | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.28 | $V_{CCIO}$ - 0.28 | 8 | -8 |
| | | | | | | | 11 | -11 |
| HSTL Class I | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | -4 |
| | | | | | | | 8 | -8 |
| HSTL18 Class I | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | -8 |
| | | | | | | | 12 | -12 |
| HSTL18 Class II | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | -16 |

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

# sysI/O Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | | 0 | — | 2.4 | V |
| $V_{CM}$ | Input Common Mode Voltage | Half the Sum of the Two Inputs | 0.05 | — | 2.35 | V |
| $V_{THD}$ | Differential Input Threshold | Difference Between the Two Inputs | +/-100 | — | — | mV |
| $I_{IN}$ | Input Current | Power On or Power Off | — | — | +/-10 | µA |
| $V_{OH}$ | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output Low Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output Voltage Differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| ýV$_{OD}$ | Change in $V_{OD}$ Between High and Low | | — | — | 50 | mV |
| $V_{OS}$ | Output Voltage Offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.20 | 1.375 | V |
| ýV$_{OS}$ | Change in $V_{OS}$ Between H and L | | — | — | 50 | mV |
| $I_{SA}$ | Output Short Circuit Current | $V_{OD}$ = 0V Driver Outputs Shorted to Ground | — | — | 24 | mA |
| $I_{SAB}$ | Output Short Circuit Current | $V_{OD}$ = 0V Driver Outputs Shorted to Each Other | — | — | 12 | mA |

## Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

## LVDS25E

The top and bottom sides of LatticeECP2/M devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

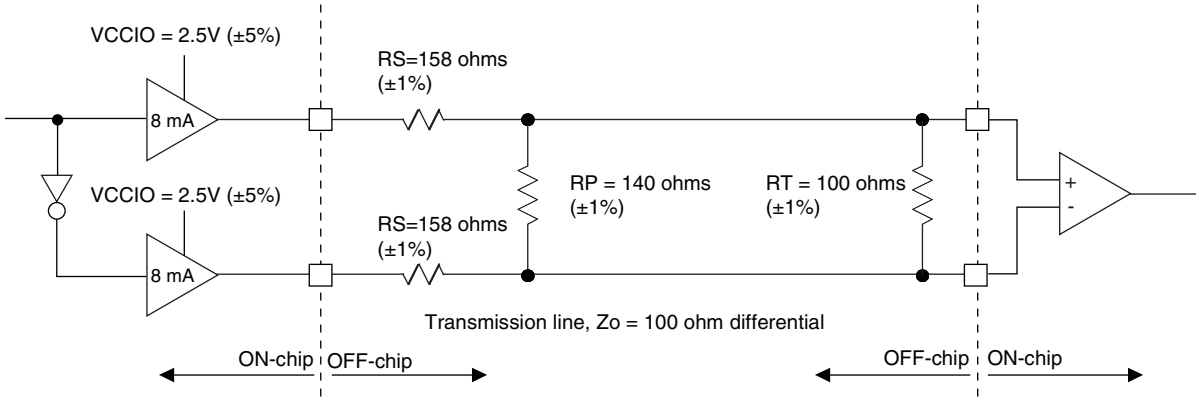



***Table 3-2. LVDS25E DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 158 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 140 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 1.43 | V |
| $V_{OL}$ | Output Low Voltage | 1.07 | V |
| $V_{OD}$ | Output Differential Voltage | 0.35 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 6.03 | mA |

## LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

## BLVDS

The LatticeECP2/M devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-2. BLVDS Multi-point Output Example***

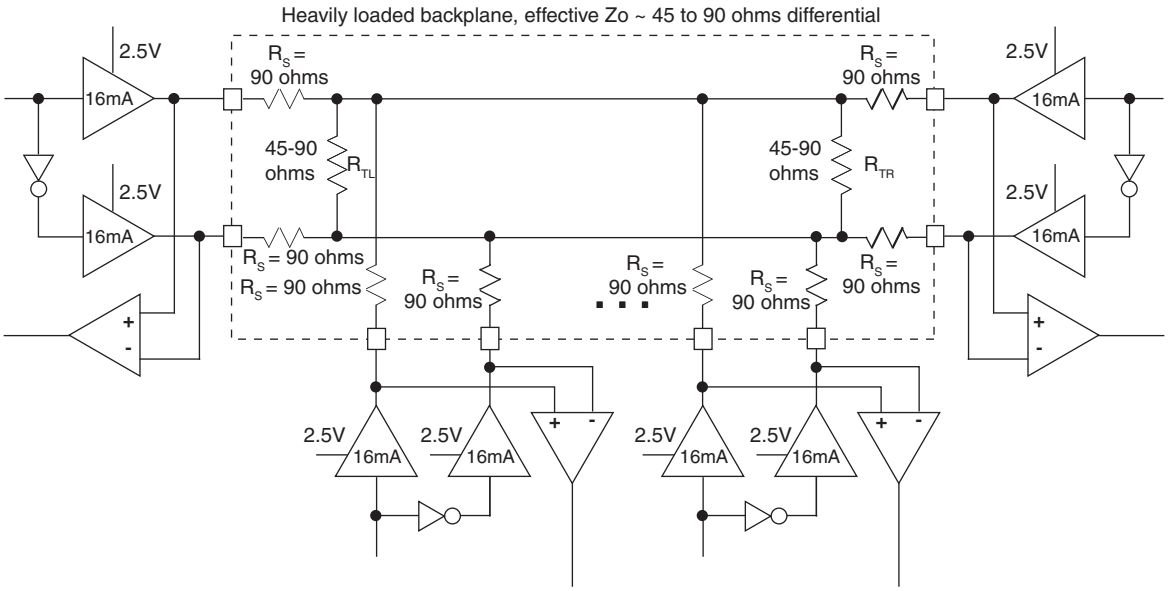



***Table 3-3. BLVDS DC Conditions[1]***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo = 45Ω | Zo = 90Ω | |
| $V_{CCIO}$ | Output Driver Supply (+/- 5%) | 2.50 | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 10.00 | 10.00 | Ω |
| $R_S$ | Driver Series Resistor (+/- 1%) | 90.00 | 90.00 | Ω |
| $R_{TL}$ | Driver Parallel Resistor (+/- 1%) | 45.00 | 90.00 | Ω |
| $R_{TR}$ | Receiver Termination (+/- 1%) | 45.00 | 90.00 | Ω |
| $V_{OH}$ | Output High Voltage | 1.38 | 1.48 | V |
| $V_{OL}$ | Output Low Voltage | 1.12 | 1.02 | V |
| $V_{OD}$ | Output Differential Voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC Output Current | 11.24 | 10.20 | mA |

1. For input buffer, see LVDS table.

## LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

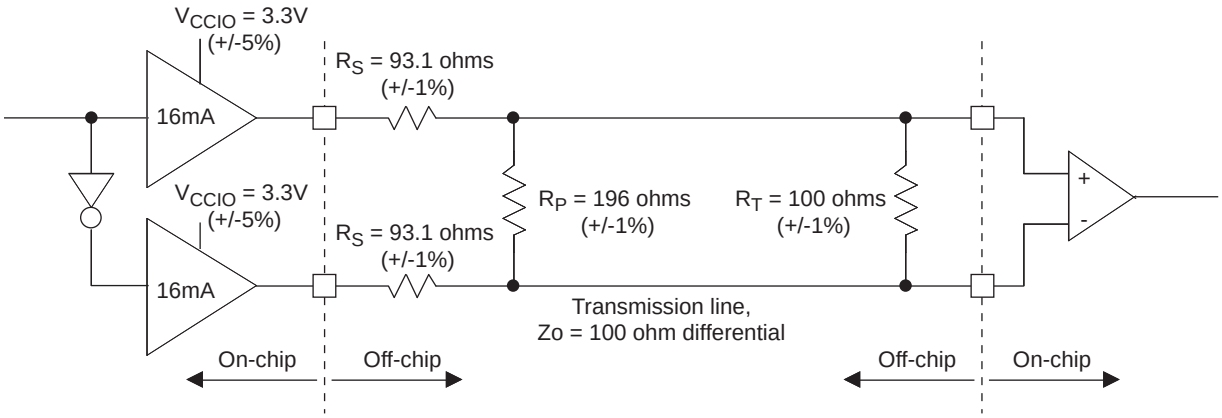



***Table 3-4. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 3.30 | V |
| $Z_{OUT}$ | Driver Impedance | 10 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 93 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 196 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 2.05 | V |
| $V_{OL}$ | Output Low Voltage | 1.25 | V |
| $V_{OD}$ | Output Differential Voltage | 0.80 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.65 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 12.11 | mA |

1. For input buffer, see LVDS table.

## RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

***Figure 3-4. RSDS (Reduced Swing Differential Signaling)***

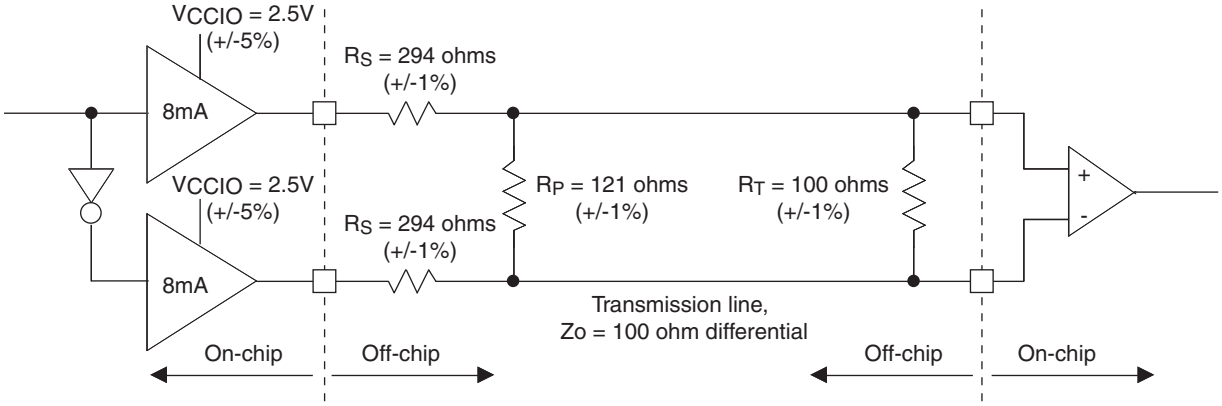



***Table 3-5. RSDS DC Conditions[1]***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 294 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 121 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 1.35 | V |
| $V_{OL}$ | Output Low Voltage | 1.15 | V |
| $V_{OD}$ | Output Differential Voltage | 0.20 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 101.5 | Ω |
| $I_{DC}$ | DC Output Current | 3.66 | mA |

1. For input buffer, see LVDS table.

## MLVDS

The LatticeECP2/M devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

***Figure 3-5. MLVDS (Multipoint Low Voltage Differential Signaling)***

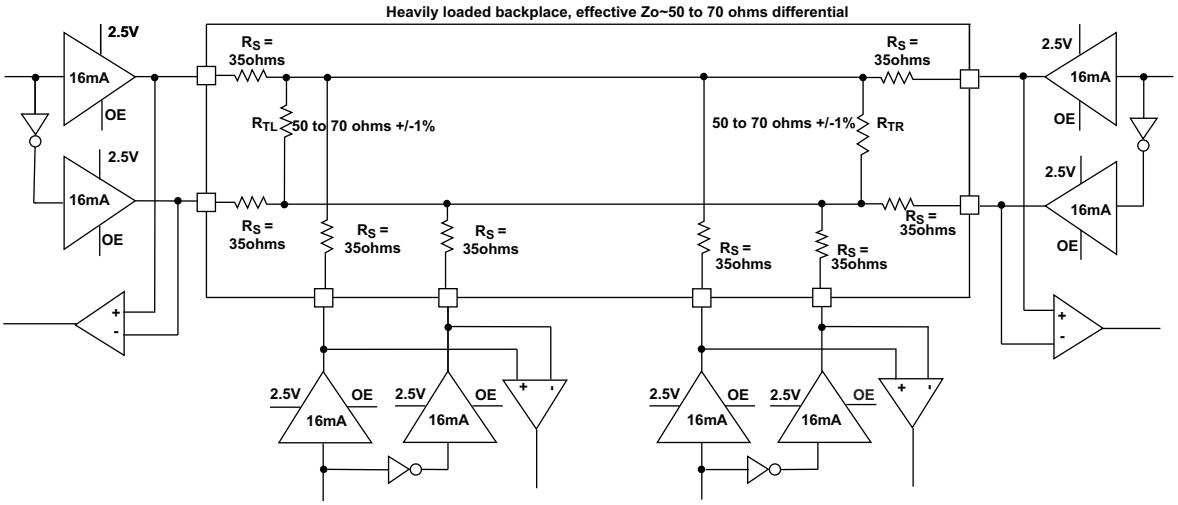



***Table 3-6. MLVDS DC Conditions[1]***

| Parameter | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo=50Ω | Zo=70Ω | |
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 2.50 | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 10.00 | 10.00 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 35.00 | 35.00 | Ω |
| $R_{TL}$ | Driver Parallel Resistor (+/-1%) | 50.00 | 70.00 | Ω |
| $R_{TR}$ | Receiver Termination (+/-1%) | 50.00 | 70.00 | Ω |
| $V_{OH}$ | Output High Voltage | 1.52 | 1.60 | V |
| $V_{OL}$ | Output Low Voltage | 0.98 | 0.90 | V |
| $V_{OD}$ | Output Differential Voltage | 0.54 | 0.70 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC Output Current | 21.74 | 20.00 | mA |

1. For input buffer, see LVDS table.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

# Typical Building Block Function Performance[1]

## Pin-to-Pin Performance (LVCMOS25 12mA Drive)

| Function | -7 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Decoder | 3.8 | ns |
| 32-bit Decoder | 4.5 | ns |
| 64-bit Decoder | 5.0 | ns |
| 4:1 MUX | 3.2 | ns |
| 8:1 MUX | 3.4 | ns |
| 16:1 MUX | 3.5 | ns |
| 32:1 MUX | 4.0 | ns |

1. These timing numbers were generated using the ispLEVER 8.0 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

## Register-to-Register Performance

| Function | -7 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Decoder | 599 | MHz |
| 32-bit Decoder | 542 | MHz |
| 64-bit Decoder | 417 | MHz |
| 4:1 MUX | 847 | MHz |
| 8:1 MUX | 803 | MHz |
| 16:1 MUX | 660 | MHz |
| 32:1 MUX | 577 | MHz |
| 8-bit Adder | 591 | MHz |
| 16-bit Adder | 500 | MHz |
| 64-bit Adder | 306 | MHz |
| 16-bit Counter | 488 | MHz |
| 32-bit Counter | 378 | MHz |
| 64-bit Counter | 260 | MHz |
| 64-bit Accumulator | 253 | MHz |
| **Embedded Memory Functions** | | |
| 512x36 Single Port RAM, EBR Output Registers | 370 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers) | 370 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers) | 280 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (One PFU) | 819 | MHz |
| 32x4 Pseudo-Dual Port RAM | 521 | MHz |
| 64x8 Pseudo-Dual Port RAM | 435 | MHz |
| **DSP Functions** | | |
| 18x18 Multiplier (All Registers) | 420 | MHz |
| 9x9 Multiplier (All Registers) | 420 | MHz |

## Register-to-Register Performance (Continued)

| Function | -7 Timing | Units |
|---|---|---|
| 36x36 Multiplier (All Registers) | 372 | MHz |
| 18x18 Multiplier/Accumulate (Input and Output Registers) | 295 | MHz |
| 18x18 Multiplier-Add/Sub-Sum (All Registers) | 420 | MHz |
| **DSP IP Functions** | | |
| 16-Tap Fully-Parallel FIR Filter | 304 | MHz |
| 1024-pt, Radix 4, Decimation in Frequency FFT | 227 | MHz |
| 8x8 Matrix Multiplier | 223 | MHz |

# Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

# LatticeECP2/M External Switching Characteristics[9]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (using Primary Clock without PLL)[1]** | | | | | | | | | |
| $t_{CO}$ | Clock to Output - PIO Output Register | LFE2-6 | — | 3.50 | — | 3.90 | — | 4.20 | ns |
| | | LFE2-12 | — | 3.50 | — | 3.90 | — | 4.20 | ns |
| | | LFE2-20 | — | 3.50 | — | 3.90 | — | 4.20 | ns |
| | | LFE2-35 | — | 3.50 | — | 3.90 | — | 4.20 | ns |
| | | LFE2-50 | — | 3.50 | — | 3.90 | — | 4.20 | ns |
| | | LFE2-70 | — | 3.70 | — | 4.10 | — | 4.40 | ns |
| | | LFE2M20 | — | 3.90 | — | 4.30 | — | 4.70 | ns |
| | | LFE2M35 | — | 3.90 | — | 4.30 | — | 4.70 | ns |
| | | LFE2M50 | — | 4.50 | — | 5.00 | — | 5.40 | ns |
| | | LFE2M70 | — | 4.50 | — | 5.00 | — | 5.40 | ns |
| | | LFE2M100 | — | 4.50 | — | 5.00 | — | 5.40 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | LFE2-6 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-12 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M100 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $t_{H}$ | Clock to Data Hold - PIO Input Register | LFE2-6 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-12 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-20 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-35 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-50 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-70 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M20 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M35 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M50 | 1.80 | — | 2.10 | — | 2.30 | — | ns |
| | | LFE2M70 | 1.80 | — | 2.10 | — | 2.30 | — | ns |
| | | LFE2M100 | 1.80 | — | 2.10 | — | 2.30 | — | ns |

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SU_DEL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | LFE2-6 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-12 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-20 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-35 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-50 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2-70 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M20 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M35 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M50 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M70 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | LFE2M100 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| $t_{H_DEL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | LFE2-6 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-12 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M100 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $f_{MAX_IO}$ | Clock Frequency of I/O Register and PFU Register | ECP2/M | — | 420 | — | 357 | — | 311 | MHz |
| **General I/O Pin Parameters (using Edge Clock without PLL)[1]** | | | | | | | | | |
| $t_{COE}$ | Clock to Output - PIO Output Register | LFE2-6 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2-12 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2-20 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2-35 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2-50 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2-70 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2M20 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2M35 | — | 2.60 | — | 2.90 | — | 3.20 | ns |
| | | LFE2M50 | — | 3.10 | — | 3.40 | — | 3.70 | ns |
| | | LFE2M70 | — | 3.10 | — | 3.40 | — | 3.70 | ns |
| | | LFE2M100 | — | 3.10 | — | 3.40 | — | 3.70 | ns |

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SUE}$ | Clock to Data Setup - PIO Input Register | LFE2-6 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-12 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M100 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $t_{HE}$ | Clock to Data Hold - PIO Input Register | LFE2-6 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2-12 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2-20 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2-35 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2-50 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2-70 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2M20 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2M35 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | LFE2M50 | 1.20 | — | 1.40 | — | 1.60 | — | ns |
| | | LFE2M70 | 1.20 | — | 1.40 | — | 1.60 | — | ns |
| | | LFE2M100 | 1.20 | — | 1.40 | — | 1.60 | — | ns |
| $t_{SU_DELE}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | LFE2-6 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | LFE2-12 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | LFE2-20 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | LFE2-35 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | LFE2-50 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | LFE2-70 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | LFE2M20 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | LFE2M35 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | LFE2M50 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | LFE2M70 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | LFE2M100 | 1.20 | — | 1.60 | — | 1.90 | — | ns |

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{H_DELE}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | LFE2-6 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-12 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M100 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $f_{MAX_IOE}$ | Clock Frequency of I/O and PFU Register | ECP2/M | — | 420 | — | 357 | — | 311 | MHz |
| **General I/O Pin Parameters (using Primary Clock with PLL)[1]** | | | | | | | | | |
| $t_{COPLL}$[10] | Clock to Output - PIO Output Register | LFE2-6 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2-12 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2-20 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2-35 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2-50 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2-70 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2M20 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2M35 | — | 2.30 | — | 2.60 | — | 2.80 | ns |
| | | LFE2M50 | — | 2.60 | — | 2.90 | — | 3.10 | ns |
| | | LFE2M70 | — | 2.60 | — | 2.90 | — | 3.10 | ns |
| | | LFE2M100 | — | 2.70 | — | 3.00 | — | 3.20 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | LFE2-6 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2-12 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2-20 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2-35 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2-50 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2-70 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2M20 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2M35 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2M50 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2M70 | 0.70 | — | 0.80 | — | 0.90 | — | ns |
| | | LFE2M100 | 0.80 | — | 0.90 | — | 1.00 | — | ns |

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | LFE2-6 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2-12 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2-20 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2-35 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2-50 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2-70 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2M20 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2M35 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2M50 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2M70 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | LFE2M100 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SU_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | LFE2-6 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2-12 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2-20 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2-35 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2-50 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2-70 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2M20 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2M35 | 1.80 | — | 2.00 | — | 2.20 | — | ns |
| | | LFE2M50 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | LFE2M70 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | LFE2M100 | 2.00 | — | 2.20 | — | 2.40 | — | ns |
| $t_{H_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | LFE2-6 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-12 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2-70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M35 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M50 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M70 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | LFE2M100 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| **DDR I/O Pin Parameters[2]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | ECP2/M | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | ECP2/M | 0.640 | — | 0.640 | — | 0.640 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS (DDR Write) | ECP2/M | 0.250 | — | 0.250 | — | 0.250 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS (DDR Write) | ECP2/M | 0.250 | — | 0.250 | — | 0.250 | — | UI |
| $f_{MAX_DDR}$ | DDR Clock Frequency[6] | ECP2/M | 95 | 200 | 95 | 166 | 95 | 133 | MHz |
| **DDR2 I/O Pin Parameters[3]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | ECP2/M | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | ECP2/M | 0.640 | — | 0.640 | — | 0.640 | — | UI |

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DQVBS}$ | Data Valid Before DQS (DDR Write) | ECP2/M | 0.250 | — | 0.250 | — | 0.250 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS (DDR Write) | ECP2/M | 0.250 | — | 0.250 | — | 0.250 | — | UI |
| $f_{MAX_DDR2}$ | DDR Clock Frequency | ECP2/M | 133 | 266 | 133 | 200 | 133 | 166 | MHz |
| **SPI4.2 I/O Pin Parameters Static Alignment[4, 8, 11]** | | | | | | | | | |
| | Maximum Data Rate | ECP2-20 | — | 750 | — | 622 | — | 622 | Mbps |
| | | ECP2-35 | — | 750 | — | 622 | — | 622 | Mbps |
| | | ECP2-50 | — | 750 | — | 622 | — | 622 | Mbps |
| | | ECP2-70 | — | 750 | — | 622 | — | 622 | Mbps |
| | | ECP2M20 | — | 622 | — | 622 | — | 622 | Mbps |
| | | ECP2M35 | — | 622 | — | 622 | — | 622 | Mbps |
| | | ECP2M50 | — | 622 | — | 622 | — | 622 | Mbps |
| | | ECP2M70 | — | 622 | — | 622 | — | 622 | Mbps |
| | | ECP2M100 | — | 622 | — | 622 | — | 622 | Mbps |
| $t_{DVACLKSPI}$ | Data Valid After CLK (Receive) | ECP2-20 | — | 0.25 | — | 0.25 | — | 0.25 | UI |
| | | ECP2-35 | — | 0.25 | — | 0.25 | — | 0.25 | UI |
| | | ECP2-50 | — | 0.25 | — | 0.25 | — | 0.25 | UI |
| | | ECP2-70 | — | 0.25 | — | 0.25 | — | 0.25 | UI |
| | | ECP2M20 | — | 0.21 | — | 0.21 | — | 0.21 | UI |
| | | ECP2M35 | — | 0.21 | — | 0.21 | — | 0.21 | UI |
| | | ECP2M50 | — | 0.21 | — | 0.21 | — | 0.21 | UI |
| | | ECP2M70 | — | 0.21 | — | 0.21 | — | 0.21 | UI |
| | | ECP2M100 | — | 0.21 | — | 0.21 | — | 0.21 | UI |
| $t_{DVECLKSPI}$ | Data Hold After CLK (Receive) | ECP2-20 | 0.75 | — | 0.75 | — | 0.75 | — | UI |
| | | ECP2-35 | 0.75 | — | 0.75 | — | 0.75 | — | UI |
| | | ECP2-50 | 0.75 | — | 0.75 | — | 0.75 | — | UI |
| | | ECP2-70 | 0.75 | — | 0.75 | — | 0.75 | — | UI |
| | | ECP2M20 | 0.79 | — | 0.79 | — | 0.79 | — | UI |
| | | ECP2M35 | 0.79 | — | 0.79 | — | 0.79 | — | UI |
| | | ECP2M50 | 0.79 | — | 0.79 | — | 0.79 | — | UI |
| | | ECP2M70 | 0.79 | — | 0.79 | — | 0.79 | — | UI |
| | | ECP2M100 | 0.79 | — | 0.79 | — | 0.79 | — | UI |
| $t_{DIASPI}$ | Data Invalid After Clock (Transmit) | ECP2-20 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-35 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-50 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-70 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2M20 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M35 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M50 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M70 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M100 | — | 230 | — | 230 | — | 230 | ps |

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DIBSPI}$ | Data Invalid Before Clock (Transmit) | ECP2-20 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-35 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-50 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-70 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2M20 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M35 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M50 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M70 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M100 | — | 230 | — | 230 | — | 230 | ps |
| **XGMII I/O Pin Parameters (312 Mbps)[5]** | | | | | | | | | |
| $t_{SUXGMII}$ | Data Setup Before Read Clock | ECP2/M | 480 | — | 480 | — | 480 | — | ps |
| $t_{HXGMII}$ | Data Hold After Read Clock | ECP2/M | 480 | — | 480 | — | 480 | — | ps |
| $t_{DVBCKXGMII}$ | Data Valid Before Clock | ECP2/M | 960 | — | 960 | — | 960 | — | ps |
| $t_{DVACKXGMII}$ | Data Valid After Clock | ECP2/M | 960 | — | 960 | — | 960 | — | ps |
| **Primary** | | | | | | | | | |
| $f_{MAX_PRI}$[7] | Frequency for Primary Clock Tree | ECP2/M | — | 420 | — | 357 | — | 311 | MHz |
| $t_{W_PRI}$ | Clock Pulse Width for Primary Clock | ECP2/M | 0.95 | — | 1.19 | — | 2.00 | — | ns |
| $t_{SKEW_PRI}$ | Primary Clock Skew Within a Bank | ECP2/M | — | 300 | — | 360 | — | 420 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX_EDGE}$[7] | Frequency for Edge Clock | ECP2/M | — | 420 | — | 357 | — | 311 | MHz |
| $t_{W_EDGE}$ | Clock Pulse Width for Edge Clock | ECP2/M | 0.95 | — | 1.19 | — | 2.00 | — | ns |
| $t_{SKEW_EDGE}$ | Edge Clock Skew Within an Edge of the Device | ECP2/M | — | 300 | — | 360 | — | 420 | ps |

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25 for BGA packages only.
3. DDR2 timing numbers based on SSTL18 for BGA packages only.
4. SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
5. XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
6. IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
7. Using the LVDS I/O standard.
8. ECP2-6 and ECP2-12 do not support SPI4.2
9. The AC numbers do not apply to PCLK6 and PCLK7.
10. Applies to CLKOP only.
11. Please refer to TN1159, LatticeECP2/M Pin Assignment Recommendations for best performance.

***Figure 3-6. SPI4.2 Parameters***

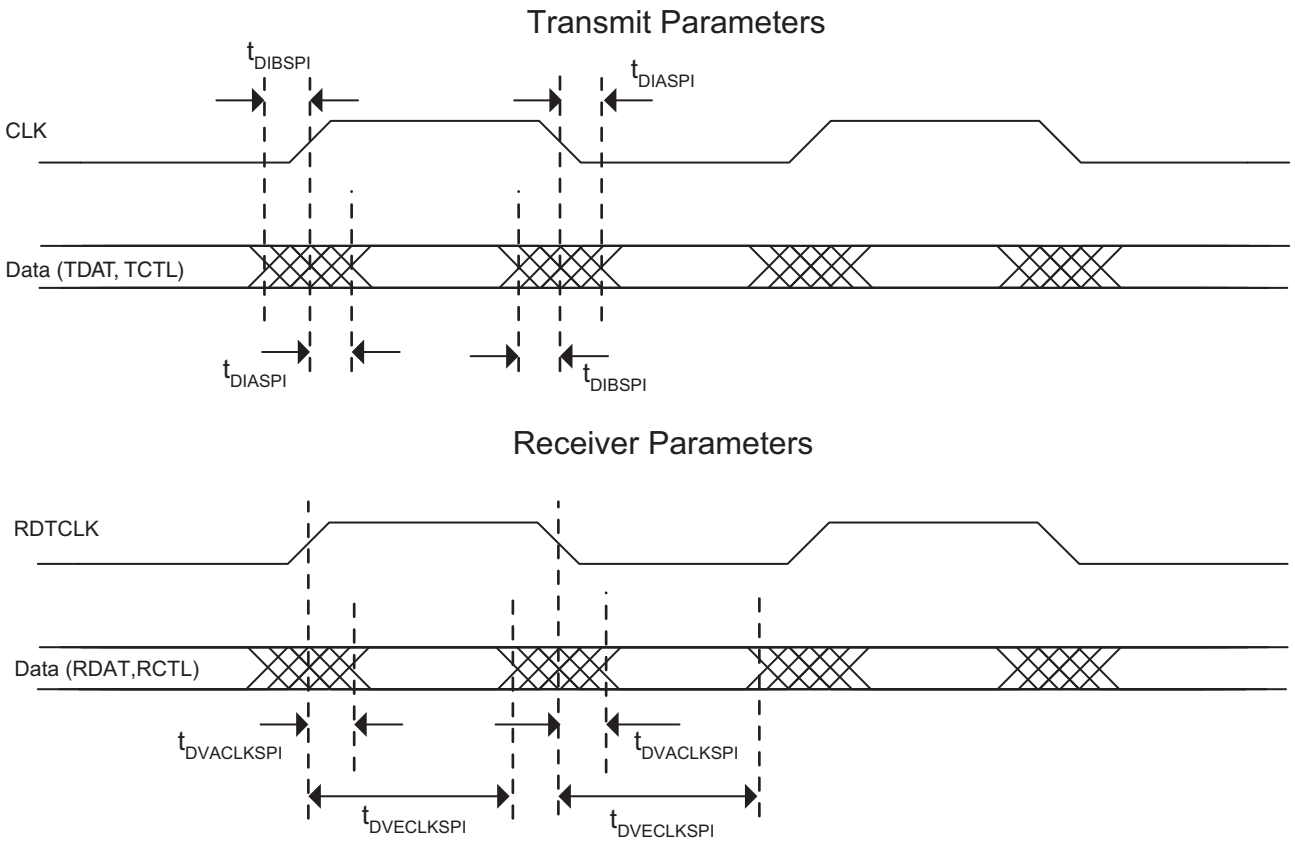


*Figure 3-7. DDR and DDR2 Parameters*

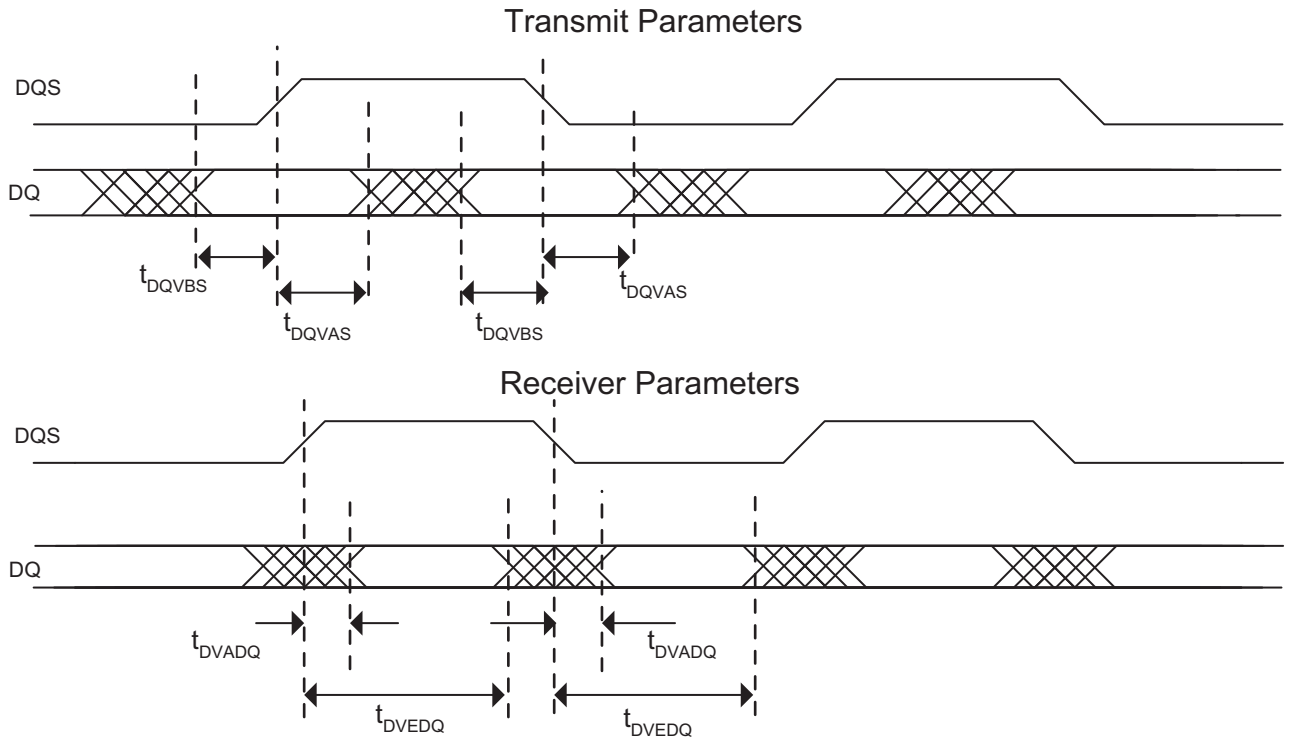
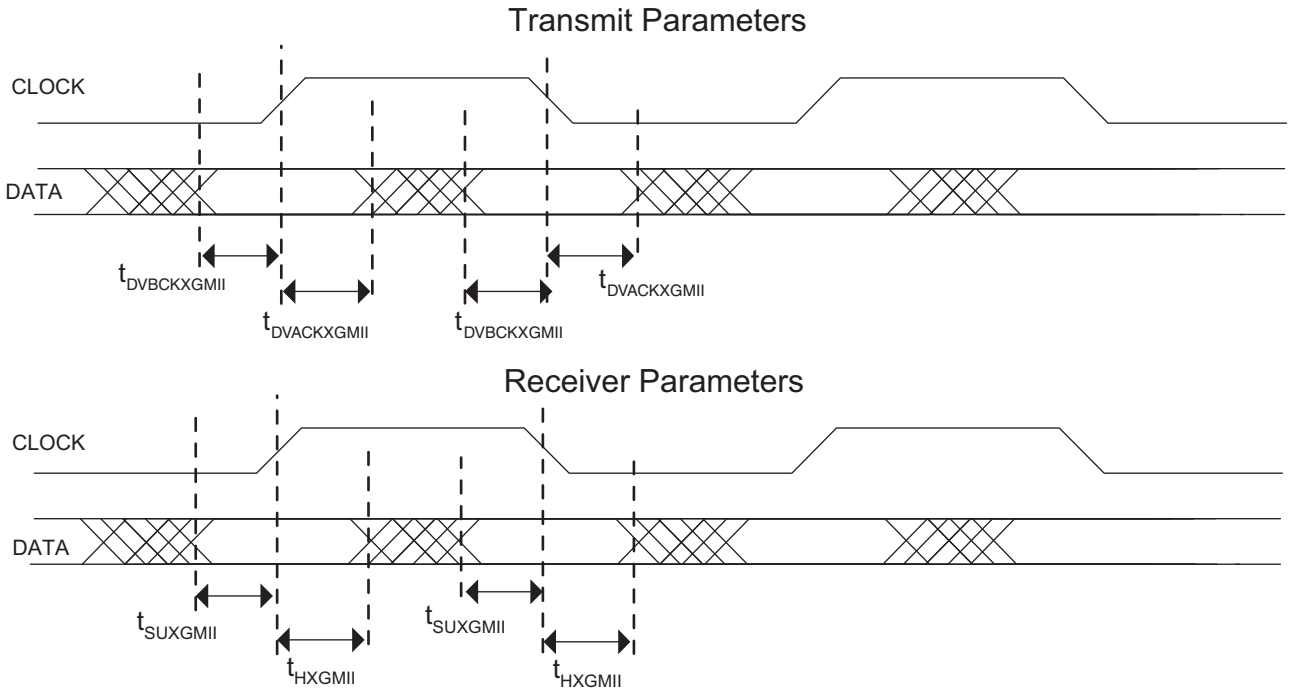



*Figure 3-8. XGMII Parameters*



# LatticeECP2/M Internal Switching Characteristics[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4_PFU}$ | LUT4 delay (A to D inputs to F output) | — | 0.180 | — | 0.198 | — | 0.216 | ns |
| $t_{LUT6_PFU}$ | LUT6 delay (A to D inputs to OFX output) | — | 0.304 | — | 0.331 | — | 0.358 | ns |
| $t_{LSR_PFU}$ | Set/Reset to output of PFU (Asynchronous) | — | 0.600 | — | 0.655 | — | 0.711 | ns |
| $t_{SUM_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.128 | — | 0.129 | — | 0.129 | — | ns |
| $t_{HM_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.051 | — | -0.049 | — | -0.046 | — | ns |
| $t_{SUD_PFU}$ | Clock to D input setup time | 0.061 | — | 0.071 | — | 0.081 | — | ns |
| $t_{HD_PFU}$ | Clock to D input hold time | 0.002 | — | 0.003 | — | 0.003 | — | ns |
| $t_{CK2Q_PFU}$ | Clock to Q delay, (D-type Register Configuration) | — | 0.285 | — | 0.309 | — | 0.333 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM_PFU}$ | Clock to Output (F Port) | — | 0.902 | — | 1.083 | — | 1.263 | ns |
| $t_{SUDATA_PFU}$ | Data Setup Time | -0.172 | — | -0.205 | — | -0.238 | — | ns |
| $t_{HDATA_PFU}$ | Data Hold Time | 0.199 | — | 0.235 | — | 0.271 | — | ns |
| $t_{SUADDR_PFU}$ | Address Setup Time | -0.245 | — | -0.284 | — | -0.323 | — | ns |
| $t_{HADDR_PFU}$ | Address Hold Time | 0.246 | — | 0.285 | — | 0.324 | — | ns |
| $t_{SUWREN_PFU}$ | Write/Read Enable Setup Time | -0.122 | — | -0.145 | — | -0.168 | — | ns |
| $t_{HWREN_PFU}$ | Write/Read Enable Hold Time | 0.132 | — | 0.156 | — | 0.180 | — | ns |
| **PIC Timing** | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN_PIO}$ | Input Buffer Delay (LVCMOS25) | — | 0.613 | — | 0.681 | — | 0.749 | ns |
| $t_{OUT_PIO}$ | Output Buffer Delay (LVCMOS25) | — | 1.115 | — | 1.115 | — | 1.343 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI_PIO}$ | Input Register Setup Time (Data Before Clock) | 0.596 | — | 0.645 | — | 0.694 | — | ns |
| $t_{HI_PIO}$ | Input Register Hold Time (Data after Clock) | -0.570 | — | -0.614 | — | -0.658 | — | ns |
| $t_{COO_PIO}$ | Output Register Clock to Output Delay | — | 0.61 | — | 0.66 | — | 0.72 | ns |
| $t_{SUCE_PIO}$ | Input Register Clock Enable Setup Time | 0.032 | — | 0.037 | — | 0.041 | — | ns |
| $t_{HCE_PIO}$ | Input Register Clock Enable Hold Time | -0.022 | — | -0.025 | — | -0.028 | — | ns |
| $t_{SULSR_PIO}$ | Set/Reset Setup Time | 0.184 | — | 0.201 | — | 0.217 | — | ns |
| $t_{HLSR_PIO}$ | Set/Reset Hold Time | -0.080 | — | -0.086 | — | -0.093 | — | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO_EBR}$ | Clock (Read) to output from Address or Data | — | 2.51 | — | 2.75 | — | 2.99 | ns |
| $t_{COO_EBR}$ | Clock (Write) to output from EBR output Register | — | 0.33 | — | 0.36 | — | 0.39 | ns |
| $t_{SUDATA_EBR}$ | Setup Data to EBR Memory | -0.157 | — | -0.181 | — | -0.205 | — | ns |
| $t_{HDATA_EBR}$ | Hold Data to EBR Memory | 0.173 | — | 0.195 | — | 0.217 | — | ns |
| $t_{SUADDR_EBR}$ | Setup Address to EBR Memory | -0.115 | — | -0.130 | — | -0.145 | — | ns |
| $t_{HADDR_EBR}$ | Hold Address to EBR Memory | 0.138 | — | 0.155 | — | 0.172 | — | ns |
| $t_{SUWREN_EBR}$ | Setup Write/Read Enable to PFU Memory | -0.128 | — | -0.149 | — | -0.170 | — | ns |

# LatticeECP2/M Internal Switching Characteristics[1] (Continued)

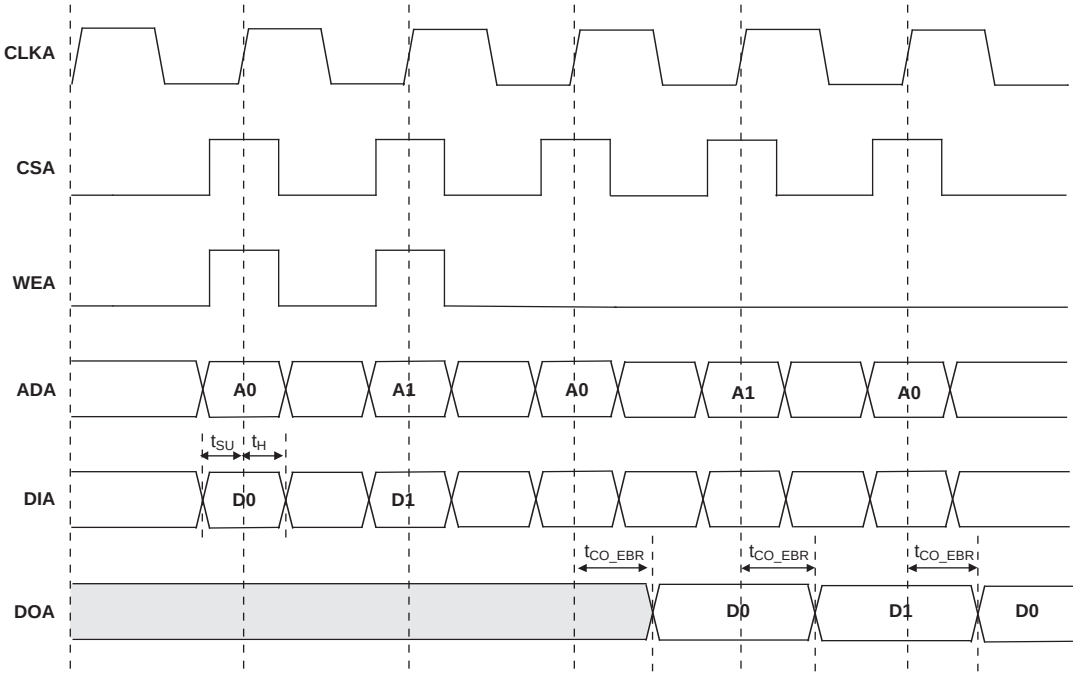
**Over Recommended Operating Conditions**

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HWREN_EBR}$ | Hold Write/Read Enable to PFU Memory | 0.139 | — | 0.156 | — | 0.173 | — | ns |
| $t_{SUCE_EBR}$ | Clock Enable Setup Time to EBR Output Register | 0.123 | — | 0.134 | — | 0.145 | — | ns |
| $t_{HCE_EBR}$ | Clock Enable Hold Time to EBR Output Register | -0.081 | — | -0.090 | — | -0.100 | — | ns |
| $t_{RSTO_EBR}$ | Reset To Output Delay Time from EBR Output Register | — | 1.03 | — | 1.15 | — | 1.26 | ns |
| $t_{SUBE_EBR}$ | Byte Enable Set-Up Time to EBR Output Register | -0.115 | — | -0.130 | — | -0.145 | — | ns |
| $t_{HBE_EBR}$ | Byte Enable Hold Time to EBR Output Register | 0.138 | — | 0.155 | — | 0.172 | — | ns |
| **GPLL Parameters** | | | | | | | | |
| $t_{RSTREC_GPLL}$ | Reset Recovery to Rising Clock | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| **SPLL Parameters** | | | | | | | | |
| $t_{RSTREC_SPLL}$ | Reset Recovery to Rising Clock | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| **DSP Block Timing**[2,3] | | | | | | | | |
| $t_{SUI_DSP}$ | Input Register Setup Time | 0.12 | — | 0.13 | — | 0.14 | — | ns |
| $t_{HI_DSP}$ | Input Register Hold Time | 0.02 | — | -0.01 | — | -0.03 | — | ns |
| $t_{SUP_DSP}$ | Pipeline Register Setup Time | 2.18 | — | 2.42 | — | 2.66 | — | ns |
| $t_{tHP_DSP}$ | Pipeline Register Hold Time | -0.68 | — | -0.77 | — | -0.86 | — | ns |
| $t_{SUO_DSP}$ | Output Register Setup Time | 4.26 | — | 4.71 | — | 5.16 | — | ns |
| $t_{HO_DSP}$ | Output Register Hold Time | -1.25 | — | -1.40 | — | -1.54 | — | ns |
| $t_{COI_DSP}$ | Input Register Clock to Output Time | — | 3.92 | — | 4.30 | — | 4.68 | ns |
| $t_{COP_DSP}$ | Pipeline Register Clock to Output Time | — | 1.87 | — | 1.98 | — | 2.08 | ns |
| $t_{COO_DSP}$ | Output Register Clock to Output Time | — | 0.50 | — | 0.52 | — | 0.55 | ns |
| $t_{SUADDSUB}$ | AddSub Input Register Setup Time | -0.24 | — | -0.26 | — | -0.28 | — | ns |
| $t_{HADDSUB}$ | AddSub Input Register Hold Time | 0.27 | — | 0.29 | — | 0.32 | — | ns |

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

# Timing Diagrams

***Figure 3-9. Read/Write Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

***Figure 3-10. Read/Write Mode with Input and Output Registers***

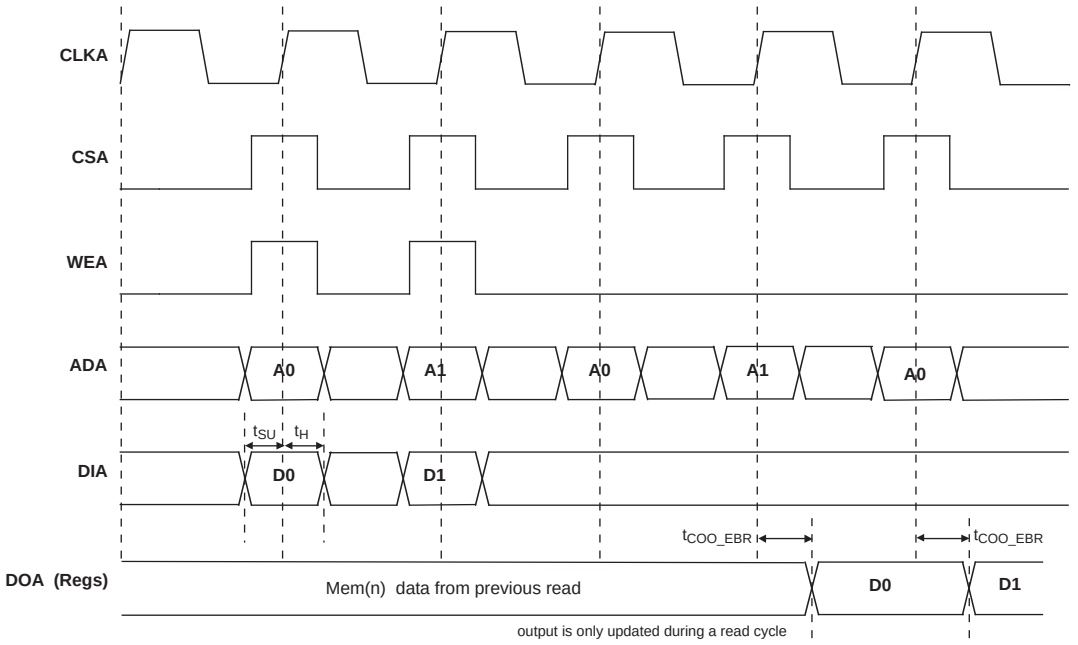
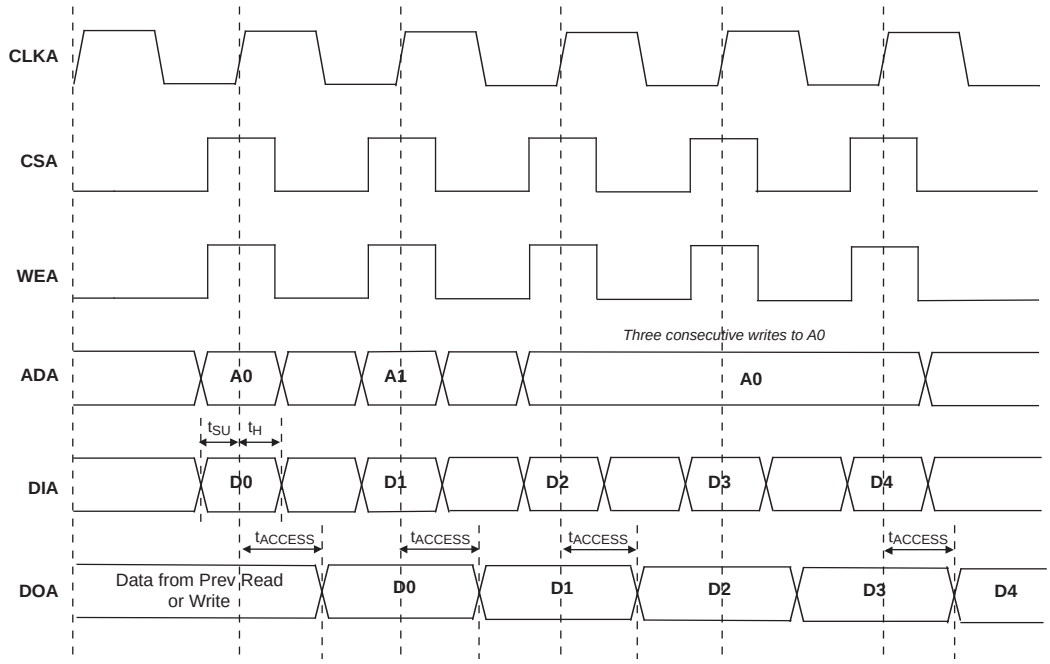


*Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)*




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

## LatticeECP2/M Family Timing Adders[1, 2, 3]

**Over Recommended Operating Conditions**

| Buffer Type | Description | -7 | -6 | -5 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVDS25 | LVDS | -0.04 | -0.02 | 0.00 | ns |
| BLVDS25 | BLVDS | -0.04 | -0.09 | -0.15 | ns |
| MLVDS | LVDS | -0.15 | -0.15 | -0.15 | ns |
| RSDS | RSDS | -0.15 | -0.15 | -0.15 | ns |
| LVPECL33 | LVPECL | 0.16 | 0.15 | 0.13 | ns |
| HSTL18_I | HSTL_18 class I | 0.01 | -0.01 | -0.04 | ns |
| HSTL18_II | HSTL_18 class II | 0.01 | -0.01 | -0.04 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.01 | -0.01 | -0.04 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.01 | -0.01 | -0.04 | ns |
| HSTL15_I | HSTL_15 class I | 0.01 | -0.01 | -0.04 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.01 | -0.01 | -0.04 | ns |
| SSTL33_I | SSTL_3 class I | -0.03 | -0.07 | -0.10 | ns |
| SSTL33_II | SSTL_3 class II | -0.03 | -0.07 | -0.10 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.03 | -0.07 | -0.10 | ns |
| SSTL33D_II | Differential SSTL_3 class II | -0.03 | -0.07 | -0.10 | ns |
| SSTL25_I | SSTL_2 class I | -0.04 | -0.07 | -0.10 | ns |
| SSTL25_II | SSTL_2 class II | -0.04 | -0.07 | -0.10 | ns |
| SSTL25D_I | Differential SSTL_2 class I | -0.04 | -0.07 | -0.10 | ns |
| SSTL25D_II | Differential SSTL_2 class II | -0.04 | -0.07 | -0.10 | ns |
| SSTL18_I | SSTL_18 class I | -0.01 | -0.04 | -0.07 | ns |
| SSTL18_II | SSTL_18 class II | -0.01 | -0.04 | -0.07 | ns |
| SSTL18D_I | Differential SSTL_18 class I | -0.01 | -0.04 | -0.07 | ns |
| SSTL18D_II | Differential SSTL_18 class II | -0.01 | -0.04 | -0.07 | ns |
| LVTTL33 | LVTTL | -0.16 | -0.16 | -0.16 | ns |
| LVCMOS33 | LVCMOS 3.3 | -0.08 | -0.12 | -0.16 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS18 | LVCMOS 1.8 | -0.16 | -0.17 | -0.17 | ns |
| LVCMOS15 | LVCMOS 1.5 | -0.14 | -0.14 | -0.14 | ns |
| LVCMOS12 | LVCMOS 1.2 | -0.04 | -0.01 | 0.01 | ns |
| PCI33 | PCI | -0.08 | -0.12 | -0.16 | ns |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 E[4] | 0.25 | 0.19 | 0.13 | ns |
| LVDS25 | LVDS 2.5 | 0.10 | 0.13 | 0.17 | ns |
| BLVDS25 | BLVDS 2.5 | 0.00 | -0.01 | -0.03 | ns |
| MLVDS | MLVDS 2.5[4] | 0.00 | -0.01 | -0.03 | ns |
| RSDS | RSDS 2.5[4] | 0.25 | 0.19 | 0.13 | ns |
| LVPECL33 | LVPECL 3.3[4] | -0.02 | -0.04 | -0.06 | ns |
| HSTL18_I | HSTL_18 class I 8mA drive | -0.19 | -0.22 | -0.25 | ns |
| HSTL18_II | HSTL_18 class II | -0.30 | -0.34 | -0.37 | ns |
| HSTL18D_I | Differential HSTL 18 class I 8mA drive | -0.19 | -0.22 | -0.25 | ns |
| HSTL18D_II | Differential HSTL 18 class II | -0.30 | -0.34 | -0.37 | ns |

## LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -7 | -6 | -5 | Units |
|---|---|---|---|---|---|
| HSTL15_I | HSTL_15 class I 4mA drive | -0.22 | -0.25 | -0.27 | ns |
| HSTL15D_I | Differential HSTL 15 class I 4mA drive | -0.22 | -0.25 | -0.27 | ns |
| SSTL33_I | SSTL_3 class I | -0.12 | -0.15 | -0.18 | ns |
| SSTL33_II | SSTL_3 class II | -0.20 | -0.23 | -0.27 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.12 | -0.15 | -0.18 | ns |
| SSTL33D_II | Differential SSTL_3 class II | -0.20 | -0.23 | -0.27 | ns |
| SSTL25_I | SSTL_2 class I 8mA drive | -0.16 | -0.19 | -0.22 | ns |
| SSTL25_II | SSTL_2 class II 16mA drive | -0.19 | -0.22 | -0.25 | ns |
| SSTL25D_I | Differential SSTL_2 class I 8mA drive | -0.16 | -0.19 | -0.22 | ns |
| SSTL25D_II | Differential SSTL_2 class II 16mA drive | -0.19 | -0.22 | -0.25 | ns |
| SSTL18_I | SSTL_1.8 class I | -0.14 | -0.17 | -0.20 | ns |
| SSTL18_II | SSTL_1.8 class II 8mA drive | -0.20 | -0.23 | -0.25 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | -0.14 | -0.17 | -0.20 | ns |
| SSTL18D_II | Differential SSTL_1.8 class II 8mA drive | -0.20 | -0.23 | -0.25 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.52 | 0.60 | 0.68 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.06 | 0.08 | 0.09 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | 0.04 | 0.04 | 0.05 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.03 | 0.02 | 0.02 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | -0.09 | -0.09 | -0.10 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive, fast slew rate | 0.52 | 0.60 | 0.68 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive, fast slew rate | 0.06 | 0.08 | 0.09 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive, fast slew rate | 0.04 | 0.04 | 0.05 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive, fast slew rate | 0.03 | 0.02 | 0.02 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive, fast slew rate | -0.09 | -0.09 | -0.10 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive, fast slew rate | 0.41 | 0.47 | 0.53 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive, fast slew rate | 0.01 | 0.01 | 0.00 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive, fast slew rate | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive, fast slew rate | 0.04 | 0.04 | 0.04 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive, fast slew rate | -0.09 | -0.10 | -0.11 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive, fast slew rate | 0.37 | 0.40 | 0.43 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive, fast slew rate | 0.10 | 0.12 | 0.13 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive, fast slew rate | -0.02 | -0.02 | -0.02 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive, fast slew rate | -0.02 | -0.03 | -0.03 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive, fast slew rate | 0.29 | 0.31 | 0.32 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive, fast slew rate | 0.05 | 0.05 | 0.06 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive, fast slew rate | 0.58 | 0.69 | 0.79 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive, fast slew rate | 0.13 | 0.19 | 0.26 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive, slow slew rate | 2.17 | 2.44 | 2.71 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive, slow slew rate | 2.50 | 2.67 | 2.83 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive, slow slew rate | 1.72 | 1.88 | 2.05 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive, slow slew rate | 1.64 | 1.63 | 1.62 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive, slow slew rate | 1.33 | 1.36 | 1.39 | ns |

## LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -7 | -6 | -5 | Units |
|---|---|---|---|---|---|
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive, slow slew rate | 2.18 | 2.26 | 2.33 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive, slow slew rate | 2.19 | 2.35 | 2.51 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive, slow slew rate | 1.50 | 1.66 | 1.82 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive, slow slew rate | 1.60 | 1.59 | 1.58 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive, slow slew rate | 1.43 | 1.39 | 1.34 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive, slow slew rate | 2.22 | 2.27 | 2.32 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive, slow slew rate | 1.93 | 2.08 | 2.23 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive, slow slew rate | 1.43 | 1.51 | 1.58 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive, slow slew rate | 1.47 | 1.46 | 1.45 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive, slow slew rate | 2.32 | 2.38 | 2.43 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive, slow slew rate | 1.84 | 1.98 | 2.12 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive, slow slew rate | 2.52 | 2.63 | 2.74 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive, slow slew rate | 1.69 | 1.83 | 1.96 | ns |
| PCI33 | PCI33 | 0.04 | 0.04 | 0.04 | ns |

1. Timing Adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. These timing adders are measured with the recommended resistor values.

Timing v.A 0.11

## sysCLOCK GPLL Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | Without external capacitor | 20 | — | 420 | MHz |
| | | With external capacitor[5, 6] | 2 | — | 420 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | Without external capacitor | 20 | — | 420 | MHz |
| | | With external capacitor[5] | 5 | — | 50 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency (CLKOK) | Without external capacitor | 0.156 | — | 210 | MHz |
| | | With external capacitor[5] | 0.039 | — | 25 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 640 | — | 1280 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | Without external capacitor | 20 | — | 420 | MHz |
| | | With external capacitor[5, 6] | 2 | — | 50 | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default duty cycle selected[3] | 45 | 50 | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | — | — | ±0.05 | UI |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | $f_{OUT} \geq 100$ MHz | — | — | ±125 | ps |
| | | $50 \leq f_{OUT} < 100$ MHz | — | | 0.025 | UIPP |
| | | $f_{OUT} < 50$ MHz | — | — | 0.04 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | N/M = integer | — | — | ±250 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10% | 1 | — | — | ns |
| $t_{LOCK}$[2] | PLL Lock-in Time | Without external capacitor | — | — | 150 | µs |
| | | With external capacitor[5] | — | — | 500 | µs |
| $t_{PA}$ | Programmable Delay Unit | | 85 | 130 | 360 | ps |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | — | ±200 | ps |
| $t_{FBKDLY}$ | External Feedback Delay | | — | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| $t_{RST}$ | RST Pulse Width (RESETM/RESETK) | | 15 | — | — | ns |
| | Reset Signal Pulse Width (CNTRST) | Without external capacitor | 500 | — | — | ns |
| | | With external capacitor[5] | 20 | — | — | µs |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. $f_{OUT}$ (max) = $f_{IN}$ * 10 for $f_{IN}$ < 5MHz.

## sysCLOCK SPLL Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | Without external capacitor | 33 | — | 420 | MHz |
| | | With external capacitor[5, 6] | 2 | — | 420 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | Without external capacitor | 33 | — | 420 | MHz |
| | | With external capacitor[5] | 5 | — | 50 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency (CLKOK) | Without external capacitor | 0.258 | — | 210 | MHz |
| | | With external capacitor[5] | 0.039 | — | 25 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 640 | — | 1280 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | Without external capacitor | 33 | — | 420 | MHz |
| | | With external capacitor[6] | 2 | — | 50 | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default Duty Cycle Selected[3] | 45 | 50 | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | — | — | ±0.05 | UI |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | $f_{OUT} \geq 100$ MHz | — | — | ±125 | ps |
| | | $50 \leq f_{OUT} < 100$ MHz | — | — | 0.025 | UIPP |
| | | $f_{OUT} < 50$ MHz | — | — | 0.04 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | Divider Ratio = Integer | — | — | ±250 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10% | 1 | — | — | ns |
| $t_{LOCK}$[2] | PLL Lock-in Time | Without external capacitor | — | — | 150 | µs |
| | | With external capacitor[5] | — | — | 500 | µs |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | — | ±200 | ps |
| $t_{FBKDLY}$ | External Feedback Delay | | — | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| $t_{RST}$ | RST Pulse Width (RSTK) | | 15 | — | — | ns |
| | Reset Signal Pulse Width (RST) | Without external capacitor | 500 | — | — | ns |
| | | With external capacitor[5] | 20 | — | — | µs |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Phase accuracy of CLKOS compared to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. $f_{OUT}$ (max) = $f_{IN}$ * 10 for $f_{IN}$ < 5MHz.

## DLL Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_{REF}$ | Input reference clock frequency (on-chip or off-chip) | 100 | — | 500 | MHz |
| $f_{FB}$ | Feedback clock frequency (on-chip or off-chip) | 100 | — | 500 | MHz |
| $f_{CLKOP}$[1] | Output clock frequency, CLKOP | 100 | — | 500 | MHz |
| $f_{CLKOS}$[2] | Output clock frequency, CLKOS | 25 | — | 500 | MHz |
| $t_{PJIT}$ | Output clock period jitter (clean input) | | — | 250 | ps p-p |
| $t_{CYJIT}$ | Output clock cycle to cycle jitter (clean input) | | | 250 | ps p-p |
| $t_{DUTY}$ | Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode) | 35 | | 65 | % |
| $t_{DUTYTRD}$ | Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode) | 40 | | 60 | % |
| $t_{DUTYCIR}$ | Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) | 40 | | 60 | % |
| $t_{SKEW}$[3] | Output clock to clock skew between two outputs with the same phase setting | — | — | 100 | ps |
| $t_{PWH}$ | Input clock minimum pulse width high (at 80% level) | 750 | — | — | ps |
| $t_{PWL}$ | Input clock minimum pulse width low (at 20% level) | 750 | — | — | ps |
| $t_{INSTB}$ | Input clock period jitter | — | — | +/-250 | ps |
| $t_{LOCK}$ | DLL lock time | 18,500 | — | — | cycles |
| $t_{RSWD}$ | Digital reset minimum pulse width (at 80% level) | 3 | — | — | ns |
| $t_{PA}$ | Delay step size | 16.5 | 42 | 59.4 | ps |
| $t_{RANGE1}$ | Max. delay setting for single delay block (144 taps) | 2.376 | 6 | 8.553 | ns |
| $t_{RANGE4}$ | Max. delay setting for four chained delay blocks | 9.504 | 24 | 34.214 | ns |

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

# SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)[1, 2]

***Table 3-7. Serial Output Timing and Levels***

| Symbol | Description | Frequency | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{TX-DIFF-P-P-1}$ | Differential swing (1V setting)[1, 2] | 0.25 to 3.125 Gbps | 0.79 | 0.99 | 1.19 | V, p-p |
| $V_{TX-DIFF-P-P-1.25}$ | Differential swing (1.25V setting)[1, 2] | 0.25 to 3.125 Gbps | 1.00 | 1.25 | 1.50 | V, p-p |
| $V_{TX-DIFF-P-P-1.3}$ | Differential swing (1.3V setting)[1, 2] | 0.25 to 3.125 Gbps | 1.04 | 1.30 | 1.56 | V, p-p |
| $V_{TX-DIFF-P-P-1.35}$ | Differential swing (1.35V setting)[1, 2] | 0.25 to 3.125 Gbps | 1.08 | 1.35 | 1.62 | V, p-p |
| $V_{OCM}$ | Output common mode voltage | — | $V_{CCOB}$ - 0.75 | $V_{CCOB}$ - 0.60 | $V_{CCOB}$ - 0.45 | V |
| $T_{TX-R}$ | Rise time (20% to 80%) | — | — | 70 | — | ps |
| $T_{TX-F}$ | Fall time (80% to 20%) | — | — | 70 | — | ps |
| $Z_{TX-OI-SE}$ | Output impedance 50/75/HiZ K Ohms (single-ended) | — | — | 50/70 HiZ | — | Ohms |
| $R_{TX-RL}$ | Return loss (with package) | — | — | 9 | — | dB |

1. All measurements are with 50 ohm impedance.
2. See TN1124, LatticeECP2M SERDES/PCS Usage Guide for actual binary settings.

***Table 3-8. Channel Output Jitter - x10 Mode***

| Description | Frequency | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | — | 0.08 | 0.12 | UI, p-p |
| Random | 3.125 Gbps | — | 0.22 | 0.38 | UI, p-p |
| Total | 3.125 Gbps | — | 0.33 | 0.43 | UI, p-p |
| Deterministic | 2.5 Gbps | — | 0.08 | 0.17 | UI, p-p |
| Random | 2.5 Gbps | — | 0.20 | 0.25 | UI, p-p |
| Total | 2.5 Gbps | — | 0.25 | 0.35 | UI, p-p |
| Deterministic | 1.25 Gbps | — | 0.03 | 0.10 | UI, p-p |
| Random | 1.25 Gbps | — | 0.14 | 0.19 | UI, p-p |
| Total | 1.25 Gbps | — | 0.17 | 0.24 | UI, p-p |
| Deterministic | 250 Mbps | — | 0.04 | 0.17 | UI, p-p |
| Random | 250 Mbps | — | 0.12 | 0.13 | UI, p-p |
| Total | 250 Mbps | — | 0.15 | 0.29 | UI, p-p |

Note: Values are measured with PRBS $2^7$-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

*Table 3-9. Channel Output Jitter - x20 Mode*

| Description | Frequency | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | — | 0.08 | 0.12 | UI, p-p |
| Random | 3.125 Gbps | — | 0.27 | 0.51 | UI, p-p |
| Total | 3.125 Gbps | — | 0.35 | 0.59 | UI, p-p |
| Deterministic | 2.5 Gbps | — | 0.09 | 0.19 | UI, p-p |
| Random | 2.5 Gbps | — | 0.23 | 0.34 | UI, p-p |
| Total | 2.5 Gbps | — | 0.29 | 0.45 | UI, p-p |
| Deterministic | 1.25 Gbps | — | 0.05 | 0.11 | UI, p-p |
| Random | 1.25 Gbps | — | 0.16 | 0.22 | UI, p-p |
| Total | 1.25 Gbps | — | 0.20 | 0.28 | UI, p-p |

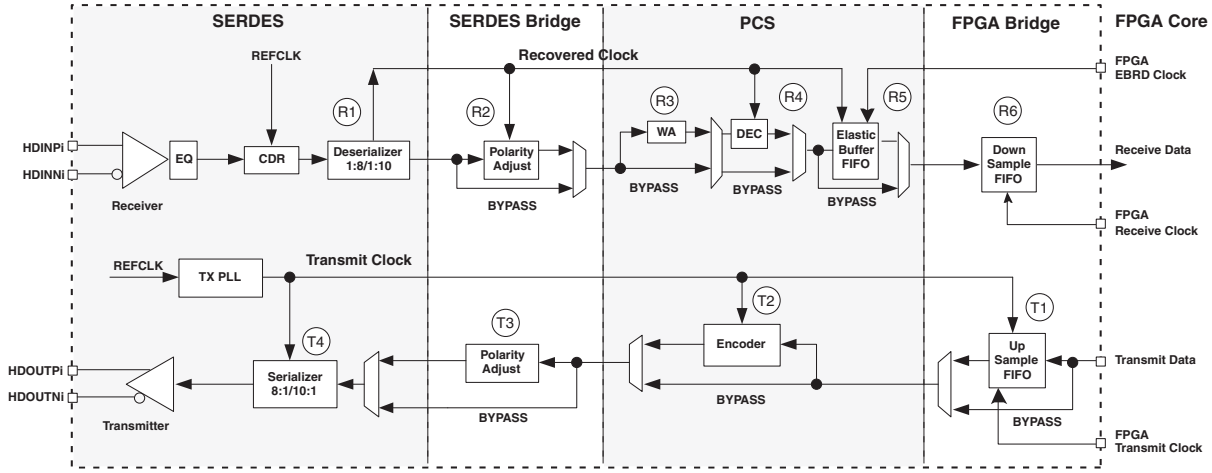
Note: Values are measured with PRBS $2^7$-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x20 mode.

*Table 3-10. SERDES/PCS Latency Breakdown (Parallel Clock Cycle)*

| Item | Description | Min. | Average | Max. | Fixed | Bypass | Units |
|---|---|---|---|---|---|---|---|
| **Transmit Data Latency** | | | | | | | |
| T1 | FPGA Bridge Transmit[2] | 1 | 3 | 5 | | 1 | word clk |
| T2 | 8b10b Encoder | — | — | — | 2 | 1 | word clk |
| T3 | SERDES Bridge Transmit | — | — | — | 2 | 1 | word clk |
| T4[3] | Serializer: 8-bit mode | — | — | — | 15 + Δ1 | — | UI + ps |
| | Serializer: 10-bit mode | — | — | — | 18 + Δ1 | — | UI + ps |
| **Receive Data Latency** | | | | | | | |
| R1[3] | Deserializer: 8-bit mode | — | — | — | 10 + Δ2 | — | UI + ps |
| | Deserializer: 10-bit mode | — | — | — | 12 + Δ2 | — | UI + ps |
| R2 | SERDES Bridge Receive | — | — | — | 2 | 1 | word clk |
| R3 | Word Alignment | 3.1 | — | 4 | — | 0 | word clk |
| R4 | 8b10b Decoder | — | — | — | 1 | 1 | word clk |
| R5 | Clock Tolerance Compensation | 7 | 15 | 23 | | 1 | word clk |
| R6 | FPGA Bridge Receive[2] | 1 | 3 | 5 | | 1 | word clk |

1. PCS internal parallel clock. This clock rate is the same as rxfullclk.
2. FPGA Bridge latency varies by the upsample/downsample FIFO read/write. The numbers given are for the 8b10b interface. The depth of the downsample/upsample FIFO is 4. The earliest read can be done after the write clock cycle (one clock) in downsample FIFO. The latest read will be done after the FIFO is full (4 + 1 = 5). For the 16b20b interface, the numbers are doubled: min. = 2, max. = 10. This latency depends on the internal FIFO flag operation.
3. Δ1 = -245ps, Δ2 = 700ps

*Figure 3-12. Transmitter and Receiver Block Diagram*



# SERDES High Speed Data Receiver (LatticeECP2M Family Only)

***Table 3-11. Serial Input Data Specifications***

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $RX\text{-}CID_S$ | Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ $10^{-12}$ BER | | 7 @ 3.125 Gbps<br>20 @ 1.25 Gbps | | Bits |
| $V_{RX\text{-}DIFF\text{-}S}$ | Differential input sensitivity | 100 | — | — | mV, p-p |
| $V_{RX\text{-}IN}$ | Input levels | 0 | — | $V_{CCRX}$ + 0.8 | V |
| $V_{RX\text{-}CM\text{-}DC}$ | Input common mode range (DC coupled) | 0.5 | — | 1.2 | V |
| $V_{RX\text{-}CM\text{-}AC}$ | Input common mode range (AC coupled)[3] | 0 | — | 1.5 | V |
| $T_{RX\text{-}RELOCK}$ | CDR re-lock time[2] | — | — | 3000 | Bits |
| $Z_{RX\text{-}TERM}$ | Input termination 50/75 Ohm/High Z | — | 50 | | Ohms |
| $RL_{RX\text{-}RL}$ | Return loss (without package) | — | 9 | — | dB |

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase of frequency within +/- 300 ppm, assuming 8b10b encoded data and the CDR is in lock state. When CDR is in un-lock state, or reset is applied, the total re-lock settling time will be approximately 4ms including analog settle time, calibration time, and acquisition time.
3. AC coupling is used to interface to LVPECL and LVDS.

## Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

***Table 3-12. Receiver Total Jitter Tolerance Specification[1]***

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | 600 mV differential eye | — | — | 0.54 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.26 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.80 | UI, p-p |
| Deterministic | 2.5 Gbps | 600 mV differential eye | — | — | 0.61 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.81 | UI, p-p |
| Deterministic | 1.25 Gbps | 600 mV differential eye | — | — | 0.53 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.80 | UI, p-p |
| Deterministic | 250 Mbps[2] | 600 mV differential eye | — | — | 0.42 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.10 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.60 | UI, p-p |

1. Values are measured with PRBS $2^7$-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.
2. Jitter specification is limited by measurement equipment capability.

*Table 3-13. Periodic Receiver Jitter Tolerance Specification[1]*

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Periodic | 3.125 Gbps | 600 mV differential eye | — | — | 0.20 | UI, p-p |
| | 2.5 Gbps | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| | 1.25 Gbps | 600 mV differential eye | — | — | 0.20 | UI, p-p |
| | 250 Mbps[2] | 600 mV differential eye | — | — | 0.08 | UI, p-p |

1. Values are measured with PRBS $2^7$-1, all channels operating.
2. Jitter specification is limited by measurement equipment capability.

## SERDES External Reference Clock (LatticeECP2M Family Only)

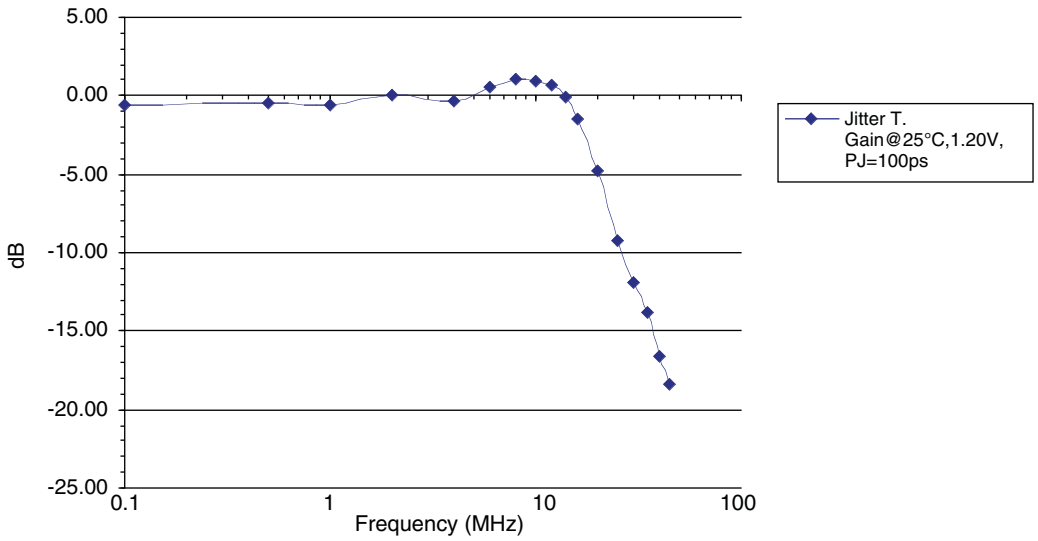
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-14 specifies reference clock requirements, over the full range of operating conditions.

***Table 3-14. External Reference Clock Specification (refclkp/refclkn)***

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $F_{REF}$ | Frequency range | 25 | — | 320 | MHz |
| $F_{REF-PPM}$ | Frequency tolerance | -300 | — | 300 | ppm |
| $V_{REF-IN-SE}$ | Input swing, single-ended clock[1] | 100 | — | 1200 | mV, p-p |
| $V_{REF-IN}$ | Input levels | 0 | — | $V_{CCP}$ + 0.8 | V |
| $V_{REF-CM-DC}$ | Input common mode range (DC coupled) | 0.5 | — | 1.2 | V |
| $V_{REF-CM-AC}$ | Input common mode range (AC coupled)[2] | 0 | — | 1.5 | V |
| $D_{REF}$ | Duty cycle[3] | 40 | — | 60 | % |
| $T_{REF-R}$ | Rise time (20% to 80%) | | 500 | 1000 | ps |
| $T_{REF-F}$ | Fall time (80% to 20%) | | 500 | 1000 | ps |
| $Z_{REF-IN-TERM}$ | Input termination | | 50/2K | | Ohms |
| $C_{REF-IN-CAP}$ | Input capacitance[4] | — | — | 1.5 | pF |

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
(Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Input capacitance of 1.5pF is total capacitance, including both device and package.

***Figure 3-13. Jitter Transfer***




Note: This graph is for a nominal device.

# SERDES Power-Down/Power-Up Specification

***Table 3-15. Power-Down and Power-Up Specification***

| Symbol | Description | Max. | Units |
|---|---|---|---|
| $t_{PWRDN}$ | Power-down time after all power down register bits set to '0' | 10 | µs |
| $t_{PWRUP}$ | Power-up time after all power down register bits set to '1' | 100 | µs |

# PCI Express Electrical and Timing Characteristics

## AC and DC Characteristics

***Table 3-16. Transmit[1, 2]***

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| UI | Unit interval | | 399.88 | 400 | 400.12 | ps |
| $V_{TX-DIFF_P-P}$ | Differential peak-to-peak output voltage | | 0.8 | 1.0 | 1.2 | V |
| $V_{TX-DE-RATIO}$ | De-emphasis differential output voltage ratio | | 0 | -3.5 | -7.96 | dB |
| $V_{TX-CM-AC_P}$ | RMS AC peak common-mode output voltage | | — | 20 | — | mV |
| $V_{TX-CM-DC-LINE-DELTA}$ | Maximum Common mode voltage delta between n and p channels | | — | — | 25 | mV |
| $V_{TX-DC-CM}$ | Tx DC common mode voltage | | 0 | — | $V_{CCOB}$ + 5% | V |
| $I_{TX-SHORT}$ | Output short circuit current | $V_{TX-D+}$=0.0V $V_{TX-D-}$=0.0V | — | — | 90 | mA |
| $Z_{TX-DIFF-DC}$ | Differential output impedance | | 80 | 100 | 120 | Ohms |
| $T_{TX-RISE}$ | Tx output rise time | 20 to 80% | 0.125 | — | — | UI |
| $T_{TX-FALL}$ | Tx output fall time | 20 to 80% | 0.125 | — | — | UI |
| $L_{TX-SKEW}$ | Lane-to-lane static output skew for all lanes in port/link | | — | — | 1.3 | ns |
| $T_{TX-EYE}$ | Transmitter eye width | | 0.75 | — | — | UI |
| $T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$[3] | | | — | — | 0.125 | UI |
| $C_{TX}$ | AC coupling capacitor | | 75 | — | 200 | nF |

1. Values are measured at 2.5 Gbps.
2. Compliant to PCI Express v1.1.
3. Measured at 60ps with plug-in board and jitter due to socket removed.

***Table 3-17. Receive***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| UI | Unit Interval | | 399.88 | 400 | 400.12 | ps |
| $V_{RX-DIFF_P-P}$ | Differential peak-to-peak input voltage | | 0.175 | — | — | V |
| $V_{RX-IDLE-DET-DIFF_P-P}$ | Idle detect threshold voltage | | 65 | — | 175 | mV |
| $Z_{RX-DIFF-DC}$ | DC differential input impedance | | 80 | 100 | 120 | Ohms |
| $Z_{RX-DC}$ | DC input impedance | | 40 | 50 | 60 | Ohms |
| $Z_{RX-HIGH-IMP-DC}$[1] | Power-down DC input impedance | | 200K | — | — | Ohms |
| $T_{RX-EYE}$ | Receiver eye width | | 0.4 | — | — | UI |
| $T_{RX-EYE-MEDIAN-TO-MAX-JITTER}$ | | | — | — | 0.3 | UI |

Notes:
1. Measured with external AC-coupling on the receiver
2. Values are measured at 2.5 Gbps

*Table 3-18. Reference Clock*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{REFCLK}$ | Reference clock frequency | | — | 100 | — | MHz |
| $V_{CM}$ | Input common mode voltage | | — | 0.65 | — | V |
| $T_R/T_F$ | Clock input rise/fall time | | — | — | 1.0 | ns |
| $V_{SW}$ | Differential input voltage swing | | 0.6 | — | 1.6 | V |
| $DC_{REFCLK}$ | Input clock duty cycle | | 40 | 50 | 60 | % |
| PPM | Reference clock tolerance | | -300 | — | +300 | ppm |

# LatticeECP2/M sysCONFIG Port Timing Specifications

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **sysCONFIG Byte Data Flow** | | | | |
| $t_{SUCBDI}$ | Byte D[0:7] Setup Time to CCLK | 7 | — | ns |
| $t_{HCBDI}$ | Byte D[0:7] Hold Time to CCLK | 1 | — | ns |
| $t_{CODO}$ | CCLK to DOUT in Flowthrough Mode | — | 12 | ns |
| $t_{SUCS}$ | CSN[0:1] Setup Time to CCLK | 7 | — | ns |
| $t_{HCS}$ | CSN[0:1] Hold Time to CCLK | 1 | — | ns |
| $t_{SUWD}$ | Write Signal Setup Time to CCLK | 7 | — | ns |
| $t_{HWD}$ | Write Signal Hold Time to CCLK | 1 | — | ns |
| $t_{DCB}$ | CCLK to BUSY Delay Time | — | 12 | ns |
| $t_{CORD}$ | CCLK to Out for Read Data | — | 12 | ns |
| **sysCONFIG Byte Slave Clocking** | | | | |
| $t_{BSCH}$ | Byte Slave CCLK Minimum High Pulse | 6 | — | ns |
| $t_{BSCL}$ | Byte Slave CCLK Minimum Low Pulse | 9 | — | ns |
| $t_{BSCYC}$ | Byte Slave CCLK Cycle Time | 15 | — | ns |
| **sysCONFIG Serial (Bit) Data Flow** | | | | |
| $t_{SUSCDI}$ | DI Setup Time to CCLK Slave Mode | 7 | — | ns |
| $t_{HSCDI}$ | DI Hold Time to CCLK Slave Mode | 1 | — | ns |
| $t_{CODO}$ | CCLK to DOUT in Flowthrough Mode | — | 12 | ns |
| **sysCONFIG Serial Slave Clocking** | | | | |
| $t_{SSCH}$ | Serial Slave CCLK Minimum High Pulse | 6 | — | ns |
| $t_{SSCL}$ | Serial Slave CCLK Minimum Low Pulse | 6 | — | ns |
| **sysCONFIG POR, Initialization and Wake-up** | | | | |
| $t_{ICFG}$ | Minimum Vcc to INITN High | — | 28 | ms |
| $t_{VMC}$ | Time from $t_{ICFG}$ to Valid Master CCLK | — | 2 | us |
| $t_{PRGMRJ}$ | PROGRAMN Pin Pulse Rejection | — | 8 | ns |
| $t_{PRGM}$ | PROGRAMN Low Time to Start Configuration | 25 | — | ns |
| $t_{DINIT}$ | PROGRAMN High to INITN High Delay[1] | — | 1.5 | ms |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INITN Low | — | 37 | ns |
| $t_{DPPDONE}$ | Delay Time from PROGRAMN Low to DONE Low | — | 37 | ns |
| $t_{IODISS}$ | User I/O Disable from PROGRAMN Low | — | 35 | ns |
| $t_{IOENSS}$ | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| $t_{MWC}$ | Additional Wake Master Clock Signals after DONE Pin High | 120 | — | cycles |
| **sysCONFIG SPI Port[2]** | | | | |
| $t_{CFGX}$ | INITN High to CCLK Low | — | 1 | µs |
| $t_{CSSPI}$ | INITN High to CSSPIN Low | — | 2 | us |
| $t_{CSCCLK}$ | CCLK Low before CSSPIN Low | 0 | — | ns |
| $t_{SOCDO}$ | CCLK Low to Output Valid | — | 15 | ns |
| $t_{SOE}$ | CSSPIN[0:1] Active Setup Time | 300 | — | ns |
| $t_{CSPID}$ | CSSPIN[0:1] Low to First CCLK Edge Setup Time | 300+3cyc | 600+6cyc | ns |

# LatticeECP2/M sysCONFIG Port Timing Specifications (Continued)

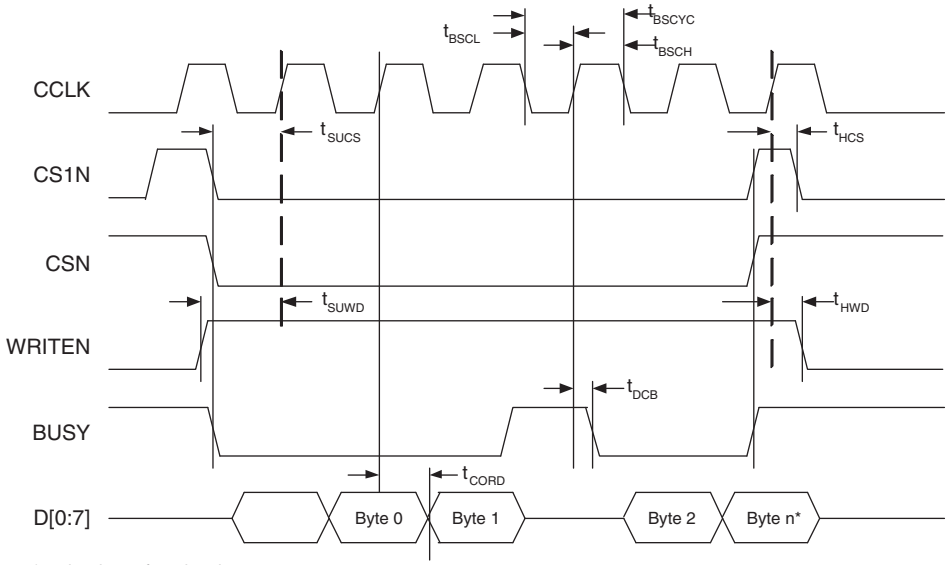
**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAXSPI}$ | Max. CCLK Frequency - SPI Flash Read Opcode (0x03) (SPIFASTN = 1) | — | 20 | MHz |
| | Max. CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN = 0) | — | 50 | MHz |
| | Max. CCLK Frequency - Encrypted Bitstream | — | 10 | MHz |
| $t_{SUSPI}$ | SOSPI Data Setup Time Before CCLK | 7 | — | ns |
| $t_{HSPI}$ | SOSPI Data Hold Time After CCLK | 2 | — | ns |
| $t_{SUMCDI}$ | DI Setup to CCLK | 7 | — | ns |
| $t_{HMCDI}$ | DI Hold from CCLK | 1 | — | ns |

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.
2. For SED (Soft Error Detect), the SEDCLKIN operating frequency must be at least 20MHz. SEDCLKIN is derived from Master Clock Frequency that has a +/-30% variation..

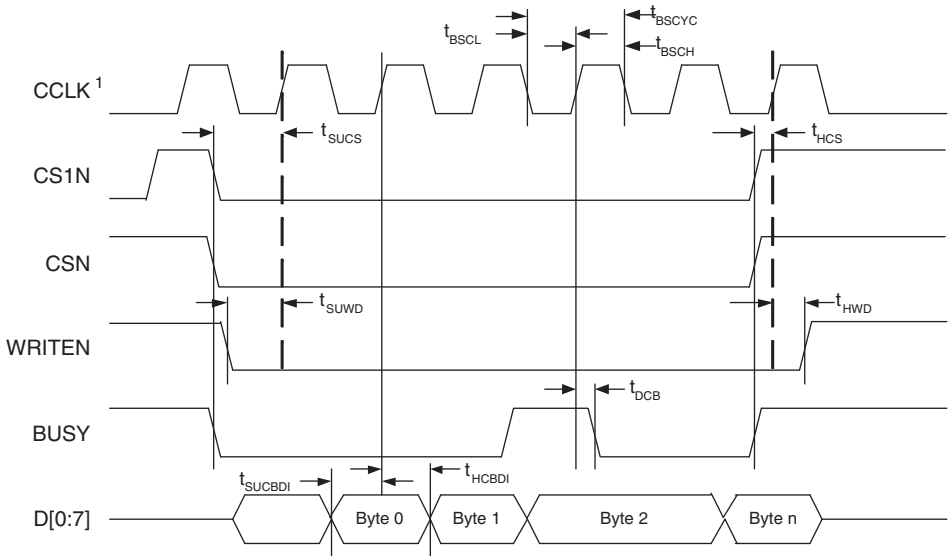
| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Master Clock Frequency | Selected value - 30% | Selected value + 30% | MHz |
| Duty Cycle | 40 | 60 | % |

***Figure 3-14. sysCONFIG Parallel Port Read Cycle***



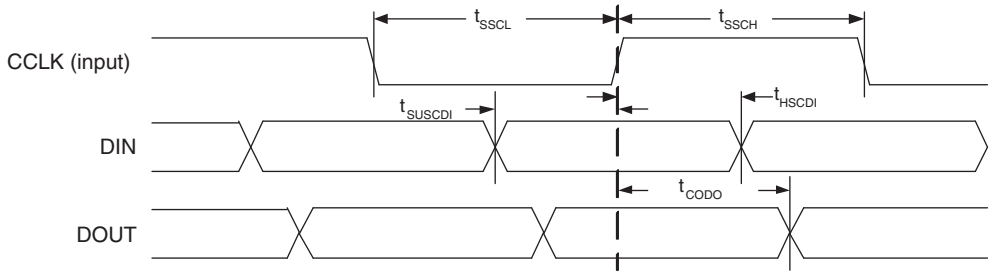

*n = last byte of read cycle.

### Figure 3-15. sysCONFIG Parallel Port Write Cycle

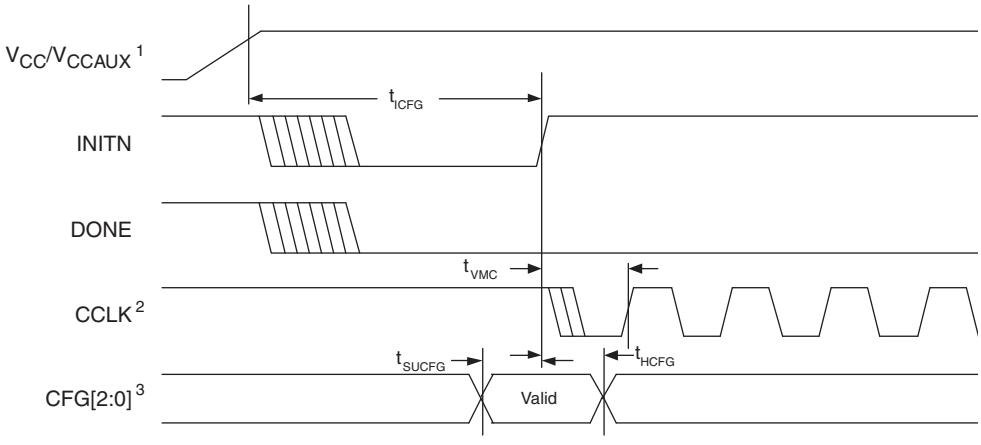



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

### Figure 3-16. sysCONFIG Slave Serial Port Timing

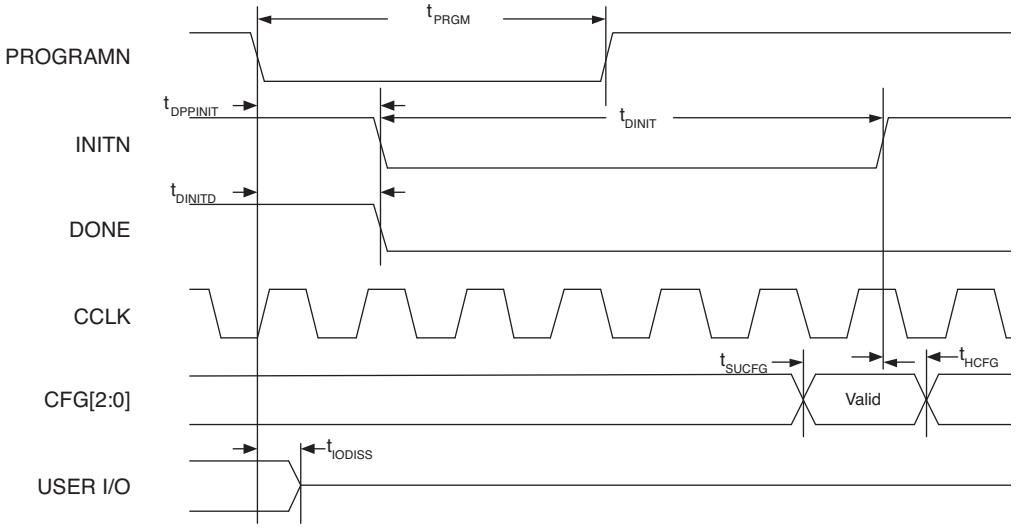



### Figure 3-17. Power-On-Reset (POR) Timing




1. Time taken from $V_{CC}$ or $V_{CCAUX}$, whichever is the last to reach its $V_{MIN}$.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

*Figure 3-18. Configuration from PROGRAMN Timing*




1. The CFG pins are normally static (hard wired)

*Figure 3-19. Wake-Up Timing*

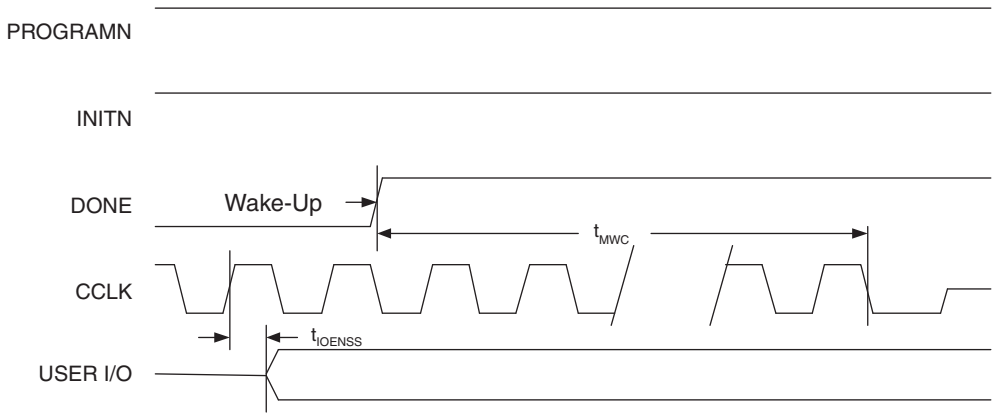
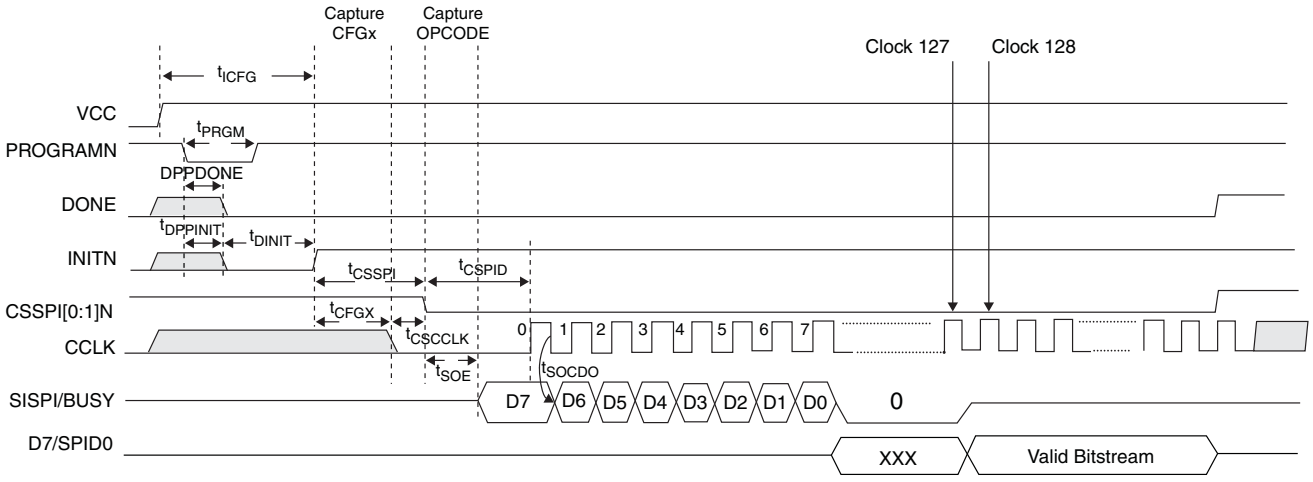



*Figure 3-20. SPI/SPIm Configuration Waveforms*



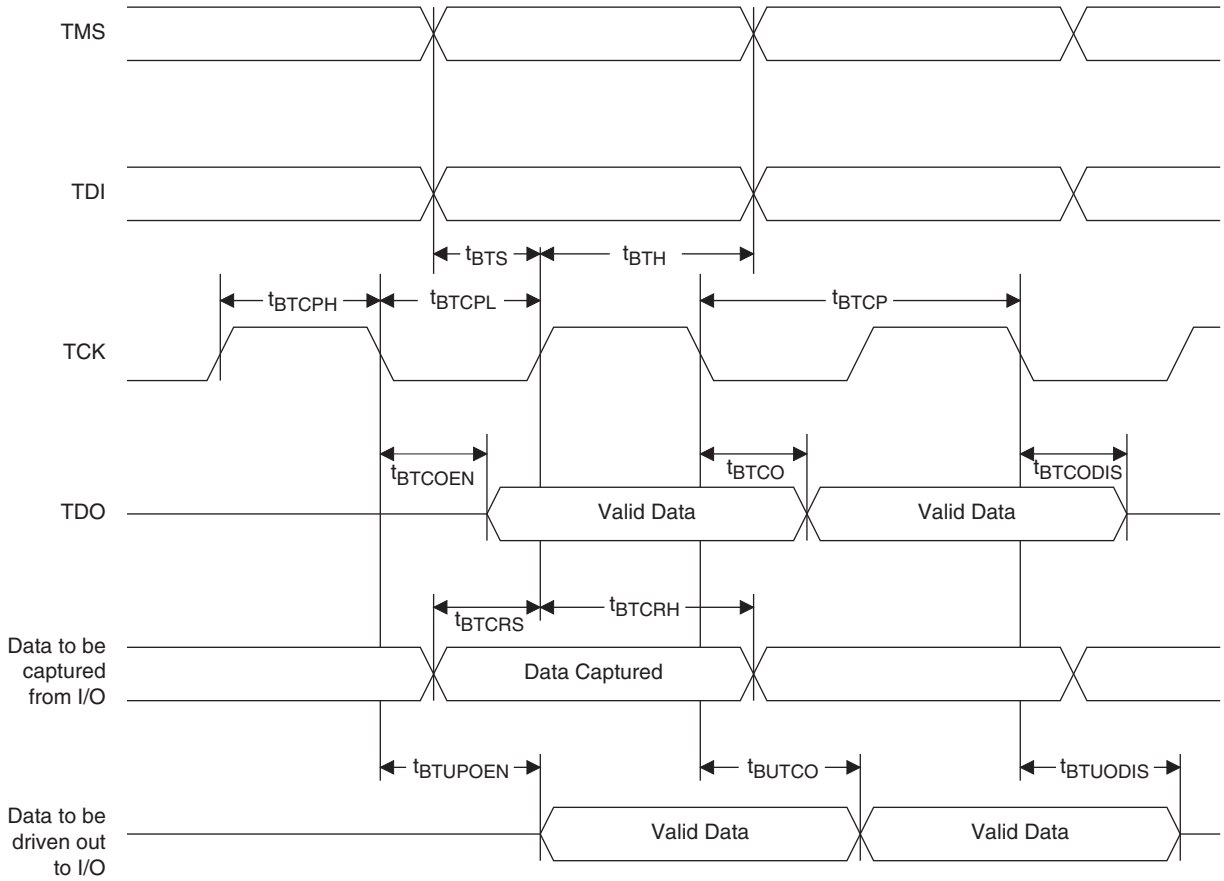
# JTAG Port Timing Specifications

**Over Recommended Operating Conditions**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 10 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

Timing v.A 0.11

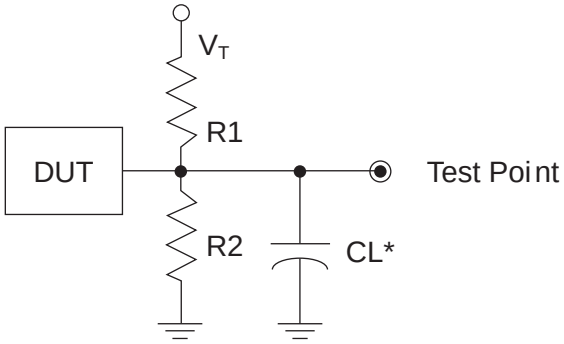
***Figure 3-21. JTAG Port Timing Waveforms***



## Switching Test Conditions

Figure 3-22 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-19.

***Figure 3-22. Output Test Load, LVTTL and LVCMOS Standards***




*CL Includes Test Fixture and Probe Capacitance

***Table 3-19. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $R_2$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | ∞ | 0pF | LVCMOS 3.3 = 1.5V | — |
| | | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | ∞ | 1MΩ | | $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> L) | 1MΩ | ∞ | | $V_{CCIO}/2$ | $V_{CCIO}$ |
| LVCMOS 2.5 I/O (H -> Z) | ∞ | 100 | | $V_{OH}$ - 0.10 | — |
| LVCMOS 2.5 I/O (L -> Z) | 100 | ∞ | | $V_{OL}$ + 0.10 | $V_{CCIO}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

## Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. See "Typical sysI/O I/O Behavior During Power-up" for more information about I/O behavior during power-up. |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| GND | — | Ground. Dedicated pins. |
| $V_{CC}$ | — | Power supply pins for core logic. Dedicated pins. |
| $V_{CCAUX}$ | — | Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. |
| $V_{CCIOx}$ | — | Dedicated power supply pins for I/O bank x. |
| $V_{CCPLL}$ | — | PLL supply pins. Should be tied to $V_{CC}$ even when the corresponding PLL is unused. |
| $V_{REF1_x}$, $V_{REF2_x}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| XRES[4] | — | 10K ohm +/-1% resistor must be connected between this pad and ground. |
| PLLCAP[4] | — | External capacitor connection for PLL. |
| **PLL, DLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_$V_{CCPLL}$ | — | Power supply pin for PLL: LUM, LLM, RUM, RLM, num = row from center. |
| [LOC][num]_GPLL[T, C]_IN_A | I | General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_GPLL[T, C]_FB_A | I | Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_SPLL[T, C]_IN_A[5] | I | Secondary PLL (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_SPLL[T, C]_FB_A[5] | I | Optional feedback (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_DLL[T, C]_IN_A | I | DLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_DLL[T, C]_FB_A | I | Optional feedback (DLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | I | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank. |

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## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| [LOC]DQS[num] | I/O | DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number. |
| [LOC]DQ[num] | I/O | DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number. |
| **Test and Programming (Dedicated Pins)** | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |
| TDO | O | Output pin. Test Data Out pin used to shift data out of a device using 1149.1. |
| VCCJ | — | Power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (Used During sysCONFIG) | | |
| CFG[2:0] | I | Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins. |
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY/SISPI | I/O | Read control command in SPI or SPIm mode. |
| CSN | I | sysCONFIG chip select (active low). During configuration, a pull-up is enabled. |
| CS1N | I | sysCONFIG chip select (active low). During configuration, a pull-up is enabled. |
| WRITEN | I | Write Data on Parallel port (active low). |
| D[0]/SPIFASTN | I/O | sysCONFIG Port Data I/O for Parallel mode.<br>sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. |
| D[1:6] | I/O | sysCONFIG Port Data I/O for Parallel |
| D[7]/SPID0 | I/O | sysCONFIG Port Data I/O for Parallel, SPI, SPIm |
| DOUT/CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. |
| DI/CSSPI0N | I/O | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIm modes. |
| **Dedicated SERDES Signals**[1, 2, 3] | | |
| [LOC]_SQ_VCCAUX33 | — | Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused. |
| [LOC]_SQ_REFCLKN | I | Negative Reference Clock Input |
| [LOC]_SQ_REFCLKP | I | Positive Reference Clock Input |
| [LOC]_SQ_VCCP | — | PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused. |

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| [LOC]_SQ_VCCIBm | — | Input buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused. |
| [LOC]_SQ_VCCOBm | — | Output buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused. |
| [LOC]_SQ_HDOUTNm | O | High-speed output, negative channel m |
| [LOC]_SQ_HDOUTPm | O | High-speed output, positive channel m |
| [LOC]_SQ_HDINNm | I | High-speed input, negative channel m |
| [LOC]_SQ_HDINPm | I | High-speed input, positive channel m |
| [LOC]_SQ_VCCTXm[4] | — | Transmitter power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused. |
| [LOC]_SQ_VCCRXm[4] | — | Receiver power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused. |

1. These signals are relevant for LatticeECP2M family.
2. m defines the associated channel in the Quad.
3. These signals are defined in Quads [LOC] indicates the corner SERDES Quad is located: ULC (upper left), URC (upper right), LLC (lower left), LRC (lower right).
4. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given. For more information, refer to TN1159, LatticeECP2/M Pin Assignment Recommendations.
5. There may be SPLLs that do not have dedicated I/Os.

## PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO Within PIC | DDR Strobe (DQS) and Data (DQ) Pins |
|---|---|---|
| **For Left and Right Edges of the Device** | | |
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |
| **For Bottom Edge of the Device** | | |
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |
| P[Edge] [n+4] | A | DQ |
| | B | DQ |

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 15 bits of data for the left and right edges and up to 17 bits of data for the bottom edge. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

## LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12

| Pin Type | | LFE2-6 | | LFE2-12 | | | |
|---|---|---|---|---|---|---|---|
| | | 144 TQFP | 256 fpBGA | 144 TQFP | 208 PQFP | 256 fpBGA | 484 fpBGA |
| Single Ended User I/O | | 90 | 190 | 93 | 131 | 193 | 297 |
| Differential Pair User I/O | | 43 | 95 | 45 | 62 | 96 | 148 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 34 | 54 | 33 | 40 | 54 | 57 |
| | Dedicated Pins | 3 | 3 | 3 | 3 | 3 | 3 |
| VCC | | 10 | 7 | 10 | 14 | 7 | 16 |
| VCCAUX | | 4 | 4 | 4 | 8 | 4 | 16 |
| VCCPLL | | 0 | 0 | 0 | 0 | 0 | 0 |
| VCCIO | Bank0 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank1 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank2 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank3 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank4 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank5 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank6 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank7 | 1 | 2 | 1 | 2 | 2 | 4 |
| | Bank8 | 1 | 1 | 1 | 2 | 1 | 2 |
| GND, GND0 to GND7 | | 12 | 20 | 12 | 22 | 20 | 60 |
| NC | | 4 | 3 | 1 | 0 | 0 | 44 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 8/4 | 18/6 | 8/4 | 18/9 | 18/9 | 50/25 |
| | Bank1 | 17/8 | 34/17 | 18/9 | 18/9 | 34/17 | 46/23 |
| | Bank2 | 4/2 | 20/10 | 4/2 | 11/5 | 20/10 | 24/12 |
| | Bank3 | 8/4 | 12/6 | 8/4 | 11/5 | 12/6 | 16/8 |
| | Bank4 | 18/9 | 32/16 | 18/9 | 19/9 | 32/16 | 46/23 |
| | Bank5 | 8/4 | 14/7 | 10/5 | 18/9 | 17/8 | 46/23 |
| | Bank6 | 9/4 | 26/13 | 9/4 | 18/8 | 26/13 | 32/16 |
| | Bank7 | 12/6 | 20/10 | 12/6 | 12/6 | 20/10 | 23/11 |
| | Bank8 | 6/2 | 14/7 | 6/2 | 6/2 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 1 | 5 | 1 | 4 | 5 | 6 |
| | Bank3 (Right Edge) | 3 | 3 | 3 | 3 | 3 | 4 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 2 | 7 | 2 | 6 | 7 | 8 |
| | Bank7 (Left Edge) | 5 | 5 | 5 | 5 | 5 | 5 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 | 0 | 0 |

## LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

| Pin Type | | LFE2-6 | | LFE2-12 | | | |
|---|---|---|---|---|---|---|---|
| | | 144 TQFP | 256 fpBGA | 144 TQFP | 208 PQFP | 256 fpBGA | 484 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 0 | 2 | 0 | 0 | 2 | 3 |
| | Bank5 | 0 | 1 | 0 | 0 | 1 | 3 |
| | Bank6 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Bank7 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 18 | 32 | 18 | 19 | 32 | 46 |
| | Bank5 | 8 | 14 | 10 | 18 | 17 | 46 |
| | Bank6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank7 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

## LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35

| Pin Type | | LFE2-20 | | | | LFE2-35 | |
|---|---|---|---|---|---|---|---|
| | | 208 PQFP | 256 fpBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA |
| Single Ended User I/O | | 131 | 193 | 331 | 402 | 331 | 450 |
| Differential Pair User I/O | | 62 | 96 | 165 | 200 | 165 | 224 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 42 | 54 | 60 | 64 | 60 | 68 |
| | Dedicated Pins | 3 | 3 | 3 | 3 | 3 | 3 |
| VCC | | 14 | 7 | 18 | 24 | 16 | 22 |
| VCCAUX | | 8 | 4 | 16 | 16 | 16 | 16 |
| VCCPLL | | 0 | 0 | 0 | 0 | 2 | 2 |
| VCCIO | Bank0 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank1 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank2 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank3 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank4 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank5 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank6 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank7 | 2 | 2 | 4 | 5 | 4 | 5 |
| | Bank8 | 2 | 1 | 2 | 2 | 2 | 2 |
| GND, GND0 to GND7 | | 22 | 20 | 60 | 72 | 60 | 72 |
| NC | | 0 | 1 | 8 | 101 | 8 | 102 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 18/9 | 18/9 | 50/25 | 67/33 | 50/25 | 67/33 |
| | Bank1 | 18/9 | 34/17 | 46/23 | 52/26 | 46/23 | 52/26 |
| | Bank2 | 11/5 | 20/10 | 34/17 | 36/18 | 34/17 | 48/24 |
| | Bank3 | 11/5 | 12/6 | 22/11 | 32/16 | 22/11 | 42/21 |
| | Bank4 | 19/9 | 32/16 | 46/23 | 50/25 | 46/23 | 54/27 |
| | Bank5 | 18/9 | 17/8 | 46/23 | 68/34 | 46/23 | 68/34 |
| | Bank6 | 18/8 | 26/13 | 40/20 | 48/24 | 40/20 | 58/29 |
| | Bank7 | 12/6 | 20/10 | 33/16 | 35/17 | 33/16 | 47/23 |
| | Bank8 | 6/2 | 14/7 | 14/7 | 14/7 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 4 | 5 | 9 | 9 | 9 | 12 |
| | Bank3 (Right Edge) | 3 | 3 | 5 | 8 | 5 | 9 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 6 | 7 | 10 | 12 | 10 | 13 |
| | Bank7 (Left Edge) | 5 | 5 | 8 | 8 | 8 | 11 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 | 0 | 0 |

## LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

| Pin Type | | LFE2-20 | | | | LFE2-35 | |
|---|---|---|---|---|---|---|---|
| | | 208 PQFP | 256 fpBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 1 | 2 | 2 | 2 | 3 |
| | Bank3 | 0 | 0 | 0 | 2 | 0 | 2 |
| | Bank4 | 0 | 2 | 3 | 3 | 3 | 3 |
| | Bank5 | 0 | 1 | 3 | 4 | 3 | 4 |
| | Bank6 | 0 | 1 | 2 | 3 | 1 | 3 |
| | Bank7 | 0 | 1 | 2 | 2 | 2 | 3 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 19 | 32 | 46 | 50 | 46 | 54 |
| | Bank5 | 18 | 17 | 46 | 68 | 46 | 68 |
| | Bank6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank7 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

## LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

| Pin Type | | LFE2-50 | | LFE2-70 | |
|---|---|---|---|---|---|
| | | 484 fpBGA | 672 fpBGA | 672 fpBGA | 900 fpBGA |
| Single Ended User I/O | | 339 | 500 | 500 | 583 |
| Differential Pair User I/O | | 169 | 249 | 249 | 290 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 68 | 79 | 79 | 89 |
| | Dedicated Pins | 3 | 3 | 3 | 3 |
| VCC | | 16 | 20 | 20 | 26 |
| VCCAUX | | 16 | 16 | 16 | 17 |
| VCCPLL | | 4 | 4 | 2 | 4 |
| VCCIO | Bank0 | 4 | 5 | 5 | 6 |
| | Bank1 | 4 | 5 | 5 | 6 |
| | Bank2 | 4 | 5 | 5 | 6 |
| | Bank3 | 4 | 5 | 5 | 6 |
| | Bank4 | 4 | 5 | 5 | 6 |
| | Bank5 | 4 | 5 | 5 | 6 |
| | Bank6 | 4 | 5 | 5 | 6 |
| | Bank7 | 4 | 5 | 5 | 6 |
| | Bank8 | 2 | 2 | 2 | 2 |
| GND, GND0 to GND7 | | 60 | 72 | 72 | 104 |
| NC | | 0 | 3 | 5 | 101 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 50/25 | 67/33 | 67/33 | 84/42 |
| | Bank1 | 46/23 | 66/33 | 66/33 | 76/38 |
| | Bank2 | 38/19 | 56/28 | 56/28 | 74/37 |
| | Bank3 | 22/11 | 48/24 | 48/24 | 48/24 |
| | Bank4 | 46/23 | 62/31 | 62/31 | 72/35 |
| | Bank5 | 46/23 | 68/34 | 68/34 | 80/40 |
| | Bank6 | 40/20 | 64/32 | 64/32 | 64/32 |
| | Bank7 | 37/18 | 55/27 | 55/27 | 71/35 |
| | Bank8 | 14/7 | 14/7 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 9 | 13 | 13 | 18 |
| | Bank3 (Right Edge) | 5 | 12 | 12 | 12 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 10 | 16 | 16 | 16 |
| | Bank7 (Left Edge) | 8 | 12 | 12 | 16 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 |

## LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70 (Cont.)

| Pin Type | | LFE2-50 | | LFE2-70 | |
|---|---|---|---|---|---|
| | | 484 fpBGA | 672 fpBGA | 672 fpBGA | 900 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 |
| | Bank2 | 2 | 3 | 3 | 4 |
| | Bank3 | 0 | 3 | 3 | 3 |
| | Bank4 | 3 | 4 | 4 | 4 |
| | Bank5 | 3 | 4 | 4 | 5 |
| | Bank6 | 1 | 4 | 4 | 4 |
| | Bank7 | 2 | 3 | 3 | 4 |
| | Bank8 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 |
| | Bank4 | 46 | 62 | 62 | 72 |
| | Bank5 | 46 | 68 | 68 | 80 |
| | Bank6 | 0 | 0 | 0 | 0 |
| | Bank7 | 0 | 0 | 0 | 0 |
| | Bank8 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

## LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

| Pin Type | | LFE2M20 | | LFE2M35 | | |
|---|---|---|---|---|---|---|
| | | 256 fpBGA | 484 fpBGA | 256 fpBGA | 484 fpBGA | 672 fpBGA |
| Single Ended User I/O | | 140 | 304 | 140 | 303 | 410 |
| Differential Pair User I/O | | 70 | 152 | 70 | 151 | 199 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 64 | 84 | 60 | 84 | 89 |
| | Dedicated Pins | 3 | 3 | 3 | 3 | 3 |
| VCC | | 6 | 16 | 6 | 16 | 29 |
| VCCAUX | | 4 | 8 | 4 | 8 | 17 |
| VCCPLL | | 1 | 4 | 1 | 4 | 8 |
| VCCIO | Bank0 | 1 | 4 | 1 | 4 | 5 |
| | Bank1 | 1 | 3 | 1 | 3 | 4 |
| | Bank2 | 2 | 4 | 2 | 4 | 5 |
| | Bank3 | 2 | 4 | 2 | 4 | 5 |
| | Bank4 | 2 | 4 | 2 | 4 | 4 |
| | Bank5 | 2 | 4 | 2 | 4 | 5 |
| | Bank6 | 2 | 4 | 2 | 4 | 5 |
| | Bank7 | 2 | 4 | 2 | 4 | 5 |
| | Bank8 | 1 | 2 | 1 | 2 | 2 |
| GND, GND0 to GND7 | | 22 | 57 | 22 | 57 | 80 |
| NC | | 17 | 11 | 17 | 12 | 37 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 0/0 | 36/18 | 0/0 | 36/18 | 63/31 |
| | Bank1 | 0/0 | 18/9 | 0/0 | 18/9 | 18/9 |
| | Bank2 | 14/7 | 30/15 | 14/7 | 30/15 | 50/25 |
| | Bank3 | 16/8 | 36/18 | 16/8 | 36/18 | 43/21 |
| | Bank4 | 32/16 | 62/31 | 32/16 | 62/31 | 50/21 |
| | Bank5 | 20/10 | 28/14 | 20/10 | 28/14 | 60/30 |
| | Bank6 | 16/8 | 40/20 | 16/8 | 39/19 | 52/25 |
| | Bank7 | 28/14 | 40/20 | 28/14 | 40/20 | 60/30 |
| | Bank8 | 14/7 | 14/7 | 14/7 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 3 | 7 | 3 | 7 | 12 |
| | Bank3 (Right Edge) | 4 | 9 | 4 | 9 | 11 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 4 | 10 | 4 | 10 | 14 |
| | Bank7 (Left Edge) | 7 | 10 | 7 | 10 | 15 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 | 0 |

## LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35 (Cont.)

| Pin Type | | LFE2M20 | | LFE2M35 | | |
|---|---|---|---|---|---|---|
| | | 256 fpBGA | 484 fpBGA | 256 fpBGA | 484 fpBGA | 672 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 1 | 0 | 1 | 3 |
| | Bank3 | 0 | 1 | 0 | 1 | 2 |
| | Bank4 | 2 | 4 | 2 | 4 | 3 |
| | Bank5 | 1 | 2 | 1 | 2 | 3 |
| | Bank6 | 0 | 3 | 0 | 1 | 2 |
| | Bank7 | 1 | 2 | 1 | 2 | 3 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 32 | 62 | 32 | 62 | 50 |
| | Bank5 | 20 | 28 | 20 | 28 | 60 |
| | Bank6 | 16 | 40 | 16 | 39 | 52 |
| | Bank7 | 28 | 40 | 28 | 40 | 60 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

# LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100

| Pin Type | | LFE2M50 | | | LFE2M70 | | LFE2M100 | |
|---|---|---|---|---|---|---|---|---|
| | | 484 fpBGA | 672 fpBGA | 900 fpBGA | 900 fpBGA | 1152 fpBGA | 900 fpBGA | 1152 fpBGA |
| Single Ended User I/O | | 270 | 372 | 410 | 416 | 436 | 416 | 520 |
| Differential Pair User I/O | | 135 | 185 | 205 | 208 | 218 | 207 | 260 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 69 | 72 | 72 | 75 | 76 | 74 | 78 |
| | Dedicated Pins | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| VCC | | 16 | 20 | 62 | 44 | 44 | 44 | 44 |
| VCCAUX | | 8 | 26 | 18 | 16 | 12 | 16 | 12 |
| VCCPLL | | 4 | 8 | 4 | 4 | 4 | 4 | 4 |
| VCCIO | Bank0 | 4 | 5 | 6 | 6 | 7 | 6 | 7 |
| | Bank1 | 3 | 4 | 6 | 6 | 7 | 6 | 7 |
| | Bank2 | 4 | 5 | 9 | 9 | 9 | 9 | 9 |
| | Bank3 | 4 | 5 | 9 | 9 | 9 | 9 | 9 |
| | Bank4 | 4 | 4 | 6 | 6 | 7 | 6 | 7 |
| | Bank5 | 4 | 5 | 6 | 6 | 7 | 6 | 7 |
| | Bank6 | 4 | 5 | 9 | 9 | 9 | 9 | 9 |
| | Bank7 | 4 | 5 | 9 | 9 | 9 | 9 | 9 |
| | Bank8 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GND, GND0 to GND7 | | 57 | 80 | 122 | 122 | 134 | 122 | 134 |
| NC | | 31 | 35 | 121 | 63 | 283 | 63 | 199 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 36/18 | 63/31 | 56/28 | 34/17 | 46/23 | 34/17 | 54/27 |
| | Bank1 | 18/9 | 18/9 | 36/18 | 42/21 | 34/17 | 42/21 | 44/22 |
| | Bank2 | 30/15 | 50/25 | 54/27 | 70/35 | 72/36 | 70/35 | 80/40 |
| | Bank3 | 36/18 | 43/21 | 44/22 | 60/30 | 64/32 | 60/30 | 80/40 |
| | Bank4 | 42/21 | 24/12 | 38/19 | 38/19 | 40/20 | 38/19 | 44/22 |
| | Bank5 | 28/14 | 60/30 | 58/29 | 40/20 | 40/20 | 40/20 | 46/23 |
| | Bank6 | 40/20 | 54/27 | 60/30 | 62/31 | 66/33 | 62/31 | 82/41 |
| | Bank7 | 40/20 | 60/30 | 64/32 | 70/35 | 74/37 | 70/35 | 90/45 |
| | Bank8 | 0/0 | 0/0 | 0/0 | 0/0 | 0/0 | 0/0 | 0/0 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 7 | 12 | 13 | 17 | 18 | 17 | 20 |
| | Bank3 (Right Edge) | 9 | 11 | 11 | 15 | 16 | 15 | 20 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 10 | 14 | 15 | 15 | 16 | 15 | 20 |
| | Bank7 (Left Edge) | 10 | 15 | 17 | 17 | 18 | 17 | 22 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 (Cont.)

| Pin Type | | LFE2M50 | | | LFE2M70 | | LFE2M100 | |
|---|---|---|---|---|---|---|---|---|
| | | 484 fpBGA | 672 fpBGA | 900 fpBGA | 900 fpBGA | 1152 fpBGA | 900 fpBGA | 1152 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 2 | 2 | 2 | 4 | 4 | 4 | 4 |
| | Bank3 | 2 | 1 | 1 | 3 | 4 | 3 | 5 |
| | Bank4 | 3 | 1 | 3 | 3 | 3 | 3 | 3 |
| | Bank5 | 2 | 3 | 3 | 2 | 3 | 2 | 3 |
| | Bank6 | 1 | 2 | 2 | 3 | 4 | 3 | 5 |
| | Bank7 | 3 | 3 | 3 | 4 | 4 | 4 | 5 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 | 72 | 0 | 80 |
| | Bank3 | 0 | 0 | 0 | 0 | 64 | 0 | 80 |
| | Bank4 | 50 | 24 | 48 | 48 | 40 | 48 | 44 |
| | Bank5 | 60 | 60 | 50 | 40 | 40 | 40 | 46 |
| | Bank6 | 52 | 54 | 60 | 62 | 66 | 62 | 82 |
| | Bank7 | 60 | 60 | 68 | 70 | 74 | 70 | 90 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

## Available Device Resources by Package, LatticeECP2

| Resource | Device | 256 fpBGA | 484 fpBGA | 672 fpBGA | 900 fpBGA |
|---|---|---|---|---|---|
| PLL/DLL | ECP2-6 | 4 | — | — | — |
| | ECP2-12 | 4 | 4 | — | — |
| | ECP2-20 | 4 | 4 | 4 | — |
| | ECP2-35 | — | 4 | 4 | — |
| | ECP2-50 | — | 6 | 6 | — |
| | ECP2-70 | — | — | 8 | 8 |

## Available Device Resources by Package, LatticeECP2M

| Resource | Device | 256 fpBGA | 484 fpBGA | 672 fpBGA | 900 fpBGA | 1152 fpBGA |
|---|---|---|---|---|---|---|
| PLL/DLL | ECP2M20 | 10 | 10 | — | — | — |
| | ECP2M35 | 10 | 10 | 10 | — | — |
| | ECP2M50 | — | 10 | 10 | 10 | — |
| | ECP2M70 | — | — | — | 10 | 10 |
| | ECP2M100 | — | — | — | 10 | 10 |

## LatticeECP2 Power Supply and NC

| Signals | 144 TQFP[3] | 208 PQFP[3] | 256 fpBGA[4] | 484 fpBGA[4] |
|---|---|---|---|---|
| VCC | 16, 22, 29, 48, 54, 83, 94, 102, 128, 135 | 12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198 | **LFE2-6:** G7, G9, G10, H7, J10, K10, K8<br>**LFE2-12/LFE2-20:** G7, G9, G10, H7, J10, K10, K8 | **LFE2-12/LFE2-20:** N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13<br>**LFE2-35/LFE2-50:** J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 |
| VCCIO0 | 139 | 195, 206 | C5, E7 | G10, G9, H8, H9 |
| VCCIO1 | 117 | 162, 170 | C12, E10 | G11, G12, G13, G14 |
| VCCIO2 | 106 | 143, 148 | E14, G12 | H14, H15, J15, K16 |
| VCCIO3 | 89 | 123, 135 | K12, M14 | L16, M16, N16, P16 |
| VCCIO4 | 64 | 93, 100 | M10, P12 | R14, T12, T13, T14 |
| VCCIO5 | 42 | 55, 63 | M7, P5 | R9, T10, T11, T9 |
| VCCIO6 | 31 | 38, 44 | K5, M3 | N7, P7, P8, R8 |
| VCCIO7 | 9 | 10, 14 | E3, G5 | J8, K7, L7, M7 |
| VCCIO8 | 85 | 113, 118 | T15 | P15, R15 |
| VCCJ | 35 | 51 | K7 | T8 |
| VCCAUX | 6, 39, 90, 142 | 7, 30, 70, 86, 125, 151, 174, 190 | G8, H10, J7, K9 | G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6 |
| VCCPLL | None | None | None | **LFE2-12/LFE2-20:** None<br>**LFE2-35:** N6, N18<br>**LFE2-50:** N6, N18, K6, J16 |
| GND[1] | 11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138 | 5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201 | A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16 | A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1 |
| NC[2] | **LFE2-6:** 45, 46, 124, 127<br>**LFE2-12:** 127 | None | **LFE2-6:** K6, R3, P4<br>**LFE2-12/LFE2-20:** None | **LFE2-12:** E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18<br>**LFE2-20/LFE2-35:** K6, J16, H6, J6, H3, H2, H17, H16, H20, H18<br>**LFE2-50:** None |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

## LatticeECP2 Power Supply and NC (Cont.)

| Signals | 672 fpBGA[3] | 900 fpBGA[3] |
|---|---|---|
| VCC | **LFE2-20:** R8, P18, M8, L20, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15<br>**LFE2-35/LFE2-50:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15<br>**LFE2-70:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 | AA11, AA20, K11, K21, K22, L11, L12, L13, L18, L19, L20, M11, M20, N11, N20, V11, V20, W11, W20, Y10, Y11, Y12, Y13, Y18, Y19, Y20 |
| VCCIO0 | D11, D6, G9, J12, K12 | J13, J14, K12, K13, K14, K15 |
| VCCIO1 | D16, D21, G18, J15, K15 | J17, J18, J20, K17, K18, K20 |
| VCCIO2 | F23, J20, L23, M17, M18 | L21, M21, M22, N21, N22, R21 |
| VCCIO3 | AA23, R17, R18, T23, V20 | U21, U22, V21, V22, W21, Y22 |
| VCCIO4 | AC16, AC21, U15, V15, Y18 | AA16, AA17, AA18, AA19, AB17, AB18 |
| VCCIO5 | AC11, AC6, U12, V12, Y9 | AA12, AA13, AA14, AB12, AB13, AB14 |
| VCCIO6 | AA4, R10, R9, T4, V7 | U10, U9, V10, W10, W9, Y9 |
| VCCIO7 | F4, J7, L4, M10, M9 | L10, L9, M10, N10, P10, R10 |
| VCCIO8 | AE25, V18 | AA21, Y21 |
| VCCJ | AB5 | AD3 |
| VCCAUX | J10, J11, J16, J17, K18, L18, T18, U18, V16, V17, V10, V11, T9, U9, K9, L9 | AA15, AB11, AB19, AB20, J11, J12, J19, K19, L22, M9, N9, P21, P9, T10, T21, V9, W22 |
| VCCPLL | **LFE2-20:** None<br>**LFE2-35/LFE2-70:** R8, P18<br>**LFE2-50:** R8, P18, M8, L20 | P22, P8, T22, Y7 |
| GND[1] | A2, A25, AA18, AA24, AA3, AA9, AD11, AD16, AD21, AD6, AE1, AE26, AF2, AF25, B1, B26, C11, C16, C21, C6, F18, F24, F3, F9, J13, J14, J21, J6, K10, K11, K13, K14, K16, K17, L10, L11, L16, L17, L24, L3, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T24, T3, U10, U11, U13, U14, U16, U17, V13, V14, V21, V6 | A1, A30, AC28, AC3, AH13, AH18, AH23, AH28, AH3, AH8, AK1, AK30, C13, C18, C23, C28, C3, C8, H28, H3, L14, L15, L16, L17, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, N28, N3, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V12, V13, V14, V15, V16, V17, V18, V19, V28, V3, W12, W13, W14, W15, W16, W17, W18, W19, Y14, Y15, Y16, Y17 |
| NC[2] | **LFE2-20:** E4, E3, E2, E1, H6, H5, F2, F1, H8, J9, G4, G3, K3, K2, K1, L2, L1, M2, M1, N2, T1, T2, P8, P6, P5, P4, U1, V1, P3, R3, R4, U2, V2, W2, T6, R5, AA19, W17, Y19, Y17, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, R22, T21, P26, P25, R24, R23, P20, R19, P21, P19, P23, P22, N22, R21, N26, N25, J26, J25, J23, K23, H26, H25, H24, H23, F22, E24, D25, C25, D24, B25, H21, G22, B24, C24, D23, C23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24<br>**LFE2-35:** K3, K2, K1, L2, L1, M2, M1, N2, M8, P3, R3, R4, U2, V2, W2, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, P26, P25, R24, R23, P20, R19, L20, J26, J25, J23, K23, H26, H25, H24, H23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24<br>**LFE2-50:** N6, P24, M3<br>**LFE2-70:** M8, L20, M3, P24, N6 | A2, A3, A4, A5, AB28, AC4, AD23, AE1, AE2, AE29, AE3, AE30, AE4, AE5, AE6, AF1, AF2, AF23, AF26, AF27, AF28, AF29, AF3, AF30, AF4, AF5, AG1, AG13, AG16, AG18, AG2, AG26, AG27, AG28, AG29, AG3, AG30, AG4, AG8, AH1, AH16, AH2, AH26, AH27, AH29, AH30, AH4, AJ1, AJ2, AJ27, AJ28, AJ29, AJ3, AJ30, AK2, AK27, AK28, AK29, AK3, B1, B2, B3, B30, B4, B5, C1, C2, C29, C30, C4, D13, D18, D23, D28, D29, D3, D30, D4, E25, E26, E27, E28, E29, E3, E30, E4, E5, E6, F25, F5, F6, G6, G7, K10, K9, N27, N4, R1, R2, V27, V4 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

## LatticeECP2M Power Supply and NC

| Signal | 256 fpBGA | 484 fpBGA |
|---|---|---|
| $V_{CC}$ | G7, G9, H7, J10, K10, K8 | J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 |
| $V_{CCIO0}$ | E7 | B5, B9, E7, H9 |
| $V_{CCIO1}$ | E10 | D13, E16, H14 |
| $V_{CCIO2}$ | E14, G12 | E21, G18, J15, K19 |
| $V_{CCIO3}$ | K12, M14 | N19, P15, T18, V21 |
| $V_{CCIO4}$ | M10, P12 | AA18, R14, V16, W13 |
| $V_{CCIO5}$ | M7, P5 | AA5, R9, V7, W10 |
| $V_{CCIO6}$ | K5, M3 | N4, P8, T5, V2 |
| $V_{CCIO7}$ | E3, G5 | E2, G5, J8, K4 |
| $V_{CCIO8}$ | T15 | AA22, U19 |
| $V_{CCJ}$ | K7 | W4 |
| $V_{CCAUX}$ | G8, H10, J7, K9 | H11, H12, L15, L8, M15, M8, R11, R12 |
| $V_{CCPLL}$ | G10 | R8, H15, H8, R15 |
| SERDES Power[3] | C15, B15, C12, A12, C11, C10, C14, C13, B9, C9, C5, C4, C8, C7, A6, C6, B3, C3 | C22, B22, C19, A19, C18, C17, C21, C20, B16, C16, C12, C11, C15, C14, A13, C13, B10, C10 |
| GND[1] | A1, A15, A16, A3, A9, B12, B6, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16 | A1, A10, A16, A22, AA19, AA4, AB1, AB22, B13, B19, B4, D16, D2, D21, D7, G19, G4, H10, H13, J14, J9, K10, K11, K12, K13, K15, K20, K3, K8, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, N15, N20, N3, N8, P14, P9, R10, R13, T19, T4, W16, W2, W21, W7, Y10, Y13 |
| NC[2] | D10, D11, D12, D13, D14, D4, D5, D6, D7, E11, E6, E8, E9, F10, F7, F8, F9 | **LFE2M20:** D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15<br>**LFE2M35:** D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15, U6<br>**LFE2M50:** Y15, W15, AB20, AB21, AA20, AB19, AB18, Y22, Y21, Y17, Y18, Y16, W17, Y19, Y20, W19, W18, V17, V18, D15, G14, G15, D14, E15, E14, F15, F14, F13, G12, G13 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

## LatticeECP2M Power Supply and NC (Cont.)

| Signal | 672 fpBGA | 900 fpBGA |
|---|---|---|
| $V_{CC}$ | **LFE2M35:** AD13, AD14, AD16, AD17, AD19, AD21, AD22, AD24, AD25, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15<br><br>**LFE2M50:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 | **LFE2M50:** AH1, AH4, AH5, AH2, AH7, AH12, AH9, AH10, AH13, C13, C10, C9, C12, C7, C2, C5, C4, C1, L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19<br><br>**LFE2M70/LFE2M100:** L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19 |
| $V_{CCIO0}$ | B12, B7, F11, J13, K12 | D14, E6, E9, F12, K12, K13 |
| $V_{CCIO1}$ | D18, F16, J14, K15 | D17, E22, E25, F19, K18, K19 |
| $V_{CCIO2}$ | G25, L21, M17, M25, N18 | F28, J25, K28, M21, M24, N21, N28, P21, R25 |
| $V_{CCIO3}$ | P18, R17, R25, T21, Y25 | AA28, AB25, AE28, T25, U21, V21, V28, W21, W24 |
| $V_{CCIO4}$ | AA16, AC18, U15, V14 | AA18, AA19, AE19, AF22, AG17, AG25 |
| $V_{CCIO5}$ | AA11, AE12, AE7, U12, V13 | AA12, AA13, AE12, AF9, AG14, AG6 |
| $V_{CCIO6}$ | P9, R10, R2, T6, Y2 | AA3, AB6, AE3, T6, U10, V10, V3, W10, W7 |
| $V_{CCIO7}$ | G2, L6, M10, M2, N9 | F3, J6, K3, M10, M7, N10, N3, P10, R6 |
| $V_{CCIO8}$ | AC24, U17 | AA25, AD28 |
| $V_{CCJ}$ | AA7 | AG1 |
| $V_{CCAUX}$ | **LFE2M35:** AE19, J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16<br><br>**LFE2M50:** J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16 | **LFE2M50:** AJ7, B7, AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21<br><br>**LFE2M70/LFE2M100:** AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21 |
| $V_{CCPLL}$ | H7, K6, P7, R8, V18, P20, J17, G19 | N13, N18, V13, V18 |
| SERDES Power[3] | **LFE2M35:** C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13<br><br>**LFE2M50:** AD13, AE13, AD16, AF16, AD17, AD18, AD14, AD15, AD19, AE19, AD23, AD24, AD20, AD21, AF22, AD22, AE25, AD25, C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13 | **LFE2M50:** AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18<br><br>**LFE2M70/LFE2M100:** C13, B13, C10, A10, C9, C8, C12, C11, B7, C7, C3, C2, C6, C5, A4, C4, B1, C1, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18, AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, AH1, AJ1, AH4, AK4, AH5, AH6, AH2, AH3, AH7, AJ7, AH11, AH12, AH8, AH9, AK10, AH10, AJ13, AH13 |

## LatticeECP2M Power Supply and NC (Cont.)

| Signal | 672 fpBGA | 900 fpBGA |
|---|---|---|
| GND[1] | A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16 | **LFE2M50:** A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17<br><br>**LFE2M70/LFE2M100:** A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 |
| NC[2] | **LFE2M35:** AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7<br><br>**LFE2M50:** AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20 | **LFE2M50:** G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9<br><br>**LFE2M70/LFE2M100:** AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

## LatticeECP2M Power Supply and NC (Cont.)

| Signal | 1152 fpBGA |
|---|---|
| $V_{CC}$ | AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB14, AB15, AB20, AB21, N14, N15, N20, N21, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R21, R22, T14, T21, U14, U21, V14, V21, W14, W21, Y13, Y14, Y21, Y22 |
| $V_{CCIO0}$ | C12, C16, E14, H12, H16, M14, M15 |
| $V_{CCIO1}$ | C19, C23, E21, H19, H23, M20, M21 |
| $V_{CCIO2}$ | G32, K28, K32, N27, N32, P23, R23, T27, T32 |
| $V_{CCIO3}$ | AA23, AB27, AB32, AE28, AE32, AH32, W27, W32, Y23 |
| $V_{CCIO4}$ | AC20, AC21, AG19, AG23, AK21, AM19, AM23 |
| $V_{CCIO5}$ | AC14, AC15, AG12, AG16, AK14, AM12, AM16 |
| $V_{CCIO6}$ | AA12, AB3, AB8, AE3, AE7, AH3, W3, W8, Y12 |
| $V_{CCIO7}$ | G3, K3, K7, N3, N8, P12, R12, T3, T8 |
| $V_{CCIO8}$ | AD28, AG32 |
| $V_{CCJ}$ | AK3 |
| $V_{CCAUX}$ | AB12, AB13, AB22, AB23, AC13, AC22, M13, M22, N12, N13, N22, N23 |
| $V_{CCPLL}$ | R15, R20, Y15, Y20 |
| SERDES Power[3] | D7, B9, B8, D9, B7, E7, B6, D8, E6, D6, D4, B5, D3, B4, C1, B3, B1, B2, B33, B34, B32, C34, B31, D32, B30, D31, E29, D29, D27, B29, E28, B28, D26, B27, B26, D28, AL28, AN26, AN27, AL26, AN28, AK28, AN29, AL27, AL29, AK29, AL31, AN30, AL32, AN31, AM34, AN32, AN34, AN33, AN2, AN1, AN3, AM1, AN4, AL3, AN5, AL4, AL6, AK6, AL8, AN6, AK7, AN7, AL9, AN8, AN9, AL7 |
| GND[1] | A1, A10, A13, A22, A25, A34, AB16, AB17, AB18, AB19, AB26, AB31, AB4, AB9, AC16, AC17, AC18, AC19, AD27, AE27, AE31, AE4, AE8, AF12, AF16, AF19, AF23, AG31, AH31, AH4, AJ14, AJ21, AK27, AK8, AL10, AL16, AL19, AL2, AL25, AL33, AP1, AP10, AP13, AP22, AP25, AP34, D10, D16, D19, D2, D25, D33, E27, E8, F14, F21, G31, G4, J12, J16, J19, J23, K27, K31, K4, K8, M16, M17, M18, M19, N16, N17, N18, N19, N26, N31, N4, N9, R16, R17, R18, R19, T12, T13, T15, T16, T17, T18, T19, T20, T22, T23, T26, T31, T4, T9, U12, U13, U15, U16, U17, U18, U19, U20, U22, U23, V12, V13, V15, V16, V17, V18, V19, V20, V22, V23, W12, W13, W15, W16, W17, W18, W19, W20, W22, W23, W26, W31, W4, W9, Y16, Y17, Y18, Y19 |
| NC[2] | **LFE2M70:** H2, H1, G5, G6, M9, M10, H3, H4, P3, P4, P9, M7, P1, P2, N7, P7, AC7, AC5, AC6, AD5, AD4, AD3, AD10, AD8, AD2, AD1, AD9, AC11, AD6, AD7, AE1, AE2, AJ12, AH12, AL13, AK13, AE14, AG13, AH22, AH21, AG22, AG21, AF33, AF34, AC27, AC28, AD29, AD30, AE33, AE34, AD32, AD31, AB25, AC25, AB28, AA26, AD33, AD34, P30, P29, P31, P32, R25, T24, N34, N33, F24, G23, J22, G22, H21, K21, L19, L20, L18, K19, J14, L15, H14, K14, F12, D11, F11, E11, A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11<br><br>**LFE2M100:** A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11,G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

| LFE2-6E/SE | | | | | LFE2-12E/12SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 1 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| 2 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| 3 | PL4A | 7 | | T (LVDS)* | PL4A | 7 | | T (LVDS)* |
| 4 | PL4B | 7 | | C (LVDS)* | PL4B | 7 | | C (LVDS)* |
| 5 | PL6A | 7 | LDQ10 | T (LVDS)* | PL6A | 7 | LDQ10 | T (LVDS)* |
| 6 | VCCAUX | - | | | VCCAUX | - | | |
| 7 | PL6B | 7 | LDQ10 | C (LVDS)* | PL6B | 7 | LDQ10 | C (LVDS)* |
| 8 | PL8A | 7 | LDQ10 | T (LVDS)* | PL8A | 7 | LDQ10 | T (LVDS)* |
| 9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 10 | PL8B | 7 | LDQ10 | C (LVDS)* | PL8B | 7 | LDQ10 | C (LVDS)* |
| 11 | GND | - | | | GND | - | | |
| 12 | PL12A | 7 | LDQ10 | T (LVDS)* | PL12A | 7 | LDQ10 | T (LVDS)* |
| 13 | PL12B | 7 | LDQ10 | C (LVDS)* | PL12B | 7 | LDQ10 | C (LVDS)* |
| 14 | PL13A | 7 | PCLKT7_0/LDQ10 | T | PL13A | 7 | PCLKT7_0/LDQ10 | T |
| 15 | PL13B | 7 | PCLKC7_0/LDQ10 | C | PL13B | 7 | PCLKC7_0/LDQ10 | C |
| 16 | VCC | - | | | VCC | - | | |
| 17 | PL15A | 6 | PCLKT6_0 | T (LVDS)* | PL15A | 6 | PCLKT6_0 | T (LVDS)* |
| 18 | PL15B | 6 | PCLKC6_0 | C (LVDS)* | PL15B | 6 | PCLKC6_0 | C (LVDS)* |
| 19 | PL16A | 6 | VREF2_6 | T | PL16A | 6 | VREF2_6 | T |
| 20 | PL16B | 6 | VREF1_6 | C | PL16B | 6 | VREF1_6 | C |
| 21 | GND | - | | | GND | - | | |
| 22 | VCC | - | | | VCC | - | | |
| 23 | PL18A | 6 | LLM0_GDLLT_FB_A | T | PL18A | 6 | LLM0_GDLLT_FB_A | T |
| 24 | PL18B | 6 | LLM0_GDLLC_FB_A | C | PL18B | 6 | LLM0_GDLLC_FB_A | C |
| 25 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| 26 | PL20A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* | PL20A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* |
| 27 | PL20B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* | PL20B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* |
| 28 | PL22A | 6 | | | PL22A | 6 | | |
| 29 | VCC | - | | | VCC | - | | |
| 30 | GND | - | | | GND | - | | |
| 31 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 32 | TCK | - | | | TCK | - | | |
| 33 | TDI | - | | | TDI | - | | |
| 34 | TDO | - | | | TDO | - | | |
| 35 | VCCJ | - | | | VCCJ | - | | |
| 36 | TMS | - | | | TMS | - | | |
| 37 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| 38 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| 39 | VCCAUX | - | | | VCCAUX | - | | |
| 40 | PB4A | 5 | BDQ6 | T | PB6A | 5 | BDQS6 | T |
| 41 | PB4B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| 42 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 43 | PB6A | 5 | BDQS6 | T | PB12A | 5 | BDQ15 | T |
| 44 | PB6B | 5 | BDQ6 | C | PB12B | 5 | BDQ15 | C |
| 45 | NC | 5 | | | PB16A | 5 | BDQ15 | T |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/12SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 46 | NC | 5 | | | PB16B | 5 | BDQ15 | C |
| 47 | GND | - | | | GND | - | | |
| 48 | VCC | | | | VCC | - | | |
| 49 | PB8A | 5 | PCLKT5_0/BDQ6 | T | PB26A | 5 | PCLKT5_0/BDQ24 | T |
| 50 | PB8B | 5 | PCLKC5_0/BDQ6 | C | PB26B | 5 | PCLKC5_0/BDQ24 | C |
| 51 | GND | - | | | GND | - | | |
| 52 | PB13A | 4 | PCLKT4_0/BDQ15 | T | PB31A | 4 | PCLKT4_0/BDQ33 | T |
| 53 | PB13B | 4 | PCLKC4_0/BDQ15 | C | PB31B | 4 | PCLKC4_0/BDQ33 | C |
| 54 | VCC | - | | | VCC | - | | |
| 55 | PB14A | 4 | BDQ15 | T | PB34A | 4 | BDQ33 | T |
| 56 | PB14B | 4 | BDQ15 | C | PB34B | 4 | BDQ33 | C |
| 57 | PB16A | 4 | BDQ15 | T | PB40A | 4 | BDQ42 | T |
| 58 | PB16B | 4 | BDQ15 | C | PB40B | 4 | BDQ42 | C |
| 59 | PB18A | 4 | BDQ15 | T | PB44A | 4 | BDQ42 | T |
| 60 | PB18B | 4 | BDQ15 | C | PB44B | 4 | BDQ42 | C |
| 61 | GND | - | | | GND | - | | |
| 62 | PB20A | 4 | BDQ24 | T | PB48A | 4 | BDQ51 | T |
| 63 | PB20B | 4 | BDQ24 | C | PB48B | 4 | BDQ51 | C |
| 64 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 65 | PB22A | 4 | BDQ24 | T | PB50A | 4 | BDQ51 | T |
| 66 | PB22B | 4 | BDQ24 | C | PB50B | 4 | BDQ51 | C |
| 67 | PB24A | 4 | BDQS24 | T | PB52A | 4 | BDQ51 | T |
| 68 | PB24B | 4 | BDQ24 | C | PB52B | 4 | BDQ51 | C |
| 69 | PB26A | 4 | BDQ24 | T | PB54A | 4 | BDQ51 | T |
| 70 | PB26B | 4 | BDQ24 | C | PB54B | 4 | BDQ51 | C |
| 71 | PB28A | 4 | VREF2_4/BDQ24 | T | PB55A | 4 | VREF2_4/BDQ51 | T |
| 72 | PB28B | 4 | VREF1_4/BDQ24 | C | PB55B | 4 | VREF1_4/BDQ51 | C |
| 73 | CFG1 | 8 | | | CFG1 | 8 | | |
| 74 | CFG2 | 8 | | | CFG2 | 8 | | |
| 75 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| 76 | INITN | 8 | | | INITN | 8 | | |
| 77 | CFG0 | 8 | | | CFG0 | 8 | | |
| 78 | CCLK | 8 | | | CCLK | 8 | | |
| 79 | DONE | 8 | | | DONE | 8 | | |
| 80 | PR29A | 8 | D0/SPIFASTN | | PR29A | 8 | D0/SPIFASTN | |
| 81 | GND | - | | | GND | - | | |
| 82 | PR26A | 8 | D6 | | PR26A | 8 | D6 | |
| 83 | VCC | - | | | VCC | - | | |
| 84 | PR25B | 8 | D7/SPID0 | C | PR25B | 8 | D7/SPID0 | C |
| 85 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| 86 | PR25A | 8 | DI/CSSPI0N | T | PR25A | 8 | DI/CSSPI0N | T |
| 87 | PR24B | 8 | DOUT/CSON | C | PR24B | 8 | DOUT/CSON | C |
| 88 | PR24A | 8 | BUSY/SISPI | T | PR24A | 8 | BUSY/SISPI | T |
| 89 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 90 | VCCAUX | - | | | VCCAUX | - | | |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/12SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 91 | PR20B | 3 | RLM0_GPLLC_IN_A** | C (LVDS)* | PR20B | 3 | RLM0_GPLLC_IN_A** | C (LVDS)* |
| 92 | PR20A | 3 | RLM0_GPLLT_IN_A** | T (LVDS)* | PR20A | 3 | RLM0_GPLLT_IN_A** | T (LVDS)* |
| 93 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| 94 | VCC | - | | | VCC | - | | |
| 95 | GND | - | | | GND | - | | |
| 96 | PR17B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR17B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* |
| 97 | PR17A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR17A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* |
| 98 | PR16B | 3 | VREF2_3 | C | PR16B | 3 | VREF2_3 | C |
| 99 | PR16A | 3 | VREF1_3 | T | PR16A | 3 | VREF1_3 | T |
| 100 | PR15B | 3 | PCLKC3_0 | C (LVDS)* | PR15B | 3 | PCLKC3_0 | C (LVDS)* |
| 101 | PR15A | 3 | PCLKT3_0 | T (LVDS)* | PR15A | 3 | PCLKT3_0 | T (LVDS)* |
| 102 | VCC | - | | | VCC | - | | |
| 103 | PR13B | 2 | PCLKC2_0/RDQ10 | C | PR13B | 2 | PCLKC2_0/RDQ10 | C |
| 104 | PR13A | 2 | PCLKT2_0/RDQ10 | T | PR13A | 2 | PCLKT2_0/RDQ10 | T |
| 105 | GND | - | | | GND | - | | |
| 106 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 107 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| 108 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| 109 | PT28B | 1 | VREF2_1 | C | PT55B | 1 | VREF2_1 | C |
| 110 | PT28A | 1 | VREF1_1 | T | PT55A | 1 | VREF1_1 | T |
| 111 | PT26B | 1 | | C | PT54B | 1 | | C |
| 112 | PT26A | 1 | | T | PT54A | 1 | | T |
| 113 | PT24B | 1 | | C | PT52B | 1 | | C |
| 114 | PT24A | 1 | | T | PT52A | 1 | | T |
| 115 | PT22B | 1 | | C | PT50B | 1 | | C |
| 116 | PT22A | 1 | | T | PT50A | 1 | | T |
| 117 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 118 | PT20B | 1 | | C | PT48B | 1 | | C |
| 119 | PT20A | 1 | | T | PT48A | 1 | | T |
| 120 | GND | - | | | GND | - | | |
| 121 | PT18B | 1 | | C | PT44B | 1 | | C |
| 122 | PT18A | 1 | | T | PT44A | 1 | | T |
| 123 | PT16A | 1 | | | PT40B | 1 | | C |
| 124 | NC | 1 | | | PT40A | 1 | | T |
| 125 | PT14B | 1 | | C | PT34B | 1 | | C |
| 126 | PT14A | 1 | | T | PT34A | 1 | | T |
| 127 | NC | 1 | | | NC | 1 | | |
| 128 | VCC | - | | | VCC | - | | |
| 129 | PT12B | 1 | PCLKC1_0 | C | PT30B | 1 | PCLKC1_0 | C |
| 130 | PT12A | 1 | PCLKT1_0 | T | PT30A | 1 | PCLKT1_0 | T |
| 131 | PT10B | 0 | PCLKC0_0 | C | PT28B | 0 | PCLKC0_0 | C |
| 132 | XRES | 0 | | | XRES | 0 | | |
| 133 | GND | - | | | GND | - | | |
| 134 | PT10A | 0 | PCLKT0_0 | T | PT28A | 0 | PCLKT0_0 | T |
| 135 | VCC | - | | | VCC | - | | |

## LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/12SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 136 | PT6B | 0 | | C | PT16B | 0 | | C |
| 137 | PT6A | 0 | | T | PT16A | 0 | | T |
| 138 | GND | - | | | GND | - | | |
| 139 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 140 | PT4B | 0 | | C | PT6B | 0 | | C |
| 141 | PT4A | 0 | | T | PT6A | 0 | | T |
| 142 | VCCAUX | - | | | VCCAUX | - | | |
| 143 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| 144 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one-to-one connection with a package ball or pin.

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 1 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| 2 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| 3 | PL4A | 7 | | T (LVDS)* | PL6A | 7 | LDQ8 | T (LVDS)* |
| 4 | PL4B | 7 | | C (LVDS)* | PL6B | 7 | LDQ8 | C (LVDS)* |
| 5 | GND | - | | | GND | - | | |
| 6 | PL6A | 7 | LDQ10 | T (LVDS)* | PL12A | 7 | LDQ16 | T (LVDS)* |
| 7 | VCCAUX | - | | | VCCAUX | - | | |
| 8 | PL6B | 7 | LDQ10 | C (LVDS)* | PL12B | 7 | LDQ16 | C (LVDS)* |
| 9 | PL8A | 7 | LDQ10 | T (LVDS)* | PL14A | 7 | LDQ16 | T (LVDS)* |
| 10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 11 | PL8B | 7 | LDQ10 | C (LVDS)* | PL14B | 7 | LDQ16 | C (LVDS)* |
| 12 | VCC | - | | | VCC | - | | |
| 13 | GND | - | | | GND | - | | |
| 14 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 15 | PL12A | 7 | LDQ10 | T (LVDS)* | PL18A | 7 | LDQ16 | T (LVDS)* |
| 16 | PL12B | 7 | LDQ10 | C (LVDS)* | PL18B | 7 | LDQ16 | C (LVDS)* |
| 17 | GND | - | | | GND | - | | |
| 18 | PL13A | 7 | PCLKT7_0/LDQ10 | T | PL19A | 7 | PCLKT7_0/LDQ16 | T |
| 19 | VCC | - | | | VCC | - | | |
| 20 | PL13B | 7 | PCLKC7_0/LDQ10 | C | PL19B | 7 | PCLKC7_0/LDQ16 | C |
| 21 | PL15A | 6 | PCLKT6_0 | T (LVDS)* | PL21A | 6 | PCLKT6_0/LDQ25 | T (LVDS)* |
| 22 | PL15B | 6 | PCLKC6_0 | C (LVDS)* | PL21B | 6 | PCLKC6_0/LDQ25 | C (LVDS)* |
| 23 | PL16A | 6 | VREF2_6 | T | PL22A | 6 | VREF2_6/LDQ25 | T |
| 24 | PL16B | 6 | VREF1_6 | C | PL22B | 6 | VREF1_6/LDQ25 | C |
| 25 | GND | - | | | GND | - | | |
| 26 | PL17A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* | PL27A | 6 | LLM0_GDLLT_IN_A**/LDQ25 | T (LVDS)* |
| 27 | PL17B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* | PL27B | 6 | LLM0_GDLLC_IN_A**/LDQ25 | C (LVDS)* |
| 28 | VCC | - | | | VCC | - | | |
| 29 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| 30 | VCCAUX | - | | | VCCAUX | - | | |
| 31 | PL20A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* | PL30A | 6 | LLM0_GPLLT_IN_A**/LDQ34 | T (LVDS)* |
| 32 | GND | - | | | GND | - | | |
| 33 | PL21A | 6 | LLM0_GPLLT_FB_A | T | PL31A | 6 | LLM0_GPLLT_FB_A/LDQ34 | T |
| 34 | PL20B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* | PL30B | 6 | LLM0_GPLLC_IN_A**/LDQ34 | C (LVDS)* |
| 35 | PL21B | 6 | LLM0_GPLLC_FB_A | C | PL31B | 6 | LLM0_GPLLC_FB_A/LDQ34 | C |
| 36 | PL23A | 6 | | | PL33A | 6 | LDQ34 | |
| 37 | PL24A | 6 | LDQ28 | T (LVDS)* | PL38A | 6 | LDQ42 | T (LVDS)* |
| 38 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 39 | PL24B | 6 | LDQ28 | C (LVDS)* | PL38B | 6 | LDQ42 | C (LVDS)* |
| 40 | VCC | - | | | VCC | - | | |
| 41 | PL26A | 6 | LDQ28 | T (LVDS)* | PL40A | 6 | LDQ42 | T (LVDS)* |
| 42 | GND | - | | | GND | - | | |
| 43 | PL26B | 6 | LDQ28 | C (LVDS)* | PL40B | 6 | LDQ42 | C (LVDS)* |
| 44 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 45 | PL28A | 6 | LDQS28 | T (LVDS)* | PL42A | 6 | LDQS42 | T (LVDS)* |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 46 | PL28B | 6 | LDQ28 | C (LVDS)* | PL42B | 6 | LDQ42 | C (LVDS)* |
| 47 | PL30A | 6 | LDQ28 | | PL44A | 6 | LDQ42 | |
| 48 | TCK | - | | | TCK | - | | |
| 49 | TDI | - | | | TDI | - | | |
| 50 | TDO | - | | | TDO | - | | |
| 51 | VCCJ | - | | | VCCJ | - | | |
| 52 | TMS | - | | | TMS | - | | |
| 53 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| 54 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| 55 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 56 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| 57 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| 58 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| 59 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| 60 | GND | - | | | GND | - | | |
| 61 | PB12A | 5 | BDQ15 | T | PB12A | 5 | BDQ15 | T |
| 62 | PB12B | 5 | BDQ15 | C | PB12B | 5 | BDQ15 | C |
| 63 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 64 | PB16A | 5 | BDQ15 | T | PB16A | 5 | BDQ15 | T |
| 65 | PB16B | 5 | BDQ15 | C | PB16B | 5 | BDQ15 | C |
| 66 | PB18A | 5 | BDQ15 | T | PB18A | 5 | BDQ15 | T |
| 67 | PB18B | 5 | BDQ15 | C | PB18B | 5 | BDQ15 | C |
| 68 | GND | - | | | GND | - | | |
| 69 | PB20A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| 70 | VCCAUX | - | | | VCCAUX | - | | |
| 71 | PB20B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| 72 | PB22A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| 73 | PB22B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| 74 | VCC | - | | | VCC | - | | |
| 75 | PB26A | 5 | PCLKT5_0/BDQ24 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| 76 | PB26B | 5 | PCLKC5_0/BDQ24 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| 77 | GND | - | | | GND | - | | |
| 78 | PB31A | 4 | PCLKT4_0/BDQ33 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| 79 | PB31B | 4 | PCLKC4_0/BDQ33 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| 80 | VCC | - | | | VCC | - | | |
| 81 | GND | - | | | GND | - | | |
| 82 | PB34A | 4 | BDQ33 | T | PB42A | 4 | BDQS42 | T |
| 83 | PB34B | 4 | BDQ33 | C | PB42B | 4 | BDQ42 | C |
| 84 | PB36A | 4 | BDQ33 | T | PB44A | 4 | BDQ42 | T |
| 85 | PB36B | 4 | BDQ33 | C | PB44B | 4 | BDQ42 | C |
| 86 | VCCAUX | - | | | VCCAUX | - | | |
| 87 | PB40A | 4 | BDQ42 | T | PB50A | 4 | BDQ51 | T |
| 88 | PB40B | 4 | BDQ42 | C | PB50B | 4 | BDQ51 | C |
| 89 | GND | - | | | GND | - | | |
| 90 | PB42A | 4 | BDQS42 | T | PB52A | 4 | BDQ51 | T |
| 91 | PB42B | 4 | BDQ42 | C | PB52B | 4 | BDQ51 | C |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 92 | PB44A | 4 | BDQ42 | T | PB54A | 4 | BDQ51 | T |
| 93 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 94 | PB44B | 4 | BDQ42 | C | PB54B | 4 | BDQ51 | C |
| 95 | PB48A | 4 | BDQ51 | T | PB58A | 4 | BDQ60 | T |
| 96 | PB48B | 4 | BDQ51 | C | PB58B | 4 | BDQ60 | C |
| 97 | VCC | - | | | VCC | - | | |
| 98 | PB52A | 4 | BDQ51 | T | PB60A | 4 | BDQS60 | T |
| 99 | PB52B | 4 | BDQ51 | C | PB60B | 4 | BDQ60 | C |
| 100 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 101 | PB54A | 4 | BDQ51 | | PB63A | 4 | BDQ60 | |
| 102 | GND | - | | | GND | - | | |
| 103 | PB55A | 4 | VREF2_4/BDQ51 | T | PB64A | 4 | VREF2_4/BDQ60 | T |
| 104 | PB55B | 4 | VREF1_4/BDQ51 | C | PB64B | 4 | VREF1_4/BDQ60 | C |
| 105 | CFG1 | 8 | | | CFG1 | 8 | | |
| 106 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| 107 | CFG2 | 8 | | | CFG2 | 8 | | |
| 108 | INITN | 8 | | | INITN | 8 | | |
| 109 | CFG0 | 8 | | | CFG0 | 8 | | |
| 110 | CCLK | 8 | | | CCLK | 8 | | |
| 111 | DONE | 8 | | | DONE | 8 | | |
| 112 | PR29A | 8 | D0/SPIFASTN | | PR43A | 8 | D0/SPIFASTN | |
| 113 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| 114 | PR26A | 8 | D6 | | PR40A | 8 | D6 | |
| 115 | GND | - | | | GND | - | | |
| 116 | VCC | - | | | VCC | - | | |
| 117 | PR25B | 8 | D7/SPID0 | C | PR39B | 8 | D7/SPID0 | C |
| 118 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| 119 | PR25A | 8 | DI/CSSPI0N | T | PR39A | 8 | DI/CSSPI0N | T |
| 120 | PR24B | 8 | DOUT/CSON | C | PR38B | 8 | DOUT/CSON | C |
| 121 | PR24A | 8 | BUSY/SISPI | T | PR38A | 8 | BUSY/SISPI | T |
| 122 | GND | - | | | GND | - | | |
| 123 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 124 | PR21A | 3 | RLM0_GPLLT_FB_A | | PR31A | 3 | RLM0_GPLLT_FB_A/RDQ34 | |
| 125 | VCCAUX | - | | | VCCAUX | - | | |
| 126 | PR20B | 3 | RLM0_GPLLC_IN_A** | C (LVDS)* | PR30B | 3 | RLM0_GPLLC_IN_A**/RDQ34 | C (LVDS)* |
| 127 | PR20A | 3 | RLM0_GPLLT_IN_A** | T (LVDS)* | PR30A | 3 | RLM0_GPLLT_IN_A**/RDQ34 | T (LVDS)* |
| 128 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| 129 | VCC | - | | | VCC | - | | |
| 130 | PR18B | 3 | RLM0_GDLLC_FB_A | C | PR28B | 3 | RLM0_GDLLC_FB_A/RDQ25 | C |
| 131 | PR18A | 3 | RLM0_GDLLT_FB_A | T | PR28A | 3 | RLM0_GDLLT_FB_A/RDQ25 | T |
| 132 | PR17B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR27B | 3 | RLM0_GDLLC_IN_A**/RDQ25 | C (LVDS)* |
| 133 | PR17A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR27A | 3 | RLM0_GDLLT_IN_A**/RDQ25 | T (LVDS)* |
| 134 | PR16B | 3 | VREF2_3 | C | PR22B | 3 | VREF2_3/RDQ25 | C |
| 135 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 136 | PR16A | 3 | VREF1_3 | T | PR22A | 3 | VREF1_3/RDQ25 | T |
| 137 | PR15B | 3 | PCLKC3_0 | C (LVDS)* | PR21B | 3 | PCLKC3_0/RDQ25 | C (LVDS)* |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 138 | PR15A | 3 | PCLKT3_0 | T (LVDS)* | PR21A | 3 | PCLKT3_0/RDQ25 | T (LVDS)* |
| 139 | GND | - | | | GND | - | | |
| 140 | VCC | - | | | VCC | - | | |
| 141 | PR13B | 2 | PCLKC2_0/RDQ10 | C | PR19B | 2 | PCLKC2_0/RDQ16 | C |
| 142 | PR13A | 2 | PCLKT2_0/RDQ10 | T | PR19A | 2 | PCLKT2_0/RDQ16 | T |
| 143 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 144 | PR12A | 2 | RDQ10 | | PR16A | 2 | RDQS16 | |
| 145 | GND | - | | | GND | - | | |
| 146 | VCC | - | | | VCC | - | | |
| 147 | PR8B | 2 | RDQ10 | C (LVDS)* | PR14B | 2 | RDQ16 | C (LVDS)* |
| 148 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 149 | PR8A | 2 | RDQ10 | T (LVDS)* | PR14A | 2 | RDQ16 | T (LVDS)* |
| 150 | PR6B | 2 | RDQ10 | C (LVDS)* | PR12B | 2 | RDQ16 | C (LVDS)* |
| 151 | VCCAUX | - | | | VCCAUX | - | | |
| 152 | PR6A | 2 | RDQ10 | T (LVDS)* | PR12A | 2 | RDQ16 | T (LVDS)* |
| 153 | PR4B | 2 | | C (LVDS)* | PR6B | 2 | RDQ8 | C (LVDS)* |
| 154 | PR4A | 2 | | T (LVDS)* | PR6A | 2 | RDQ8 | T (LVDS)* |
| 155 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| 156 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| 157 | PT55B | 1 | VREF2_1 | C | PT64B | 1 | VREF2_1 | C |
| 158 | PT55A | 1 | VREF1_1 | T | PT64A | 1 | VREF1_1 | T |
| 159 | GND | - | | | GND | - | | |
| 160 | PT54B | 1 | | C | PT62B | 1 | | C |
| 161 | PT54A | 1 | | T | PT62A | 1 | | T |
| 162 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 163 | PT52B | 1 | | C | PT60B | 1 | | C |
| 164 | PT52A | 1 | | T | PT60A | 1 | | T |
| 165 | PT50B | 1 | | C | PT58B | 1 | | C |
| 166 | PT50A | 1 | | T | PT58A | 1 | | T |
| 167 | PT48B | 1 | | C | PT56B | 1 | | C |
| 168 | PT48A | 1 | | T | PT56A | 1 | | T |
| 169 | GND | - | | | GND | - | | |
| 170 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 171 | VCC | - | | | VCC | - | | |
| 172 | PT40B | 1 | | C | PT50B | 1 | | C |
| 173 | PT40A | 1 | | T | PT50A | 1 | | T |
| 174 | VCCAUX | - | | | VCCAUX | - | | |
| 175 | GND | - | | | GND | - | | |
| 176 | PT36B | 1 | | C | PT44B | 1 | | C |
| 177 | PT36A | 1 | | T | PT44A | 1 | | T |
| 178 | PT34B | 1 | | C | PT42B | 1 | | C |
| 179 | PT34A | 1 | | T | PT42A | 1 | | T |
| 180 | PT30B | 1 | PCLKC1_0 | C | PT39B | 1 | PCLKC1_0 | C |
| 181 | PT30A | 1 | PCLKT1_0 | T | PT39A | 1 | PCLKT1_0 | T |
| 182 | XRES | 1 | | | XRES | 1 | | |
| 183 | PT28B | 0 | PCLKC0_0 | C | PT37B | 0 | PCLKC0_0 | C |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 184 | GND | - | | | GND | - | | |
| 185 | PT28A | 0 | PCLKT0_0 | T | PT37A | 0 | PCLKT0_0 | T |
| 186 | PT26B | 0 | | C | PT36B | 0 | | C |
| 187 | PT26A | 0 | | T | PT36A | 0 | | T |
| 188 | VCC | - | | | VCC | - | | |
| 189 | PT20B | 0 | | C | PT30B | 0 | | C |
| 190 | VCCAUX | - | | | VCCAUX | - | | |
| 191 | PT20A | 0 | | T | PT30A | 0 | | T |
| 192 | GND | - | | | GND | - | | |
| 193 | PT18B | 0 | | C | PT26B | 0 | | C |
| 194 | PT18A | 0 | | T | PT26A | 0 | | T |
| 195 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 196 | PT16B | 0 | | C | PT20B | 0 | | C |
| 197 | PT16A | 0 | | T | PT20A | 0 | | T |
| 198 | VCC | - | | | VCC | - | | |
| 199 | PT12B | 0 | | C | PT12B | 0 | | C |
| 200 | PT12A | 0 | | T | PT12A | 0 | | T |
| 201 | GND | - | | | GND | - | | |
| 202 | PT8B | 0 | | C | PT8B | 0 | | C |
| 203 | PT8A | 0 | | T | PT8A | 0 | | T |
| 204 | PT6B | 0 | | C | PT6B | 0 | | C |
| 205 | PT6A | 0 | | T | PT6A | 0 | | T |
| 206 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 207 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| 208 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C3 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| C2 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| - | - | - | | | - | - | | |
| D3 | PL5A | 7 | | T | PL5A | 7 | | T |
| D4 | PL4A | 7 | | T (LVDS)* | PL4A | 7 | | T (LVDS)* |
| D2 | PL5B | 7 | | C | PL5B | 7 | | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| E4 | PL4B | 7 | | C (LVDS)* | PL4B | 7 | | C (LVDS)* |
| B1 | PL7A | 7 | LDQ10 | T | PL7A | 7 | LDQ10 | T |
| C1 | PL7B | 7 | LDQ10 | C | PL7B | 7 | LDQ10 | C |
| F5 | PL9A | 7 | LDQ10 | T | PL9A | 7 | LDQ10 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F4 | PL8A | 7 | LDQ10 | T (LVDS)* | PL8A | 7 | LDQ10 | T (LVDS)* |
| G6 | PL9B | 7 | LDQ10 | C | PL9B | 7 | LDQ10 | C |
| G4 | PL8B | 7 | LDQ10 | C (LVDS)* | PL8B | 7 | LDQ10 | C (LVDS)* |
| D1 | PL10A | 7 | LDQS10 | T (LVDS)* | PL10A | 7 | LDQS10 | T (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| E1 | PL10B | 7 | LDQ10 | C (LVDS)* | PL10B | 7 | LDQ10 | C (LVDS)* |
| F3 | PL11A | 7 | LDQ10 | T | PL11A | 7 | LDQ10 | T |
| G3 | PL11B | 7 | LDQ10 | C | PL11B | 7 | LDQ10 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F2 | PL12A | 7 | LDQ10 | T (LVDS)* | PL12A | 7 | LDQ10 | T (LVDS)* |
| F1 | PL12B | 7 | LDQ10 | C (LVDS)* | PL12B | 7 | LDQ10 | C (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| G2 | PL13A | 7 | PCLKT7_0/LDQ10 | T | PL13A | 7 | PCLKT7_0/LDQ10 | T |
| G1 | PL13B | 7 | PCLKC7_0/LDQ10 | C | PL13B | 7 | PCLKC7_0/LDQ10 | C |
| H6 | PL15A | 6 | PCLKT6_0 | T (LVDS)* | PL15A | 6 | PCLKT6_0 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| H5 | PL15B | 6 | PCLKC6_0 | C (LVDS)* | PL15B | 6 | PCLKC6_0 | C (LVDS)* |
| H4 | PL16A | 6 | VREF2_6 | T | PL16A | 6 | VREF2_6 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| H3 | PL16B | 6 | VREF1_6 | C | PL16B | 6 | VREF1_6 | C |
| H2 | PL17A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* | PL17A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* |
| H1 | PL17B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* | PL17B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* |
| G10 | VCC | - | | | VCC | - | | |
| J4 | PL18A | 6 | LLM0_GDLLT_FB_A | T | PL18A | 6 | LLM0_GDLLT_FB_A | T |
| J5 | PL18B | 6 | LLM0_GDLLC_FB_A | C | PL18B | 6 | LLM0_GDLLC_FB_A | C |
| J6 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| K4 | PL20A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* | PL20A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| J1 | PL21A | 6 | LLM0_GPLLT_FB_A | T | PL21A | 6 | LLM0_GPLLT_FB_A | T |
| K3 | PL20B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* | PL20B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| J2 | PL21B | 6 | LLM0_GPLLC_FB_A | C | PL21B | 6 | LLM0_GPLLC_FB_A | C |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| L2 | PL24A | 6 | LDQ28 | T (LVDS)* | PL24A | 6 | LDQ28 | T (LVDS)* |
| K2 | PL25A | 6 | LDQ28 | T | PL25A | 6 | LDQ28 | T |
| L3 | PL24B | 6 | LDQ28 | C (LVDS)* | PL24B | 6 | LDQ28 | C (LVDS)* |
| K1 | PL25B | 6 | LDQ28 | C | PL25B | 6 | LDQ28 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| L4 | PL26A | 6 | LDQ28 | T (LVDS)* | PL26A | 6 | LDQ28 | T (LVDS)* |
| L1 | PL27A | 6 | LDQ28 | T | PL27A | 6 | LDQ28 | T |
| L5 | PL26B | 6 | LDQ28 | C (LVDS)* | PL26B | 6 | LDQ28 | C (LVDS)* |
| M1 | PL27B | 6 | LDQ28 | C | PL27B | 6 | LDQ28 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| N1 | PL29A | 6 | LDQ28 | T | PL29A | 6 | LDQ28 | T |
| N2 | PL28A | 6 | LDQS28 | T (LVDS)* | PL28A | 6 | LDQS28 | T (LVDS)* |
| P1 | PL29B | 6 | LDQ28 | C | PL29B | 6 | LDQ28 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P2 | PL28B | 6 | LDQ28 | C (LVDS)* | PL28B | 6 | LDQ28 | C (LVDS)* |
| R1 | PL30A | 6 | LDQ28 | T (LVDS)* | PL30A | 6 | LDQ28 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| R2 | PL30B | 6 | LDQ28 | C (LVDS)* | PL30B | 6 | LDQ28 | C (LVDS)* |
| N4 | TDI | - | | | TDI | - | | |
| M4 | TCK | - | | | TCK | - | | |
| P3 | TDO | - | | | TDO | - | | |
| N3 | TMS | - | | | TMS | - | | |
| K7 | VCCJ | - | | | VCCJ | - | | |
| M5 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| K6 | NC | - | | | PB3A | 5 | BDQ6 | |
| M6 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| R3 | NC | - | | | PB5A | 5 | BDQ6 | T |
| P4 | NC | - | | | PB5B | 5 | BDQ6 | C |
| - | - | - | | | VCCIO | 5 | | |
| - | - | - | | | GNDIO5 | 5 | | |
| N5 | PB3A | 5 | BDQ6 | T | PB21A | 5 | BDQ24 | T |
| N6 | PB3B | 5 | BDQ6 | C | PB21B | 5 | BDQ24 | C |
| T2 | PB4A | 5 | BDQ6 | T | PB22A | 5 | BDQ24 | T |
| P6 | PB5A | 5 | BDQ6 | T | PB23A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T3 | PB4B | 5 | BDQ6 | C | PB22B | 5 | BDQ24 | C |
| R6 | PB5B | 5 | BDQ6 | C | PB23B | 5 | BDQ24 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| R4 | PB6A | 5 | BDQS6 | T | PB24A | 5 | BDQS24 | T |
| L6 | PB7A | 5 | BDQ6 | T | PB25A | 5 | BDQ24 | T |
| T4 | PB6B | 5 | BDQ6 | C | PB24B | 5 | BDQ24 | C |
| L7 | PB7B | 5 | BDQ6 | C | PB25B | 5 | BDQ24 | C |
| N7 | PB8A | 5 | PCLKT5_0/BDQ6 | T | PB26A | 5 | PCLKT5_0/BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M8 | PB8B | 5 | PCLKC5_0/BDQ6 | C | PB26B | 5 | PCLKC5_0/BDQ24 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| P7 | PB13A | 4 | PCLKT4_0/BDQ15 | T | PB31A | 4 | PCLKT4_0/BDQ33 | T |
| R8 | PB13B | 4 | PCLKC4_0/BDQ15 | C | PB31B | 4 | PCLKC4_0/BDQ33 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T5 | PB14A | 4 | BDQ15 | T | PB32A | 4 | BDQ33 | T |
| T6 | PB14B | 4 | BDQ15 | C | PB32B | 4 | BDQ33 | C |
| T8 | PB15A | 4 | BDQS15 | T | PB33A | 4 | BDQS33 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| R7 | PB16A | 4 | BDQ15 | T | PB34A | 4 | BDQ33 | T |
| T9 | PB15B | 4 | BDQ15 | C | PB33B | 4 | BDQ33 | C |
| T7 | PB16B | 4 | BDQ15 | C | PB34B | 4 | BDQ33 | C |
| L8 | PB17A | 4 | BDQ15 | T | PB35A | 4 | BDQ33 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| P8 | PB18A | 4 | BDQ15 | T | PB36A | 4 | BDQ33 | T |
| L9 | PB17B | 4 | BDQ15 | C | PB35B | 4 | BDQ33 | C |
| N8 | PB18B | 4 | BDQ15 | C | PB36B | 4 | BDQ33 | C |
| R9 | PB19A | 4 | BDQ15 | T | PB37A | 4 | BDQ33 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| R10 | PB19B | 4 | BDQ15 | C | PB37B | 4 | BDQ33 | C |
| - | - | - | | | VCCIO | 4 | | |
| - | - | - | | | GNDIO4 | 4 | | |
| N9 | PB20A | 4 | BDQ24 | T | PB47A | 4 | BDQ51 | T |
| T10 | PB21A | 4 | BDQ24 | T | PB48A | 4 | BDQ51 | T |
| M9 | PB20B | 4 | BDQ24 | C | PB47B | 4 | BDQ51 | C |
| R11 | PB21B | 4 | BDQ24 | C | PB48B | 4 | BDQ51 | C |
| P10 | PB22A | 4 | BDQ24 | T | PB49A | 4 | BDQ51 | T |
| N11 | PB23A | 4 | BDQ24 | T | PB50A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| N10 | PB22B | 4 | BDQ24 | C | PB49B | 4 | BDQ51 | C |
| P11 | PB23B | 4 | BDQ24 | C | PB50B | 4 | BDQ51 | C |
| T11 | PB24A | 4 | BDQS24 | T | PB51A | 4 | BDQS51 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| M11 | PB25A | 4 | BDQ24 | T | PB52A | 4 | BDQ51 | T |
| T12 | PB24B | 4 | BDQ24 | C | PB51B | 4 | BDQ51 | C |
| L11 | PB25B | 4 | BDQ24 | C | PB52B | 4 | BDQ51 | C |
| T13 | PB26A | 4 | BDQ24 | T | PB53A | 4 | BDQ51 | T |
| R13 | PB27A | 4 | BDQ24 | T | PB54A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T14 | PB26B | 4 | BDQ24 | C | PB53B | 4 | BDQ51 | C |
| P13 | PB27B | 4 | BDQ24 | C | PB54B | 4 | BDQ51 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| N12 | PB28A | 4 | VREF2_4/BDQ24 | T | PB55A | 4 | VREF2_4/BDQ51 | T |
| M12 | PB28B | 4 | VREF1_4/BDQ24 | C | PB55B | 4 | VREF1_4/BDQ51 | C |
| R15 | CFG2 | 8 | | | CFG2 | 8 | | |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N14 | CFG1 | 8 | | | CFG1 | 8 | | |
| N13 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| N15 | CFG0 | 8 | | | CFG0 | 8 | | |
| P15 | PR30B | 8 | WRITEN | C | PR30B | 8 | WRITEN | C |
| L12 | INITN | 8 | | | INITN | 8 | | |
| N16 | PR29B | 8 | CSN | C | PR29B | 8 | CSN | C |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| R14 | CCLK | 8 | | | CCLK | 8 | | |
| P14 | PR30A | 8 | CS1N | T | PR30A | 8 | CS1N | T |
| M13 | DONE | 8 | | | DONE | 8 | | |
| R16 | PR28B | 8 | D1 | C | PR28B | 8 | D1 | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| M16 | PR29A | 8 | D0/SPIFASTN | T | PR29A | 8 | D0/SPIFASTN | T |
| P16 | PR28A | 8 | D2 | T | PR28A | 8 | D2 | T |
| L15 | PR27B | 8 | D3 | C | PR27B | 8 | D3 | C |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| L14 | PR26A | 8 | D6 | T | PR26A | 8 | D6 | T |
| L16 | PR27A | 8 | D4 | T | PR27A | 8 | D4 | T |
| L10 | PR25B | 8 | D7/SPID0 | C | PR25B | 8 | D7/SPID0 | C |
| L13 | PR26B | 8 | D5 | C | PR26B | 8 | D5 | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| K11 | PR25A | 8 | DI/CSSPI0N | T | PR25A | 8 | DI/CSSPI0N | T |
| K14 | PR24B | 8 | DOUT/CSON | C | PR24B | 8 | DOUT/CSON | C |
| K13 | PR24A | 8 | BUSY/SISPI | T | PR24A | 8 | BUSY/SISPI | T |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| K15 | PR21B | 3 | RLM0_GPLLC_FB_A | C | PR21B | 3 | RLM0_GPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| K16 | PR21A | 3 | RLM0_GPLLT_FB_A | T | PR21A | 3 | RLM0_GPLLT_FB_A | T |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| J16 | PR20B | 3 | RLM0_GPLLC_IN_A** | C (LVDS)* | PR20B | 3 | RLM0_GPLLC_IN_A** | C (LVDS)* |
| J15 | PR20A | 3 | RLM0_GPLLT_IN_A** | T (LVDS)* | PR20A | 3 | RLM0_GPLLT_IN_A** | T (LVDS)* |
| J14 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| J13 | PR18B | 3 | RLM0_GDLLC_FB_A | C | PR18B | 3 | RLM0_GDLLC_FB_A | C |
| J12 | PR18A | 3 | RLM0_GDLLT_FB_A | T | PR18A | 3 | RLM0_GDLLT_FB_A | T |
| H12 | PR17B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR17B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| H13 | PR17A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR17A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* |
| H15 | PR16B | 3 | VREF2_3 | C | PR16B | 3 | VREF2_3 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| H16 | PR16A | 3 | VREF1_3 | T | PR16A | 3 | VREF1_3 | T |
| H11 | PR15B | 3 | PCLKC3_0 | C (LVDS)* | PR15B | 3 | PCLKC3_0 | C (LVDS)* |
| J11 | PR15A | 3 | PCLKT3_0 | T (LVDS)* | PR15A | 3 | PCLKT3_0 | T (LVDS)* |
| G16 | PR13B | 2 | PCLKC2_0/RDQ10 | C | PR13B | 2 | PCLKC2_0/RDQ10 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| G15 | PR13A | 2 | PCLKT2_0/RDQ10 | T | PR13A | 2 | PCLKT2_0/RDQ10 | T |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F15 | PR11B | 2 | RDQ10 | C | PR11B | 2 | RDQ10 | C |
| G11 | PR12B | 2 | RDQ10 | C (LVDS)* | PR12B | 2 | RDQ10 | C (LVDS)* |
| F14 | PR11A | 2 | RDQ10 | T | PR11A | 2 | RDQ10 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F12 | PR12A | 2 | RDQ10 | T (LVDS)* | PR12A | 2 | RDQ10 | T (LVDS)* |
| G14 | PR10B | 2 | RDQ10 | C (LVDS)* | PR10B | 2 | RDQ10 | C (LVDS)* |
| G13 | PR10A | 2 | RDQS10 | T (LVDS)* | PR10A | 2 | RDQS10 | T (LVDS)* |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| F16 | PR8B | 2 | RDQ10 | C (LVDS)* | PR8B | 2 | RDQ10 | C (LVDS)* |
| F9 | PR9B | 2 | RDQ10 | C | PR9B | 2 | RDQ10 | C |
| E16 | PR8A | 2 | RDQ10 | T (LVDS)* | PR8A | 2 | RDQ10 | T (LVDS)* |
| F10 | PR9A | 2 | RDQ10 | T | PR9A | 2 | RDQ10 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| D16 | PR7B | 2 | RDQ10 | C | PR7B | 2 | RDQ10 | C |
| D15 | PR7A | 2 | RDQ10 | T | PR7A | 2 | RDQ10 | T |
| C15 | PR4B | 2 | | C (LVDS)* | PR4B | 2 | | C (LVDS)* |
| C16 | PR5B | 2 | | C | PR5B | 2 | | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| D14 | PR4A | 2 | | T (LVDS)* | PR4A | 2 | | T (LVDS)* |
| B16 | PR5A | 2 | | T | PR5A | 2 | | T |
| F13 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| E13 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| F11 | PT28B | 1 | VREF2_1 | C | PT55B | 1 | VREF2_1 | C |
| E11 | PT28A | 1 | VREF1_1 | T | PT55A | 1 | VREF1_1 | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A15 | PT27B | 1 | | C | PT54B | 1 | | C |
| E12 | PT26B | 1 | | C | PT53B | 1 | | C |
| B15 | PT27A | 1 | | T | PT54A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D12 | PT26A | 1 | | T | PT53A | 1 | | T |
| B14 | PT25B | 1 | | C | PT52B | 1 | | C |
| C14 | PT24B | 1 | | C | PT51B | 1 | | C |
| A14 | PT25A | 1 | | T | PT52A | 1 | | T |
| D13 | PT24A | 1 | | T | PT51A | 1 | | T |
| C13 | PT23B | 1 | | C | PT50B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A13 | PT22B | 1 | | C | PT49B | 1 | | C |
| B13 | PT23A | 1 | | T | PT50A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A12 | PT22A | 1 | | T | PT49A | 1 | | T |
| B11 | PT21B | 1 | | C | PT48B | 1 | | C |
| D11 | PT20B | 1 | | C | PT47B | 1 | | C |
| A11 | PT21A | 1 | | T | PT48A | 1 | | T |
| C11 | PT20A | 1 | | T | PT47A | 1 | | T |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| - | - | - | | | GNDIO1 | 1 | | |
| - | - | - | | | VCCIO | 1 | | |
| D10 | PT19B | 1 | | C | PT37B | 1 | | C |
| C10 | PT19A | 1 | | T | PT37A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| B10 | PT18B | 1 | | C | PT36B | 1 | | C |
| A9 | PT17B | 1 | | C | PT35B | 1 | | C |
| A10 | PT18A | 1 | | T | PT36A | 1 | | T |
| B9 | PT17A | 1 | | T | PT35A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A8 | PT16B | 1 | | C | PT34B | 1 | | C |
| D9 | PT15B | 1 | | C | PT33B | 1 | | C |
| B8 | PT16A | 1 | | T | PT34A | 1 | | T |
| C9 | PT15A | 1 | | T | PT33A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| B7 | PT14B | 1 | | C | PT32B | 1 | | C |
| E9 | PT13B | 1 | | C | PT31B | 1 | | C |
| A7 | PT14A | 1 | | T | PT32A | 1 | | T |
| D8 | PT13A | 1 | | T | PT31A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A6 | PT12B | 1 | PCLKC1_0 | C | PT30B | 1 | PCLKC1_0 | C |
| B6 | PT12A | 1 | PCLKT1_0 | T | PT30A | 1 | PCLKT1_0 | T |
| E6 | XRES | - | | | XRES | 1 | | |
| F8 | PT10B | 0 | PCLKC0_0 | C | PT28B | 0 | PCLKC0_0 | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| E8 | PT10A | 0 | PCLKT0_0 | T | PT28A | 0 | PCLKT0_0 | T |
| A5 | PT9B | 0 | | C | PT27B | 0 | | C |
| A3 | PT8B | 0 | | C | PT26B | 0 | | C |
| A4 | PT9A | 0 | | T | PT27A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B3 | PT8A | 0 | | T | PT26A | 0 | | T |
| A2 | PT7B | 0 | | C | PT25B | 0 | | C |
| C7 | PT6B | 0 | | C | PT24B | 0 | | C |
| B2 | PT7A | 0 | | T | PT25A | 0 | | T |
| D7 | PT6A | 0 | | T | PT24A | 0 | | T |
| D6 | PT5B | 0 | | C | PT23B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| F7 | PT4B | 0 | | C | PT22B | 0 | | C |
| C6 | PT5A | 0 | | T | PT23A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F6 | PT4A | 0 | | T | PT22A | 0 | | T |
| C4 | PT3B | 0 | | C | PT21B | 0 | | C |
| B4 | PT3A | 0 | | T | PT21A | 0 | | T |
| - | - | - | | | GNDIO0 | 0 | | |
| - | - | - | | | VCCIO | 0 | | |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D5 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| E5 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |
| G7 | VCC | - | | | VCC | - | | |
| G9 | VCC | - | | | VCC | - | | |
| H7 | VCC | - | | | VCC | - | | |
| J10 | VCC | - | | | VCC | - | | |
| K10 | VCC | - | | | VCC | - | | |
| K8 | VCC | - | | | VCC | - | | |
| G8 | VCCAUX | - | | | VCCAUX | - | | |
| H10 | VCCAUX | - | | | VCCAUX | - | | |
| J7 | VCCAUX | - | | | VCCAUX | - | | |
| K9 | VCCAUX | - | | | VCCAUX | - | | |
| C5 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E7 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C12 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E10 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E14 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G12 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K12 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M14 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M10 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| P12 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| M7 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P5 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| K5 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| M3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| E3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G5 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T15 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| A1 | GND | - | | | GND | - | | |
| A16 | GND | - | | | GND | - | | |
| B12 | GND | - | | | GND | - | | |
| B5 | GND | - | | | GND | - | | |
| C8 | GND | - | | | GND | - | | |
| E15 | GND | - | | | GND | - | | |
| E2 | GND | - | | | GND | - | | |
| H14 | GND | - | | | GND | - | | |
| H8 | GND | - | | | GND | - | | |
| H9 | GND | - | | | GND | - | | |
| J3 | GND | - | | | GND | - | | |
| J8 | GND | - | | | GND | - | | |
| J9 | GND | - | | | GND | - | | |
| M15 | GND | - | | | GND | - | | |
| M2 | GND | - | | | GND | - | | |
| P9 | GND | - | | | GND | - | | |

## LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| R12 | GND | - | | | GND | - | | |
| R5 | GND | - | | | GND | - | | |
| T1 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| C3 | C3 | PL2A | 7 | VREF2_7 | T (LVDS)* |
| C2 | C2 | PL2B | 7 | VREF1_7 | C (LVDS)* |
| VCCIO | VCCIO | VCCIO7 | 7 | | |
| - | GND | GNDIO7 | 7 | | |
| D3 | D3 | PL7A | 7 | LDQ8 | T |
| D4 | D4 | PL6A | 7 | LDQ8 | T (LVDS)* |
| D2 | D2 | PL7B | 7 | LDQ8 | C |
| GND | GND | GNDIO7 | - | | |
| E4 | E4 | PL6B | 7 | LDQ8 | C (LVDS)* |
| B1 | B1 | PL13A | 7 | LDQ16 | T |
| C1 | C1 | PL13B | 7 | LDQ16 | C |
| F5 | F5 | PL15A | 7 | LDQ16 | T |
| VCCIO | VCC | VCCIO | 7 | | |
| F4 | F4 | PL14A | 7 | LDQ16 | T (LVDS)* |
| G6 | G6 | PL15B | 7 | LDQ16 | C |
| G4 | G4 | PL14B | 7 | LDQ16 | C (LVDS)* |
| D1 | D1 | PL16A | 7 | LDQS16 | T (LVDS)* |
| GND | GND | GNDIO7 | - | | |
| E1 | E1 | PL16B | 7 | LDQ16 | C (LVDS)* |
| F3 | F3 | PL17A | 7 | LDQ16 | T |
| G3 | G3 | PL17B | 7 | LDQ16 | C |
| VCCIO | VCCIO | VCCIO7 | 7 | | |
| F2 | F2 | PL18A | 7 | LDQ16 | T (LVDS)* |
| F1 | F1 | PL18B | 7 | LDQ16 | C (LVDS)* |
| GND | GND | GNDIO7 | - | | |
| G2 | G2 | PL19A | 7 | PCLKT7_0/LDQ16 | T |
| G1 | G1 | PL19B | 7 | PCLKC7_0/LDQ16 | C |
| H6 | H6 | PL21A | 6 | PCLKT6_0/LDQ25 | T (LVDS)* |
| VCCIO | VCCIO | VCCIO6 | 6 | | |
| H5 | H5 | PL21B | 6 | PCLKC6_0/LDQ25 | C (LVDS)* |
| H4 | H4 | PL22A | 6 | VREF2_6/LDQ25 | T |
| GND | GND | GNDIO6 | - | | |
| H3 | H3 | PL22B | 6 | VREF1_6/LDQ25 | C |
| H2 | H2 | PL27A | 6 | LLM0_GDLLT_IN_A**/LDQ25 | T (LVDS)* |
| H1 | H1 | PL27B | 6 | LLM0_GDLLC_IN_A**/LDQ25 | C (LVDS)* |
| G10 | G10 | VCC | - | | |
| J4 | J4 | PL28A | 6 | LLM0_GDLLT_FB_A/LDQ25 | T |
| J5 | J5 | PL28B | 6 | LLM0_GDLLC_FB_A/LDQ25 | C |
| J6 | J6 | LLM0_PLLCAP | 6 | | |
| K4 | K4 | PL30A | 6 | LLM0_GPLLT_IN_A**/LDQ34 | T (LVDS)* |
| GND | GND | GNDIO6 | - | | |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| J1 | J1 | PL31A | 6 | LLM0_GPLLT_FB_A/LDQ34 | T |
| K3 | K3 | PL30B | 6 | LLM0_GPLLC_IN_A**/LDQ34 | C (LVDS)* |
| VCCIO | VCCIO | VCCIO6 | 6 | | |
| J2 | J2 | PL31B | 6 | LLM0_GPLLC_FB_A/LDQ34 | C |
| GND | GND | GNDIO6 | - | | |
| L2 | L2 | PL38A | 6 | LDQ42 | T (LVDS)* |
| K2 | K2 | PL39A | 6 | LDQ42 | T |
| L3 | L3 | PL38B | 6 | LDQ42 | C (LVDS)* |
| K1 | K1 | PL39B | 6 | LDQ42 | C |
| VCCIO | VCCIO | VCCIO6 | 6 | | |
| L4 | L4 | PL40A | 6 | LDQ42 | T (LVDS)* |
| L1 | L1 | PL41A | 6 | LDQ42 | T |
| L5 | L5 | PL40B | 6 | LDQ42 | C (LVDS)* |
| M1 | M1 | PL41B | 6 | LDQ42 | C |
| GND | GND | GNDIO6 | - | | |
| N1 | N1 | PL43A | 6 | LDQ42 | T |
| N2 | N2 | PL42A | 6 | LDQS42 | T (LVDS)* |
| P1 | P1 | PL43B | 6 | LDQ42 | C |
| VCCIO | VCCIO | VCCIO6 | 6 | | |
| P2 | P2 | PL42B | 6 | LDQ42 | C (LVDS)* |
| R1 | R1 | PL44A | 6 | LDQ42 | T (LVDS)* |
| GND | GND | GNDIO6 | - | | |
| R2 | R2 | PL44B | 6 | LDQ42 | C (LVDS)* |
| N4 | N4 | TDI | - | | |
| M4 | M4 | TCK | - | | |
| P3 | P3 | TDO | - | | |
| N3 | N3 | TMS | - | | |
| K7 | K7 | VCCJ | - | | |
| M5 | M5 | PB2A | 5 | VREF2_5/BDQ6 | T |
| K6 | K6 | PB3A | 5 | BDQ6 | |
| M6 | M6 | PB2B | 5 | VREF1_5/BDQ6 | C |
| R3 | R3 | PB5A | 5 | BDQ6 | T |
| P4 | P4 | PB5B | 5 | BDQ6 | C |
| - | VCC | VCCIO | 5 | | |
| - | GND | GNDIO5 | 5 | | |
| N5 | N5 | PB30A | 5 | BDQ33 | T |
| N6 | N6 | PB30B | 5 | BDQ33 | C |
| T2 | T2 | PB31A | 5 | BDQ33 | T |
| P6 | P6 | PB32A | 5 | BDQ33 | T |
| VCCIO | VCCIO | VCCIO5 | 5 | | |
| T3 | T3 | PB31B | 5 | BDQ33 | C |
| R6 | R6 | PB32B | 5 | BDQ33 | C |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GND | GNDIO5 | - | | |
| R4 | R4 | PB33A | 5 | BDQS33 | T |
| L6 | L6 | PB34A | 5 | BDQ33 | T |
| T4 | T4 | PB33B | 5 | BDQ33 | C |
| L7 | L7 | PB34B | 5 | BDQ33 | C |
| N7 | N7 | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| VCCIO | VCCIO | VCCIO5 | 5 | | |
| M8 | M8 | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| GND | GND | GNDIO5 | - | | |
| P7 | P7 | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| R8 | R8 | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| VCCIO | VCCIO | VCCIO4 | 4 | | |
| T5 | T5 | PB41A | 4 | BDQ42 | T |
| T6 | T6 | PB41B | 4 | BDQ42 | C |
| T8 | T8 | PB42A | 4 | BDQS42 | T |
| GND | GND | GNDIO4 | - | | |
| R7 | R7 | PB43A | 4 | BDQ42 | T |
| T9 | T9 | PB42B | 4 | BDQ42 | C |
| T7 | T7 | PB43B | 4 | BDQ42 | C |
| L8 | L8 | PB44A | 4 | BDQ42 | T |
| VCCIO | VCCIO | VCCIO4 | 4 | | |
| P8 | P8 | PB45A | 4 | BDQ42 | T |
| L9 | L9 | PB44B | 4 | BDQ42 | C |
| N8 | N8 | PB45B | 4 | BDQ42 | C |
| R9 | R9 | PB46A | 4 | BDQ42 | T |
| GND | GND | GNDIO4 | - | | |
| R10 | R10 | PB46B | 4 | BDQ42 | C |
| - | VCC | VCCIO | 4 | | |
| - | GND | GNDIO4 | 4 | | |
| N9 | N9 | PB56A | 4 | BDQ60 | T |
| T10 | T10 | PB57A | 4 | BDQ60 | T |
| M9 | M9 | PB56B | 4 | BDQ60 | C |
| R11 | R11 | PB57B | 4 | BDQ60 | C |
| P10 | P10 | PB58A | 4 | BDQ60 | T |
| N11 | N11 | PB59A | 4 | BDQ60 | T |
| VCCIO | VCCIO | VCCIO4 | 4 | | |
| N10 | N10 | PB58B | 4 | BDQ60 | C |
| P11 | P11 | PB59B | 4 | BDQ60 | C |
| T11 | T11 | PB60A | 4 | BDQS60 | T |
| GND | GND | GNDIO4 | - | | |
| M11 | M11 | PB61A | 4 | BDQ60 | T |
| T12 | T12 | PB60B | 4 | BDQ60 | C |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| L11 | L11 | PB61B | 4 | BDQ60 | C |
| T13 | T13 | PB62A | 4 | BDQ60 | T |
| R13 | R13 | PB63A | 4 | BDQ60 | T |
| VCCIO | VCCIO | VCCIO4 | 4 | | |
| T14 | T14 | PB62B | 4 | BDQ60 | C |
| P13 | P13 | PB63B | 4 | BDQ60 | C |
| GND | GND | GNDIO4 | - | | |
| N12 | N12 | PB64A | 4 | VREF2_4/BDQ60 | T |
| M12 | M12 | PB64B | 4 | VREF1_4/BDQ60 | C |
| R15 | R15 | CFG2 | 8 | | |
| N14 | N14 | CFG1 | 8 | | |
| N13 | N13 | PROGRAMN | 8 | | |
| N15 | N15 | CFG0 | 8 | | |
| P15 | P15 | PR44B | 8 | WRITEN | C |
| L12 | L12 | INITN | 8 | | |
| N16 | N16 | PR43B | 8 | CSN | C |
| GND | GND | GNDIO8 | - | | |
| R14 | R14 | CCLK | 8 | | |
| P14 | P14 | PR44A | 8 | CS1N | T |
| M13 | M13 | DONE | 8 | | |
| R16 | R16 | PR42B | 8 | D1 | C |
| VCCIO | VCCIO | VCCIO8 | 8 | | |
| M16 | M16 | PR43A | 8 | D0/SPIFASTN | T |
| P16 | P16 | PR42A | 8 | D2 | T |
| L15 | L15 | PR41B | 8 | D3 | C |
| GND | GND | GNDIO8 | - | | |
| L14 | L14 | PR40A | 8 | D6 | T |
| L16 | L16 | PR41A | 8 | D4 | T |
| L10 | L10 | PR39B | 8 | D7/SPID0 | C |
| L13 | L13 | PR40B | 8 | D5 | C |
| VCCIO | VCCIO | VCCIO8 | 8 | | |
| K11 | K11 | PR39A | 8 | DI/CSSPI0N | T |
| K14 | K14 | PR38B | 8 | DOUT/CSON | C |
| K13 | K13 | PR38A | 8 | BUSY/SISPI | T |
| GND | GND | GNDIO8 | - | | |
| K15 | K15 | PR31B | 3 | RLM0_GPLLC_FB_A/RDQ34 | C |
| VCCIO | VCCIO | VCCIO3 | 3 | | |
| K16 | K16 | PR31A | 3 | RLM0_GPLLT_FB_A/RDQ34 | T |
| GND | GND | GNDIO3 | - | | |
| J16 | J16 | PR30B | 3 | RLM0_GPLLC_IN_A**/RDQ34 | C (LVDS)* |
| J15 | J15 | PR30A | 3 | RLM0_GPLLT_IN_A**/RDQ34 | T (LVDS)* |
| J14 | J14 | RLM0_PLLCAP | 3 | | |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| J13 | J13 | PR28B | 3 | RLM0_GDLLC_FB_A/RDQ25 | C |
| J12 | J12 | PR28A | 3 | RLM0_GDLLT_FB_A/RDQ25 | T |
| H12 | H12 | PR27B | 3 | RLM0_GDLLC_IN_A**/RDQ25 | C (LVDS)* |
| GND | GND | GNDIO3 | - | | |
| H13 | H13 | PR27A | 3 | RLM0_GDLLT_IN_A**/RDQ25 | T (LVDS)* |
| H15 | H15 | PR22B | 3 | VREF2_3/RDQ25 | C |
| VCCIO | VCCIO | VCCIO3 | 3 | | |
| H16 | H16 | PR22A | 3 | VREF1_3/RDQ25 | T |
| H11 | H11 | PR21B | 3 | PCLKC3_0/RDQ25 | C (LVDS)* |
| J11 | J11 | PR21A | 3 | PCLKT3_0/RDQ25 | T (LVDS)* |
| G16 | G16 | PR19B | 2 | PCLKC2_0/RDQ16 | C |
| GND | GND | GNDIO2 | - | | |
| G15 | G15 | PR19A | 2 | PCLKT2_0/RDQ16 | T |
| F15 | F15 | PR17B | 2 | RDQ16 | C |
| G11 | G11 | PR18B | 2 | RDQ16 | C (LVDS)* |
| F14 | F14 | PR17A | 2 | RDQ16 | T |
| VCCIO | VCCIO | VCCIO2 | 2 | | |
| F12 | F12 | PR18A | 2 | RDQ16 | T (LVDS)* |
| G14 | G14 | PR16B | 2 | RDQ16 | C (LVDS)* |
| G13 | G13 | PR16A | 2 | RDQS16 | T (LVDS)* |
| GND | GND | GNDIO2 | - | | |
| F16 | F16 | PR14B | 2 | RDQ16 | C (LVDS)* |
| F9 | F9 | PR15B | 2 | RDQ16 | C |
| E16 | E16 | PR14A | 2 | RDQ16 | T (LVDS)* |
| F10 | F10 | PR15A | 2 | RDQ16 | T |
| VCCIO | VCCIO | VCCIO2 | 2 | | |
| D16 | D16 | PR13B | 2 | RDQ16 | C |
| D15 | D15 | PR13A | 2 | RDQ16 | T |
| C15 | C15 | PR6B | 2 | RDQ8 | C (LVDS)* |
| C16 | C16 | PR7B | 2 | RDQ8 | C |
| GND | GND | GNDIO2 | - | | |
| D14 | D14 | PR6A | 2 | RDQ8 | T (LVDS)* |
| B16 | B16 | PR7A | 2 | RDQ8 | T |
| F13 | F13 | PR2B | 2 | VREF2_2 | C (LVDS)* |
| VCCIO | VCCIO | VCCIO2 | 2 | | |
| E13 | E13 | PR2A | 2 | VREF1_2 | T (LVDS)* |
| F11 | F11 | PT64B | 1 | VREF2_1 | C |
| E11 | E11 | PT64A | 1 | VREF1_1 | T |
| GND | GND | GNDIO1 | - | | |
| A15 | A15 | PT63B | 1 | | C |
| E12 | E12 | PT62B | 1 | | C |
| B15 | B15 | PT63A | 1 | | T |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| VCCIO | VCCIO | VCCIO1 | 1 | | |
| D12 | D12 | PT62A | 1 | | T |
| B14 | B14 | PT61B | 1 | | C |
| C14 | C14 | PT60B | 1 | | C |
| A14 | A14 | PT61A | 1 | | T |
| D13 | D13 | PT60A | 1 | | T |
| C13 | C13 | PT59B | 1 | | C |
| GND | GND | GNDIO1 | - | | |
| A13 | A13 | PT58B | 1 | | C |
| B13 | B13 | PT59A | 1 | | T |
| VCCIO | VCCIO | VCCIO1 | 1 | | |
| A12 | A12 | PT58A | 1 | | T |
| B11 | B11 | PT57B | 1 | | C |
| D11 | D11 | PT56B | 1 | | C |
| A11 | A11 | PT57A | 1 | | T |
| C11 | C11 | PT56A | 1 | | T |
| - | GND | GNDIO1 | 1 | | |
| - | VCC | VCCIO | 1 | | |
| D10 | D10 | PT46B | 1 | | C |
| C10 | C10 | PT46A | 1 | | T |
| GND | GND | GNDIO1 | - | | |
| B10 | B10 | PT45B | 1 | | C |
| A9 | A9 | PT44B | 1 | | C |
| A10 | A10 | PT45A | 1 | | T |
| B9 | B9 | PT44A | 1 | | T |
| VCCIO | VCCIO | VCCIO1 | 1 | | |
| A8 | A8 | PT43B | 1 | | C |
| D9 | D9 | PT42B | 1 | | C |
| B8 | B8 | PT43A | 1 | | T |
| C9 | C9 | PT42A | 1 | | T |
| GND | GND | GNDIO1 | - | | |
| B7 | B7 | PT41B | 1 | | C |
| E9 | E9 | PT40B | 1 | | C |
| A7 | A7 | PT41A | 1 | | T |
| D8 | D8 | PT40A | 1 | | T |
| VCCIO | VCCIO | VCCIO1 | 1 | | |
| A6 | A6 | PT39B | 1 | PCLKC1_0 | C |
| B6 | B6 | PT39A | 1 | PCLKT1_0 | T |
| E6 | E6 | XRES | 1 | | |
| F8 | F8 | PT37B | 0 | PCLKC0_0 | C |
| GND | GND | GNDIO0 | - | | |
| E8 | E8 | PT37A | 0 | PCLKT0_0 | T |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| A5 | A5 | PT36B | 0 | | C |
| A3 | A3 | PT35B | 0 | | C |
| A4 | A4 | PT36A | 0 | | T |
| VCCIO | VCCIO | VCCIO0 | 0 | | |
| B3 | B3 | PT35A | 0 | | T |
| A2 | A2 | PT34B | 0 | | C |
| C7 | C7 | PT33B | 0 | | C |
| B2 | B2 | PT34A | 0 | | T |
| D7 | D7 | PT33A | 0 | | T |
| D6 | D6 | PT32B | 0 | | C |
| GND | GND | GNDIO0 | - | | |
| F7 | F7 | PT31B | 0 | | C |
| C6 | C6 | PT32A | 0 | | T |
| VCCIO | VCCIO | VCCIO0 | 0 | | |
| F6 | F6 | PT31A | 0 | | T |
| C4 | C4 | PT30B | 0 | | C |
| B4 | B4 | PT30A | 0 | | T |
| - | GND | GNDIO0 | 0 | | |
| - | VCC | VCCIO | 0 | | |
| D5 | D5 | PT2B | 0 | VREF2_0 | C |
| E5 | E5 | PT2A | 0 | VREF1_0 | T |
| G7 | G7 | VCC | - | | |
| G9 | G9 | VCC | - | | |
| H7 | H7 | VCC | - | | |
| J10 | J10 | VCC | - | | |
| K10 | K10 | VCC | - | | |
| K8 | K8 | VCC | - | | |
| G8 | G8 | VCCAUX | - | | |
| H10 | H10 | VCCAUX | - | | |
| J7 | J7 | VCCAUX | - | | |
| K9 | K9 | VCCAUX | - | | |
| C5 | C5 | VCCIO0 | 0 | | |
| E7 | E7 | VCCIO0 | 0 | | |
| C12 | C12 | VCCIO1 | 1 | | |
| E10 | E10 | VCCIO1 | 1 | | |
| E14 | E14 | VCCIO2 | 2 | | |
| G12 | G12 | VCCIO2 | 2 | | |
| K12 | K12 | VCCIO3 | 3 | | |
| M14 | M14 | VCCIO3 | 3 | | |
| M10 | M10 | VCCIO4 | 4 | | |
| P12 | P12 | VCCIO4 | 4 | | |
| M7 | M7 | VCCIO5 | 5 | | |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| P5 | P5 | VCCIO5 | 5 | | |
| K5 | K5 | VCCIO6 | 6 | | |
| M3 | M3 | VCCIO6 | 6 | | |
| E3 | E3 | VCCIO7 | 7 | | |
| G5 | G5 | VCCIO7 | 7 | | |
| T15 | T15 | VCCIO8 | 8 | | |
| A1 | A1 | GND | - | | |
| A16 | A16 | GND | - | | |
| B12 | B12 | GND | - | | |
| B5 | B5 | GND | - | | |
| C8 | C8 | GND | - | | |
| E15 | E15 | GND | - | | |
| E2 | E2 | GND | - | | |
| H14 | H14 | GND | - | | |
| H8 | H8 | GND | - | | |
| H9 | H9 | GND | - | | |
| J3 | J3 | GND | - | | |
| J8 | J8 | GND | - | | |
| J9 | J9 | GND | - | | |
| M15 | M15 | GND | - | | |
| M2 | M2 | GND | - | | |
| P9 | P9 | GND | - | | |
| R12 | R12 | GND | - | | |
| R5 | R5 | GND | - | | |
| T1 | T1 | GND | - | | |
| T16 | T16 | GND | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E4 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| E5 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| - | - | - | | | GNDIO7 | - | | |
| E3 | NC | - | | | PL4A | 7 | LDQ8 | T (LVDS)* |
| F4 | PL3A | 7 | | T | PL5A | 7 | LDQ8 | T |
| F3 | NC | - | | | PL4B | 7 | LDQ8 | C (LVDS)* |
| F5 | PL3B | 7 | | C | PL5B | 7 | LDQ8 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E2 | PL4A | 7 | | T (LVDS)* | PL6A | 7 | LDQ8 | T (LVDS)* |
| G6 | PL5A | 7 | | T | PL7A | 7 | LDQ8 | T |
| E1 | PL4B | 7 | | C (LVDS)* | PL6B | 7 | LDQ8 | C (LVDS)* |
| G7 | PL5B | 7 | | C | PL7B | 7 | LDQ8 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| F1 | NC | - | | | PL9A | 7 | LDQ8 | T |
| H4 | NC | - | | | PL8A | 7 | LDQS8 | T (LVDS)* |
| F2 | NC | - | | | PL9B | 7 | LDQ8 | C |
| - | - | - | | | VCCIO7 | 7 | | |
| H5 | NC | - | | | PL8B | 7 | LDQ8 | C (LVDS)* |
| G1 | NC | - | | | PL11A | 7 | LDQ8 | T |
| G3 | NC | - | | | PL10A | 7 | LDQ8 | T (LVDS)* |
| G2 | NC | - | | | PL11B | 7 | LDQ8 | C |
| - | - | - | | | GNDIO | - | | |
| G4 | NC | - | | | PL10B | 7 | LDQ8 | C (LVDS)* |
| J4 | PL7A | 7 | LDQ10 | T | PL13A | 7 | LDQ16 | T |
| H1 | PL6A | 7 | LDQ10 | | PL12A | 7 | LDQ16 | T (LVDS)* |
| J5 | PL7B | 7 | LDQ10 | C | PL13B | 7 | LDQ16 | C |
| L6 | PL9A | 7 | LDQ10 | T | PL15A | 7 | LDQ16 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J2 | PL8A | 7 | LDQ10 | T (LVDS)* | PL14A | 7 | LDQ16 | T (LVDS)* |
| L5 | PL9B | 7 | LDQ10 | C | PL15B | 7 | LDQ16 | C |
| J1 | PL8B | 7 | LDQ10 | C (LVDS)* | PL14B | 7 | LDQ16 | C (LVDS)* |
| K3 | PL10A | 7 | LDQS10 | T (LVDS)* | PL16A | 7 | LDQS16 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO | - | | |
| K4 | PL10B | 7 | LDQ10 | C (LVDS)* | PL16B | 7 | LDQ16 | C (LVDS)* |
| K2 | PL11A | 7 | LDQ10 | T | PL17A | 7 | LDQ16 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K1 | PL11B | 7 | LDQ10 | C | PL17B | 7 | LDQ16 | C |
| L4 | PL12A | 7 | LDQ10 | T (LVDS)* | PL18A | 7 | LDQ16 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO | - | | |
| L3 | PL12B | 7 | LDQ10 | C (LVDS)* | PL18B | 7 | LDQ16 | C (LVDS)* |
| L2 | PL13A | 7 | PCLKT7_0/LDQ10 | T | PL19A | 7 | PCLKT7_0/LDQ16 | T |
| L1 | PL13B | 7 | PCLKC7_0/LDQ10 | C | PL19B | 7 | PCLKC7_0/LDQ16 | C |
| M5 | PL15A | 6 | PCLKT6_0 | T (LVDS)* | PL21A | 6 | PCLKT6_0/LDQ25 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | - | - | | |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M6 | PL15B | 6 | PCLKC6_0 | C (LVDS)* | PL21B | 6 | PCLKC6_0/LDQ25 | C (LVDS)* |
| M3 | PL16A | 6 | VREF2_6 | T | PL22A | 6 | VREF2_6/LDQ25 | T |
| GNDIO | GNDIO6 | - | | | - | - | | |
| M4 | PL16B | 6 | VREF1_6 | C | PL22B | 6 | VREF1_6/LDQ25 | C |
| - | - | - | | | VCCIO6 | 6 | | |
| N1 | NC | - | | | PL24A | 6 | LDQ25 | T |
| M2 | NC | - | | | PL23A | 6 | LDQ25 | T (LVDS)* |
| N2 | NC | - | | | PL24B | 6 | LDQ25 | C |
| M1 | NC | - | | | PL23B | 6 | LDQ25 | C (LVDS)* |
| - | - | - | | | GNDIO | - | | |
| N3 | NC | - | | | PL25A | 6 | LDQS25 | T (LVDS)* |
| N5 | NC | - | | | PL26A | 6 | LDQ25 | T |
| N4 | NC | - | | | PL25B | 6 | LDQ25 | C (LVDS)* |
| - | - | - | | | VCCIO6 | 6 | | |
| P5 | NC | - | | | PL26B | 6 | LDQ25 | C |
| P1 | PL17A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* | PL27A | 6 | LLM0_GDLLT_IN_A**/LDQ25 | T (LVDS)* |
| P2 | PL17B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* | PL27B | 6 | LLM0_GDLLC_IN_A**/LDQ25 | C (LVDS)* |
| P4 | PL18A | 6 | LLM0_GDLLT_FB_A | T | PL28A | 6 | LLM0_GDLLT_FB_A/LDQ25 | T |
| - | - | - | | | GNDIO | - | | |
| R4 | PL18B | 6 | LLM0_GDLLC_FB_A | C | PL28B | 6 | LLM0_GDLLC_FB_A/LDQ25 | C |
| P6 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| R1 | PL20A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* | PL30A | 6 | LLM0_GPLLT_IN_A**/LDQ34 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | - | - | | |
| R3 | PL21A | 6 | LLM0_GPLLT_FB_A | T | PL31A | 6 | LLM0_GPLLT_FB_A/LDQ34 | T |
| R2 | PL20B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* | PL30B | 6 | LLM0_GPLLC_IN_A/LDQ34 | C (LVDS)* |
| T4 | PL21B | 6 | LLM0_GPLLC_FB_A | C | PL31B | 6 | LLM0_GPLLC_FB_A/LDQ34 | C |
| T5 | PL23A | 6 | | T | PL33A | 6 | LDQ34 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T1 | PL22A | 6 | | T (LVDS)* | PL32A | 6 | LDQ34 | T (LVDS)* |
| T3 | PL23B | 6 | | C | PL33B | 6 | LDQ34 | C |
| T2 | PL22B | 6 | | C (LVDS)* | PL32B | 6 | LDQ34 | C (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| - | - | - | | | VCCIO6 | 6 | | |
| V1 | PL25A | 6 | LDQ28 | T | PL39A | 6 | LDQ42 | T |
| - | - | - | | | GNDIO | - | | |
| V2 | PL25B | 6 | LDQ28 | C | PL39B | 6 | LDQ42 | C |
| U1 | PL24A | 6 | LDQ28 | T (LVDS)* | PL38A | 6 | LDQ42 | T (LVDS)* |
| U3 | PL27A | 6 | LDQ28 | T | PL41A | 6 | LDQ42 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U2 | PL24B | 6 | LDQ28 | C (LVDS)* | PL38B | 6 | LDQ42 | C (LVDS)* |
| U4 | PL27B | 6 | LDQ28 | C | PL41B | 6 | LDQ42 | C |
| R6 | PL26A | 6 | LDQ28 | T (LVDS)* | PL40A | 6 | LDQ42 | T (LVDS)* |
| R7 | PL29A | 6 | LDQ28 | T | PL43A | 6 | LDQ42 | T |
| GNDIO | GNDIO6 | - | | | GNDIO | - | | |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T7 | PL29B | 6 | LDQ28 | C | PL43B | 6 | LDQ42 | C |
| T6 | PL26B | 6 | LDQ28 | C (LVDS)* | PL40B | 6 | LDQ42 | C (LVDS)* |
| AA2 | PL31A | 6 | LDQ28 | T | PL45A | 6 | LDQ42 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y1 | PL28A | 6 | LDQS28 | T (LVDS)* | PL42A | 6 | LDQS42 | T (LVDS)* |
| AA1 | PL31B | 6 | LDQ28 | C | PL45B | 6 | LDQ42 | C |
| W1 | PL28B | 6 | LDQ28 | C (LVDS)* | PL42B | 6 | LDQ42 | C (LVDS)* |
| V3 | PL30B | 6 | LDQ28 | C (LVDS)* | PL44B | 6 | LDQ42 | C (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO | - | | |
| V4 | PL30A | 6 | LDQ28 | T (LVDS)* | PL44A | 6 | LDQ42 | T (LVDS)* |
| U5 | TDI | - | | | TDI | - | | |
| U7 | TCK | - | | | TCK | - | | |
| V6 | TDO | - | | | TDO | - | | |
| V5 | TMS | - | | | TMS | - | | |
| T8 | VCCJ | - | | | VCCJ | - | | |
| W4 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| Y3 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| W3 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| Y2 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| AB3 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| W5 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| AB2 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| W6 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| AB5 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| Y4 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| AB4 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA3 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AB6 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA5 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| AA6 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| Y5 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| - | - | - | | | VCCIO5 | 5 | | |
| Y6 | PB12A | 5 | BDQ15 | T | PB21A | 5 | BDQ24 | T |
| W7 | PB11A | 5 | BDQ15 | T | PB20A | 5 | BDQ24 | T |
| Y7 | PB12B | 5 | BDQ15 | C | PB21B | 5 | BDQ24 | C |
| W8 | PB11B | 5 | BDQ15 | C | PB20B | 5 | BDQ24 | C |
| U8 | PB14A | 5 | BDQ15 | T | PB23A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA7 | PB13A | 5 | BDQ15 | T | PB22A | 5 | BDQ24 | T |
| U9 | PB14B | 5 | BDQ15 | C | PB23B | 5 | BDQ24 | C |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AB7 | PB13B | 5 | BDQ15 | C | PB22B | 5 | BDQ24 | C |
| Y8 | PB16A | 5 | BDQ15 | T | PB25A | 5 | BDQ24 | T |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| W9 | PB15A | 5 | BDQS15 | T | PB24A | 5 | BDQS24 | T |
| AA8 | PB16B | 5 | BDQ15 | C | PB25B | 5 | BDQ24 | C |
| V9 | PB15B | 5 | BDQ15 | C | PB24B | 5 | BDQ24 | C |
| AB8 | PB18A | 5 | BDQ15 | T | PB27A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| W10 | PB17A | 5 | BDQ15 | T | PB26A | 5 | BDQ24 | T |
| AA9 | PB18B | 5 | BDQ15 | C | PB27B | 5 | BDQ24 | C |
| V10 | PB17B | 5 | BDQ15 | C | PB26B | 5 | BDQ24 | C |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| Y10 | PB21A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| AB9 | PB20A | 5 | BDQ24 | T | PB29A | 5 | BDQ33 | T |
| AA10 | PB21B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| AB10 | PB20B | 5 | BDQ24 | C | PB29B | 5 | BDQ33 | C |
| AB11 | PB23A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| U10 | PB22A | 5 | BDQ24 | T | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA11 | PB23B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| U11 | PB22B | 5 | BDQ24 | C | PB31B | 5 | BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AB12 | PB25A | 5 | BDQ24 | T | PB34A | 5 | BDQ33 | T |
| Y11 | PB24A | 5 | BDQS24 | T | PB33A | 5 | BDQS33 | T |
| AA12 | PB25B | 5 | BDQ24 | C | PB34B | 5 | BDQ33 | C |
| W11 | PB24B | 5 | BDQ24 | C | PB33B | 5 | BDQ33 | C |
| AB13 | PB26A | 5 | PCLKT5_0/BDQ24 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AB14 | PB26B | 5 | PCLKC5_0/BDQ24 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| Y12 | PB32A | 4 | BDQ33 | T | PB41A | 4 | BDQ42 | T |
| W12 | PB32B | 4 | BDQ33 | C | PB41B | 4 | BDQ42 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U12 | PB31A | 4 | PCLKT4_0/BDQ33 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| V12 | PB31B | 4 | PCLKC4_0/BDQ33 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| U13 | PB34A | 4 | BDQ33 | T | PB43A | 4 | BDQ42 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA13 | PB33A | 4 | BDQS33 | T | PB42A | 4 | BDQS42 | T |
| U14 | PB34B | 4 | BDQ33 | C | PB43B | 4 | BDQ42 | C |
| Y13 | PB33B | 4 | BDQ33 | C | PB42B | 4 | BDQ42 | C |
| AB16 | PB36A | 4 | BDQ33 | T | PB45A | 4 | BDQ42 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AB15 | PB35A | 4 | BDQ33 | T | PB44A | 4 | BDQ42 | T |
| AB17 | PB36B | 4 | BDQ33 | C | PB45B | 4 | BDQ42 | C |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA14 | PB35B | 4 | BDQ33 | C | PB44B | 4 | BDQ42 | C |
| W13 | PB37A | 4 | BDQ33 | T | PB46A | 4 | BDQ42 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W14 | PB37B | 4 | BDQ33 | C | PB46B | 4 | BDQ42 | C |
| AB18 | PB39A | 4 | BDQ42 | T | PB48A | 4 | BDQ51 | T |
| AB19 | PB39B | 4 | BDQ42 | C | PB48B | 4 | BDQ51 | C |
| Y15 | PB41A | 4 | BDQ42 | T | PB50A | 4 | BDQ51 | T |
| V14 | PB40A | 4 | BDQ42 | T | PB49A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA15 | PB41B | 4 | BDQ42 | C | PB50B | 4 | BDQ51 | C |
| W15 | PB40B | 4 | BDQ42 | C | PB49B | 4 | BDQ51 | C |
| GNDIO | GNDIO4 | - | | | GNDIO | - | | |
| AB20 | PB43A | 4 | BDQ42 | T | PB52A | 4 | BDQ51 | T |
| AA16 | PB42A | 4 | BDQS42 | T | PB51A | 4 | BDQS51 | T |
| AB21 | PB43B | 4 | BDQ42 | C | PB52B | 4 | BDQ51 | C |
| AA17 | PB42B | 4 | BDQ42 | C | PB51B | 4 | BDQ51 | C |
| Y16 | PB45A | 4 | BDQ42 | T | PB54A | 4 | BDQ51 | T |
| U15 | PB44A | 4 | BDQ42 | T | PB53A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W16 | PB45B | 4 | BDQ42 | C | PB54B | 4 | BDQ51 | C |
| U16 | PB44B | 4 | BDQ42 | C | PB53B | 4 | BDQ51 | C |
| AA18 | PB46A | 4 | BDQ42 | T | PB55A | 4 | BDQ51 | T |
| AA20 | PB46B | 4 | BDQ42 | C | PB55B | 4 | BDQ51 | C |
| GNDIO | GNDIO4 | - | | | GNDIO | - | | |
| V16 | PB49A | 4 | BDQ51 | T | PB58A | 4 | BDQ60 | T |
| V17 | PB49B | 4 | BDQ51 | C | PB58B | 4 | BDQ60 | C |
| AA21 | PB48A | 4 | BDQ51 | T | PB57A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y19 | PB51A | 4 | BDQS51 | T | PB60A | 4 | BDQS60 | T |
| AA22 | PB48B | 4 | BDQ51 | C | PB57B | 4 | BDQ60 | C |
| Y20 | PB51B | 4 | BDQ51 | C | PB60B | 4 | BDQ60 | C |
| Y18 | PB50A | 4 | BDQ51 | T | PB59A | 4 | BDQ60 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| Y21 | PB53A | 4 | BDQ51 | T | PB62A | 4 | BDQ60 | T |
| Y17 | PB50B | 4 | BDQ51 | C | PB59B | 4 | BDQ60 | C |
| Y22 | PB53B | 4 | BDQ51 | C | PB62B | 4 | BDQ60 | C |
| W17 | PB52A | 4 | BDQ51 | T | PB61A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U18 | PB54A | 4 | BDQ51 | T | PB63A | 4 | BDQ60 | T |
| W18 | PB52B | 4 | BDQ51 | C | PB61B | 4 | BDQ60 | C |
| V18 | PB54B | 4 | BDQ51 | C | PB63B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| T15 | PB55A | 4 | VREF2_4/BDQ51 | T | PB64A | 4 | VREF2_4/BDQ60 | T |
| T16 | PB55B | 4 | VREF1_4/BDQ51 | C | PB64B | 4 | VREF1_4/BDQ60 | C |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W19 | CFG2 | 8 | | | CFG2 | 8 | | |
| V19 | CFG1 | 8 | | | CFG1 | 8 | | |
| V20 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| W20 | CFG0 | 8 | | | CFG0 | 8 | | |
| U22 | PR28B | 8 | D1 | C | PR42B | 8 | D1 | C |
| V22 | INITN | 8 | | | INITN | 8 | | |
| R16 | PR30B | 8 | WRITEN | C | PR44B | 8 | WRITEN | C |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| W22 | CCLK | 8 | | | CCLK | 8 | | |
| R17 | PR30A | 8 | CS1N | T | PR44A | 8 | CS1N | T |
| V21 | DONE | 8 | | | DONE | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| U19 | PR29B | 8 | CSN | C | PR43B | 8 | CSN | C |
| T17 | PR26B | 8 | D5 | C | PR40B | 8 | D5 | C |
| U20 | PR29A | 8 | D0/SPIFASTN | T | PR43A | 8 | D0/SPIFASTN | T |
| U21 | PR28A | 8 | D2 | T | PR42A | 8 | D2 | T |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| T18 | PR26A | 8 | D6 | T | PR40A | 8 | D6 | T |
| T20 | PR27B | 8 | D3 | C | PR41B | 8 | D3 | C |
| T21 | PR25B | 8 | D7/SPID0 | C | PR39B | 8 | D7/SPID0 | C |
| T19 | PR27A | 8 | D4 | T | PR41A | 8 | D4 | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| T22 | PR25A | 8 | DI/CSSPI0N | T | PR39A | 8 | DI/CSSPI0N | T |
| R18 | PR24B | 8 | DOUT/CSON | C | PR38B | 8 | DOUT/CSON | C |
| R19 | PR24A | 8 | BUSY/SISPI | T | PR38A | 8 | BUSY/SISPI | T |
| - | - | - | | | VCCIO3 | 3 | | |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| P18 | PR22B | 3 | | C (LVDS)* | PR32B | 3 | RDQ34 | C (LVDS)* |
| R22 | PR23B | 3 | | C | PR33B | 3 | RDQ34 | C |
| P19 | PR22A | 3 | | T (LVDS)* | PR32A | 3 | RDQ34 | T (LVDS)* |
| R21 | PR23A | 3 | | T | PR33A | 3 | RDQ34 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R20 | PR21B | 3 | RLM0_GPLLC_FB_A | C | PR31B | 3 | RLM0_GPLLC_FB_A/RDQ34 | C |
| P22 | PR21A | 3 | RLM0_GPLLT_FB_A | T | PR31A | 3 | RLM0_GPLLT_FB_A/RDQ34 | T |
| P21 | PR20B | 3 | RLM0_GPLLC_IN_A** | C (LVDS)* | PR30B | 3 | RLM0_GPLLC_IN_A**/RDQ34 | C (LVDS)* |
| N21 | PR20A | 3 | RLM0_GPLLT_IN_A** | T (LVDS)* | PR30A | 3 | RLM0_GPLLT_IN_A**/RDQ34 | T (LVDS)* |
| N17 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| N22 | PR18B | 3 | RLM0_GDLLC_FB_A | C | PR28B | 3 | RLM0_GDLLC_FB_A/RDQ25 | C |
| M22 | PR17B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR27B | 3 | RLM0_GDLLC_IN_A**/RDQ25 | C (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| N20 | PR18A | 3 | RLM0_GDLLT_FB_A | T | PR28A | 3 | RLM0_GDLLT_FB_A/RDQ25 | T |
| M21 | PR17A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR27A | 3 | RLM0_GDLLT_IN_A**/RDQ25 | T (LVDS)* |
| N19 | NC | - | | | PR26B | 3 | RDQ25 | C |
| - | - | - | | | VCCIO3 | 3 | | |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M19 | NC | - | | | PR26A | 3 | RDQ25 | T |
| J22 | NC | - | | | PR23B | 3 | RDQ25 | C (LVDS)* |
| - | - | - | | | GNDIO | - | | |
| L22 | NC | - | | | PR24B | 3 | RDQ25 | C |
| H22 | NC | - | | | PR23A | 3 | RDQ25 | T (LVDS)* |
| K22 | NC | - | | | PR24A | 3 | RDQ25 | T |
| M20 | PR16B | 3 | VREF2_3 | C | PR22B | 3 | VREF2_3/RDQ25 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| L21 | PR16A | 3 | VREF1_3 | T | PR22A | 3 | VREF1_3/RDQ25 | T |
| K21 | PR15B | 3 | PCLKC3_0 | C (LVDS)* | PR21B | 3 | PCLKC3_0/RDQ25 | C (LVDS)* |
| J21 | PR15A | 3 | PCLKT3_0 | T (LVDS)* | PR21A | 3 | PCLKT3_0/RDQ25 | T (LVDS)* |
| M18 | PR13B | 2 | PCLKC2_0/RDQ10 | C | PR19B | 2 | PCLKC2_0/RDQ16 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| L17 | PR13A | 2 | PCLKT2_0/RDQ10 | T | PR19A | 2 | PCLKT2_0/RDQ16 | T |
| L19 | PR12B | 2 | RDQ10 | C (LVDS)* | PR18B | 2 | RDQ16 | C (LVDS)* |
| K18 | PR10B | 2 | RDQ10 | C (LVDS)* | PR16B | 2 | RDQ16 | C (LVDS)* |
| L20 | PR12A | 2 | RDQ10 | T (LVDS)* | PR18A | 2 | RDQ16 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K19 | PR10A | 2 | RDQS10 | T (LVDS)* | PR16A | 2 | RDQS16 | T (LVDS)* |
| L18 | PR11B | 2 | RDQ10 | C | PR17B | 2 | RDQ16 | C |
| K17 | PR11A | 2 | RDQ10 | T | PR17A | 2 | RDQ16 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| J17 | PR8B | 2 | RDQ10 | C (LVDS)* | PR14B | 2 | RDQ16 | C (LVDS)* |
| G22 | PR9B | 2 | RDQ10 | C | PR15B | 2 | RDQ16 | C |
| J18 | PR8A | 2 | RDQ10 | T (LVDS)* | PR14A | 2 | RDQ16 | T (LVDS)* |
| F22 | PR9A | 2 | RDQ10 | T | PR15A | 2 | RDQ16 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H21 | PR6B | 2 | RDQ10 | C (LVDS)* | PR12B | 2 | RDQ16 | C (LVDS)* |
| K20 | PR7B | 2 | RDQ10 | C | PR13B | 2 | RDQ16 | C |
| G21 | PR6A | 2 | RDQ10 | T (LVDS)* | PR12A | 2 | RDQ16 | T (LVDS)* |
| J19 | PR7A | 2 | RDQ10 | T | PR13A | 2 | RDQ16 | T |
| D22 | NC | - | | | PR10B | 2 | RDQ8 | C (LVDS)* |
| F21 | NC | - | | | PR11B | 2 | RDQ8 | C |
| - | - | - | | | GNDIO | - | | |
| E21 | NC | - | | | PR10A | 2 | RDQ8 | T (LVDS)* |
| E22 | NC | - | | | PR11A | 2 | RDQ8 | T |
| H19 | NC | - | | | PR8B | 2 | RDQ8 | C (LVDS)* |
| G20 | NC | - | | | PR9B | 2 | RDQ8 | C |
| - | - | - | | | VCCIO2 | 2 | | |
| G19 | NC | - | | | PR8A | 2 | RDQS8 | T (LVDS)* |
| F20 | NC | - | | | PR9A | 2 | RDQ8 | T |
| G17 | PR5B | 2 | | C | PR7B | 2 | RDQ8 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| E20 | PR4B | 2 | | C (LVDS)* | PR6B | 2 | RDQ8 | C (LVDS)* |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F19 | PR5A | 2 | | T | PR7A | 2 | RDQ8 | T |
| D20 | PR4A | 2 | | T (LVDS)* | PR6A | 2 | RDQ8 | T (LVDS)* |
| F18 | PR3B | 2 | | C | PR5B | 2 | RDQ8 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| C21 | NC | - | | | PR4B | 2 | RDQ8 | C (LVDS)* |
| F16 | PR3A | 2 | | T | PR5A | 2 | RDQ8 | T |
| C22 | NC | - | | | PR4A | 2 | RDQ8 | T (LVDS)* |
| - | - | - | | | GNDIO | - | | |
| D19 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| E19 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| B21 | PT55B | 1 | VREF2_1 | C | PT64B | 1 | VREF2_1 | C |
| B22 | PT55A | 1 | VREF1_1 | T | PT64A | 1 | VREF1_1 | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| D18 | PT53B | 1 | | C | PT62B | 1 | | C |
| C20 | PT54B | 1 | | C | PT63B | 1 | | C |
| E18 | PT53A | 1 | | T | PT62A | 1 | | T |
| C19 | PT54A | 1 | | T | PT63A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D17 | PT51B | 1 | | C | PT60B | 1 | | C |
| B20 | PT52B | 1 | | C | PT61B | 1 | | C |
| C18 | PT51A | 1 | | T | PT60A | 1 | | T |
| A19 | PT52A | 1 | | T | PT61A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A18 | PT49B | 1 | | C | PT58B | 1 | | C |
| A21 | PT50B | 1 | | C | PT59B | 1 | | C |
| B18 | PT49A | 1 | | T | PT58A | 1 | | T |
| A20 | PT50A | 1 | | T | PT59A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D16 | PT47B | 1 | | C | PT56B | 1 | | C |
| G16 | PT48B | 1 | | C | PT57B | 1 | | C |
| E16 | PT47A | 1 | | T | PT56A | 1 | | T |
| G15 | PT48A | 1 | | T | PT57A | 1 | | T |
| C17 | PT46B | 1 | | C | PT55B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| C16 | PT46A | 1 | | T | PT55A | 1 | | T |
| A17 | PT44B | 1 | | C | PT53B | 1 | | C |
| B17 | PT45B | 1 | | C | PT54B | 1 | | C |
| A16 | PT44A | 1 | | T | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B16 | PT45A | 1 | | T | PT54A | 1 | | T |
| E15 | PT42B | 1 | | C | PT51B | 1 | | C |
| C15 | PT43B | 1 | | C | PT52B | 1 | | C |
| F15 | PT42A | 1 | | T | PT51A | 1 | | T |
| D15 | PT43A | 1 | | T | PT52A | 1 | | T |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| B15 | PT40B | 1 | | C | PT49B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A15 | PT40A | 1 | | T | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A14 | PT39A | 1 | | T | PT48A | 1 | | T |
| B14 | PT39B | 1 | | C | PT48B | 1 | | C |
| D14 | PT37B | 1 | | C | PT46B | 1 | | C |
| E14 | PT36B | 1 | | C | PT45B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| C13 | PT37A | 1 | | T | PT46A | 1 | | T |
| F14 | PT36A | 1 | | T | PT45A | 1 | | T |
| A13 | PT35B | 1 | | C | PT44B | 1 | | C |
| E13 | PT34B | 1 | | C | PT43B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B13 | PT35A | 1 | | T | PT44A | 1 | | T |
| D13 | PT34A | 1 | | T | PT43A | 1 | | T |
| E12 | PT33B | 1 | | C | PT42B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| D12 | PT33A | 1 | | T | PT42A | 1 | | T |
| A12 | PT31B | 1 | | C | PT40B | 1 | | C |
| B12 | PT30B | 1 | PCLKC1_0 | C | PT39B | 1 | PCLKC1_0 | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A11 | PT31A | 1 | | T | PT40A | 1 | | T |
| C12 | PT30A | 1 | PCLKT1_0 | T | PT39A | 1 | PCLKT1_0 | T |
| F12 | XRES | 1 | | | XRES | 1 | | |
| B10 | PT28B | 0 | PCLKC0_0 | C | PT37B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| B11 | PT28A | 0 | PCLKT0_0 | T | PT37A | 0 | PCLKT0_0 | T |
| C11 | PT26B | 0 | | C | PT35B | 0 | | C |
| A10 | PT27B | 0 | | C | PT36B | 0 | | C |
| C10 | PT26A | 0 | | T | PT35A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| A9 | PT27A | 0 | | T | PT36A | 0 | | T |
| A8 | PT24B | 0 | | C | PT33B | 0 | | C |
| E11 | PT25B | 0 | | C | PT34B | 0 | | C |
| A7 | PT24A | 0 | | T | PT33A | 0 | | T |
| F11 | PT25A | 0 | | T | PT34A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| B8 | PT23B | 0 | | C | PT32B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B9 | PT23A | 0 | | T | PT32A | 0 | | T |
| C8 | PT20B | 0 | | C | PT29B | 0 | | C |
| B7 | PT21B | 0 | | C | PT30B | 0 | | C |
| D8 | PT20A | 0 | | T | PT29A | 0 | | T |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A6 | PT21A | 0 | | T | PT30A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| C7 | PT17B | 0 | | C | PT26B | 0 | | C |
| D10 | PT18B | 0 | | C | PT27B | 0 | | C |
| C6 | PT17A | 0 | | T | PT26A | 0 | | T |
| E10 | PT18A | 0 | | T | PT27A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F10 | PT15B | 0 | | C | PT24B | 0 | | C |
| B6 | PT16B | 0 | | C | PT25B | 0 | | C |
| D9 | PT15A | 0 | | T | PT24A | 0 | | T |
| B5 | PT16A | 0 | | T | PT25A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| A5 | PT13B | 0 | | C | PT22B | 0 | | C |
| F9 | PT14B | 0 | | C | PT23B | 0 | | C |
| A4 | PT13A | 0 | | T | PT22A | 0 | | T |
| E9 | PT14A | 0 | | T | PT23A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G8 | PT11B | 0 | | C | PT20B | 0 | | C |
| A3 | PT12B | 0 | | C | PT21B | 0 | | C |
| E8 | PT11A | 0 | | T | PT20A | 0 | | T |
| A2 | PT12A | 0 | | T | PT21A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| - | - | - | | | VCCIO0 | 0 | | |
| C3 | PT10B | 0 | | C | PT10B | 0 | | C |
| B3 | PT10A | 0 | | T | PT10A | 0 | | T |
| - | - | - | | | GNDIO0 | - | | |
| E7 | PT8B | 0 | | C | PT8B | 0 | | C |
| F8 | PT9B | 0 | | C | PT9B | 0 | | C |
| F7 | PT8A | 0 | | T | PT8A | 0 | | T |
| D7 | PT9A | 0 | | T | PT9A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D4 | PT6B | 0 | | C | PT6B | 0 | | C |
| D5 | PT7B | 0 | | C | PT7B | 0 | | C |
| C4 | PT6A | 0 | | T | PT6A | 0 | | T |
| D6 | PT7A | 0 | | T | PT7A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO | - | | |
| J7 | PT4B | 0 | | C | PT4B | 0 | | C |
| B2 | PT5B | 0 | | C | PT5B | 0 | | C |
| H7 | PT4A | 0 | | T | PT4A | 0 | | T |
| B1 | PT5A | 0 | | T | PT5A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D1 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| D3 | PT3B | 0 | | C | PT3B | 0 | | C |
| C1 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C2 | PT3A | 0 | | T | PT3A | 0 | | T |
| J10 | VCC | - | | | VCC | - | | |
| J11 | VCC | - | | | VCC | - | | |
| J12 | VCC | - | | | VCC | - | | |
| J13 | VCC | - | | | VCC | - | | |
| K14 | VCC | - | | | VCC | - | | |
| K9 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L9 | VCC | - | | | VCC | - | | |
| M14 | VCC | - | | | VCC | - | | |
| M9 | VCC | - | | | VCC | - | | |
| N14 | VCC | - | | | VCC | - | | |
| N9 | VCC | - | | | VCC | - | | |
| P10 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P12 | VCC | - | | | VCC | - | | |
| P13 | VCC | - | | | VCC | - | | |
| G10 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H8 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G11 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G12 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G13 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H14 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K16 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| N16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| P16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T12 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T13 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| R9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T10 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| N7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| R8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| J8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| P15 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| R15 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| C5 | VCCAUX | - | | | VCCAUX | - | | |
| D11 | VCCAUX | - | | | VCCAUX | - | | |
| E17 | VCCAUX | - | | | VCCAUX | - | | |
| E6 | VCCAUX | - | | | VCCAUX | - | | |
| F13 | VCCAUX | - | | | VCCAUX | - | | |
| G18 | VCCAUX | - | | | VCCAUX | - | | |
| G5 | VCCAUX | - | | | VCCAUX | - | | |
| K5 | VCCAUX | - | | | VCCAUX | - | | |
| M17 | VCCAUX | - | | | VCCAUX | - | | |
| P17 | VCCAUX | - | | | VCCAUX | - | | |
| R5 | VCCAUX | - | | | VCCAUX | - | | |
| V11 | VCCAUX | - | | | VCCAUX | - | | |
| V13 | VCCAUX | - | | | VCCAUX | - | | |
| V15 | VCCAUX | - | | | VCCAUX | - | | |
| V7 | VCCAUX | - | | | VCCAUX | - | | |
| V8 | VCCAUX | - | | | VCCAUX | - | | |
| A1 | GND | - | | | GND | - | | |
| A22 | GND | - | | | GND | - | | |
| AA19 | GND | - | | | GND | - | | |
| AA4 | GND | - | | | GND | - | | |
| AB1 | GND | - | | | GND | - | | |
| AB22 | GND | - | | | GND | - | | |
| B19 | GND | - | | | GND | - | | |
| B4 | GND | - | | | GND | - | | |
| C14 | GND | - | | | GND | - | | |
| C9 | GND | - | | | GND | - | | |
| D2 | GND | - | | | GND | - | | |
| D21 | GND | - | | | GND | - | | |
| F17 | GND | - | | | GND | - | | |
| F6 | GND | - | | | GND | - | | |
| H10 | GND | - | | | GND | - | | |
| H11 | GND | - | | | GND | - | | |
| H12 | GND | - | | | GND | - | | |
| H13 | GND | - | | | GND | - | | |
| J14 | GND | - | | | GND | - | | |
| J20 | GND | - | | | GND | - | | |
| J3 | GND | - | | | GND | - | | |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J9 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K12 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K15 | GND | - | | | GND | - | | |
| K8 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |
| L12 | GND | - | | | GND | - | | |
| L13 | GND | - | | | GND | - | | |
| L15 | GND | - | | | GND | - | | |
| L8 | GND | - | | | GND | - | | |
| M10 | GND | - | | | GND | - | | |
| M11 | GND | - | | | GND | - | | |
| M12 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M15 | GND | - | | | GND | - | | |
| M8 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N11 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N8 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P20 | GND | - | | | GND | - | | |
| P3 | GND | - | | | GND | - | | |
| P9 | GND | - | | | GND | - | | |
| R10 | GND | - | | | GND | - | | |
| R11 | GND | - | | | GND | - | | |
| R12 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| U6 | GND | - | | | GND | - | | |
| W2 | GND | - | | | GND | - | | |
| W21 | GND | - | | | GND | - | | |
| Y14 | GND | - | | | GND | - | | |
| Y9 | GND | - | | | GND | - | | |
| H6 | NC | - | | | NC | - | | |
| J6 | NC | - | | | NC | - | | |
| H3 | NC | - | | | NC | - | | |
| H2 | NC | - | | | NC | - | | |
| H17 | NC | - | | | NC | - | | |

## LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| H16 | NC | - | | | NC | - | | |
| H20 | NC | - | | | NC | - | | |
| H18 | NC | - | | | NC | - | | |
| K6 | NC | - | | | NC | - | | |
| J16 | NC | - | | | NC | - | | |
| N18 | VCC | - | | | VCC | - | | |
| N6 | VCC | - | | | VCC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E4 | PL2A | 7 | VREF2_7/LDQ6 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| E5 | PL2B | 7 | VREF1_7/LDQ6 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| VCCIO | VCCIO7 | - | | | GNDIO7 | - | | |
| GNDIO | GNDIO7 | - | | | VCCIO | 7 | | |
| E3 | PL10A | 7 | LDQ14 | T (LVDS)* | PL12A | 7 | LDQ16 | T (LVDS)* |
| F3 | PL10B | 7 | LDQ14 | C (LVDS)* | PL12B | 7 | LDQ16 | C (LVDS)* |
| F4 | PL11A | 7 | LDQ14 | T | PL13A | 7 | LDQ16 | T |
| F5 | PL11B | 7 | LDQ14 | C | PL13B | 7 | LDQ16 | C |
| E2 | PL12A | 7 | LDQ14 | T (LVDS)* | PL14A | 7 | LDQ16 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |
| E1 | PL12B | 7 | LDQ14 | C (LVDS)* | PL14B | 7 | LDQ16 | C (LVDS)* |
| G6 | PL13A | 7 | LDQ14 | T | PL15A | 7 | LDQ16 | T |
| G7 | PL13B | 7 | LDQ14 | C | PL15B | 7 | LDQ16 | C |
| H4 | PL14A | 7 | LDQS14 | T (LVDS)* | PL16A | 7 | LDQS16 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| H5 | PL14B | 7 | LDQ14 | C (LVDS)* | PL16B | 7 | LDQ16 | C (LVDS)* |
| F1 | PL15A | 7 | LDQ14 | T | PL17A | 7 | LDQ16 | T |
| F2 | PL15B | 7 | LDQ14 | C | PL17B | 7 | LDQ16 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |
| G3 | PL16A | 7 | LDQ14 | T (LVDS)* | PL18A | 7 | LDQ16 | T (LVDS)* |
| G4 | PL16B | 7 | LDQ14 | C (LVDS)* | PL18B | 7 | LDQ16 | C (LVDS)* |
| G1 | PL17A | 7 | LDQ14 | T | PL19A | 7 | LDQ16 | T |
| G2 | PL17B | 7 | LDQ14 | C | PL19B | 7 | LDQ16 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| - | - | - | | | VCCIO | 7 | | |
| H6 | NC | - | | | PL25A | 7 | LUM0_SPLLT_IN_A/LDQ24 | T |
| - | - | - | | | VCCIO | 7 | | |
| J6 | NC | - | | | PL25B | 7 | LUM0_SPLLC_IN_A/LDQ24 | C |
| H3 | NC | - | | | PL26A | 7 | LUM0_SPLLT_FB_A/LDQ24 | T |
| H2 | NC | - | | | PL26B | 7 | LUM0_SPLLC_FB_A/LDQ24 | C |
| - | - | - | | | GNDIO7 | - | | |
| - | - | - | | | VCCIO | 7 | | |
| H1 | PL18A | 7 | LDQ22 | | PL37A | 7 | LDQ41 | |
| J4 | PL19A | 7 | LDQ22 | T | PL38A | 7 | LDQ41 | T |
| J5 | PL19B | 7 | LDQ22 | C | PL38B | 7 | LDQ41 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |
| J2 | PL20A | 7 | LDQ22 | T (LVDS)* | PL39A | 7 | LDQ41 | T (LVDS)* |
| J1 | PL20B | 7 | LDQ22 | C (LVDS)* | PL39B | 7 | LDQ41 | C (LVDS)* |
| L6 | PL21A | 7 | LDQ22 | T | PL40A | 7 | LDQ41 | T |
| L5 | PL21B | 7 | LDQ22 | C | PL40B | 7 | LDQ41 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| K3 | PL22A | 7 | LDQS22 | T (LVDS)* | PL41A | 7 | LDQS41 | T (LVDS)* |
| K4 | PL22B | 7 | LDQ22 | C (LVDS)* | PL41B | 7 | LDQ41 | C (LVDS)* |
| K2 | PL23A | 7 | LDQ22 | T | PL42A | 7 | LDQ41 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K1 | PL23B | 7 | LDQ22 | C | PL42B | 7 | LDQ41 | C |
| L4 | PL24A | 7 | LDQ22 | T (LVDS)* | PL43A | 7 | LDQ41 | T (LVDS)* |
| L3 | PL24B | 7 | LDQ22 | C (LVDS)* | PL43B | 7 | LDQ41 | C (LVDS)* |
| L2 | PL25A | 7 | PCLKT7_0/LDQ22 | T | PL44A | 7 | PCLKT7_0/LDQ41 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| L1 | PL25B | 7 | PCLKC7_0/LDQ22 | C | PL44B | 7 | PCLKC7_0/LDQ41 | C |
| M5 | PL27A | 6 | PCLKT6_0/LDQ31 | T (LVDS)* | PL46A | 6 | PCLKT6_0/LDQ50 | T (LVDS)* |
| M6 | PL27B | 6 | PCLKC6_0/LDQ31 | C (LVDS)* | PL46B | 6 | PCLKC6_0/LDQ50 | C (LVDS)* |
| M3 | PL28A | 6 | VREF2_6/LDQ31 | T | PL47A | 6 | VREF2_6/LDQ50 | T |
| M4 | PL28B | 6 | VREF1_6/LDQ31 | C | PL47B | 6 | VREF1_6/LDQ50 | C |
| M2 | PL29A | 6 | LDQ31 | T (LVDS)* | PL48A | 6 | LDQ50 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO | 6 | | |
| M1 | PL29B | 6 | LDQ31 | C (LVDS)* | PL48B | 6 | LDQ50 | C (LVDS)* |
| N1 | PL30A | 6 | LDQ31 | T | PL49A | 6 | LDQ50 | T |
| N2 | PL30B | 6 | LDQ31 | C | PL49B | 6 | LDQ50 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| VCCIO | VCCIO6 | 6 | | | VCCIO | 6 | | |
| N3 | PL39A | 6 | LDQS39*** | T (LVDS)* | PL58A | 6 | LDQS58*** | T (LVDS)* |
| N4 | PL39B | 6 | LDQ39 | C (LVDS)* | PL58B | 6 | LDQ58 | C (LVDS)* |
| N5 | PL40A | 6 | LDQ39 | T | PL59A | 6 | LDQ58 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO | 6 | | |
| P5 | PL40B | 6 | LDQ39 | C | PL59B | 6 | LDQ58 | C |
| P1 | PL41A | 6 | LLM0_GDLLT_IN_A**/LDQ39 | T (LVDS)* | PL60A | 6 | LLM0_GDLLT_IN_A**/LDQ58 | T (LVDS)* |
| P2 | PL41B | 6 | LLM0_GDLLC_IN_A**/LDQ39 | C (LVDS)* | PL60B | 6 | LLM0_GDLLC_IN_A**/LDQ58 | C (LVDS)* |
| P4 | PL42A | 6 | LLM0_GDLLT_FB_A/LDQ39 | T | PL61A | 6 | LLM0_GDLLT_FB_A/LDQ58 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| R4 | PL42B | 6 | LLM0_GDLLC_FB_A/LDQ39 | C | PL61B | 6 | LLM0_GDLLC_FB_D/LDQ58 | C |
| P6 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| R1 | PL44A | 6 | LLM0_GPLLT_IN_A**/LDQ48 | T (LVDS)* | PL63A | 6 | LLM0_GPLLT_IN_A**/LDQ67 | T (LVDS)* |
| R2 | PL44B | 6 | LLM0_GPLLC_IN_A**/LDQ48 | C (LVDS)* | PL63B | 6 | LLM0_GPLLC_IN_A**/LDQ67 | C (LVDS)* |
| R3 | PL45A | 6 | LLM0_GPLLT_FB_A/LDQ48 | T | PL64A | 6 | LLM0_GPLLT_FB_A/LDQ67 | T |
| T4 | PL45B | 6 | LLM0_GPLLC_FB_A/LDQ48 | C | PL64B | 6 | LLM0_GPLLC_FB_A/LDQ67 | C |
| T1 | PL46A | 6 | LDQ48 | T (LVDS)* | PL65A | 6 | LDQ67 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO | 6 | | |
| T2 | PL46B | 6 | LDQ48 | C (LVDS)* | PL65B | 6 | LDQ67 | C (LVDS)* |
| T5 | PL47A | 6 | LDQ48 | T | PL66A | 6 | LDQ67 | T |
| T3 | PL47B | 6 | LDQ48 | C | PL66B | 6 | LDQ67 | C |
| GNDIO | GNDIO6 | - | | | VCCIO | 6 | | |
| VCCIO | VCCIO6 | - | | | GNDIO6 | - | | |
| U1 | PL52A | 6 | LDQ56 | T (LVDS)* | PL71A | 6 | LDQ75 | T (LVDS)* |
| U2 | PL52B | 6 | LDQ56 | C (LVDS)* | PL71B | 6 | LDQ75 | C (LVDS)* |
| V1 | PL53A | 6 | LDQ56 | T | PL72A | 6 | LDQ75 | T |
| V2 | PL53B | 6 | LDQ56 | C | PL72B | 6 | LDQ75 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO | 6 | | |
| R6 | PL54A | 6 | LDQ56 | T (LVDS)* | PL73A | 6 | LDQ75 | T (LVDS)* |
| T6 | PL54B | 6 | LDQ56 | C (LVDS)* | PL73B | 6 | LDQ75 | C (LVDS)* |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U3 | PL55A | 6 | LDQ56 | T | PL74A | 6 | LDQ75 | T |
| U4 | PL55B | 6 | LDQ56 | C | PL74B | 6 | LDQ75 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| Y1 | PL56A | 6 | LDQS56 | T (LVDS)* | PL75A | 6 | LDQS75 | T (LVDS)* |
| W1 | PL56B | 6 | LDQ56 | C (LVDS)* | PL75B | 6 | LDQ75 | C (LVDS)* |
| R7 | PL57A | 6 | LDQ56 | T | PL76A | 6 | LDQ75 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO | 6 | | |
| T7 | PL57B | 6 | LDQ56 | C | PL76B | 6 | LDQ75 | C |
| V4 | PL58A | 6 | LDQ56 | T (LVDS)* | PL77A | 6 | LDQ75 | T (LVDS)* |
| V3 | PL58B | 6 | LDQ56 | C (LVDS)* | PL77B | 6 | LDQ75 | C (LVDS)* |
| AA2 | PL59A | 6 | LDQ56 | T | PL78A | 6 | LDQ75 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA1 | PL59B | 6 | LDQ56 | C | PL78B | 6 | LDQ75 | C |
| U7 | TCK | - | | | TCK | - | | |
| U5 | TDI | - | | | TDI | - | | |
| V5 | TMS | - | | | TMS | - | | |
| V6 | TDO | - | | | TDO | - | | |
| T8 | VCCJ | - | | | VCCJ | - | | |
| Y3 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| Y2 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| W4 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| W3 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| W5 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| W6 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| AB3 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| AB2 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| Y4 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| AA3 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AB5 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| AB4 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA5 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| Y5 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| AB6 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| AA6 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| W7 | PB20A | 5 | BDQ24 | T | PB29A | 5 | BDQ33 | T |
| W8 | PB20B | 5 | BDQ24 | C | PB29B | 5 | BDQ33 | C |
| Y6 | PB21A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| Y7 | PB21B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| AA7 | PB22A | 5 | BDQ24 | T | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| AB7 | PB22B | 5 | BDQ24 | C | PB31B | 5 | BDQ33 | C |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U8 | PB23A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| U9 | PB23B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| W9 | PB24A | 5 | BDQS24 | T | PB33A | 5 | BDQS33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| V9 | PB24B | 5 | BDQ24 | C | PB33B | 5 | BDQ33 | C |
| Y8 | PB25A | 5 | BDQ24 | T | PB34A | 5 | BDQ33 | T |
| AA8 | PB25B | 5 | BDQ24 | C | PB34B | 5 | BDQ33 | C |
| W10 | PB26A | 5 | BDQ24 | T | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| V10 | PB26B | 5 | BDQ24 | C | PB35B | 5 | BDQ33 | C |
| AB8 | PB27A | 5 | BDQ24 | T | PB36A | 5 | BDQ33 | T |
| AA9 | PB27B | 5 | BDQ24 | C | PB36B | 5 | BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AB9 | PB29A | 5 | BDQ33 | T | PB38A | 5 | BDQ42 | T |
| AB10 | PB29B | 5 | BDQ33 | C | PB38B | 5 | BDQ42 | C |
| Y10 | PB30A | 5 | BDQ33 | T | PB39A | 5 | BDQ42 | T |
| AA10 | PB30B | 5 | BDQ33 | C | PB39B | 5 | BDQ42 | C |
| U10 | PB31A | 5 | BDQ33 | T | PB40A | 5 | BDQ42 | T |
| U11 | PB31B | 5 | BDQ33 | C | PB40B | 5 | BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| AB11 | PB32A | 5 | BDQ33 | T | PB41A | 5 | BDQ42 | T |
| AA11 | PB32B | 5 | BDQ33 | C | PB41B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| Y11 | PB33A | 5 | BDQS33 | T | PB42A | 5 | BDQS42 | T |
| W11 | PB33B | 5 | BDQ33 | C | PB42B | 5 | BDQ42 | C |
| AB12 | PB34A | 5 | BDQ33 | T | PB43A | 5 | BDQ42 | T |
| AA12 | PB34B | 5 | BDQ33 | C | PB43B | 5 | BDQ42 | C |
| AB13 | PB35A | 5 | PCLKT5_0/BDQ33 | T | PB44A | 5 | PCLKT5_0/BDQ42 | T |
| AB14 | PB35B | 5 | PCLKC5_0/BDQ33 | C | PB44B | 5 | PCLKC5_0/BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| U12 | PB40A | 4 | PCLKT4_0/BDQ42 | T | PB49A | 4 | PCLKT4_0/BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| V12 | PB40B | 4 | PCLKC4_0/BDQ42 | C | PB49B | 4 | PCLKC4_0/BDQ51 | C |
| Y12 | PB41A | 4 | BDQ42 | T | PB50A | 4 | BDQ51 | T |
| W12 | PB41B | 4 | BDQ42 | C | PB50B | 4 | BDQ51 | C |
| AA13 | PB42A | 4 | BDQS42 | T | PB51A | 4 | BDQS51 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| Y13 | PB42B | 4 | BDQ42 | C | PB51B | 4 | BDQ51 | C |
| U13 | PB43A | 4 | BDQ42 | T | PB52A | 4 | BDQ51 | T |
| U14 | PB43B | 4 | BDQ42 | C | PB52B | 4 | BDQ51 | C |
| AB15 | PB44A | 4 | BDQ42 | T | PB53A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| AA14 | PB44B | 4 | BDQ42 | C | PB53B | 4 | BDQ51 | C |
| AB16 | PB45A | 4 | BDQ42 | T | PB54A | 4 | BDQ51 | T |
| AB17 | PB45B | 4 | BDQ42 | C | PB54B | 4 | BDQ51 | C |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W13 | PB46A | 4 | BDQ42 | T | PB55A | 4 | BDQ51 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W14 | PB46B | 4 | BDQ42 | C | PB55B | 4 | BDQ51 | C |
| AB18 | PB48A | 4 | BDQ51 | T | PB57A | 4 | BDQ60 | T |
| AB19 | PB48B | 4 | BDQ51 | C | PB57B | 4 | BDQ60 | C |
| V14 | PB49A | 4 | BDQ51 | T | PB58A | 4 | BDQ60 | T |
| W15 | PB49B | 4 | BDQ51 | C | PB58B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| Y15 | PB50A | 4 | BDQ51 | T | PB59A | 4 | BDQ60 | T |
| AA15 | PB50B | 4 | BDQ51 | C | PB59B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA16 | PB51A | 4 | BDQS51 | T | PB60A | 4 | BDQS60 | T |
| AA17 | PB51B | 4 | BDQ51 | C | PB60B | 4 | BDQ60 | C |
| AB20 | PB52A | 4 | BDQ51 | T | PB61A | 4 | BDQ60 | T |
| AB21 | PB52B | 4 | BDQ51 | C | PB61B | 4 | BDQ60 | C |
| U15 | PB53A | 4 | BDQ51 | T | PB62A | 4 | BDQ60 | T |
| U16 | PB53B | 4 | BDQ51 | C | PB62B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| Y16 | PB54A | 4 | BDQ51 | T | PB63A | 4 | BDQ60 | T |
| W16 | PB54B | 4 | BDQ51 | C | PB63B | 4 | BDQ60 | C |
| AA18 | PB55A | 4 | BDQ51 | T | PB64A | 4 | BDQ60 | T |
| AA20 | PB55B | 4 | BDQ51 | C | PB64B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| AA21 | PB66A | 4 | BDQ69 | T | PB75A | 4 | BDQ78 | T |
| AA22 | PB66B | 4 | BDQ69 | C | PB75B | 4 | BDQ78 | C |
| V16 | PB67A | 4 | BDQ69 | T | PB76A | 4 | BDQ78 | T |
| V17 | PB67B | 4 | BDQ69 | C | PB76B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| Y18 | PB68A | 4 | BDQ69 | T | PB77A | 4 | BDQ78 | T |
| Y17 | PB68B | 4 | BDQ69 | C | PB77B | 4 | BDQ78 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| Y19 | PB69A | 4 | BDQS69 | T | PB78A | 4 | BDQS78 | T |
| Y20 | PB69B | 4 | BDQ69 | C | PB78B | 4 | BDQ78 | C |
| W17 | PB70A | 4 | BDQ69 | T | PB79A | 4 | BDQ78 | T |
| W18 | PB70B | 4 | BDQ69 | C | PB79B | 4 | BDQ78 | C |
| Y21 | PB71A | 4 | BDQ69 | T | PB80A | 4 | BDQ78 | T |
| Y22 | PB71B | 4 | BDQ69 | C | PB80B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| U18 | PB72A | 4 | BDQ69 | T | PB81A | 4 | BDQ78 | T |
| V18 | PB72B | 4 | BDQ69 | C | PB81B | 4 | BDQ78 | C |
| T15 | PB73A | 4 | VREF2_4/BDQ69 | T | PB82A | 4 | VREF2_4/BDQ78 | T |
| T16 | PB73B | 4 | VREF1_4/BDQ69 | C | PB82B | 4 | VREF1_4/BDQ78 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W19 | CFG2 | 8 | | | CFG2 | 8 | | |
| V19 | CFG1 | 8 | | | CFG1 | 8 | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W20 | CFG0 | 8 | | | CFG0 | 8 | | |
| V20 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| W22 | CCLK | 8 | | | CCLK | 8 | | |
| V22 | INITN | 8 | | | INITN | 8 | | |
| V21 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| R16 | PR58B | 8 | WRITEN | C | PR77B | 8 | WRITEN | C |
| R17 | PR58A | 8 | CS1N | T | PR77A | 8 | CS1N | T |
| U19 | PR57B | 8 | CSN | C | PR76B | 8 | CSN | C |
| U20 | PR57A | 8 | D0/SPIFASTN | T | PR76A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO | 8 | | |
| U22 | PR56B | 8 | D1 | C | PR75B | 8 | D1 | C |
| U21 | PR56A | 8 | D2 | T | PR75A | 8 | D2 | T |
| T20 | PR55B | 8 | D3 | C | PR74B | 8 | D3 | C |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| T19 | PR55A | 8 | D4 | T | PR74A | 8 | D4 | T |
| T17 | PR54B | 8 | D5 | C | PR73B | 8 | D5 | C |
| T18 | PR54A | 8 | D6 | T | PR73A | 8 | D6 | T |
| T21 | PR53B | 8 | D7/SPID0 | C | PR72B | 8 | D7/SPID0 | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO | 8 | | |
| T22 | PR53A | 8 | DI/CSSPI0N | T | PR72A | 8 | DI/CSSPI0N | T |
| R18 | PR52B | 8 | DOUT/CSON | C | PR71B | 8 | DOUT/CSON | C |
| R19 | PR52A | 8 | BUSY/SISPI | T | PR71A | 8 | BUSY/SISPI | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| R22 | PR47B | 3 | RDQ48 | C | PR66B | 3 | RDQ67 | C |
| R21 | PR47A | 3 | RDQ48 | T | PR66A | 3 | RDQ67 | T |
| P18 | PR46B | 3 | RDQ48 | C (LVDS)* | PR65B | 3 | RDQ67 | C (LVDS)* |
| P19 | PR46A | 3 | RDQ48 | T (LVDS)* | PR65A | 3 | RDQ67 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| R20 | PR45B | 3 | RLM0_GPLLC_FB_A/RDQ48 | C | PR64B | 3 | RLM0_GPLLC_FB_A/RDQ67 | C |
| P22 | PR45A | 3 | RLM0_GPLLT_FB_A/RDQ48 | T | PR64A | 3 | RLM0_GPLLT_FB_A/RDQ67 | T |
| P21 | PR44B | 3 | RLM0_GPLLC_IN_A**/RDQ48 | C (LVDS)* | PR63B | 3 | RLM0_GPLLC_IN_A**/RDQ67 | C (LVDS)* |
| N21 | PR44A | 3 | RLM0_GPLLT_IN_A**/RDQ48 | T (LVDS)* | PR63A | 3 | RLM0_GPLLT_IN_A**/RDQ67 | T (LVDS)* |
| N17 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| N22 | PR42B | 3 | RLM0_GDLLC_FB_A/RDQ39 | C | PR61B | 3 | RLM0_GDLLC_FB_A/RDQ58 | C |
| N20 | PR42A | 3 | RLM0_GDLLT_FB_A/RDQ39 | T | PR61A | 3 | RLM0_GDLLT_FB_A/RDQ58 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| M22 | PR41B | 3 | RLM0_GDLLC_IN_A**/RDQ39 | C (LVDS)* | PR60B | 3 | RLM0_GDLLC_IN_A**/RDQ58 | C (LVDS)* |
| M21 | PR41A | 3 | RLM0_GDLLT_IN_A**/RDQ39 | T (LVDS)* | PR60A | 3 | RLM0_GDLLT_IN_A**/RDQ58 | T (LVDS)* |
| N19 | PR40B | 3 | RDQ39 | C | PR59B | 3 | RDQ58 | C |
| M19 | PR40A | 3 | RDQ39 | T | PR59A | 3 | RDQ58 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| L22 | PR30B | 3 | RDQ31 | C | PR49B | 3 | RDQ50 | C |
| K22 | PR30A | 3 | RDQ31 | T | PR49A | 3 | RDQ50 | T |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J22 | PR29B | 3 | RDQ31 | C (LVDS)* | PR48B | 3 | RDQ50 | C (LVDS)* |
| H22 | PR29A | 3 | RDQ31 | T (LVDS)* | PR48A | 3 | RDQ50 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| M20 | PR28B | 3 | VREF2_3/RDQ31 | C | PR47B | 3 | VREF2_3/RDQ50 | C |
| L21 | PR28A | 3 | VREF1_3/RDQ31 | T | PR47A | 3 | VREF1_3/RDQ50 | T |
| K21 | PR27B | 3 | PCLKC3_0/RDQ31 | C (LVDS)* | PR46B | 3 | PCLKC3_0/RDQ50 | C (LVDS)* |
| J21 | PR27A | 3 | PCLKT3_0/RDQ31 | T (LVDS)* | PR46A | 3 | PCLKT3_0/RDQ50 | T (LVDS)* |
| M18 | PR25B | 2 | PCLKC2_0/RDQ22 | C | PR44B | 2 | PCLKC2_0/RDQ41 | C |
| L17 | PR25A | 2 | PCLKT2_0/RDQ22 | T | PR44A | 2 | PCLKT2_0/RDQ41 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| L19 | PR24B | 2 | RDQ22 | C (LVDS)* | PR43B | 2 | RDQ41 | C (LVDS)* |
| L20 | PR24A | 2 | RDQ22 | T (LVDS)* | PR43A | 2 | RDQ41 | T (LVDS)* |
| L18 | PR23B | 2 | RDQ22 | C | PR42B | 2 | RDQ41 | C |
| K17 | PR23A | 2 | RDQ22 | T | PR42A | 2 | RDQ41 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| K18 | PR22B | 2 | RDQ22 | C (LVDS)* | PR41B | 2 | RDQ41 | C (LVDS)* |
| K19 | PR22A | 2 | RDQS22 | T (LVDS)* | PR41A | 2 | RDQS41 | T (LVDS)* |
| G22 | PR21B | 2 | RDQ22 | C | PR40B | 2 | RDQ41 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| F22 | PR21A | 2 | RDQ22 | T | PR40A | 2 | RDQ41 | T |
| J17 | PR20B | 2 | RDQ22 | C (LVDS)* | PR39B | 2 | RDQ41 | C (LVDS)* |
| J18 | PR20A | 2 | RDQ22 | T (LVDS)* | PR39A | 2 | RDQ41 | T (LVDS)* |
| K20 | PR19B | 2 | RDQ22 | C | PR38B | 2 | RDQ41 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| J19 | PR19A | 2 | RDQ22 | T | PR38A | 2 | RDQ41 | T |
| H21 | PR18B | 2 | RDQ22 | C (LVDS)* | PR37B | 2 | RDQ41 | C (LVDS)* |
| G21 | PR18A | 2 | RDQ22 | T (LVDS)* | PR37A | 2 | RDQ41 | T (LVDS)* |
| - | - | - | | | GNDIO2 | - | | |
| - | - | - | | | VCCIO | 2 | | |
| H17 | NC | - | | | PR26B | 2 | RUM0_SPLLC_FB_A/RDQ24 | C |
| H16 | NC | - | | | PR26A | 2 | RUM0_SPLLT_FB_A/RDQ24 | T |
| H20 | NC | - | | | PR25B | 2 | RUM0_SPLLC_IN_A/RDQ24 | C |
| H18 | NC | - | | | PR25A | 2 | RUM0_SPLLT_IN_A/RDQ24 | T |
| - | - | - | | | GNDIO2 | - | | |
| - | - | - | | | VCCIO | 2 | | |
| F21 | PR17B | 2 | RDQ14 | C | PR19B | 2 | RDQ16 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR17A | 2 | RDQ14 | T | PR19A | 2 | RDQ16 | T |
| D22 | PR16B | 2 | RDQ14 | C (LVDS)* | PR18B | 2 | RDQ16 | C (LVDS)* |
| E21 | PR16A | 2 | RDQ14 | T (LVDS)* | PR18A | 2 | RDQ16 | T (LVDS)* |
| G20 | PR15B | 2 | RDQ14 | C | PR17B | 2 | RDQ16 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| F20 | PR15A | 2 | RDQ14 | T | PR17A | 2 | RDQ16 | T |
| H19 | PR14B | 2 | RDQ14 | C (LVDS)* | PR16B | 2 | RDQ16 | C (LVDS)* |
| G19 | PR14A | 2 | RDQS14 | T (LVDS)* | PR16A | 2 | RDQS16 | T (LVDS)* |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G17 | PR13B | 2 | RDQ14 | C | PR15B | 2 | RDQ16 | C |
| F19 | PR13A | 2 | RDQ14 | T | PR15A | 2 | RDQ16 | T |
| E20 | PR12B | 2 | RDQ14 | C (LVDS)* | PR14B | 2 | RDQ16 | C (LVDS)* |
| D20 | PR12A | 2 | RDQ14 | T (LVDS)* | PR14A | 2 | RDQ16 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| F18 | PR11B | 2 | RDQ14 | C | PR13B | 2 | RDQ16 | C |
| F16 | PR11A | 2 | RDQ14 | T | PR13A | 2 | RDQ16 | T |
| C21 | PR10B | 2 | RDQ14 | C (LVDS)* | PR12B | 2 | RDQ16 | C (LVDS)* |
| C22 | PR10A | 2 | RDQ14 | T (LVDS)* | PR12A | 2 | RDQ16 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| D19 | PR2B | 2 | VREF2_2/RDQ6 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| E19 | PR2A | 2 | VREF1_2/RDQ6 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| B21 | PT73B | 1 | VREF2_1 | C | PT82B | 1 | VREF2_1 | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| B22 | PT73A | 1 | VREF1_1 | T | PT82A | 1 | VREF1_1 | T |
| C20 | PT72B | 1 | | C | PT81B | 1 | | C |
| C19 | PT72A | 1 | | T | PT81A | 1 | | T |
| D18 | PT71B | 1 | | C | PT80B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| E18 | PT71A | 1 | | T | PT80A | 1 | | T |
| B20 | PT70B | 1 | | C | PT79B | 1 | | C |
| A19 | PT70A | 1 | | T | PT79A | 1 | | T |
| D17 | PT69B | 1 | | C | PT78B | 1 | | C |
| C18 | PT69A | 1 | | T | PT78A | 1 | | T |
| A21 | PT68B | 1 | | C | PT77B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A20 | PT68A | 1 | | T | PT77A | 1 | | T |
| A18 | PT67B | 1 | | C | PT76B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| B18 | PT67A | 1 | | T | PT76A | 1 | | T |
| G16 | PT66B | 1 | | C | PT75B | 1 | | C |
| G15 | PT66A | 1 | | T | PT75A | 1 | | T |
| D16 | PT65B | 1 | | C | PT74B | 1 | | C |
| E16 | PT65A | 1 | | T | PT74A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| C17 | PT55B | 1 | | C | PT64B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| C16 | PT55A | 1 | | T | PT64A | 1 | | T |
| B17 | PT54B | 1 | | C | PT63B | 1 | | C |
| B16 | PT54A | 1 | | T | PT63A | 1 | | T |
| A17 | PT53B | 1 | | C | PT62B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| A16 | PT53A | 1 | | T | PT62A | 1 | | T |
| C15 | PT52B | 1 | | C | PT61B | 1 | | C |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D15 | PT52A | 1 | | T | PT61A | 1 | | T |
| E15 | PT51B | 1 | | C | PT60B | 1 | | C |
| F15 | PT51A | 1 | | T | PT60A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| B15 | PT49B | 1 | | C | PT58B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| A15 | PT49A | 1 | | T | PT58A | 1 | | T |
| B14 | PT48B | 1 | | C | PT57B | 1 | | C |
| A14 | PT48A | 1 | | T | PT57A | 1 | | T |
| D14 | PT46B | 1 | | C | PT55B | 1 | | C |
| C13 | PT46A | 1 | | T | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E14 | PT45B | 1 | | C | PT54B | 1 | | C |
| F14 | PT45A | 1 | | T | PT54A | 1 | | T |
| A13 | PT44B | 1 | | C | PT53B | 1 | | C |
| B13 | PT44A | 1 | | T | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| E13 | PT43B | 1 | | C | PT52B | 1 | | C |
| D13 | PT43A | 1 | | T | PT52A | 1 | | T |
| E12 | PT42B | 1 | | C | PT51B | 1 | | C |
| D12 | PT42A | 1 | | T | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A12 | PT40B | 1 | | C | PT49B | 1 | | C |
| A11 | PT40A | 1 | | T | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| B12 | PT39B | 1 | PCLKC1_0 | C | PT48B | 1 | PCLKC1_0 | C |
| C12 | PT39A | 1 | PCLKT1_0 | T | PT48A | 1 | PCLKT1_0 | T |
| F12 | XRES | 1 | | | XRES | 1 | | |
| B10 | PT37B | 0 | PCLKC0_0 | C | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B11 | PT37A | 0 | PCLKT0_0 | T | PT46A | 0 | PCLKT0_0 | T |
| A10 | PT36B | 0 | | C | PT45B | 0 | | C |
| A9 | PT36A | 0 | | T | PT45A | 0 | | T |
| C11 | PT35B | 0 | | C | PT44B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| C10 | PT35A | 0 | | T | PT44A | 0 | | T |
| E11 | PT34B | 0 | | C | PT43B | 0 | | C |
| F11 | PT34A | 0 | | T | PT43A | 0 | | T |
| A8 | PT33B | 0 | | C | PT42B | 0 | | C |
| A7 | PT33A | 0 | | T | PT42A | 0 | | T |
| B8 | PT32B | 0 | | C | PT41B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B9 | PT32A | 0 | | T | PT41A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| B7 | PT30B | 0 | | C | PT39B | 0 | | C |
| A6 | PT30A | 0 | | T | PT39A | 0 | | T |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C8 | PT29B | 0 | | C | PT38B | 0 | | C |
| D8 | PT29A | 0 | | T | PT38A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| D10 | PT27B | 0 | | C | PT36B | 0 | | C |
| E10 | PT27A | 0 | | T | PT36A | 0 | | T |
| C7 | PT26B | 0 | | C | PT35B | 0 | | C |
| C6 | PT26A | 0 | | T | PT35A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| B6 | PT25B | 0 | | C | PT34B | 0 | | C |
| B5 | PT25A | 0 | | T | PT34A | 0 | | T |
| F10 | PT24B | 0 | | C | PT33B | 0 | | C |
| D9 | PT24A | 0 | | T | PT33A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| F9 | PT23B | 0 | | C | PT32B | 0 | | C |
| E9 | PT23A | 0 | | T | PT32A | 0 | | T |
| A5 | PT22B | 0 | | C | PT31B | 0 | | C |
| A4 | PT22A | 0 | | T | PT31A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| A3 | PT21B | 0 | | C | PT30B | 0 | | C |
| A2 | PT21A | 0 | | T | PT30A | 0 | | T |
| G8 | PT20B | 0 | | C | PT29B | 0 | | C |
| E8 | PT20A | 0 | | T | PT29A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| C3 | PT10B | 0 | | C | PT10B | 0 | | C |
| B3 | PT10A | 0 | | T | PT10A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| F8 | PT9B | 0 | | C | PT9B | 0 | | C |
| D7 | PT9A | 0 | | T | PT9A | 0 | | T |
| E7 | PT8B | 0 | | C | PT8B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| F7 | PT8A | 0 | | T | PT8A | 0 | | T |
| D5 | PT7B | 0 | | C | PT7B | 0 | | C |
| D6 | PT7A | 0 | | T | PT7A | 0 | | T |
| D4 | PT6B | 0 | | C | PT6B | 0 | | C |
| C4 | PT6A | 0 | | T | PT6A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B2 | PT5B | 0 | | C | PT5B | 0 | | C |
| B1 | PT5A | 0 | | T | PT5A | 0 | | T |
| J7 | PT4B | 0 | | C | PT4B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| H7 | PT4A | 0 | | T | PT4A | 0 | | T |
| D3 | PT3B | 0 | | C | PT3B | 0 | | C |
| C2 | PT3A | 0 | | T | PT3A | 0 | | T |
| D1 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| C1 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J10 | VCC | - | | | VCC | - | | |
| J11 | VCC | - | | | VCC | - | | |
| J12 | VCC | - | | | VCC | - | | |
| J13 | VCC | - | | | VCC | - | | |
| K14 | VCC | - | | | VCC | - | | |
| K9 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L9 | VCC | - | | | VCC | - | | |
| M14 | VCC | - | | | VCC | - | | |
| M9 | VCC | - | | | VCC | - | | |
| N14 | VCC | - | | | VCC | - | | |
| N9 | VCC | - | | | VCC | - | | |
| P10 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P12 | VCC | - | | | VCC | - | | |
| P13 | VCC | - | | | VCC | - | | |
| G5 | VCCAUX | - | | | VCCAUX | 0 | | |
| K5 | VCCAUX | - | | | VCCAUX | 0 | | |
| R5 | VCCAUX | - | | | VCCAUX | 1 | | |
| V7 | VCCAUX | - | | | VCCAUX | 1 | | |
| V11 | VCCAUX | - | | | VCCAUX | 2 | | |
| V8 | VCCAUX | - | | | VCCAUX | 2 | | |
| V13 | VCCAUX | - | | | VCCAUX | 3 | | |
| V15 | VCCAUX | - | | | VCCAUX | 3 | | |
| M17 | VCCAUX | - | | | VCCAUX | 4 | | |
| P17 | VCCAUX | - | | | VCCAUX | 4 | | |
| E17 | VCCAUX | - | | | VCCAUX | 5 | | |
| G18 | VCCAUX | - | | | VCCAUX | 5 | | |
| D11 | VCCAUX | - | | | VCCAUX | 6 | | |
| F13 | VCCAUX | - | | | VCCAUX | 6 | | |
| C5 | VCCAUX | - | | | VCCAUX | 7 | | |
| E6 | VCCAUX | - | | | VCCAUX | 7 | | |
| G10 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H8 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G11 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G12 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G13 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H14 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K16 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| P16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T12 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T13 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| R9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T10 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| N7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| J8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| P15 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| R15 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| A22 | GND | - | | | GND | - | | |
| AA19 | GND | - | | | GND | - | | |
| AA4 | GND | - | | | GND | - | | |
| AB1 | GND | - | | | GND | - | | |
| AB22 | GND | - | | | GND | - | | |
| B19 | GND | - | | | GND | - | | |
| B4 | GND | - | | | GND | - | | |
| C14 | GND | - | | | GND | - | | |
| C9 | GND | - | | | GND | - | | |
| D2 | GND | - | | | GND | - | | |
| D21 | GND | - | | | GND | - | | |
| F17 | GND | - | | | GND | - | | |
| F6 | GND | - | | | GND | - | | |
| H10 | GND | - | | | GND | - | | |
| H11 | GND | - | | | GND | - | | |
| H12 | GND | - | | | GND | - | | |
| H13 | GND | - | | | GND | - | | |
| J14 | GND | - | | | GND | - | | |
| J20 | GND | - | | | GND | - | | |
| J3 | GND | - | | | GND | - | | |
| J9 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K12 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K15 | GND | - | | | GND | - | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K8 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |
| L12 | GND | - | | | GND | - | | |
| L13 | GND | - | | | GND | - | | |
| L15 | GND | - | | | GND | - | | |
| L8 | GND | - | | | GND | - | | |
| M10 | GND | - | | | GND | - | | |
| M11 | GND | - | | | GND | - | | |
| M12 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M15 | GND | - | | | GND | - | | |
| M8 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N11 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N8 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P20 | GND | - | | | GND | - | | |
| P3 | GND | - | | | GND | - | | |
| P9 | GND | - | | | GND | - | | |
| R10 | GND | - | | | GND | - | | |
| R11 | GND | - | | | GND | - | | |
| R12 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| U6 | GND | - | | | GND | - | | |
| W2 | GND | - | | | GND | - | | |
| W21 | GND | - | | | GND | - | | |
| Y14 | GND | - | | | GND | - | | |
| Y9 | GND | - | | | GND | - | | |
| A1 | GND | - | | | GND | - | | |
| N18 | VCCPLL | - | | | VCCPLL | - | | |
| K6 | NC | - | | | VCCPLL | - | | |
| N6 | VCCPLL | - | | | VCCPLL | - | | |
| J16 | NC | - | | | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D2 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7/LDQ6 | T (LVDS)* |
| D1 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7/LDQ6 | C (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| F6 | PL3A | 7 | | T | PL3A | 7 | LDQ6 | T |
| F5 | PL3B | 7 | | C | PL3B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E4 | NC | - | | | PL4A | 7 | LDQ6 | T (LVDS)* |
| E3 | NC | - | | | PL4B | 7 | LDQ6 | C (LVDS)* |
| E2 | NC | - | | | PL5A | 7 | LDQ6 | T |
| E1 | NC | - | | | PL5B | 7 | LDQ6 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| H6 | NC | - | | | PL6A | 7 | LDQS6 | T (LVDS)* |
| H5 | NC | - | | | PL6B | 7 | LDQ6 | C (LVDS)* |
| F2 | NC | - | | | PL7A | 7 | LDQ6 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F1 | NC | - | | | PL7B | 7 | LDQ6 | C |
| H8 | NC | - | | | PL8A | 7 | LDQ6 | T (LVDS)* |
| J9 | NC | - | | | PL8B | 7 | LDQ6 | C (LVDS)* |
| G4 | NC | - | | | PL9A | 7 | LDQ6 | T |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| G3 | NC | - | | | PL9B | 7 | LDQ6 | C |
| H7 | PL4A | 7 | LDQ8 | T (LVDS)* | PL10A | 7 | LDQ14 | T (LVDS)* |
| J8 | PL4B | 7 | LDQ8 | C (LVDS)* | PL10B | 7 | LDQ14 | C (LVDS)* |
| G2 | PL5A | 7 | LDQ8 | T | PL11A | 7 | LDQ14 | T |
| G1 | PL5B | 7 | LDQ8 | C | PL11B | 7 | LDQ14 | C |
| H3 | PL6A | 7 | LDQ8 | T (LVDS)* | PL12A | 7 | LDQ14 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H4 | PL6B | 7 | LDQ8 | C (LVDS)* | PL12B | 7 | LDQ14 | C (LVDS)* |
| J5 | PL7A | 7 | LDQ8 | T | PL13A | 7 | LDQ14 | T |
| J4 | PL7B | 7 | LDQ8 | C | PL13B | 7 | LDQ14 | C |
| J3 | PL8A | 7 | LDQS8 | T (LVDS)* | PL14A | 7 | LDQS14 | T (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K4 | PL8B | 7 | LDQ8 | C (LVDS)* | PL14B | 7 | LDQ14 | C (LVDS)* |
| H1 | PL9A | 7 | LDQ8 | T | PL15A | 7 | LDQ14 | T |
| H2 | PL9B | 7 | LDQ8 | C | PL15B | 7 | LDQ14 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K6 | PL10A | 7 | LDQ8 | T (LVDS)* | PL16A | 7 | LDQ14 | T (LVDS)* |
| K7 | PL10B | 7 | LDQ8 | C (LVDS)* | PL16B | 7 | LDQ14 | C (LVDS)* |
| J1 | PL11A | 7 | LDQ8 | T | PL17A | 7 | LDQ14 | T |
| J2 | PL11B | 7 | LDQ8 | C | PL17B | 7 | LDQ14 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K3 | NC | - | | | NC | - | | |
| K2 | NC | - | | | NC | - | | |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K1 | NC | - | | | NC | - | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L2 | NC | - | | | NC | - | | |
| L1 | NC | - | | | NC | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M2 | NC | - | | | NC | - | | |
| M1 | NC | - | | | NC | - | | |
| N2 | NC | - | | | NC | - | | |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| M8 | VCC | - | | | NC | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| N1 | PL12A | 7 | LDQ16 | | PL18A | 7 | LDQ22 | |
| L8 | PL13A | 7 | LDQ16 | T | PL19A | 7 | LDQ22 | T |
| K8 | PL13B | 7 | LDQ16 | C | PL19B | 7 | LDQ22 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L6 | PL14A | 7 | LDQ16 | T (LVDS)* | PL20A | 7 | LDQ22 | T (LVDS)* |
| K5 | PL14B | 7 | LDQ16 | C (LVDS)* | PL20B | 7 | LDQ22 | C (LVDS)* |
| L7 | PL15A | 7 | LDQ16 | T | PL21A | 7 | LDQ22 | T |
| L5 | PL15B | 7 | LDQ16 | C | PL21B | 7 | LDQ22 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| P1 | PL16A | 7 | LDQS16 | T (LVDS)* | PL22A | 7 | LDQS22 | T (LVDS)* |
| P2 | PL16B | 7 | LDQ16 | C (LVDS)* | PL22B | 7 | LDQ22 | C (LVDS)* |
| M6 | PL17A | 7 | LDQ16 | T | PL23A | 7 | LDQ22 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N8 | PL17B | 7 | LDQ16 | C | PL23B | 7 | LDQ22 | C |
| R1 | PL18A | 7 | LDQ16 | T (LVDS)* | PL24A | 7 | LDQ22 | T (LVDS)* |
| R2 | PL18B | 7 | LDQ16 | C (LVDS)* | PL24B | 7 | LDQ22 | C (LVDS)* |
| M7 | PL19A | 7 | PCLKT7_0/LDQ16 | T | PL25A | 7 | PCLKT7_0/LDQ22 | T |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| N9 | PL19B | 7 | PCLKC7_0/LDQ16 | C | PL25B | 7 | PCLKC7_0/LDQ22 | C |
| M4 | PL21A | 6 | PCLKT6_0/LDQ25 | T (LVDS)* | PL27A | 6 | PCLKT6_0/LDQ31 | T (LVDS)* |
| M5 | PL21B | 6 | PCLKC6_0/LDQ25 | C (LVDS)* | PL27B | 6 | PCLKC6_0/LDQ31 | C (LVDS)* |
| N7 | PL22A | 6 | VREF2_6/LDQ25 | T | PL28A | 6 | VREF2_6/LDQ31 | T |
| P9 | PL22B | 6 | VREF1_6/LDQ25 | C | PL28B | 6 | VREF1_6/LDQ31 | C |
| N3 | PL23A | 6 | LDQ25 | T (LVDS)* | PL29A | 6 | LDQ31 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| N4 | PL23B | 6 | LDQ25 | C (LVDS)* | PL29B | 6 | LDQ31 | C (LVDS)* |
| N5 | PL24A | 6 | LDQ25 | T | PL30A | 6 | LDQ31 | T |
| P7 | PL24B | 6 | LDQ25 | C | PL30B | 6 | LDQ31 | C |
| T1 | NC | - | | | PL31A | 6 | LDQS31 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| T2 | NC | - | | | PL31B | 6 | LDQ31 | C (LVDS)* |
| P8 | NC | - | | | PL32A | 6 | LDQ31 | T |
| P6 | NC | - | | | PL32B | 6 | LDQ31 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P5 | NC | - | | | PL33A | 6 | LDQ31 | T (LVDS)* |
| P4 | NC | - | | | PL33B | 6 | LDQ31 | C (LVDS)* |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U1 | NC | - | | | PL34A | 6 | LDQ31 | T |
| V1 | NC | - | | | PL34B | 6 | LDQ31 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| P3 | NC | - | | | NC | - | | |
| R3 | NC | - | | | NC | - | | |
| R4 | NC | - | | | NC | - | | |
| U2 | NC | - | | | NC | - | | |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V2 | NC | - | | | NC | - | | |
| W2 | NC | - | | | NC | - | | |
| T6 | NC | - | | | PL38A | 6 | LDQ39 | T |
| R5 | NC | - | | | PL38B | 6 | LDQ39 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| R6 | PL25A | 6 | LDQS25*** | T (LVDS)* | PL39A | 6 | LDQS39*** | T (LVDS)* |
| R7 | PL25B | 6 | LDQ25 | C (LVDS)* | PL39B | 6 | LDQ39 | C (LVDS)* |
| W1 | PL26A | 6 | LDQ25 | T | PL40A | 6 | LDQ39 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | PL26B | 6 | LDQ25 | C | PL40B | 6 | LDQ39 | C |
| Y1 | PL27A | 6 | LLM0_GDLLT_IN_A**/LDQ25 | T (LVDS)* | PL41A | 6 | LLM0_GDLLT_IN_A**/LDQ39 | T (LVDS)* |
| AA2 | PL27B | 6 | LLM0_GDLLC_IN_A**/LDQ25 | C (LVDS)* | PL41B | 6 | LLM0_GDLLC_IN_A**/LDQ39 | C (LVDS)* |
| T5 | PL28A | 6 | LLM0_GDLLT_FB_A/LDQ25 | T | PL42A | 6 | LLM0_GDLLT_FB_A/LDQ39 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| T7 | PL28B | 6 | LLM0_GDLLC_FB_A/LDQ25 | C | PL42B | 6 | LLM0_GDLLC_FB_A/LDQ39 | C |
| R8 | VCC | 6 | | | VCCPLL | 6 | | |
| T8 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| U3 | PL30A | 6 | LLM0_GPLLT_IN_A**/LDQ34 | T (LVDS)* | PL44A | 6 | LLM0_GPLLT_IN_A**/LDQ48 | T (LVDS)* |
| U4 | PL30B | 6 | LLM0_GPLLC_IN_A**/LDQ34 | C (LVDS)* | PL44B | 6 | LLM0_GPLLC_IN_A**/LDQ48 | C (LVDS)* |
| V3 | PL31A | 6 | LLM0_GPLLT_FB_A/LDQ34 | T | PL45A | 6 | LLM0_GPLLT_FB_A/LDQ48 | T |
| U5 | PL31B | 6 | LLM0_GPLLC_FB_A/LDQ34 | C | PL45B | 6 | LLM0_GPLLC_FB_A/LDQ48 | C |
| V4 | PL32A | 6 | LDQ34 | T (LVDS)* | PL46A | 6 | LDQ48 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V5 | PL32B | 6 | LDQ34 | C (LVDS)* | PL46B | 6 | LDQ48 | C (LVDS)* |
| Y3 | PL33A | 6 | LDQ34 | T | PL47A | 6 | LDQ48 | T |
| Y4 | PL33B | 6 | LDQ34 | C | PL47B | 6 | LDQ48 | C |
| W3 | PL34A | 6 | LDQS34 | T (LVDS)* | PL48A | 6 | LDQS48 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W4 | PL34B | 6 | LDQ34 | C (LVDS)* | PL48B | 6 | LDQ48 | C (LVDS)* |
| AA1 | PL35A | 6 | LDQ34 | T | PL49A | 6 | LDQ48 | T |
| AB1 | PL35B | 6 | LDQ34 | C | PL49B | 6 | LDQ48 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U8 | PL36A | 6 | LDQ34 | T (LVDS)* | PL50A | 6 | LDQ48 | T (LVDS)* |
| U7 | PL36B | 6 | LDQ34 | C (LVDS)* | PL50B | 6 | LDQ48 | C (LVDS)* |
| V8 | PL37A | 6 | LDQ34 | T | PL51A | 6 | LDQ48 | T |
| U6 | PL37B | 6 | LDQ34 | C | PL51B | 6 | LDQ48 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W6 | PL38A | 6 | LDQ42 | T (LVDS)* | PL52A | 6 | LDQ56 | T (LVDS)* |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W5 | PL38B | 6 | LDQ42 | C (LVDS)* | PL52B | 6 | LDQ56 | C (LVDS)* |
| AC1 | PL39A | 6 | LDQ42 | T | PL53A | 6 | LDQ56 | T |
| AD1 | PL39B | 6 | LDQ42 | C | PL53B | 6 | LDQ56 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y6 | PL40A | 6 | LDQ42 | T (LVDS)* | PL54A | 6 | LDQ56 | T (LVDS)* |
| Y5 | PL40B | 6 | LDQ42 | C (LVDS)* | PL54B | 6 | LDQ56 | C (LVDS)* |
| AE2 | PL41A | 6 | LDQ42 | T | PL55A | 6 | LDQ56 | T |
| AD2 | PL41B | 6 | LDQ42 | C | PL55B | 6 | LDQ56 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| AB3 | PL42A | 6 | LDQS42 | T (LVDS)* | PL56A | 6 | LDQS56 | T (LVDS)* |
| AB2 | PL42B | 6 | LDQ42 | C (LVDS)* | PL56B | 6 | LDQ56 | C (LVDS)* |
| W7 | PL43A | 6 | LDQ42 | T | PL57A | 6 | LDQ56 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W8 | PL43B | 6 | LDQ42 | C | PL57B | 6 | LDQ56 | C |
| Y7 | PL44A | 6 | LDQ42 | T (LVDS)* | PL58A | 6 | LDQ56 | T (LVDS)* |
| Y8 | PL44B | 6 | LDQ42 | C (LVDS)* | PL58B | 6 | LDQ56 | C (LVDS)* |
| AC2 | PL45A | 6 | LDQ42 | T | PL59A | 6 | LDQ56 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| AD3 | PL45B | 6 | LDQ42 | C | PL59B | 6 | LDQ56 | C |
| AC3 | TCK | - | | | TCK | - | | |
| AA8 | TDI | - | | | TDI | - | | |
| AB4 | TMS | - | | | TMS | - | | |
| AA5 | TDO | - | | | TDO | - | | |
| AB5 | VCCJ | - | | | VCCJ | - | | |
| AE3 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| AF3 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| AC4 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| AD4 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| AE4 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| AF4 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V9 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| W9 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AA6 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| AB6 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AC5 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| AD5 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA7 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| AB7 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE5 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| AF5 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| AC7 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| AD7 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| W10 | PB11A | 5 | BDQ15 | T | PB11A | 5 | BDQ15 | T |
| Y10 | PB11B | 5 | BDQ15 | C | PB11B | 5 | BDQ15 | C |
| W11 | PB12A | 5 | BDQ15 | T | PB12A | 5 | BDQ15 | T |
| AA10 | PB12B | 5 | BDQ15 | C | PB12B | 5 | BDQ15 | C |
| AC8 | PB13A | 5 | BDQ15 | T | PB13A | 5 | BDQ15 | T |
| AD8 | PB13B | 5 | BDQ15 | C | PB13B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AB8 | PB14A | 5 | BDQ15 | T | PB14A | 5 | BDQ15 | T |
| AB10 | PB14B | 5 | BDQ15 | C | PB14B | 5 | BDQ15 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AE6 | PB15A | 5 | BDQS15 | T | PB15A | 5 | BDQS15 | T |
| AF6 | PB15B | 5 | BDQ15 | C | PB15B | 5 | BDQ15 | C |
| AA11 | PB16A | 5 | BDQ15 | T | PB16A | 5 | BDQ15 | T |
| AC9 | PB16B | 5 | BDQ15 | C | PB16B | 5 | BDQ15 | C |
| AB9 | PB17A | 5 | BDQ15 | T | PB17A | 5 | BDQ15 | T |
| AD9 | PB17B | 5 | BDQ15 | C | PB17B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y11 | PB18A | 5 | BDQ15 | T | PB18A | 5 | BDQ15 | T |
| AB11 | PB18B | 5 | BDQ15 | C | PB18B | 5 | BDQ15 | C |
| AE7 | PB19A | 5 | BDQ15 | T | PB19A | 5 | BDQ15 | T |
| AF7 | PB19B | 5 | BDQ15 | C | PB19B | 5 | BDQ15 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AC10 | PB20A | 5 | BDQ24 | T | PB20A | 5 | BDQ24 | T |
| AD10 | PB20B | 5 | BDQ24 | C | PB20B | 5 | BDQ24 | C |
| AA12 | PB21A | 5 | BDQ24 | T | PB21A | 5 | BDQ24 | T |
| W12 | PB21B | 5 | BDQ24 | C | PB21B | 5 | BDQ24 | C |
| AB12 | PB22A | 5 | BDQ24 | T | PB22A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y12 | PB22B | 5 | BDQ24 | C | PB22B | 5 | BDQ24 | C |
| AD12 | PB23A | 5 | BDQ24 | T | PB23A | 5 | BDQ24 | T |
| AC12 | PB23B | 5 | BDQ24 | C | PB23B | 5 | BDQ24 | C |
| AC13 | PB24A | 5 | BDQS24 | T | PB24A | 5 | BDQS24 | T |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AA13 | PB24B | 5 | BDQ24 | C | PB24B | 5 | BDQ24 | C |
| AD13 | PB25A | 5 | BDQ24 | T | PB25A | 5 | BDQ24 | T |
| AC14 | PB25B | 5 | BDQ24 | C | PB25B | 5 | BDQ24 | C |
| AE8 | PB26A | 5 | BDQ24 | T | PB26A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AF8 | PB26B | 5 | BDQ24 | C | PB26B | 5 | BDQ24 | C |
| AB15 | PB27A | 5 | BDQ24 | T | PB27A | 5 | BDQ24 | T |
| Y13 | PB27B | 5 | BDQ24 | C | PB27B | 5 | BDQ24 | C |
| AE9 | PB28A | 5 | BDQ24 | T | PB28A | 5 | BDQ24 | T |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AF9 | PB28B | 5 | BDQ24 | C | PB28B | 5 | BDQ24 | C |
| W13 | PB29A | 5 | BDQ33 | T | PB29A | 5 | BDQ33 | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA14 | PB29B | 5 | BDQ33 | C | PB29B | 5 | BDQ33 | C |
| AE10 | PB30A | 5 | BDQ33 | T | PB30A | 5 | BDQ33 | T |
| AF10 | PB30B | 5 | BDQ33 | C | PB30B | 5 | BDQ33 | C |
| W14 | PB31A | 5 | BDQ33 | T | PB31A | 5 | BDQ33 | T |
| AB13 | PB31B | 5 | BDQ33 | C | PB31B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y14 | PB32A | 5 | BDQ33 | T | PB32A | 5 | BDQ33 | T |
| AB14 | PB32B | 5 | BDQ33 | C | PB32B | 5 | BDQ33 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AE11 | PB33A | 5 | BDQS33 | T | PB33A | 5 | BDQS33 | T |
| AF11 | PB33B | 5 | BDQ33 | C | PB33B | 5 | BDQ33 | C |
| AD14 | PB34A | 5 | BDQ33 | T | PB34A | 5 | BDQ33 | T |
| AA15 | PB34B | 5 | BDQ33 | C | PB34B | 5 | BDQ33 | C |
| AE12 | PB35A | 5 | PCLKT5_0/BDQ33 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| AF12 | PB35B | 5 | PCLKC5_0/BDQ33 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AD15 | PB40A | 4 | PCLKT4_0/BDQ42 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC15 | PB40B | 4 | PCLKC4_0/BDQ42 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| AE13 | PB41A | 4 | BDQ42 | T | PB41A | 4 | BDQ42 | T |
| AF13 | PB41B | 4 | BDQ42 | C | PB41B | 4 | BDQ42 | C |
| AB17 | PB42A | 4 | BDQS42 | T | PB42A | 4 | BDQS42 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| Y15 | PB42B | 4 | BDQ42 | C | PB42B | 4 | BDQ42 | C |
| AE14 | PB43A | 4 | BDQ42 | T | PB43A | 4 | BDQ42 | T |
| AF14 | PB43B | 4 | BDQ42 | C | PB43B | 4 | BDQ42 | C |
| AA16 | PB44A | 4 | BDQ42 | T | PB44A | 4 | BDQ42 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W15 | PB44B | 4 | BDQ42 | C | PB44B | 4 | BDQ42 | C |
| AC17 | PB45A | 4 | BDQ42 | T | PB45A | 4 | BDQ42 | T |
| AB16 | PB45B | 4 | BDQ42 | C | PB45B | 4 | BDQ42 | C |
| AE15 | PB46A | 4 | BDQ42 | T | PB46A | 4 | BDQ42 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AF15 | PB46B | 4 | BDQ42 | C | PB46B | 4 | BDQ42 | C |
| AE16 | PB47A | 4 | BDQ51 | T | PB47A | 4 | BDQ51 | T |
| AF16 | PB47B | 4 | BDQ51 | C | PB47B | 4 | BDQ51 | C |
| Y16 | PB48A | 4 | BDQ51 | T | PB48A | 4 | BDQ51 | T |
| AB18 | PB48B | 4 | BDQ51 | C | PB48B | 4 | BDQ51 | C |
| AD17 | PB49A | 4 | BDQ51 | T | PB49A | 4 | BDQ51 | T |
| AD18 | PB49B | 4 | BDQ51 | C | PB49B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC18 | PB50A | 4 | BDQ51 | T | PB50A | 4 | BDQ51 | T |
| AD19 | PB50B | 4 | BDQ51 | C | PB50B | 4 | BDQ51 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AC19 | PB51A | 4 | BDQS51 | T | PB51A | 4 | BDQS51 | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AE17 | PB51B | 4 | BDQ51 | C | PB51B | 4 | BDQ51 | C |
| AB19 | PB52A | 4 | BDQ51 | T | PB52A | 4 | BDQ51 | T |
| AE19 | PB52B | 4 | BDQ51 | C | PB52B | 4 | BDQ51 | C |
| AF17 | PB53A | 4 | BDQ51 | T | PB53A | 4 | BDQ51 | T |
| AE18 | PB53B | 4 | BDQ51 | C | PB53B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W16 | PB54A | 4 | BDQ51 | T | PB54A | 4 | BDQ51 | T |
| AA17 | PB54B | 4 | BDQ51 | C | PB54B | 4 | BDQ51 | C |
| AF18 | PB55A | 4 | BDQ51 | T | PB55A | 4 | BDQ51 | T |
| AF19 | PB55B | 4 | BDQ51 | C | PB55B | 4 | BDQ51 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AA19 | NC | - | | | PB56A | 4 | BDQ60 | T |
| W17 | NC | - | | | PB56B | 4 | BDQ60 | C |
| Y19 | NC | - | | | PB57A | 4 | BDQ60 | T |
| Y17 | NC | - | | | PB57B | 4 | BDQ60 | C |
| AF20 | NC | - | | | NC | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AE20 | NC | - | | | NC | - | | |
| AA20 | NC | - | | | NC | - | | |
| W18 | NC | - | | | NC | - | | |
| AD20 | NC | - | | | NC | - | | |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AE21 | NC | - | | | NC | - | | |
| AF21 | NC | - | | | NC | - | | |
| AF22 | NC | - | | | NC | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AE22 | PB56A | 4 | BDQ60 | T | PB65A | 4 | BDQ69 | T |
| AD22 | PB56B | 4 | BDQ60 | C | PB65B | 4 | BDQ69 | C |
| AF23 | PB57A | 4 | BDQ60 | T | PB66A | 4 | BDQ69 | T |
| AE23 | PB57B | 4 | BDQ60 | C | PB66B | 4 | BDQ69 | C |
| AD23 | PB58A | 4 | BDQ60 | T | PB67A | 4 | BDQ69 | T |
| AC23 | PB58B | 4 | BDQ60 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AB20 | PB59A | 4 | BDQ60 | T | PB68A | 4 | BDQ69 | T |
| AC20 | PB59B | 4 | BDQ60 | C | PB68B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AB21 | PB60A | 4 | BDQS60 | T | PB69A | 4 | BDQS69 | T |
| AC22 | PB60B | 4 | BDQ60 | C | PB69B | 4 | BDQ69 | C |
| W19 | PB61A | 4 | BDQ60 | T | PB70A | 4 | BDQ69 | T |
| AA21 | PB61B | 4 | BDQ60 | C | PB70B | 4 | BDQ69 | C |
| AF24 | PB62A | 4 | BDQ60 | T | PB71A | 4 | BDQ69 | T |
| AE24 | PB62B | 4 | BDQ60 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y20 | PB63A | 4 | BDQ60 | T | PB72A | 4 | BDQ69 | T |
| AB22 | PB63B | 4 | BDQ60 | C | PB72B | 4 | BDQ69 | C |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| Y21 | PB64A | 4 | VREF2_4/BDQ60 | T | PB73A | 4 | VREF2_4/BDQ69 | T |
| AB23 | PB64B | 4 | VREF1_4/BDQ60 | C | PB73B | 4 | VREF1_4/BDQ69 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AD24 | CFG2 | 8 | | | CFG2 | 8 | | |
| W20 | CFG1 | 8 | | | CFG1 | 8 | | |
| AC24 | CFG0 | 8 | | | CFG0 | 8 | | |
| V19 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| AA22 | CCLK | 8 | | | CCLK | 8 | | |
| AB24 | INITN | 8 | | | INITN | 8 | | |
| AD25 | DONE | 8 | | | DONE | 8 | | |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| W21 | PR44B | 8 | WRITEN | C | PR58B | 8 | WRITEN | C |
| Y22 | PR44A | 8 | CS1N | T | PR58A | 8 | CS1N | T |
| AC25 | PR43B | 8 | CSN | C | PR57B | 8 | CSN | C |
| AB25 | PR43A | 8 | D0/SPIFASTN | T | PR57A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AD26 | PR42B | 8 | D1 | C | PR56B | 8 | D1 | C |
| AC26 | PR42A | 8 | D2 | T | PR56A | 8 | D2 | T |
| Y23 | PR41B | 8 | D3 | C | PR55B | 8 | D3 | C |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| W22 | PR41A | 8 | D4 | T | PR55A | 8 | D4 | T |
| AA25 | PR40B | 8 | D5 | C | PR54B | 8 | D5 | C |
| AB26 | PR40A | 8 | D6 | T | PR54A | 8 | D6 | T |
| W23 | PR39B | 8 | D7/SPID0 | C | PR53B | 8 | D7/SPID0 | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| V22 | PR39A | 8 | DI/CSSPI0N | T | PR53A | 8 | DI/CSSPI0N | T |
| Y24 | PR38B | 8 | DOUT/CSON | C | PR52B | 8 | DOUT/CSON | C |
| Y25 | PR38A | 8 | BUSY/SISPI | T | PR52A | 8 | BUSY/SISPI | T |
| W24 | PR37B | 3 | RDQ34 | C | PR51B | 3 | RDQ48 | C |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| V23 | PR37A | 3 | RDQ34 | T | PR51A | 3 | RDQ48 | T |
| AA26 | PR36B | 3 | RDQ34 | C (LVDS)* | PR50B | 3 | RDQ48 | C (LVDS)* |
| Y26 | PR36A | 3 | RDQ34 | T (LVDS)* | PR50A | 3 | RDQ48 | T (LVDS)* |
| U21 | PR35B | 3 | RDQ34 | C | PR49B | 3 | RDQ48 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U19 | PR35A | 3 | RDQ34 | T | PR49A | 3 | RDQ48 | T |
| W25 | PR34B | 3 | RDQ34 | C (LVDS)* | PR48B | 3 | RDQ48 | C (LVDS)* |
| W26 | PR34A | 3 | RDQS34 | T (LVDS)* | PR48A | 3 | RDQS48 | T (LVDS)* |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| V24 | PR33B | 3 | RDQ34 | C | PR47B | 3 | RDQ48 | C |
| V25 | PR33A | 3 | RDQ34 | T | PR47A | 3 | RDQ48 | T |
| V26 | PR32B | 3 | RDQ34 | C (LVDS)* | PR46B | 3 | RDQ48 | C (LVDS)* |
| U26 | PR32A | 3 | RDQ34 | T (LVDS)* | PR46A | 3 | RDQ48 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U22 | PR31B | 3 | RLM0_GPLLC_FB_A/RDQ34 | C | PR45B | 3 | RLM0_GPLLC_FB_A/RDQ48 | C |
| U23 | PR31A | 3 | RLM0_GPLLT_FB_A/RDQ34 | T | PR45A | 3 | RLM0_GPLLT_FB_A/RDQ48 | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U24 | PR30B | 3 | RLM0_GPLLC_IN_A**/RDQ34 | C (LVDS)* | PR44B | 3 | RLM0_GPLLC_IN_A**/RDQ48 | C (LVDS)* |
| U25 | PR30A | 3 | RLM0_GPLLT_IN_A**/RDQ34 | T (LVDS)* | PR44A | 3 | RLM0_GPLLT_IN_A**/RDQ48 | T (LVDS)* |
| R20 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| P18 | VCC | 3 | | | VCCPLL | 3 | | |
| T19 | PR28B | 3 | RLM0_GDLLC_FB_A/RDQ25 | C | PR42B | 3 | RLM0_GDLLC_FB_A/RDQ39 | C |
| U20 | PR28A | 3 | RLM0_GDLLT_FB_A/RDQ25 | T | PR42A | 3 | RLM0_GDLLT_FB_A/RDQ39 | T |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| T25 | PR27B | 3 | RLM0_GDLLC_IN_A**/RDQ25 | C (LVDS)* | PR41B | 3 | RLM0_GDLLC_IN_A**/RDQ39 | C (LVDS)* |
| T26 | PR27A | 3 | RLM0_GDLLT_IN_A**/RDQ25 | T (LVDS)* | PR41A | 3 | RLM0_GDLLT_IN_A**/RDQ39 | T (LVDS)* |
| T20 | PR26B | 3 | RDQ25 | C | PR40B | 3 | RDQ39 | C |
| T22 | PR26A | 3 | RDQ25 | T | PR40A | 3 | RDQ39 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R26 | PR25B | 3 | RDQ25 | C (LVDS)* | PR39B | 3 | RDQ39 | C (LVDS)* |
| R25 | PR25A | 3 | RDQS25*** | T (LVDS)* | PR39A | 3 | RDQS39*** | T (LVDS)* |
| R22 | NC | - | | | PR38B | 3 | RDQ39 | C |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| T21 | NC | - | | | PR38A | 3 | RDQ39 | T |
| P26 | NC | - | | | NC | - | | |
| P25 | NC | - | | | NC | - | | |
| R24 | NC | - | | | NC | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R23 | NC | - | | | NC | - | | |
| P20 | NC | - | | | NC | - | | |
| R19 | NC | - | | | NC | - | | |
| P21 | NC | - | | | PR34B | 3 | RDQ31 | C |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| P19 | NC | - | | | PR34A | 3 | RDQ31 | T |
| P23 | NC | - | | | PR33B | 3 | RDQ31 | C (LVDS)* |
| P22 | NC | - | | | PR33A | 3 | RDQ31 | T (LVDS)* |
| N22 | NC | - | | | PR32B | 3 | RDQ31 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R21 | NC | - | | | PR32A | 3 | RDQ31 | T |
| N26 | NC | - | | | PR31B | 3 | RDQ31 | C (LVDS)* |
| N25 | NC | - | | | PR31A | 3 | RDQS31 | T (LVDS)* |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| N19 | PR24B | 3 | RDQ25 | C | PR30B | 3 | RDQ31 | C |
| N20 | PR24A | 3 | RDQ25 | T | PR30A | 3 | RDQ31 | T |
| M26 | PR23B | 3 | RDQ25 | C (LVDS)* | PR29B | 3 | RDQ31 | C (LVDS)* |
| M25 | PR23A | 3 | RDQ25 | T (LVDS)* | PR29A | 3 | RDQ31 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| N18 | PR22B | 3 | VREF2_3/RDQ25 | C | PR28B | 3 | VREF2_3/RDQ31 | C |
| N21 | PR22A | 3 | VREF1_3/RDQ25 | T | PR28A | 3 | VREF1_3/RDQ31 | T |
| L26 | PR21B | 3 | PCLKC3_0/RDQ25 | C (LVDS)* | PR27B | 3 | PCLKC3_0/RDQ31 | C (LVDS)* |
| L25 | PR21A | 3 | PCLKT3_0/RDQ25 | T (LVDS)* | PR27A | 3 | PCLKT3_0/RDQ31 | T (LVDS)* |
| N24 | PR19B | 2 | PCLKC2_0/RDQ16 | C | PR25B | 2 | PCLKC2_0/RDQ22 | C |
| M23 | PR19A | 2 | PCLKT2_0/RDQ16 | T | PR25A | 2 | PCLKT2_0/RDQ22 | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| L21 | PR18B | 2 | RDQ16 | C (LVDS)* | PR24B | 2 | RDQ22 | C (LVDS)* |
| K22 | PR18A | 2 | RDQ16 | T (LVDS)* | PR24A | 2 | RDQ22 | T (LVDS)* |
| M24 | PR17B | 2 | RDQ16 | C | PR23B | 2 | RDQ22 | C |
| N23 | PR17A | 2 | RDQ16 | T | PR23A | 2 | RDQ22 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K26 | PR16B | 2 | RDQ16 | C (LVDS)* | PR22B | 2 | RDQ22 | C (LVDS)* |
| K25 | PR16A | 2 | RDQS16 | T (LVDS)* | PR22A | 2 | RDQS22 | T (LVDS)* |
| M20 | PR15B | 2 | RDQ16 | C | PR21B | 2 | RDQ22 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| M19 | PR15A | 2 | RDQ16 | T | PR21A | 2 | RDQ22 | T |
| L22 | PR14B | 2 | RDQ16 | C (LVDS)* | PR20B | 2 | RDQ22 | C (LVDS)* |
| M22 | PR14A | 2 | RDQ16 | T (LVDS)* | PR20A | 2 | RDQ22 | T (LVDS)* |
| K21 | PR13B | 2 | RDQ16 | C | PR19B | 2 | RDQ22 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M21 | PR13A | 2 | RDQ16 | T | PR19A | 2 | RDQ22 | T |
| K24 | PR12B | 2 | RDQ16 | C (LVDS)* | PR18B | 2 | RDQ22 | C (LVDS)* |
| J24 | PR12A | 2 | RDQ16 | T (LVDS)* | PR18A | 2 | RDQ22 | T (LVDS)* |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L20 | VCC | - | | | NC | - | | |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| J26 | NC | - | | | NC | - | | |
| J25 | NC | - | | | NC | - | | |
| J23 | NC | - | | | NC | - | | |
| K23 | NC | - | | | NC | - | | |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H26 | NC | - | | | NC | - | | |
| H25 | NC | - | | | NC | - | | |
| H24 | NC | - | | | NC | - | | |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| H23 | NC | - | | | NC | - | | |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G26 | PR11B | 2 | RDQ8 | C | PR17B | 2 | RDQ14 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| G25 | PR11A | 2 | RDQ8 | T | PR17A | 2 | RDQ14 | T |
| F26 | PR10B | 2 | RDQ8 | C (LVDS)* | PR16B | 2 | RDQ14 | C (LVDS)* |
| F25 | PR10A | 2 | RDQ8 | T (LVDS)* | PR16A | 2 | RDQ14 | T (LVDS)* |
| K20 | PR9B | 2 | RDQ8 | C | PR15B | 2 | RDQ14 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L19 | PR9A | 2 | RDQ8 | T | PR15A | 2 | RDQ14 | T |
| E26 | PR8B | 2 | RDQ8 | C (LVDS)* | PR14B | 2 | RDQ14 | C (LVDS)* |
| E25 | PR8A | 2 | RDQS8 | T (LVDS)* | PR14A | 2 | RDQS14 | T (LVDS)* |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| J22 | PR7B | 2 | RDQ8 | C | PR13B | 2 | RDQ14 | C |
| H22 | PR7A | 2 | RDQ8 | T | PR13A | 2 | RDQ14 | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G24 | PR6B | 2 | RDQ8 | C (LVDS)* | PR12B | 2 | RDQ14 | C (LVDS)* |
| G23 | PR6A | 2 | RDQ8 | T (LVDS)* | PR12A | 2 | RDQ14 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K19 | PR5B | 2 | RDQ8 | C | PR11B | 2 | RDQ14 | C |
| J19 | PR5A | 2 | RDQ8 | T | PR11A | 2 | RDQ14 | T |
| D26 | PR4B | 2 | RDQ8 | C (LVDS)* | PR10B | 2 | RDQ14 | C (LVDS)* |
| C26 | PR4A | 2 | RDQ8 | T (LVDS)* | PR10A | 2 | RDQ14 | T (LVDS)* |
| F22 | NC | - | | | PR9B | 2 | RDQ6 | C |
| E24 | NC | - | | | PR9A | 2 | RDQ6 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| D25 | NC | - | | | PR8B | 2 | RDQ6 | C (LVDS)* |
| C25 | NC | - | | | PR8A | 2 | RDQ6 | T (LVDS)* |
| D24 | NC | - | | | PR7B | 2 | RDQ6 | C |
| B25 | NC | - | | | PR7A | 2 | RDQ6 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H21 | NC | - | | | PR6B | 2 | RDQ6 | C (LVDS)* |
| G22 | NC | - | | | PR6A | 2 | RDQS6 | T (LVDS)* |
| B24 | NC | - | | | PR5B | 2 | RDQ6 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| C24 | NC | - | | | PR5A | 2 | RDQ6 | T |
| D23 | NC | - | | | PR4B | 2 | RDQ6 | C (LVDS)* |
| C23 | NC | - | | | PR4A | 2 | RDQ6 | T (LVDS)* |
| G21 | PR3B | 2 | | C | PR3B | 2 | RDQ6 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H20 | PR3A | 2 | | T | PR3A | 2 | RDQ6 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2/RDQ6 | C (LVDS)* |
| F21 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2/RDQ6 | T (LVDS)* |
| E23 | PT64B | 1 | VREF2_1 | C | PT73B | 1 | VREF2_1 | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D22 | PT64A | 1 | VREF1_1 | T | PT73A | 1 | VREF1_1 | T |
| G20 | PT63B | 1 | | C | PT72B | 1 | | C |
| J18 | PT63A | 1 | | T | PT72A | 1 | | T |
| F20 | PT62B | 1 | | C | PT71B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H19 | PT62A | 1 | | T | PT71A | 1 | | T |
| A24 | PT61B | 1 | | C | PT70B | 1 | | C |
| A23 | PT61A | 1 | | T | PT70A | 1 | | T |
| E21 | PT60B | 1 | | C | PT69B | 1 | | C |
| F19 | PT60A | 1 | | T | PT69A | 1 | | T |
| C22 | PT59B | 1 | | C | PT68B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E20 | PT59A | 1 | | T | PT68A | 1 | | T |
| B22 | PT58B | 1 | | C | PT67B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B23 | PT58A | 1 | | T | PT67A | 1 | | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C20 | PT57B | 1 | | C | PT66B | 1 | | C |
| D20 | PT57A | 1 | | T | PT66A | 1 | | T |
| A22 | PT56B | 1 | | C | PT65B | 1 | | C |
| A21 | PT56A | 1 | | T | PT65A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E19 | NC | - | | | NC | - | | |
| C19 | NC | - | | | NC | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B21 | NC | - | | | NC | - | | |
| B20 | NC | - | | | NC | - | | |
| D19 | NC | - | | | NC | - | | |
| B19 | NC | - | | | NC | - | | |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G17 | NC | - | | | NC | - | | |
| E18 | NC | - | | | NC | - | | |
| G19 | NC | - | | | NC | - | | |
| F17 | NC | - | | | NC | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A20 | NC | - | | | NC | - | | |
| A19 | NC | - | | | NC | - | | |
| E17 | NC | - | | | NC | - | | |
| D18 | NC | - | | | NC | - | | |
| B18 | PT55B | 1 | | C | PT55B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A18 | PT55A | 1 | | T | PT55A | 1 | | T |
| E16 | PT54B | 1 | | C | PT54B | 1 | | C |
| G16 | PT54A | 1 | | T | PT54A | 1 | | T |
| F16 | PT53B | 1 | | C | PT53B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H18 | PT53A | 1 | | T | PT53A | 1 | | T |
| A17 | PT52B | 1 | | C | PT52B | 1 | | C |
| B17 | PT52A | 1 | | T | PT52A | 1 | | T |
| C18 | PT51B | 1 | | C | PT51B | 1 | | C |
| B16 | PT51A | 1 | | T | PT51A | 1 | | T |
| C17 | PT50B | 1 | | C | PT50B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D17 | PT50A | 1 | | T | PT50A | 1 | | T |
| E15 | PT49B | 1 | | C | PT49B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G15 | PT49A | 1 | | T | PT49A | 1 | | T |
| A16 | PT48B | 1 | | C | PT48B | 1 | | C |
| B15 | PT48A | 1 | | T | PT48A | 1 | | T |
| D15 | PT47B | 1 | | C | PT47B | 1 | | C |
| F15 | PT47A | 1 | | T | PT47A | 1 | | T |
| A14 | PT46B | 1 | | C | PT46B | 1 | | C |
| B14 | PT46A | 1 | | T | PT46A | 1 | | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| C15 | PT45B | 1 | | C | PT45B | 1 | | C |
| A15 | PT45A | 1 | | T | PT45A | 1 | | T |
| A13 | PT44B | 1 | | C | PT44B | 1 | | C |
| B13 | PT44A | 1 | | T | PT44A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H17 | PT43B | 1 | | C | PT43B | 1 | | C |
| H15 | PT43A | 1 | | T | PT43A | 1 | | T |
| D13 | PT42B | 1 | | C | PT42B | 1 | | C |
| C14 | PT42A | 1 | | T | PT42A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G14 | PT41B | 1 | | C | PT41B | 1 | | C |
| E14 | PT41A | 1 | | T | PT41A | 1 | | T |
| A12 | PT40B | 1 | | C | PT40B | 1 | | C |
| B12 | PT40A | 1 | | T | PT40A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F14 | PT39B | 1 | PCLKC1_0 | C | PT39B | 1 | PCLKC1_0 | C |
| D14 | PT39A | 1 | PCLKT1_0 | T | PT39A | 1 | PCLKT1_0 | T |
| H16 | XRES | 1 | | | XRES | 1 | | |
| H14 | PT37B | 0 | PCLKC0_0 | C | PT37B | 0 | PCLKC0_0 | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| H13 | PT37A | 0 | PCLKT0_0 | T | PT37A | 0 | PCLKT0_0 | T |
| A11 | PT36B | 0 | | C | PT36B | 0 | | C |
| B11 | PT36A | 0 | | T | PT36A | 0 | | T |
| C13 | PT35B | 0 | | C | PT35B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E13 | PT35A | 0 | | T | PT35A | 0 | | T |
| D12 | PT34B | 0 | | C | PT34B | 0 | | C |
| F13 | PT34A | 0 | | T | PT34A | 0 | | T |
| A10 | PT33B | 0 | | C | PT33B | 0 | | C |
| B10 | PT33A | 0 | | T | PT33A | 0 | | T |
| C12 | PT32B | 0 | | C | PT32B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| C10 | PT32A | 0 | | T | PT32A | 0 | | T |
| G13 | PT31B | 0 | | C | PT31B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H12 | PT31A | 0 | | T | PT31A | 0 | | T |
| A9 | PT30B | 0 | | C | PT30B | 0 | | C |
| B9 | PT30A | 0 | | T | PT30A | 0 | | T |
| E12 | PT29B | 0 | | C | PT29B | 0 | | C |
| G12 | PT29A | 0 | | T | PT29A | 0 | | T |
| A8 | PT28B | 0 | | C | PT28B | 0 | | C |
| B8 | PT28A | 0 | | T | PT28A | 0 | | T |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| E11 | PT27B | 0 | | C | PT27B | 0 | | C |
| C9 | PT27A | 0 | | T | PT27A | 0 | | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A7 | PT26B | 0 | | C | PT26B | 0 | | C |
| B7 | PT26A | 0 | | T | PT26A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F12 | PT25B | 0 | | C | PT25B | 0 | | C |
| D10 | PT25A | 0 | | T | PT25A | 0 | | T |
| H11 | PT24B | 0 | | C | PT24B | 0 | | C |
| G11 | PT24A | 0 | | T | PT24A | 0 | | T |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| A6 | PT23B | 0 | | C | PT23B | 0 | | C |
| B6 | PT23A | 0 | | T | PT23A | 0 | | T |
| D8 | PT22B | 0 | | C | PT22B | 0 | | C |
| C8 | PT22A | 0 | | T | PT22A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F11 | PT21B | 0 | | C | PT21B | 0 | | C |
| E10 | PT21A | 0 | | T | PT21A | 0 | | T |
| E9 | PT20B | 0 | | C | PT20B | 0 | | C |
| D9 | PT20A | 0 | | T | PT20A | 0 | | T |
| G10 | PT19B | 0 | | C | PT19B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| H10 | PT19A | 0 | | T | PT19A | 0 | | T |
| A5 | PT18B | 0 | | C | PT18B | 0 | | C |
| B5 | PT18A | 0 | | T | PT18A | 0 | | T |
| C7 | PT17B | 0 | | C | PT17B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D7 | PT17A | 0 | | T | PT17A | 0 | | T |
| E8 | PT16B | 0 | | C | PT16B | 0 | | C |
| F10 | PT16A | 0 | | T | PT16A | 0 | | T |
| F8 | PT15B | 0 | | C | PT15B | 0 | | C |
| H9 | PT15A | 0 | | T | PT15A | 0 | | T |
| C5 | PT14B | 0 | | C | PT14B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| D5 | PT14A | 0 | | T | PT14A | 0 | | T |
| B4 | PT13B | 0 | | | PT13B | 0 | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C4 | PT10B | 0 | | C | PT10B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| C3 | PT10A | 0 | | T | PT10A | 0 | | T |
| A4 | PT9B | 0 | | C | PT9B | 0 | | C |
| A3 | PT9A | 0 | | T | PT9A | 0 | | T |
| B3 | PT8B | 0 | | C | PT8B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B2 | PT8A | 0 | | T | PT8A | 0 | | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D4 | PT7B | 0 | | C | PT7B | 0 | | C |
| D3 | PT7A | 0 | | T | PT7A | 0 | | T |
| C2 | PT6B | 0 | | C | PT6B | 0 | | C |
| C1 | PT6A | 0 | | T | PT6A | 0 | | T |
| G8 | PT5B | 0 | | C | PT5B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| G7 | PT5A | 0 | | T | PT5A | 0 | | T |
| E7 | PT4B | 0 | | C | PT4B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F7 | PT4A | 0 | | T | PT4A | 0 | | T |
| E6 | PT3B | 0 | | C | PT3B | 0 | | C |
| E5 | PT3A | 0 | | T | PT3A | 0 | | T |
| G6 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| G5 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |
| L12 | VCC | - | | | VCC | - | | |
| L13 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L15 | VCC | - | | | VCC | - | | |
| M11 | VCC | - | | | VCC | - | | |
| M12 | VCC | - | | | VCC | - | | |
| M15 | VCC | - | | | VCC | - | | |
| M16 | VCC | - | | | VCC | - | | |
| N11 | VCC | - | | | VCC | - | | |
| N16 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P16 | VCC | - | | | VCC | - | | |
| R11 | VCC | - | | | VCC | - | | |
| R12 | VCC | - | | | VCC | - | | |
| R15 | VCC | - | | | VCC | - | | |
| R16 | VCC | - | | | VCC | - | | |
| T12 | VCC | - | | | VCC | - | | |
| T13 | VCC | - | | | VCC | - | | |
| T14 | VCC | - | | | VCC | - | | |
| T15 | VCC | - | | | VCC | - | | |
| D11 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D6 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D21 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J20 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M17 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| AA23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R17 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V20 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AC16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC21 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC6 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| U12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R9 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| F4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AE25 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| V18 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| J10 | VCCAUX | - | | | VCCAUX | - | | |
| J11 | VCCAUX | - | | | VCCAUX | - | | |
| J16 | VCCAUX | - | | | VCCAUX | - | | |
| J17 | VCCAUX | - | | | VCCAUX | - | | |
| K18 | VCCAUX | - | | | VCCAUX | - | | |
| K9 | VCCAUX | - | | | VCCAUX | - | | |
| L18 | VCCAUX | - | | | VCCAUX | - | | |
| L9 | VCCAUX | - | | | VCCAUX | - | | |
| T18 | VCCAUX | - | | | VCCAUX | - | | |
| T9 | VCCAUX | - | | | VCCAUX | - | | |
| U18 | VCCAUX | - | | | VCCAUX | - | | |
| U9 | VCCAUX | - | | | VCCAUX | - | | |
| V10 | VCCAUX | - | | | VCCAUX | - | | |
| V11 | VCCAUX | - | | | VCCAUX | - | | |
| V16 | VCCAUX | - | | | VCCAUX | - | | |
| V17 | VCCAUX | - | | | VCCAUX | - | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A2 | GND | - | | | GND | - | | |
| A25 | GND | - | | | GND | - | | |
| AA18 | GND | - | | | GND | - | | |
| AA24 | GND | - | | | GND | - | | |
| AA3 | GND | - | | | GND | - | | |
| AA9 | GND | - | | | GND | - | | |
| AD11 | GND | - | | | GND | - | | |
| AD16 | GND | - | | | GND | - | | |
| AD21 | GND | - | | | GND | - | | |
| AD6 | GND | - | | | GND | - | | |
| AE1 | GND | - | | | GND | - | | |
| AE26 | GND | - | | | GND | - | | |
| AF2 | GND | - | | | GND | - | | |
| AF25 | GND | - | | | GND | - | | |
| B1 | GND | - | | | GND | - | | |
| B26 | GND | - | | | GND | - | | |
| C11 | GND | - | | | GND | - | | |
| C16 | GND | - | | | GND | - | | |
| C21 | GND | - | | | GND | - | | |
| C6 | GND | - | | | GND | - | | |
| F18 | GND | - | | | GND | - | | |
| F24 | GND | - | | | GND | - | | |
| F3 | GND | - | | | GND | - | | |
| F9 | GND | - | | | GND | - | | |
| J13 | GND | - | | | GND | - | | |
| J14 | GND | - | | | GND | - | | |
| J21 | GND | - | | | GND | - | | |
| J6 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K14 | GND | - | | | GND | - | | |
| K16 | GND | - | | | GND | - | | |
| K17 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |
| L16 | GND | - | | | GND | - | | |
| L17 | GND | - | | | GND | - | | |
| L24 | GND | - | | | GND | - | | |
| L3 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M14 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N14 | GND | - | | | GND | - | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N15 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| P10 | GND | - | | | GND | - | | |
| P12 | GND | - | | | GND | - | | |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T24 | GND | - | | | GND | - | | |
| T3 | GND | - | | | GND | - | | |
| U10 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| V13 | GND | - | | | GND | - | | |
| V14 | GND | - | | | GND | - | | |
| V21 | GND | - | | | GND | - | | |
| V6 | GND | - | | | GND | - | | |
| M3 | NC | - | | | NC | - | | |
| N6 | NC | - | | | NC | - | | |
| P24 | NC | - | | | NC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D2 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| D1 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| F6 | PL5A | 7 | LDQ8 | T | PL18A | 7 | LDQ21 | T |
| F5 | PL5B | 7 | LDQ8 | C | PL18B | 7 | LDQ21 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E4 | PL6A | 7 | LDQ8 | T (LVDS)* | PL19A | 7 | LDQ21 | T (LVDS)* |
| E3 | PL6B | 7 | LDQ8 | C (LVDS)* | PL19B | 7 | LDQ21 | C (LVDS)* |
| E2 | PL7A | 7 | LDQ8 | T | PL20A | 7 | LDQ21 | T |
| E1 | PL7B | 7 | LDQ8 | C | PL20B | 7 | LDQ21 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| H6 | PL8A | 7 | LDQS8 | T (LVDS)* | PL21A | 7 | LDQS21 | T (LVDS)* |
| H5 | PL8B | 7 | LDQ8 | C (LVDS)* | PL21B | 7 | LDQ21 | C (LVDS)* |
| F2 | PL9A | 7 | LDQ8 | T | PL22A | 7 | LDQ21 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F1 | PL9B | 7 | LDQ8 | C | PL22B | 7 | LDQ21 | C |
| H8 | PL10A | 7 | LDQ8 | T (LVDS)* | PL23A | 7 | LDQ21 | T (LVDS)* |
| J9 | PL10B | 7 | LDQ8 | C (LVDS)* | PL23B | 7 | LDQ21 | C (LVDS)* |
| G4 | PL11A | 7 | LDQ8 | T | PL24A | 7 | LDQ21 | T |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| G3 | PL11B | 7 | LDQ8 | C | PL24B | 7 | LDQ21 | C |
| H7 | PL12A | 7 | LDQ16 | T (LVDS)* | PL25A | 7 | LDQ29 | T (LVDS)* |
| J8 | PL12B | 7 | LDQ16 | C (LVDS)* | PL25B | 7 | LDQ29 | C (LVDS)* |
| G2 | PL13A | 7 | LDQ16 | T | PL26A | 7 | LDQ29 | T |
| G1 | PL13B | 7 | LDQ16 | C | PL26B | 7 | LDQ29 | C |
| H3 | PL14A | 7 | LDQ16 | T (LVDS)* | PL27A | 7 | LDQ29 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H4 | PL14B | 7 | LDQ16 | C (LVDS)* | PL27B | 7 | LDQ29 | C (LVDS)* |
| J5 | PL15A | 7 | LDQ16 | T | PL28A | 7 | LDQ29 | T |
| J4 | PL15B | 7 | LDQ16 | C | PL28B | 7 | LDQ29 | C |
| J3 | PL16A | 7 | LDQS16 | T (LVDS)* | PL29A | 7 | LDQS29 | T (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K4 | PL16B | 7 | LDQ16 | C (LVDS)* | PL29B | 7 | LDQ29 | C (LVDS)* |
| H1 | PL17A | 7 | LDQ16 | T | PL30A | 7 | LDQ29 | T |
| H2 | PL17B | 7 | LDQ16 | C | PL30B | 7 | LDQ29 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K6 | PL18A | 7 | LDQ16 | T (LVDS)* | PL31A | 7 | LDQ29 | T (LVDS)* |
| K7 | PL18B | 7 | LDQ16 | C (LVDS)* | PL31B | 7 | LDQ29 | C (LVDS)* |
| J1 | PL19A | 7 | LDQ16 | T | PL32A | 7 | LDQ29 | T |
| J2 | PL19B | 7 | LDQ16 | C | PL32B | 7 | LDQ29 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K3 | PL23A | 7 | LDQ24 | T | PL36A | 7 | LDQ37 | T |
| K2 | PL23B | 7 | LDQ24 | C | PL36B | 7 | LDQ37 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K1 | PL24A | 7 | LDQS24*** | T (LVDS)* | PL37A | 7 | LDQS37*** | T (LVDS)* |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L2 | PL24B | 7 | LDQ24 | C (LVDS)* | PL37B | 7 | LDQ37 | C (LVDS)* |
| L1 | PL25A | 7 | LUM0_SPLLT_IN_A/LDQ24 | T | PL38A | 7 | LUM0_SPLLT_IN_A/LDQ37 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M2 | PL25B | 7 | LUM0_SPLLC_IN_A/LDQ24 | C | PL38B | 7 | LUM0_SPLLC_IN_A/LDQ37 | C |
| M1 | PL26A | 7 | LUM0_SPLLT_FB_A/LDQ24 | T | PL39A | 7 | LUM0_SPLLT_FB_A/LDQ37 | T |
| N2 | PL26B | 7 | LUM0_SPLLC_FB_A/LDQ24 | C | PL39B | 7 | LUM0_SPLLC_FB_A/LDQ37 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| M8 | VCCPLL | 7 | | | NC | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| N1 | PL37A | 7 | LDQ41 | | PL50A | 7 | LDQ54 | |
| L8 | PL38A | 7 | LDQ41 | T | PL51A | 7 | LDQ54 | T |
| K8 | PL38B | 7 | LDQ41 | C | PL51B | 7 | LDQ54 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L6 | PL39A | 7 | LDQ41 | T (LVDS)* | PL52A | 7 | LDQ54 | T (LVDS)* |
| K5 | PL39B | 7 | LDQ41 | C (LVDS)* | PL52B | 7 | LDQ54 | C (LVDS)* |
| L7 | PL40A | 7 | LDQ41 | T | PL53A | 7 | LDQ54 | T |
| L5 | PL40B | 7 | LDQ41 | C | PL53B | 7 | LDQ54 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| P1 | PL41A | 7 | LDQS41 | T (LVDS)* | PL54A | 7 | LDQS54 | T (LVDS)* |
| P2 | PL41B | 7 | LDQ41 | C (LVDS)* | PL54B | 7 | LDQ54 | C (LVDS)* |
| M6 | PL42A | 7 | LDQ41 | T | PL55A | 7 | LDQ54 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N8 | PL42B | 7 | LDQ41 | C | PL55B | 7 | LDQ54 | C |
| R1 | PL43A | 7 | LDQ41 | T (LVDS)* | PL56A | 7 | LDQ54 | T (LVDS)* |
| R2 | PL43B | 7 | LDQ41 | C (LVDS)* | PL56B | 7 | LDQ54 | C (LVDS)* |
| M7 | PL44A | 7 | PCLKT7_0/LDQ41 | T | PL57A | 7 | PCLKT7_0/LDQ54 | T |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| N9 | PL44B | 7 | PCLKC7_0/LDQ41 | C | PL57B | 7 | PCLKC7_0/LDQ54 | C |
| M4 | PL46A | 6 | PCLKT6_0/LDQ50 | T (LVDS)* | PL59A | 6 | PCLKT6_0/LDQ63 | T (LVDS)* |
| M5 | PL46B | 6 | PCLKC6_0/LDQ50 | C (LVDS)* | PL59B | 6 | PCLKC6_0/LDQ63 | C (LVDS)* |
| N7 | PL47A | 6 | VREF2_6/LDQ50 | T | PL60A | 6 | VREF2_6/LDQ63 | T |
| P9 | PL47B | 6 | VREF1_6/LDQ50 | C | PL60B | 6 | VREF1_6/LDQ63 | C |
| N3 | PL48A | 6 | LDQ50 | T (LVDS)* | PL61A | 6 | LDQ63 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| N4 | PL48B | 6 | LDQ50 | C (LVDS)* | PL61B | 6 | LDQ63 | C (LVDS)* |
| N5 | PL49A | 6 | LDQ50 | T | PL62A | 6 | LDQ63 | T |
| P7 | PL49B | 6 | LDQ50 | C | PL62B | 6 | LDQ63 | C |
| T1 | PL50A | 6 | LDQS50 | T (LVDS)* | PL63A | 6 | LDQS63 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| T2 | PL50B | 6 | LDQ50 | C (LVDS)* | PL63B | 6 | LDQ63 | C (LVDS)* |
| P8 | PL51A | 6 | LDQ50 | T | PL64A | 6 | LDQ63 | T |
| P6 | PL51B | 6 | LDQ50 | C | PL64B | 6 | LDQ63 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P5 | PL52A | 6 | LDQ50 | T (LVDS)* | PL65A | 6 | LDQ63 | T (LVDS)* |
| P4 | PL52B | 6 | LDQ50 | C (LVDS)* | PL65B | 6 | LDQ63 | C (LVDS)* |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U1 | PL53A | 6 | LDQ50 | T | PL66A | 6 | LDQ63 | T |
| V1 | PL53B | 6 | LDQ50 | C | PL66B | 6 | LDQ63 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| P3 | PL54A | 6 | LDQ58 | T (LVDS)* | PL67A | 6 | LDQ71 | T (LVDS)* |
| R3 | PL54B | 6 | LDQ58 | C (LVDS)* | PL67B | 6 | LDQ71 | C (LVDS)* |
| R4 | PL55A | 6 | LDQ58 | T | PL68A | 6 | LDQ71 | T |
| U2 | PL55B | 6 | LDQ58 | C | PL68B | 6 | LDQ71 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V2 | PL56A | 6 | LDQ58 | T (LVDS)* | PL69A | 6 | LDQ71 | T (LVDS)* |
| W2 | PL56B | 6 | LDQ58 | C (LVDS)* | PL69B | 6 | LDQ71 | C (LVDS)* |
| T6 | PL57A | 6 | LDQ58 | T | PL70A | 6 | LDQ71 | T |
| R5 | PL57B | 6 | LDQ58 | C | PL70B | 6 | LDQ71 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| R6 | PL58A | 6 | LDQS58 | T (LVDS)* | PL71A | 6 | LDQS71 | T (LVDS)* |
| R7 | PL58B | 6 | LDQ58 | C (LVDS)* | PL71B | 6 | LDQ71 | C (LVDS)* |
| W1 | PL59A | 6 | LDQ58 | T | PL72A | 6 | LDQ71 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | PL59B | 6 | LDQ58 | C | PL72B | 6 | LDQ71 | C |
| Y1 | PL60A | 6 | LLM0_GDLLT_IN_A**/LDQ58 | T (LVDS)* | PL73A | 6 | LLM0_GDLLT_IN_A**/LDQ71 | T (LVDS)* |
| AA2 | PL60B | 6 | LLM0_GDLLC_IN_A**/LDQ58 | C (LVDS)* | PL73B | 6 | LLM0_GDLLC_IN_A**/LDQ71 | C (LVDS)* |
| T5 | PL61A | 6 | LLM0_GDLLT_FB_A/LDQ58 | T | PL74A | 6 | LLM0_GDLLT_FB_A/LDQ71 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| T7 | PL61B | 6 | LLM0_GDLLC_FB_D/LDQ58 | C | PL74B | 6 | LLM0_GDLLC_FB_D/LDQ71 | C |
| R8 | VCCPLL | 6 | | | VCCPLL | - | | |
| T8 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| U3 | PL63A | 6 | LLM0_GPLLT_IN_A**/LDQ67 | T (LVDS)* | PL76A | 6 | LLM0_GPLLT_IN_A**/LDQ80 | T (LVDS)* |
| U4 | PL63B | 6 | LLM0_GPLLC_IN_A**/LDQ67 | C (LVDS)* | PL76B | 6 | LLM0_GPLLC_IN_A**/LDQ80 | C (LVDS)* |
| V3 | PL64A | 6 | LLM0_GPLLT_FB_A/LDQ67 | T | PL77A | 6 | LLM0_GPLLT_FB_A/LDQ80 | T |
| U5 | PL64B | 6 | LLM0_GPLLC_FB_A/LDQ67 | C | PL77B | 6 | LLM0_GPLLC_FB_A/LDQ80 | C |
| V4 | PL65A | 6 | LDQ67 | T (LVDS)* | PL78A | 6 | LDQ80 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V5 | PL65B | 6 | LDQ67 | C (LVDS)* | PL78B | 6 | LDQ80 | C (LVDS)* |
| Y3 | PL66A | 6 | LDQ67 | T | PL79A | 6 | LDQ80 | T |
| Y4 | PL66B | 6 | LDQ67 | C | PL79B | 6 | LDQ80 | C |
| W3 | PL67A | 6 | LDQS67 | T (LVDS)* | PL80A | 6 | LDQS80 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W4 | PL67B | 6 | LDQ67 | C (LVDS)* | PL80B | 6 | LDQ80 | C (LVDS)* |
| AA1 | PL68A | 6 | LDQ67 | T | PL81A | 6 | LDQ80 | T |
| AB1 | PL68B | 6 | LDQ67 | C | PL81B | 6 | LDQ80 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U8 | PL69A | 6 | LDQ67 | T (LVDS)* | PL82A | 6 | LDQ80 | T (LVDS)* |
| U7 | PL69B | 6 | LDQ67 | C (LVDS)* | PL82B | 6 | LDQ80 | C (LVDS)* |
| V8 | PL70A | 6 | LDQ67 | T | PL83A | 6 | LDQ80 | T |
| U6 | PL70B | 6 | LDQ67 | C | PL83B | 6 | LDQ80 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W6 | PL71A | 6 | LDQ75 | T (LVDS)* | PL84A | 6 | LDQ88 | T (LVDS)* |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W5 | PL71B | 6 | LDQ75 | C (LVDS)* | PL84B | 6 | LDQ88 | C (LVDS)* |
| AC1 | PL72A | 6 | LDQ75 | T | PL85A | 6 | LDQ88 | T |
| AD1 | PL72B | 6 | LDQ75 | C | PL85B | 6 | LDQ88 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y6 | PL73A | 6 | LDQ75 | T (LVDS)* | PL86A | 6 | LDQ88 | T (LVDS)* |
| Y5 | PL73B | 6 | LDQ75 | C (LVDS)* | PL86B | 6 | LDQ88 | C (LVDS)* |
| AE2 | PL74A | 6 | LDQ75 | T | PL87A | 6 | LDQ88 | T |
| AD2 | PL74B | 6 | LDQ75 | C | PL87B | 6 | LDQ88 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| AB3 | PL75A | 6 | LDQS75 | T (LVDS)* | PL88A | 6 | LDQS88 | T (LVDS)* |
| AB2 | PL75B | 6 | LDQ75 | C (LVDS)* | PL88B | 6 | LDQ88 | C (LVDS)* |
| W7 | PL76A | 6 | LDQ75 | T | PL89A | 6 | LDQ88 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W8 | PL76B | 6 | LDQ75 | C | PL89B | 6 | LDQ88 | C |
| Y7 | PL77A | 6 | LDQ75 | T (LVDS)* | PL90A | 6 | LDQ88 | T (LVDS)* |
| Y8 | PL77B | 6 | LDQ75 | C (LVDS)* | PL90B | 6 | LDQ88 | C (LVDS)* |
| AC2 | PL78A | 6 | LDQ75 | T | PL91A | 6 | LDQ88 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| AD3 | PL78B | 6 | LDQ75 | C | PL91B | 6 | LDQ88 | C |
| AC3 | TCK | - | | | TCK | - | | |
| AA8 | TDI | - | | | TDI | - | | |
| AB4 | TMS | - | | | TMS | - | | |
| AA5 | TDO | - | | | TDO | - | | |
| AB5 | VCCJ | - | | | VCCJ | - | | |
| AE3 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| AF3 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| AC4 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| AD4 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| AE4 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| AF4 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V9 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| W9 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AA6 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| AB6 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AC5 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| AD5 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA7 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| AB7 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE5 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| AF5 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| AC7 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| AD7 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| W10 | PB20A | 5 | BDQ24 | T | PB29A | 5 | BDQ33 | T |
| Y10 | PB20B | 5 | BDQ24 | C | PB29B | 5 | BDQ33 | C |
| W11 | PB21A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| AA10 | PB21B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| AC8 | PB22A | 5 | BDQ24 | T | PB31A | 5 | BDQ33 | T |
| AD8 | PB22B | 5 | BDQ24 | C | PB31B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AB8 | PB23A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| AB10 | PB23B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AE6 | PB24A | 5 | BDQS24 | T | PB33A | 5 | BDQS33 | T |
| AF6 | PB24B | 5 | BDQ24 | C | PB33B | 5 | BDQ33 | C |
| AA11 | PB25A | 5 | BDQ24 | T | PB34A | 5 | BDQ33 | T |
| AC9 | PB25B | 5 | BDQ24 | C | PB34B | 5 | BDQ33 | C |
| AB9 | PB26A | 5 | BDQ24 | T | PB35A | 5 | BDQ33 | T |
| AD9 | PB26B | 5 | BDQ24 | C | PB35B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y11 | PB27A | 5 | BDQ24 | T | PB36A | 5 | BDQ33 | T |
| AB11 | PB27B | 5 | BDQ24 | C | PB36B | 5 | BDQ33 | C |
| AE7 | PB28A | 5 | BDQ24 | T | PB37A | 5 | BDQ33 | T |
| AF7 | PB28B | 5 | BDQ24 | C | PB37B | 5 | BDQ33 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AC10 | PB29A | 5 | BDQ33 | T | PB38A | 5 | BDQ42 | T |
| AD10 | PB29B | 5 | BDQ33 | C | PB38B | 5 | BDQ42 | C |
| AA12 | PB30A | 5 | BDQ33 | T | PB39A | 5 | BDQ42 | T |
| W12 | PB30B | 5 | BDQ33 | C | PB39B | 5 | BDQ42 | C |
| AB12 | PB31A | 5 | BDQ33 | T | PB40A | 5 | BDQ42 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y12 | PB31B | 5 | BDQ33 | C | PB40B | 5 | BDQ42 | C |
| AD12 | PB32A | 5 | BDQ33 | T | PB41A | 5 | BDQ42 | T |
| AC12 | PB32B | 5 | BDQ33 | C | PB41B | 5 | BDQ42 | C |
| AC13 | PB33A | 5 | BDQS33 | T | PB42A | 5 | BDQS42 | T |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AA13 | PB33B | 5 | BDQ33 | C | PB42B | 5 | BDQ42 | C |
| AD13 | PB34A | 5 | BDQ33 | T | PB43A | 5 | BDQ42 | T |
| AC14 | PB34B | 5 | BDQ33 | C | PB43B | 5 | BDQ42 | C |
| AE8 | PB35A | 5 | BDQ33 | T | PB44A | 5 | BDQ42 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AF8 | PB35B | 5 | BDQ33 | C | PB44B | 5 | BDQ42 | C |
| AB15 | PB36A | 5 | BDQ33 | T | PB45A | 5 | BDQ42 | T |
| Y13 | PB36B | 5 | BDQ33 | C | PB45B | 5 | BDQ42 | C |
| AE9 | PB37A | 5 | BDQ33 | T | PB46A | 5 | BDQ42 | T |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AF9 | PB37B | 5 | BDQ33 | C | PB46B | 5 | BDQ42 | C |
| W13 | PB38A | 5 | BDQ42 | T | PB47A | 5 | BDQ51 | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA14 | PB38B | 5 | BDQ42 | C | PB47B | 5 | BDQ51 | C |
| AE10 | PB39A | 5 | BDQ42 | T | PB48A | 5 | BDQ51 | T |
| AF10 | PB39B | 5 | BDQ42 | C | PB48B | 5 | BDQ51 | C |
| W14 | PB40A | 5 | BDQ42 | T | PB49A | 5 | BDQ51 | T |
| AB13 | PB40B | 5 | BDQ42 | C | PB49B | 5 | BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y14 | PB41A | 5 | BDQ42 | T | PB50A | 5 | BDQ51 | T |
| AB14 | PB41B | 5 | BDQ42 | C | PB50B | 5 | BDQ51 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AE11 | PB42A | 5 | BDQS42 | T | PB51A | 5 | BDQS51 | T |
| AF11 | PB42B | 5 | BDQ42 | C | PB51B | 5 | BDQ51 | C |
| AD14 | PB43A | 5 | BDQ42 | T | PB52A | 5 | BDQ51 | T |
| AA15 | PB43B | 5 | BDQ42 | C | PB52B | 5 | BDQ51 | C |
| AE12 | PB44A | 5 | PCLKT5_0/BDQ42 | T | PB53A | 5 | PCLKT5_0/BDQ51 | T |
| AF12 | PB44B | 5 | PCLKC5_0/BDQ42 | C | PB53B | 5 | PCLKC5_0/BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| AD15 | PB49A | 4 | PCLKT4_0/BDQ51 | T | PB58A | 4 | PCLKT4_0/BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC15 | PB49B | 4 | PCLKC4_0/BDQ51 | C | PB58B | 4 | PCLKC4_0/BDQ60 | C |
| AE13 | PB50A | 4 | BDQ51 | T | PB59A | 4 | BDQ60 | T |
| AF13 | PB50B | 4 | BDQ51 | C | PB59B | 4 | BDQ60 | C |
| AB17 | PB51A | 4 | BDQS51 | T | PB60A | 4 | BDQS60 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| Y15 | PB51B | 4 | BDQ51 | C | PB60B | 4 | BDQ60 | C |
| AE14 | PB52A | 4 | BDQ51 | T | PB61A | 4 | BDQ60 | T |
| AF14 | PB52B | 4 | BDQ51 | C | PB61B | 4 | BDQ60 | C |
| AA16 | PB53A | 4 | BDQ51 | T | PB62A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W15 | PB53B | 4 | BDQ51 | C | PB62B | 4 | BDQ60 | C |
| AC17 | PB54A | 4 | BDQ51 | T | PB63A | 4 | BDQ60 | T |
| AB16 | PB54B | 4 | BDQ51 | C | PB63B | 4 | BDQ60 | C |
| AE15 | PB55A | 4 | BDQ51 | T | PB64A | 4 | BDQ60 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AF15 | PB55B | 4 | BDQ51 | C | PB64B | 4 | BDQ60 | C |
| AE16 | PB56A | 4 | BDQ60 | T | PB65A | 4 | BDQ69 | T |
| AF16 | PB56B | 4 | BDQ60 | C | PB65B | 4 | BDQ69 | C |
| Y16 | PB57A | 4 | BDQ60 | T | PB66A | 4 | BDQ69 | T |
| AB18 | PB57B | 4 | BDQ60 | C | PB66B | 4 | BDQ69 | C |
| AD17 | PB58A | 4 | BDQ60 | T | PB67A | 4 | BDQ69 | T |
| AD18 | PB58B | 4 | BDQ60 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC18 | PB59A | 4 | BDQ60 | T | PB68A | 4 | BDQ69 | T |
| AD19 | PB59B | 4 | BDQ60 | C | PB68B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AC19 | PB60A | 4 | BDQS60 | T | PB69A | 4 | BDQS69 | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AE17 | PB60B | 4 | BDQ60 | C | PB69B | 4 | BDQ69 | C |
| AB19 | PB61A | 4 | BDQ60 | T | PB70A | 4 | BDQ69 | T |
| AE19 | PB61B | 4 | BDQ60 | C | PB70B | 4 | BDQ69 | C |
| AF17 | PB62A | 4 | BDQ60 | T | PB71A | 4 | BDQ69 | T |
| AE18 | PB62B | 4 | BDQ60 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W16 | PB63A | 4 | BDQ60 | T | PB72A | 4 | BDQ69 | T |
| AA17 | PB63B | 4 | BDQ60 | C | PB72B | 4 | BDQ69 | C |
| AF18 | PB64A | 4 | BDQ60 | T | PB73A | 4 | BDQ69 | T |
| AF19 | PB64B | 4 | BDQ60 | C | PB73B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AA19 | PB65A | 4 | BDQ69 | T | PB74A | 4 | BDQ78 | T |
| W17 | PB65B | 4 | BDQ69 | C | PB74B | 4 | BDQ78 | C |
| Y19 | PB66A | 4 | BDQ69 | T | PB75A | 4 | BDQ78 | T |
| Y17 | PB66B | 4 | BDQ69 | C | PB75B | 4 | BDQ78 | C |
| AF20 | PB67A | 4 | BDQ69 | T | PB76A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AE20 | PB67B | 4 | BDQ69 | C | PB76B | 4 | BDQ78 | C |
| AA20 | PB68A | 4 | BDQ69 | T | PB77A | 4 | BDQ78 | T |
| W18 | PB68B | 4 | BDQ69 | C | PB77B | 4 | BDQ78 | C |
| AD20 | PB69A | 4 | BDQS69 | T | PB78A | 4 | BDQS78 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AE21 | PB69B | 4 | BDQ69 | C | PB78B | 4 | BDQ78 | C |
| AF21 | PB70A | 4 | BDQ69 | T | PB79A | 4 | BDQ78 | T |
| AF22 | PB70B | 4 | BDQ69 | C | PB79B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AE22 | PB74A | 4 | BDQ78 | T | PB92A | 4 | BDQ96 | T |
| AD22 | PB74B | 4 | BDQ78 | C | PB92B | 4 | BDQ96 | C |
| AF23 | PB75A | 4 | BDQ78 | T | PB93A | 4 | BDQ96 | T |
| AE23 | PB75B | 4 | BDQ78 | C | PB93B | 4 | BDQ96 | C |
| AD23 | PB76A | 4 | BDQ78 | T | PB94A | 4 | BDQ96 | T |
| AC23 | PB76B | 4 | BDQ78 | C | PB94B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AB20 | PB77A | 4 | BDQ78 | T | PB95A | 4 | BDQ96 | T |
| AC20 | PB77B | 4 | BDQ78 | C | PB95B | 4 | BDQ96 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AB21 | PB78A | 4 | BDQS78 | T | PB96A | 4 | BDQS96 | T |
| AC22 | PB78B | 4 | BDQ78 | C | PB96B | 4 | BDQ96 | C |
| W19 | PB79A | 4 | BDQ78 | T | PB97A | 4 | BDQ96 | T |
| AA21 | PB79B | 4 | BDQ78 | C | PB97B | 4 | BDQ96 | C |
| AF24 | PB80A | 4 | BDQ78 | T | PB98A | 4 | BDQ96 | T |
| AE24 | PB80B | 4 | BDQ78 | C | PB98B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y20 | PB81A | 4 | BDQ78 | T | PB99A | 4 | BDQ96 | T |
| AB22 | PB81B | 4 | BDQ78 | C | PB99B | 4 | BDQ96 | C |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| Y21 | PB82A | 4 | VREF2_4/BDQ78 | T | PB100A | 4 | VREF2_4/BDQ96 | T |
| AB23 | PB82B | 4 | VREF1_4/BDQ78 | C | PB100B | 4 | VREF1_4/BDQ96 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AD24 | CFG2 | 8 | | | CFG2 | 8 | | |
| W20 | CFG1 | 8 | | | CFG1 | 8 | | |
| AC24 | CFG0 | 8 | | | CFG0 | 8 | | |
| V19 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| AA22 | CCLK | 8 | | | CCLK | 8 | | |
| AB24 | INITN | 8 | | | INITN | 8 | | |
| AD25 | DONE | 8 | | | DONE | 8 | | |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| W21 | PR77B | 8 | WRITEN | C | PR90B | 8 | WRITEN | C |
| Y22 | PR77A | 8 | CS1N | T | PR90A | 8 | CS1N | T |
| AC25 | PR76B | 8 | CSN | C | PR89B | 8 | CSN | C |
| AB25 | PR76A | 8 | D0/SPIFASTN | T | PR89A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AD26 | PR75B | 8 | D1 | C | PR88B | 8 | D1 | C |
| AC26 | PR75A | 8 | D2 | T | PR88A | 8 | D2 | T |
| Y23 | PR74B | 8 | D3 | C | PR87B | 8 | D3 | C |
| GND | GNDIO8 | - | | | GNDIO8 | - | | |
| W22 | PR74A | 8 | D4 | T | PR87A | 8 | D4 | T |
| AA25 | PR73B | 8 | D5 | C | PR86B | 8 | D5 | C |
| AB26 | PR73A | 8 | D6 | T | PR86A | 8 | D6 | T |
| W23 | PR72B | 8 | D7/SPID0 | C | PR85B | 8 | D7/SPID0 | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| V22 | PR72A | 8 | DI/CSSPI0N | T | PR85A | 8 | DI/CSSPI0N | T |
| Y24 | PR71B | 8 | DOUT/CSON | C | PR84B | 8 | DOUT/CSON | C |
| Y25 | PR71A | 8 | BUSY/SISPI | T | PR84A | 8 | BUSY/SISPI | T |
| W24 | PR70B | 3 | RDQ67 | C | PR83B | 3 | RDQ80 | C |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| V23 | PR70A | 3 | RDQ67 | T | PR83A | 3 | RDQ80 | T |
| AA26 | PR69B | 3 | RDQ67 | C (LVDS)* | PR82B | 3 | RDQ80 | C (LVDS)* |
| Y26 | PR69A | 3 | RDQ67 | T (LVDS)* | PR82A | 3 | RDQ80 | T (LVDS)* |
| U21 | PR68B | 3 | RDQ67 | C | PR81B | 3 | RDQ80 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U19 | PR68A | 3 | RDQ67 | T | PR81A | 3 | RDQ80 | T |
| W25 | PR67B | 3 | RDQ67 | C (LVDS)* | PR80B | 3 | RDQ80 | C (LVDS)* |
| W26 | PR67A | 3 | RDQS67 | T (LVDS)* | PR80A | 3 | RDQS80 | T (LVDS)* |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| V24 | PR66B | 3 | RDQ67 | C | PR79B | 3 | RDQ80 | C |
| V25 | PR66A | 3 | RDQ67 | T | PR79A | 3 | RDQ80 | T |
| V26 | PR65B | 3 | RDQ67 | C (LVDS)* | PR78B | 3 | RDQ80 | C (LVDS)* |
| U26 | PR65A | 3 | RDQ67 | T (LVDS)* | PR78A | 3 | RDQ80 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U22 | PR64B | 3 | RLM0_GPLLC_FB_A/RDQ67 | C | PR77B | 3 | RLM0_GPLLC_FB_A/RDQ80 | C |
| U23 | PR64A | 3 | RLM0_GPLLT_FB_A/RDQ67 | T | PR77A | 3 | RLM0_GPLLT_FB_A/RDQ80 | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U24 | PR63B | 3 | RLM0_GPLLC_IN_A**/RDQ67 | C (LVDS)* | PR76B | 3 | RLM0_GPLLC_IN_A**/RDQ80 | C (LVDS)* |
| U25 | PR63A | 3 | RLM0_GPLLT_IN_A**/RDQ67 | T (LVDS)* | PR76A | 3 | RLM0_GPLLT_IN_A**/RDQ80 | T (LVDS)* |
| R20 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| P18 | VCCPLL | 3 | | | VCCPLL | - | | |
| T19 | PR61B | 3 | RLM0_GDLLC_FB_A/RDQ58 | C | PR74B | 3 | RLM0_GDLLC_FB_A/RDQ71 | C |
| U20 | PR61A | 3 | RLM0_GDLLT_FB_A/RDQ58 | T | PR74A | 3 | RLM0_GDLLT_FB_A/RDQ71 | T |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| T25 | PR60B | 3 | RLM0_GDLLC_IN_A**/RDQ58 | C (LVDS)* | PR73B | 3 | RLM0_GDLLC_IN_A**/RDQ71 | C (LVDS)* |
| T26 | PR60A | 3 | RLM0_GDLLT_IN_A**/RDQ58 | T (LVDS)* | PR73A | 3 | RLM0_GDLLT_IN_A**/RDQ71 | T (LVDS)* |
| T20 | PR59B | 3 | RDQ58 | C | PR72B | 3 | RDQ71 | C |
| T22 | PR59A | 3 | RDQ58 | T | PR72A | 3 | RDQ71 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R26 | PR58B | 3 | RDQ58 | C (LVDS)* | PR71B | 3 | RDQ71 | C (LVDS)* |
| R25 | PR58A | 3 | RDQS58 | T (LVDS)* | PR71A | 3 | RDQS71 | T (LVDS)* |
| R22 | PR57B | 3 | RDQ58 | C | PR70B | 3 | RDQ71 | C |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| T21 | PR57A | 3 | RDQ58 | T | PR70A | 3 | RDQ71 | T |
| P26 | PR56B | 3 | RDQ58 | C (LVDS)* | PR69B | 3 | RDQ71 | C (LVDS)* |
| P25 | PR56A | 3 | RDQ58 | T (LVDS)* | PR69A | 3 | RDQ71 | T (LVDS)* |
| R24 | PR55B | 3 | RDQ58 | C | PR68B | 3 | RDQ71 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R23 | PR55A | 3 | RDQ58 | T | PR68A | 3 | RDQ71 | T |
| P20 | PR54B | 3 | RDQ58 | C (LVDS)* | PR67B | 3 | RDQ71 | C (LVDS)* |
| R19 | PR54A | 3 | RDQ58 | T (LVDS)* | PR67A | 3 | RDQ71 | T (LVDS)* |
| P21 | PR53B | 3 | RDQ50 | C | PR66B | 3 | RDQ63 | C |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| P19 | PR53A | 3 | RDQ50 | T | PR66A | 3 | RDQ63 | T |
| P23 | PR52B | 3 | RDQ50 | C (LVDS)* | PR65B | 3 | RDQ63 | C (LVDS)* |
| P22 | PR52A | 3 | RDQ50 | T (LVDS)* | PR65A | 3 | RDQ63 | T (LVDS)* |
| N22 | PR51B | 3 | RDQ50 | C | PR64B | 3 | RDQ63 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R21 | PR51A | 3 | RDQ50 | T | PR64A | 3 | RDQ63 | T |
| N26 | PR50B | 3 | RDQ50 | C (LVDS)* | PR63B | 3 | RDQ63 | C (LVDS)* |
| N25 | PR50A | 3 | RDQS50 | T (LVDS)* | PR63A | 3 | RDQS63 | T (LVDS)* |
| GND | GNDIO3 | - | | | GNDIO3 | - | | |
| N19 | PR49B | 3 | RDQ50 | C | PR62B | 3 | RDQ63 | C |
| N20 | PR49A | 3 | RDQ50 | T | PR62A | 3 | RDQ63 | T |
| M26 | PR48B | 3 | RDQ50 | C (LVDS)* | PR61B | 3 | RDQ63 | C (LVDS)* |
| M25 | PR48A | 3 | RDQ50 | T (LVDS)* | PR61A | 3 | RDQ63 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| N18 | PR47B | 3 | VREF2_3/RDQ50 | C | PR60B | 3 | VREF2_3/RDQ63 | C |
| N21 | PR47A | 3 | VREF1_3/RDQ50 | T | PR60A | 3 | VREF1_3/RDQ63 | T |
| L26 | PR46B | 3 | PCLKC3_0/RDQ50 | C (LVDS)* | PR59B | 3 | PCLKC3_0/RDQ63 | C (LVDS)* |
| L25 | PR46A | 3 | PCLKT3_0/RDQ50 | T (LVDS)* | PR59A | 3 | PCLKT3_0/RDQ63 | T (LVDS)* |
| N24 | PR44B | 2 | PCLKC2_0/RDQ41 | C | PR57B | 2 | PCLKC2_0/RDQ54 | C |
| M23 | PR44A | 2 | PCLKT2_0/RDQ41 | T | PR57A | 2 | PCLKT2_0/RDQ54 | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| L21 | PR43B | 2 | RDQ41 | C (LVDS)* | PR56B | 2 | RDQ54 | C (LVDS)* |
| K22 | PR43A | 2 | RDQ41 | T (LVDS)* | PR56A | 2 | RDQ54 | T (LVDS)* |
| M24 | PR42B | 2 | RDQ41 | C | PR55B | 2 | RDQ54 | C |
| N23 | PR42A | 2 | RDQ41 | T | PR55A | 2 | RDQ54 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K26 | PR41B | 2 | RDQ41 | C (LVDS)* | PR54B | 2 | RDQ54 | C (LVDS)* |
| K25 | PR41A | 2 | RDQS41 | T (LVDS)* | PR54A | 2 | RDQS54 | T (LVDS)* |
| M20 | PR40B | 2 | RDQ41 | C | PR53B | 2 | RDQ54 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| M19 | PR40A | 2 | RDQ41 | T | PR53A | 2 | RDQ54 | T |
| L22 | PR39B | 2 | RDQ41 | C (LVDS)* | PR52B | 2 | RDQ54 | C (LVDS)* |
| M22 | PR39A | 2 | RDQ41 | T (LVDS)* | PR52A | 2 | RDQ54 | T (LVDS)* |
| K21 | PR38B | 2 | RDQ41 | C | PR51B | 2 | RDQ54 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M21 | PR38A | 2 | RDQ41 | T | PR51A | 2 | RDQ54 | T |
| K24 | PR37B | 2 | RDQ41 | C (LVDS)* | PR50B | 2 | RDQ54 | C (LVDS)* |
| J24 | PR37A | 2 | RDQ41 | T (LVDS)* | PR50A | 2 | RDQ54 | T (LVDS)* |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L20 | VCCPLL | 2 | | | NC | - | | |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| J26 | PR26B | 2 | RUM0_SPLLC_FB_A/RDQ24 | C | PR39B | 2 | RUM0_SPLLC_FB_A/RDQ37 | C |
| J25 | PR26A | 2 | RUM0_SPLLT_FB_A/RDQ24 | T | PR39A | 2 | RUM0_SPLLT_FB_A/RDQ37 | T |
| J23 | PR25B | 2 | RUM0_SPLLC_IN_A/RDQ24 | C | PR38B | 2 | RUM0_SPLLC_IN_A/RDQ37 | C |
| K23 | PR25A | 2 | RUM0_SPLLT_IN_A/RDQ24 | T | PR38A | 2 | RUM0_SPLLT_IN_A/RDQ37 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H26 | PR24B | 2 | RDQ24 | C (LVDS)* | PR37B | 2 | RDQ37 | C (LVDS)* |
| H25 | PR24A | 2 | RDQS24*** | T (LVDS)* | PR37A | 2 | RDQS37*** | T (LVDS)* |
| H24 | PR23B | 2 | RDQ24 | C | PR36B | 2 | RDQ37 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| H23 | PR23A | 2 | RDQ24 | T | PR36A | 2 | RDQ37 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G26 | PR19B | 2 | RDQ16 | C | PR32B | 2 | RDQ29 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| G25 | PR19A | 2 | RDQ16 | T | PR32A | 2 | RDQ29 | T |
| F26 | PR18B | 2 | RDQ16 | C (LVDS)* | PR31B | 2 | RDQ29 | C (LVDS)* |
| F25 | PR18A | 2 | RDQ16 | T (LVDS)* | PR31A | 2 | RDQ29 | T (LVDS)* |
| K20 | PR17B | 2 | RDQ16 | C | PR30B | 2 | RDQ29 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L19 | PR17A | 2 | RDQ16 | T | PR30A | 2 | RDQ29 | T |
| E26 | PR16B | 2 | RDQ16 | C (LVDS)* | PR29B | 2 | RDQ29 | C (LVDS)* |
| E25 | PR16A | 2 | RDQS16 | T (LVDS)* | PR29A | 2 | RDQS29 | T (LVDS)* |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| J22 | PR15B | 2 | RDQ16 | C | PR28B | 2 | RDQ29 | C |
| H22 | PR15A | 2 | RDQ16 | T | PR28A | 2 | RDQ29 | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G24 | PR14B | 2 | RDQ16 | C (LVDS)* | PR27B | 2 | RDQ29 | C (LVDS)* |
| G23 | PR14A | 2 | RDQ16 | T (LVDS)* | PR27A | 2 | RDQ29 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K19 | PR13B | 2 | RDQ16 | C | PR26B | 2 | RDQ29 | C |
| J19 | PR13A | 2 | RDQ16 | T | PR26A | 2 | RDQ29 | T |
| D26 | PR12B | 2 | RDQ16 | C (LVDS)* | PR25B | 2 | RDQ29 | C (LVDS)* |
| C26 | PR12A | 2 | RDQ16 | T (LVDS)* | PR25A | 2 | RDQ29 | T (LVDS)* |
| F22 | PR11B | 2 | RDQ8 | C | PR24B | 2 | RDQ21 | C |
| E24 | PR11A | 2 | RDQ8 | T | PR24A | 2 | RDQ21 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| D25 | PR10B | 2 | RDQ8 | C (LVDS)* | PR23B | 2 | RDQ21 | C (LVDS)* |
| C25 | PR10A | 2 | RDQ8 | T (LVDS)* | PR23A | 2 | RDQ21 | T (LVDS)* |
| D24 | PR9B | 2 | RDQ8 | C | PR22B | 2 | RDQ21 | C |
| B25 | PR9A | 2 | RDQ8 | T | PR22A | 2 | RDQ21 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H21 | PR8B | 2 | RDQ8 | C (LVDS)* | PR21B | 2 | RDQ21 | C (LVDS)* |
| G22 | PR8A | 2 | RDQS8 | T (LVDS)* | PR21A | 2 | RDQS21 | T (LVDS)* |
| B24 | PR7B | 2 | RDQ8 | C | PR20B | 2 | RDQ21 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| C24 | PR7A | 2 | RDQ8 | T | PR20A | 2 | RDQ21 | T |
| D23 | PR6B | 2 | RDQ8 | C (LVDS)* | PR19B | 2 | RDQ21 | C (LVDS)* |
| C23 | PR6A | 2 | RDQ8 | T (LVDS)* | PR19A | 2 | RDQ21 | T (LVDS)* |
| G21 | PR5B | 2 | RDQ8 | C | PR18B | 2 | RDQ21 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H20 | PR5A | 2 | RDQ8 | T | PR18A | 2 | RDQ21 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| F21 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| E23 | PT82B | 1 | VREF2_1 | C | PT100B | 1 | VREF2_1 | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D22 | PT82A | 1 | VREF1_1 | T | PT100A | 1 | VREF1_1 | T |
| G20 | PT81B | 1 | | C | PT99B | 1 | | C |
| J18 | PT81A | 1 | | T | PT99A | 1 | | T |
| F20 | PT80B | 1 | | C | PT98B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H19 | PT80A | 1 | | T | PT98A | 1 | | T |
| A24 | PT79B | 1 | | C | PT97B | 1 | | C |
| A23 | PT79A | 1 | | T | PT97A | 1 | | T |
| E21 | PT78B | 1 | | C | PT96B | 1 | | C |
| F19 | PT78A | 1 | | T | PT96A | 1 | | T |
| C22 | PT77B | 1 | | C | PT95B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E20 | PT77A | 1 | | T | PT95A | 1 | | T |
| B22 | PT76B | 1 | | C | PT94B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B23 | PT76A | 1 | | T | PT94A | 1 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C20 | PT75B | 1 | | C | PT93B | 1 | | C |
| D20 | PT75A | 1 | | T | PT93A | 1 | | T |
| A22 | PT74B | 1 | | C | PT92B | 1 | | C |
| A21 | PT74A | 1 | | T | PT92A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E19 | PT71B | 1 | | C | PT85B | 1 | | C |
| C19 | PT71A | 1 | | T | PT85A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B21 | PT70B | 1 | | C | PT79B | 1 | | C |
| B20 | PT70A | 1 | | T | PT79A | 1 | | T |
| D19 | PT69B | 1 | | C | PT78B | 1 | | C |
| B19 | PT69A | 1 | | T | PT78A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G17 | PT68B | 1 | | C | PT77B | 1 | | C |
| E18 | PT68A | 1 | | T | PT77A | 1 | | T |
| G19 | PT67B | 1 | | C | PT76B | 1 | | C |
| F17 | PT67A | 1 | | T | PT76A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A20 | PT66B | 1 | | C | PT75B | 1 | | C |
| A19 | PT66A | 1 | | T | PT75A | 1 | | T |
| E17 | PT65B | 1 | | C | PT74B | 1 | | C |
| D18 | PT65A | 1 | | T | PT74A | 1 | | T |
| B18 | PT64B | 1 | | C | PT73B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A18 | PT64A | 1 | | T | PT73A | 1 | | T |
| E16 | PT63B | 1 | | C | PT72B | 1 | | C |
| G16 | PT63A | 1 | | T | PT72A | 1 | | T |
| F16 | PT62B | 1 | | C | PT71B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H18 | PT62A | 1 | | T | PT71A | 1 | | T |
| A17 | PT61B | 1 | | C | PT70B | 1 | | C |
| B17 | PT61A | 1 | | T | PT70A | 1 | | T |
| C18 | PT60B | 1 | | C | PT69B | 1 | | C |
| B16 | PT60A | 1 | | T | PT69A | 1 | | T |
| C17 | PT59B | 1 | | C | PT68B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D17 | PT59A | 1 | | T | PT68A | 1 | | T |
| E15 | PT58B | 1 | | C | PT67B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G15 | PT58A | 1 | | T | PT67A | 1 | | T |
| A16 | PT57B | 1 | | C | PT66B | 1 | | C |
| B15 | PT57A | 1 | | T | PT66A | 1 | | T |
| D15 | PT56B | 1 | | C | PT65B | 1 | | C |
| F15 | PT56A | 1 | | T | PT65A | 1 | | T |
| A14 | PT55B | 1 | | C | PT64B | 1 | | C |
| B14 | PT55A | 1 | | T | PT64A | 1 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| C15 | PT54B | 1 | | C | PT63B | 1 | | C |
| A15 | PT54A | 1 | | T | PT63A | 1 | | T |
| A13 | PT53B | 1 | | C | PT62B | 1 | | C |
| B13 | PT53A | 1 | | T | PT62A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H17 | PT52B | 1 | | C | PT61B | 1 | | C |
| H15 | PT52A | 1 | | T | PT61A | 1 | | T |
| D13 | PT51B | 1 | | C | PT60B | 1 | | C |
| C14 | PT51A | 1 | | T | PT60A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G14 | PT50B | 1 | | C | PT59B | 1 | | C |
| E14 | PT50A | 1 | | T | PT59A | 1 | | T |
| A12 | PT49B | 1 | | C | PT58B | 1 | | C |
| B12 | PT49A | 1 | | T | PT58A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F14 | PT48B | 1 | PCLKC1_0 | C | PT57B | 1 | PCLKC1_0 | C |
| D14 | PT48A | 1 | PCLKT1_0 | T | PT57A | 1 | PCLKT1_0 | T |
| H16 | XRES | 1 | | | XRES | 1 | | |
| H14 | PT46B | 0 | PCLKC0_0 | C | PT55B | 0 | PCLKC0_0 | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| H13 | PT46A | 0 | PCLKT0_0 | T | PT55A | 0 | PCLKT0_0 | T |
| A11 | PT45B | 0 | | C | PT54B | 0 | | C |
| B11 | PT45A | 0 | | T | PT54A | 0 | | T |
| C13 | PT44B | 0 | | C | PT53B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E13 | PT44A | 0 | | T | PT53A | 0 | | T |
| D12 | PT43B | 0 | | C | PT52B | 0 | | C |
| F13 | PT43A | 0 | | T | PT52A | 0 | | T |
| A10 | PT42B | 0 | | C | PT51B | 0 | | C |
| B10 | PT42A | 0 | | T | PT51A | 0 | | T |
| C12 | PT41B | 0 | | C | PT50B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| C10 | PT41A | 0 | | T | PT50A | 0 | | T |
| G13 | PT40B | 0 | | C | PT49B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H12 | PT40A | 0 | | T | PT49A | 0 | | T |
| A9 | PT39B | 0 | | C | PT48B | 0 | | C |
| B9 | PT39A | 0 | | T | PT48A | 0 | | T |
| E12 | PT38B | 0 | | C | PT47B | 0 | | C |
| G12 | PT38A | 0 | | T | PT47A | 0 | | T |
| A8 | PT37B | 0 | | C | PT46B | 0 | | C |
| B8 | PT37A | 0 | | T | PT46A | 0 | | T |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| E11 | PT36B | 0 | | C | PT45B | 0 | | C |
| C9 | PT36A | 0 | | T | PT45A | 0 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A7 | PT35B | 0 | | C | PT44B | 0 | | C |
| B7 | PT35A | 0 | | T | PT44A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F12 | PT34B | 0 | | C | PT43B | 0 | | C |
| D10 | PT34A | 0 | | T | PT43A | 0 | | T |
| H11 | PT33B | 0 | | C | PT42B | 0 | | C |
| G11 | PT33A | 0 | | T | PT42A | 0 | | T |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| A6 | PT32B | 0 | | C | PT41B | 0 | | C |
| B6 | PT32A | 0 | | T | PT41A | 0 | | T |
| D8 | PT31B | 0 | | C | PT40B | 0 | | C |
| C8 | PT31A | 0 | | T | PT40A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F11 | PT30B | 0 | | C | PT39B | 0 | | C |
| E10 | PT30A | 0 | | T | PT39A | 0 | | T |
| E9 | PT29B | 0 | | C | PT38B | 0 | | C |
| D9 | PT29A | 0 | | T | PT38A | 0 | | T |
| G10 | PT28B | 0 | | C | PT37B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| H10 | PT28A | 0 | | T | PT37A | 0 | | T |
| A5 | PT27B | 0 | | C | PT36B | 0 | | C |
| B5 | PT27A | 0 | | T | PT36A | 0 | | T |
| C7 | PT26B | 0 | | C | PT35B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D7 | PT26A | 0 | | T | PT35A | 0 | | T |
| E8 | PT25B | 0 | | C | PT34B | 0 | | C |
| F10 | PT25A | 0 | | T | PT34A | 0 | | T |
| F8 | PT24B | 0 | | C | PT33B | 0 | | C |
| H9 | PT24A | 0 | | T | PT33A | 0 | | T |
| C5 | PT23B | 0 | | C | PT32B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| D5 | PT23A | 0 | | T | PT32A | 0 | | T |
| B4 | PT22B | 0 | | | PT31B | 0 | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C4 | PT10B | 0 | | C | PT10B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| C3 | PT10A | 0 | | T | PT10A | 0 | | T |
| A4 | PT9B | 0 | | C | PT9B | 0 | | C |
| A3 | PT9A | 0 | | T | PT9A | 0 | | T |
| B3 | PT8B | 0 | | C | PT8B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B2 | PT8A | 0 | | T | PT8A | 0 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D4 | PT7B | 0 | | C | PT7B | 0 | | C |
| D3 | PT7A | 0 | | T | PT7A | 0 | | T |
| C2 | PT6B | 0 | | C | PT6B | 0 | | C |
| C1 | PT6A | 0 | | T | PT6A | 0 | | T |
| G8 | PT5B | 0 | | C | PT5B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| G7 | PT5A | 0 | | T | PT5A | 0 | | T |
| E7 | PT4B | 0 | | C | PT4B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F7 | PT4A | 0 | | T | PT4A | 0 | | T |
| E6 | PT3B | 0 | | C | PT3B | 0 | | C |
| E5 | PT3A | 0 | | T | PT3A | 0 | | T |
| G6 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| G5 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |
| L12 | VCC | - | | | VCC | - | | |
| L13 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L15 | VCC | - | | | VCC | - | | |
| M11 | VCC | - | | | VCC | - | | |
| M12 | VCC | - | | | VCC | - | | |
| M15 | VCC | - | | | VCC | - | | |
| M16 | VCC | - | | | VCC | - | | |
| N11 | VCC | - | | | VCC | - | | |
| N16 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P16 | VCC | - | | | VCC | - | | |
| R11 | VCC | - | | | VCC | - | | |
| R12 | VCC | - | | | VCC | - | | |
| R15 | VCC | - | | | VCC | - | | |
| R16 | VCC | - | | | VCC | - | | |
| T12 | VCC | - | | | VCC | - | | |
| T13 | VCC | - | | | VCC | - | | |
| T14 | VCC | - | | | VCC | - | | |
| T15 | VCC | - | | | VCC | - | | |
| D11 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D6 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D21 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J20 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M17 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| AA23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R17 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V20 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AC16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC21 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC6 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| U12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R9 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| F4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AE25 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| V18 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| J10 | VCCAUX | - | | | VCCAUX | - | | |
| J11 | VCCAUX | - | | | VCCAUX | - | | |
| J16 | VCCAUX | - | | | VCCAUX | - | | |
| J17 | VCCAUX | - | | | VCCAUX | - | | |
| K18 | VCCAUX | - | | | VCCAUX | - | | |
| K9 | VCCAUX | - | | | VCCAUX | - | | |
| L18 | VCCAUX | - | | | VCCAUX | - | | |
| L9 | VCCAUX | - | | | VCCAUX | - | | |
| T18 | VCCAUX | - | | | VCCAUX | - | | |
| T9 | VCCAUX | - | | | VCCAUX | - | | |
| U18 | VCCAUX | - | | | VCCAUX | - | | |
| U9 | VCCAUX | - | | | VCCAUX | - | | |
| V10 | VCCAUX | - | | | VCCAUX | - | | |
| V11 | VCCAUX | - | | | VCCAUX | - | | |
| V16 | VCCAUX | - | | | VCCAUX | - | | |
| V17 | VCCAUX | - | | | VCCAUX | - | | |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A2 | GND | - | | | GND | - | | |
| A25 | GND | - | | | GND | - | | |
| AA18 | GND | - | | | GND | - | | |
| AA24 | GND | - | | | GND | - | | |
| AA3 | GND | - | | | GND | - | | |
| AA9 | GND | - | | | GND | - | | |
| AD11 | GND | - | | | GND | - | | |
| AD16 | GND | - | | | GND | - | | |
| AD21 | GND | - | | | GND | - | | |
| AD6 | GND | - | | | GND | - | | |
| AE1 | GND | - | | | GND | - | | |
| AE26 | GND | - | | | GND | - | | |
| AF2 | GND | - | | | GND | - | | |
| AF25 | GND | - | | | GND | - | | |
| B1 | GND | - | | | GND | - | | |
| B26 | GND | - | | | GND | - | | |
| C11 | GND | - | | | GND | - | | |
| C16 | GND | - | | | GND | - | | |
| C21 | GND | - | | | GND | - | | |
| C6 | GND | - | | | GND | - | | |
| F18 | GND | - | | | GND | - | | |
| F24 | GND | - | | | GND | - | | |
| F3 | GND | - | | | GND | - | | |
| F9 | GND | - | | | GND | - | | |
| J13 | GND | - | | | GND | - | | |
| J14 | GND | - | | | GND | - | | |
| J21 | GND | - | | | GND | - | | |
| J6 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K14 | GND | - | | | GND | - | | |
| K16 | GND | - | | | GND | - | | |
| K17 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |
| L16 | GND | - | | | GND | - | | |
| L17 | GND | - | | | GND | - | | |
| L24 | GND | - | | | GND | - | | |
| L3 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M14 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N14 | GND | - | | | GND | - | | |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N15 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| P10 | GND | - | | | GND | - | | |
| P12 | GND | - | | | GND | - | | |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T24 | GND | - | | | GND | - | | |
| T3 | GND | - | | | GND | - | | |
| U10 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| V13 | GND | - | | | GND | - | | |
| V14 | GND | - | | | GND | - | | |
| V21 | GND | - | | | GND | - | | |
| V6 | GND | - | | | GND | - | | |
| M3 | NC | - | | | NC | - | | |
| N6 | NC | - | | | NC | - | | |
| P24 | NC | - | | | NC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| VCCIO | VCCIO7 | 7 | | |
| F4 | PL2A | 7 | VREF2_7 | T (LVDS)* |
| F3 | PL2B | 7 | VREF1_7 | C (LVDS)* |
| H4 | PL3A | 7 | | T |
| G5 | PL3B | 7 | | C |
| GND | GNDIO7 | - | | |
| D2 | PL4A | 7 | | T (LVDS)* |
| D1 | PL4B | 7 | | C (LVDS)* |
| E2 | PL5A | 7 | | T |
| VCCIO | VCCIO7 | 7 | | |
| E1 | PL5B | 7 | | C |
| GND | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| F1 | PL14A | 7 | LUM1_SPLLT_IN_A/LDQ12 | T (LVDS)* |
| F2 | PL14B | 7 | LUM1_SPLLC_IN_A/LDQ12 | C (LVDS)* |
| G1 | PL15A | 7 | LUM1_SPLLT_FB_A/LDQ12 | T |
| G2 | PL15B | 7 | LUM1_SPLLC_FB_A/LDQ12 | C |
| GND | GNDIO7 | - | | |
| H8 | PL18A | 7 | LDQ21 | T |
| H6 | PL18B | 7 | LDQ21 | C |
| VCCIO | VCCIO7 | 7 | | |
| G4 | PL19A | 7 | LDQ21 | T (LVDS)* |
| G3 | PL19B | 7 | LDQ21 | C (LVDS)* |
| H7 | PL20A | 7 | LDQ21 | T |
| H5 | PL20B | 7 | LDQ21 | C |
| GND | GNDIO7 | - | | |
| H2 | PL21A | 7 | LDQS21 | T (LVDS)* |
| H1 | PL21B | 7 | LDQ21 | C (LVDS)* |
| J6 | PL22A | 7 | LDQ21 | T |
| VCCIO | VCCIO7 | 7 | | |
| J8 | PL22B | 7 | LDQ21 | C |
| J2 | PL23A | 7 | LDQ21 | T (LVDS)* |
| J1 | PL23B | 7 | LDQ21 | C (LVDS)* |
| J5 | PL24A | 7 | LDQ21 | T |
| GND | GNDIO7 | - | | |
| J7 | PL24B | 7 | LDQ21 | C |
| J4 | PL25A | 7 | LDQ29 | T (LVDS)* |
| J3 | PL25B | 7 | LDQ29 | C (LVDS)* |
| K6 | PL26A | 7 | LDQ29 | T |
| K8 | PL26B | 7 | LDQ29 | C |
| VCCIO | VCCIO7 | 7 | | |
| K2 | PL27A | 7 | LDQ29 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| K1 | PL27B | 7 | LDQ29 | C (LVDS)* |
| K5 | PL28A | 7 | LDQ29 | T |
| K7 | PL28B | 7 | LDQ29 | C |
| GND | GNDIO7 | - | | |
| K4 | PL29A | 7 | LDQS29 | T (LVDS)* |
| K3 | PL29B | 7 | LDQ29 | C (LVDS)* |
| L8 | PL30A | 7 | LDQ29 | T |
| VCCIO | VCCIO7 | 7 | | |
| L6 | PL30B | 7 | LDQ29 | C |
| L2 | PL31A | 7 | LDQ29 | T (LVDS)* |
| L1 | PL31B | 7 | LDQ29 | C (LVDS)* |
| L7 | PL32A | 7 | LDQ29 | T |
| GND | GNDIO7 | - | | |
| L5 | PL32B | 7 | LDQ29 | C |
| L4 | PL33A | 7 | LDQ37 | T (LVDS)* |
| L3 | PL33B | 7 | LDQ37 | C (LVDS)* |
| M8 | PL34A | 7 | LDQ37 | T |
| M6 | PL34B | 7 | LDQ37 | C |
| VCCIO | VCCIO7 | 7 | | |
| M2 | PL35A | 7 | LDQ37 | T (LVDS)* |
| M1 | PL35B | 7 | LDQ37 | C (LVDS)* |
| M7 | PL36A | 7 | LDQ37 | T |
| M5 | PL36B | 7 | LDQ37 | C |
| GND | GNDIO7 | - | | |
| M4 | PL37A | 7 | LDQS37 | T (LVDS)* |
| M3 | PL37B | 7 | LDQ37 | C (LVDS)* |
| N6 | PL38A | 7 | LUM0_SPLLT_IN_A/LDQ37 | T |
| VCCIO | VCCIO7 | 7 | | |
| N8 | PL38B | 7 | LUM0_SPLLC_IN_A/LDQ37 | C |
| N5 | PL39A | 7 | LUM0_SPLLT_FB_A/LDQ37 | T |
| N7 | PL39B | 7 | LUM0_SPLLC_FB_A/LDQ37 | C |
| GND | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| T9 | PL50A | 7 | LDQ54 | |
| R9 | PL51A | 7 | LDQ54 | T |
| P7 | PL51B | 7 | LDQ54 | C |
| VCCIO | VCCIO7 | 7 | | |
| N2 | PL52A | 7 | LDQ54 | T (LVDS)* |
| N1 | PL52B | 7 | LDQ54 | C (LVDS)* |
| P6 | PL53A | 7 | LDQ54 | T |
| P5 | PL53B | 7 | LDQ54 | C |
| GND | GNDIO7 | - | | |
| P4 | PL54A | 7 | LDQS54 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| P3 | PL54B | 7 | LDQ54 | C (LVDS)* |
| R6 | PL55A | 7 | LDQ54 | T |
| VCCIO | VCCIO7 | 7 | | |
| R8 | PL55B | 7 | LDQ54 | C |
| P2 | PL56A | 7 | LDQ54 | T (LVDS)* |
| P1 | PL56B | 7 | LDQ54 | C (LVDS)* |
| R5 | PL57A | 7 | PCLKT7_0/LDQ54 | T |
| GND | GNDIO7 | - | | |
| R7 | PL57B | 7 | PCLKC7_0/LDQ54 | C |
| R4 | PL59A | 6 | PCLKT6_0/LDQ63 | T (LVDS)* |
| R3 | PL59B | 6 | PCLKC6_0/LDQ63 | C (LVDS)* |
| T5 | PL60A | 6 | VREF2_6/LDQ63 | T |
| T7 | PL60B | 6 | VREF1_6/LDQ63 | C |
| T3 | PL61A | 6 | LDQ63 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| T4 | PL61B | 6 | LDQ63 | C (LVDS)* |
| T6 | PL62A | 6 | LDQ63 | T |
| T8 | PL62B | 6 | LDQ63 | C |
| T2 | PL63A | 6 | LDQS63 | T (LVDS)* |
| GND | GNDIO6 | - | | |
| T1 | PL63B | 6 | LDQ63 | C (LVDS)* |
| U7 | PL64A | 6 | LDQ63 | T |
| U5 | PL64B | 6 | LDQ63 | C |
| VCCIO | VCCIO6 | 6 | | |
| U4 | PL65A | 6 | LDQ63 | T (LVDS)* |
| U3 | PL65B | 6 | LDQ63 | C (LVDS)* |
| U8 | PL66A | 6 | LDQ63 | T |
| U6 | PL66B | 6 | LDQ63 | C |
| GND | GNDIO6 | - | | |
| U2 | PL67A | 6 | LDQ71 | T (LVDS)* |
| U1 | PL67B | 6 | LDQ71 | C (LVDS)* |
| V7 | PL68A | 6 | LDQ71 | T |
| V5 | PL68B | 6 | LDQ71 | C |
| VCCIO | VCCIO6 | 6 | | |
| V2 | PL69A | 6 | LDQ71 | T (LVDS)* |
| V1 | PL69B | 6 | LDQ71 | C (LVDS)* |
| V8 | PL70A | 6 | LDQ71 | T |
| V6 | PL70B | 6 | LDQ71 | C |
| GND | GNDIO6 | - | | |
| W1 | PL71A | 6 | LDQS71 | T (LVDS)* |
| W2 | PL71B | 6 | LDQ71 | C (LVDS)* |
| W5 | PL72A | 6 | LDQ71 | T |
| VCCIO | VCCIO6 | 6 | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| W7 | PL72B | 6 | LDQ71 | C |
| W4 | PL73A | 6 | LLM0_GDLLT_IN_A**/LDQ71 | T (LVDS)* |
| W3 | PL73B | 6 | LLM0_GDLLC_IN_A**/LDQ71 | C (LVDS)* |
| W6 | PL74A | 6 | LLM0_GDLLT_FB_A/LDQ71 | T |
| GND | GNDIO6 | - | | |
| W8 | PL74B | 6 | LLM0_GDLLC_FB_D/LDQ71 | C |
| Y8 | LLM0_PLLCAP | 6 | | |
| Y1 | PL76A | 6 | LLM0_GPLLT_IN_A**/LDQ80 | T (LVDS)* |
| Y2 | PL76B | 6 | LLM0_GPLLC_IN_A**/LDQ80 | C (LVDS)* |
| Y5 | PL77A | 6 | LLM0_GPLLT_FB_A/LDQ80 | T |
| Y6 | PL77B | 6 | LLM0_GPLLC_FB_A/LDQ80 | C |
| Y4 | PL78A | 6 | LDQ80 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| Y3 | PL78B | 6 | LDQ80 | C (LVDS)* |
| AA6 | PL79A | 6 | LDQ80 | T |
| AA8 | PL79B | 6 | LDQ80 | C |
| AA2 | PL80A | 6 | LDQS80 | T (LVDS)* |
| GND | GNDIO6 | - | | |
| AA1 | PL80B | 6 | LDQ80 | C (LVDS)* |
| AA7 | PL81A | 6 | LDQ80 | T |
| AA5 | PL81B | 6 | LDQ80 | C |
| VCCIO | VCCIO6 | 6 | | |
| AA4 | PL82A | 6 | LDQ80 | T (LVDS)* |
| AA3 | PL82B | 6 | LDQ80 | C (LVDS)* |
| AB7 | PL83A | 6 | LDQ80 | T |
| AB5 | PL83B | 6 | LDQ80 | C |
| GND | GNDIO6 | - | | |
| AB2 | PL84A | 6 | LDQ88 | T (LVDS)* |
| AB1 | PL84B | 6 | LDQ88 | C (LVDS)* |
| AB8 | PL85A | 6 | LDQ88 | T |
| AB6 | PL85B | 6 | LDQ88 | C |
| VCCIO | VCCIO6 | 6 | | |
| AB4 | PL86A | 6 | LDQ88 | T (LVDS)* |
| AB3 | PL86B | 6 | LDQ88 | C (LVDS)* |
| AC7 | PL87A | 6 | LDQ88 | T |
| AC5 | PL87B | 6 | LDQ88 | C |
| GND | GNDIO6 | - | | |
| AC2 | PL88A | 6 | LDQS88 | T (LVDS)* |
| AC1 | PL88B | 6 | LDQ88 | C (LVDS)* |
| AC6 | PL89A | 6 | LDQ88 | T |
| VCCIO | VCCIO6 | 6 | | |
| AD6 | PL89B | 6 | LDQ88 | C |
| AD1 | PL90A | 6 | LDQ88 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AD2 | PL90B | 6 | LDQ88 | C (LVDS)* |
| AD7 | PL91A | 6 | LDQ88 | T |
| GND | GNDIO6 | - | | |
| AB9 | PL91B | 6 | LDQ88 | C |
| AD5 | TCK | - | | |
| AE7 | TDI | - | | |
| AD4 | TMS | - | | |
| AA9 | TDO | - | | |
| AD3 | VCCJ | - | | |
| AC8 | PB2A | 5 | VREF2_5/BDQ6 | T |
| AE8 | PB2B | 5 | VREF1_5/BDQ6 | C |
| AD8 | PB3A | 5 | BDQ6 | T |
| AF8 | PB3B | 5 | BDQ6 | C |
| AG7 | PB4A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | |
| AH7 | PB4B | 5 | BDQ6 | C |
| AC9 | PB5A | 5 | BDQ6 | T |
| AE9 | PB5B | 5 | BDQ6 | C |
| AD9 | PB6A | 5 | BDQS6 | T |
| GND | GNDIO5 | - | | |
| AF9 | PB6B | 5 | BDQ6 | C |
| AB10 | PB7A | 5 | BDQ6 | T |
| AA10 | PB7B | 5 | BDQ6 | C |
| AJ7 | PB8A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | |
| AK7 | PB8B | 5 | BDQ6 | C |
| AC10 | PB9A | 5 | BDQ6 | T |
| AE10 | PB9B | 5 | BDQ6 | C |
| AJ8 | PB10A | 5 | BDQ6 | T |
| GND | GNDIO5 | - | | |
| AK8 | PB10B | 5 | BDQ6 | C |
| AF6 | PB11A | 5 | BDQ15 | T |
| AF7 | PB11B | 5 | BDQ15 | C |
| AG5 | PB12A | 5 | BDQ15 | T |
| AH5 | PB12B | 5 | BDQ15 | C |
| AG6 | PB13A | 5 | BDQ15 | T |
| AH6 | PB13B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | |
| AJ4 | PB14A | 5 | BDQ15 | T |
| AK4 | PB14B | 5 | BDQ15 | C |
| GND | GNDIO5 | - | | |
| AJ5 | PB15A | 5 | BDQS15 | T |
| AK5 | PB15B | 5 | BDQ15 | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| AJ6 | PB16A | 5 | BDQ15 | T |
| AK6 | PB16B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | |
| GND | GNDIO5 | - | | |
| AD10 | PB29A | 5 | BDQ33 | T |
| AF10 | PB29B | 5 | BDQ33 | C |
| AC11 | PB30A | 5 | BDQ33 | T |
| AD11 | PB30B | 5 | BDQ33 | C |
| AG9 | PB31A | 5 | BDQ33 | T |
| AH9 | PB31B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 99 | | |
| AE11 | PB32A | 5 | BDQ33 | T |
| AG10 | PB32B | 5 | BDQ33 | C |
| GND | GNDIO5 | - | | |
| AJ9 | PB33A | 5 | BDQS33 | T |
| AK9 | PB33B | 5 | BDQ33 | C |
| AF11 | PB34A | 5 | BDQ33 | T |
| AH10 | PB34B | 5 | BDQ33 | C |
| AC12 | PB35A | 5 | BDQ33 | T |
| AE12 | PB35B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | |
| AD12 | PB36A | 5 | BDQ33 | T |
| AF12 | PB36B | 5 | BDQ33 | C |
| AJ10 | PB37A | 5 | BDQ33 | T |
| AK10 | PB37B | 5 | BDQ33 | C |
| GND | GNDIO5 | - | | |
| AG11 | PB38A | 5 | BDQ42 | T |
| AH11 | PB38B | 5 | BDQ42 | C |
| AE13 | PB39A | 5 | BDQ42 | T |
| AC13 | PB39B | 5 | BDQ42 | C |
| AF13 | PB40A | 5 | BDQ42 | T |
| VCCIO | VCCIO5 | 5 | | |
| AD13 | PB40B | 5 | BDQ42 | C |
| AJ11 | PB41A | 5 | BDQ42 | T |
| AK11 | PB41B | 5 | BDQ42 | C |
| AD14 | PB42A | 5 | BDQS42 | T |
| GND | GNDIO5 | - | | |
| AC14 | PB42B | 5 | BDQ42 | C |
| AG12 | PB43A | 5 | BDQ42 | T |
| AE14 | PB43B | 5 | BDQ42 | C |
| AJ12 | PB44A | 5 | BDQ42 | T |
| VCCIO | VCCIO5 | 5 | | |
| AK12 | PB44B | 5 | BDQ42 | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AH12 | PB45A | 5 | BDQ42 | T |
| AF14 | PB45B | 5 | BDQ42 | C |
| AJ13 | PB46A | 5 | BDQ42 | T |
| GND | GNDIO5 | - | | |
| AK13 | PB46B | 5 | BDQ42 | C |
| AB15 | PB47A | 5 | BDQ51 | T |
| AD15 | PB47B | 5 | BDQ51 | C |
| AE15 | PB48A | 5 | BDQ51 | T |
| AF15 | PB48B | 5 | BDQ51 | C |
| AG15 | PB49A | 5 | BDQ51 | T |
| AG14 | PB49B | 5 | BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | |
| AH15 | PB50A | 5 | BDQ51 | T |
| AH14 | PB50B | 5 | BDQ51 | C |
| GND | GNDIO5 | - | | |
| AJ14 | PB51A | 5 | BDQS51 | T |
| AK14 | PB51B | 5 | BDQ51 | C |
| AD16 | PB52A | 5 | BDQ51 | T |
| AF16 | PB52B | 5 | BDQ51 | C |
| AJ15 | PB53A | 5 | PCLKT5_0/BDQ51 | T |
| AK15 | PB53B | 5 | PCLKC5_0/BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | |
| GND | GNDIO5 | - | | |
| AE16 | PB58A | 4 | PCLKT4_0/BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | |
| AC15 | PB58B | 4 | PCLKC4_0/BDQ60 | C |
| AJ16 | PB59A | 4 | BDQ60 | T |
| AK16 | PB59B | 4 | BDQ60 | C |
| AC16 | PB60A | 4 | BDQS60 | T |
| GND | GNDIO4 | - | | |
| AB16 | PB60B | 4 | BDQ60 | C |
| AH17 | PB61A | 4 | BDQ60 | T |
| AG17 | PB61B | 4 | BDQ60 | C |
| AF17 | PB62A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | |
| AD17 | PB62B | 4 | BDQ60 | C |
| AE17 | PB63A | 4 | BDQ60 | T |
| AC17 | PB63B | 4 | BDQ60 | C |
| AJ17 | PB64A | 4 | BDQ60 | T |
| GND | GNDIO4 | - | | |
| AK17 | PB64B | 4 | BDQ60 | C |
| AK18 | PB65A | 4 | BDQ69 | T |
| AJ18 | PB65B | 4 | BDQ69 | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AD18 | PB66A | 4 | BDQ69 | T |
| AF18 | PB66B | 4 | BDQ69 | C |
| AC18 | PB67A | 4 | BDQ69 | T |
| AE18 | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | |
| AG19 | PB68A | 4 | BDQ69 | T |
| AH19 | PB68B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | |
| AE19 | PB69A | 4 | BDQS69 | T |
| AF19 | PB69B | 4 | BDQ69 | C |
| AC19 | PB70A | 4 | BDQ69 | T |
| AD19 | PB70B | 4 | BDQ69 | C |
| AJ19 | PB71A | 4 | BDQ69 | T |
| AK19 | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | |
| AF20 | PB72A | 4 | BDQ69 | T |
| AH20 | PB72B | 4 | BDQ69 | C |
| AE20 | PB73A | 4 | BDQ69 | T |
| AG20 | PB73B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | |
| AD20 | PB74A | 4 | BDQ78 | T |
| AC20 | PB74B | 4 | BDQ78 | C |
| AH21 | PB75A | 4 | BDQ78 | T |
| AF21 | PB75B | 4 | BDQ78 | C |
| AJ20 | PB76A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK20 | PB76B | 4 | BDQ78 | C |
| AG21 | PB77A | 4 | BDQ78 | T |
| AE21 | PB77B | 4 | BDQ78 | C |
| AD21 | PB78A | 4 | BDQS78 | T |
| GND | GNDIO4 | - | | |
| AC21 | PB78B | 4 | BDQ78 | C |
| AD22 | PB79A | 4 | BDQ78 | T |
| AB21 | PB79B | 4 | BDQ78 | C |
| AJ21 | PB80A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK21 | PB80B | 4 | BDQ78 | C |
| GND | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | |
| AJ25 | PB87A | 4 | BDQS87*** | T |
| AK24 | PB87B | 4 | BDQ87 | C |
| AJ24 | PB88A | 4 | BDQ87 | T |
| AK25 | PB88B | 4 | BDQ87 | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AH24 | PB89A | 4 | BDQ87 | T |
| AH25 | PB89B | 4 | BDQ87 | C |
| VCCIO | VCCIO4 | 4 | | |
| AJ26 | PB90A | 4 | BDQ87 | T |
| AK26 | PB90B | 4 | BDQ87 | C |
| AF25 | PB91A | 4 | BDQ87 | T |
| AG25 | PB91B | 4 | BDQ87 | C |
| GND | GNDIO4 | - | | |
| AK22 | PB92A | 4 | BDQ96 | T |
| AJ22 | PB92B | 4 | BDQ96 | C |
| AE22 | PB93A | 4 | BDQ96 | T |
| AF22 | PB93B | 4 | BDQ96 | C |
| AG22 | PB94A | 4 | BDQ96 | T |
| VCCIO | VCCIO4 | 4 | | |
| AH22 | PB94B | 4 | BDQ96 | C |
| AG24 | PB95A | 4 | BDQ96 | T |
| AG23 | PB95B | 4 | BDQ96 | C |
| AE23 | PB96A | 4 | BDQS96 | |
| GND | GNDIO4 | - | | |
| AC22 | PB97A | 4 | BDQ96 | |
| AJ23 | PB98A | 4 | BDQ96 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK23 | PB98B | 4 | BDQ96 | C |
| AD24 | PB99A | 4 | BDQ96 | T |
| AF24 | PB99B | 4 | BDQ96 | C |
| AC23 | PB100A | 4 | VREF2_4/BDQ96 | T |
| GND | GNDIO4 | - | | |
| AE24 | PB100B | 4 | VREF1_4/BDQ96 | C |
| AE25 | CFG2 | 8 | | |
| AB22 | CFG1 | 8 | | |
| AE26 | CFG0 | 8 | | |
| AA22 | PROGRAMN | 8 | | |
| AD25 | CCLK | 8 | | |
| AD26 | INITN | 8 | | |
| AC24 | DONE | 8 | | |
| GND | GNDIO4 | - | | |
| AC25 | PR90B | 8 | WRITEN | C |
| AE27 | PR90A | 8 | CS1N | T |
| AC26 | PR89B | 8 | CSN | C |
| AE28 | PR89A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | |
| AD27 | PR88B | 8 | D1 | C |
| AD28 | PR88A | 8 | D2 | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AB24 | PR87B | 8 | D3 | C |
| GND | GNDIO4 | - | | |
| AB23 | PR87A | 8 | D4 | T |
| AB25 | PR86B | 8 | D5 | C |
| AB26 | PR86A | 8 | D6 | T |
| AC27 | PR85B | 8 | D7/SPID0 | C |
| VCCIO | VCCIO8 | 8 | | |
| AB27 | PR85A | 8 | DI/CSSPI0N | T |
| AD29 | PR84B | 8 | DOUT/CSON | C |
| AD30 | PR84A | 8 | BUSY/SISPI | T |
| AA25 | PR83B | 3 | RDQ80 | C |
| GND | GNDIO3 | - | | |
| AA23 | PR83A | 3 | RDQ80 | T |
| AC29 | PR82B | 3 | RDQ80 | C (LVDS)* |
| AC30 | PR82A | 3 | RDQ80 | T (LVDS)* |
| AA26 | PR81B | 3 | RDQ80 | C |
| VCCIO | VCCIO3 | 3 | | |
| AA24 | PR81A | 3 | RDQ80 | T |
| AB29 | PR80B | 3 | RDQ80 | C (LVDS)* |
| AB30 | PR80A | 3 | RDQS80 | T (LVDS)* |
| GND | GNDIO3 | - | | |
| Y23 | PR79B | 3 | RDQ80 | C |
| Y25 | PR79A | 3 | RDQ80 | T |
| AA27 | PR78B | 3 | RDQ80 | C (LVDS)* |
| AA28 | PR78A | 3 | RDQ80 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| Y24 | PR77B | 3 | RLM0_GPLLC_FB_A/RDQ80 | C |
| Y26 | PR77A | 3 | RLM0_GPLLT_FB_A/RDQ80 | T |
| AA29 | PR76B | 3 | RLM0_GPLLC_IN_A**/RDQ80 | C (LVDS)* |
| AA30 | PR76A | 3 | RLM0_GPLLT_IN_A**/RDQ80 | T (LVDS)* |
| R22 | RLM0_PLLCAP | 3 | | |
| W23 | PR74B | 3 | RLM0_GDLLC_FB_A/RDQ71 | C |
| W25 | PR74A | 3 | RLM0_GDLLT_FB_A/RDQ71 | T |
| GND | GNDIO3 | - | | |
| Y27 | PR73B | 3 | RLM0_GDLLC_IN_A**/RDQ71 | C (LVDS)* |
| Y28 | PR73A | 3 | RLM0_GDLLT_IN_A**/RDQ71 | T (LVDS)* |
| W24 | PR72B | 3 | RDQ71 | C |
| W26 | PR72A | 3 | RDQ71 | T |
| VCCIO | VCCIO3 | 3 | | |
| Y29 | PR71B | 3 | RDQ71 | C (LVDS)* |
| Y30 | PR71A | 3 | RDQS71 | T (LVDS)* |
| V25 | PR70B | 3 | RDQ71 | C |
| GND | GNDIO3 | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| V23 | PR70A | 3 | RDQ71 | T |
| W27 | PR69B | 3 | RDQ71 | C (LVDS)* |
| W28 | PR69A | 3 | RDQ71 | T (LVDS)* |
| V26 | PR68B | 3 | RDQ71 | C |
| VCCIO | VCCIO3 | 3 | | |
| V24 | PR68A | 3 | RDQ71 | T |
| W29 | PR67B | 3 | RDQ71 | C (LVDS)* |
| W30 | PR67A | 3 | RDQ71 | T (LVDS)* |
| U25 | PR66B | 3 | RDQ63 | C |
| GND | GNDIO3 | - | | |
| U23 | PR66A | 3 | RDQ63 | T |
| V29 | PR65B | 3 | RDQ63 | C (LVDS)* |
| V30 | PR65A | 3 | RDQ63 | T (LVDS)* |
| U26 | PR64B | 3 | RDQ63 | C |
| VCCIO | VCCIO3 | 3 | | |
| U24 | PR64A | 3 | RDQ63 | T |
| U27 | PR63B | 3 | RDQ63 | C (LVDS)* |
| U28 | PR63A | 3 | RDQS63 | T (LVDS)* |
| GND | GNDIO3 | - | | |
| T23 | PR62B | 3 | RDQ63 | C |
| T25 | PR62A | 3 | RDQ63 | T |
| U29 | PR61B | 3 | RDQ63 | C (LVDS)* |
| U30 | PR61A | 3 | RDQ63 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| T24 | PR60B | 3 | VREF2_3/RDQ63 | C |
| T26 | PR60A | 3 | VREF1_3/RDQ63 | T |
| T27 | PR59B | 3 | PCLKC3_0/RDQ63 | C (LVDS)* |
| T28 | PR59A | 3 | PCLKT3_0/RDQ63 | T (LVDS)* |
| R24 | PR57B | 2 | PCLKC2_0/RDQ54 | C |
| R26 | PR57A | 2 | PCLKT2_0/RDQ54 | T |
| GND | GNDIO2 | - | | |
| T29 | PR56B | 2 | RDQ54 | C (LVDS)* |
| T30 | PR56A | 2 | RDQ54 | T (LVDS)* |
| R23 | PR55B | 2 | RDQ54 | C |
| R25 | PR55A | 2 | RDQ54 | T |
| VCCIO | VCCIO2 | 2 | | |
| R27 | PR54B | 2 | RDQ54 | C (LVDS)* |
| R28 | PR54A | 2 | RDQS54 | T (LVDS)* |
| P26 | PR53B | 2 | RDQ54 | C |
| GND | GNDIO2 | - | | |
| P24 | PR53A | 2 | RDQ54 | T |
| R29 | PR52B | 2 | RDQ54 | C (LVDS)* |
| R30 | PR52A | 2 | RDQ54 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| P25 | PR51B | 2 | RDQ54 | C |
| VCCIO | VCCIO2 | 2 | | |
| P23 | PR51A | 2 | RDQ54 | T |
| P27 | PR50B | 2 | RDQ54 | C (LVDS)* |
| P28 | PR50A | 2 | RDQ54 | T (LVDS)* |
| GND | GNDIO2 | - | | |
| VCCIO | VCCIO2 | 2 | | |
| N24 | PR39B | 2 | RUM0_SPLLC_FB_A/RDQ37 | C |
| N26 | PR39A | 2 | RUM0_SPLLT_FB_A/RDQ37 | T |
| N23 | PR38B | 2 | RUM0_SPLLC_IN_A/RDQ37 | C |
| N25 | PR38A | 2 | RUM0_SPLLT_IN_A/RDQ37 | T |
| VCCIO | VCCIO2 | 2 | | |
| P29 | PR37B | 2 | RDQ37 | C (LVDS)* |
| P30 | PR37A | 2 | RDQS37 | T (LVDS)* |
| M26 | PR36B | 2 | RDQ37 | C |
| GND | GNDIO2 | - | | |
| M24 | PR36A | 2 | RDQ37 | T |
| N29 | PR35B | 2 | RDQ37 | C (LVDS)* |
| N30 | PR35A | 2 | RDQ37 | T (LVDS)* |
| M25 | PR34B | 2 | RDQ37 | C |
| VCCIO | VCCIO2 | 2 | | |
| M23 | PR34A | 2 | RDQ37 | T |
| M27 | PR33B | 2 | RDQ37 | C (LVDS)* |
| M28 | PR33A | 2 | RDQ37 | T (LVDS)* |
| L26 | PR32B | 2 | RDQ29 | C |
| GND | GNDIO2 | - | | |
| L24 | PR32A | 2 | RDQ29 | T |
| M29 | PR31B | 2 | RDQ29 | C (LVDS)* |
| M30 | PR31A | 2 | RDQ29 | T (LVDS)* |
| L25 | PR30B | 2 | RDQ29 | C |
| VCCIO | VCCIO2 | 2 | | |
| L23 | PR30A | 2 | RDQ29 | T |
| L27 | PR29B | 2 | RDQ29 | C (LVDS)* |
| L28 | PR29A | 2 | RDQS29 | T (LVDS)* |
| GND | GNDIO2 | - | | |
| K24 | PR28B | 2 | RDQ29 | C |
| K26 | PR28A | 2 | RDQ29 | T |
| L29 | PR27B | 2 | RDQ29 | C (LVDS)* |
| L30 | PR27A | 2 | RDQ29 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| K23 | PR26B | 2 | RDQ29 | C |
| K25 | PR26A | 2 | RDQ29 | T |
| K27 | PR25B | 2 | RDQ29 | C (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| K28 | PR25A | 2 | RDQ29 | T (LVDS)* |
| J24 | PR24B | 2 | RDQ21 | C |
| J26 | PR24A | 2 | RDQ21 | T |
| GND | GNDIO2 | - | | |
| K29 | PR23B | 2 | RDQ21 | C (LVDS)* |
| K30 | PR23A | 2 | RDQ21 | T (LVDS)* |
| J23 | PR22B | 2 | RDQ21 | C |
| J25 | PR22A | 2 | RDQ21 | T |
| VCCIO | VCCIO2 | 99 | | |
| J27 | PR21B | 2 | RDQ21 | C (LVDS)* |
| J28 | PR21A | 2 | RDQS21 | T (LVDS)* |
| H26 | PR20B | 2 | RDQ21 | C |
| GND | GNDIO2 | - | | |
| H24 | PR20A | 2 | RDQ21 | T |
| J29 | PR19B | 2 | RDQ21 | C (LVDS)* |
| J30 | PR19A | 2 | RDQ21 | T (LVDS)* |
| H25 | PR18B | 2 | RDQ21 | C |
| VCCIO | VCCIO2 | 2 | | |
| H23 | PR18A | 2 | RDQ21 | T |
| G27 | PR15B | 2 | RUM1_SPLLC_FB_A/RDQ12 | C |
| GND | GNDIO2 | - | | |
| H27 | PR15A | 2 | RUM1_SPLLT_FB_A/RDQ12 | T |
| G29 | PR14B | 2 | RUM1_SPLLC_IN_A/RDQ12 | C (LVDS)* |
| G28 | PR14A | 2 | RUM1_SPLLT_IN_A/RDQ12 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| GND | GNDIO2 | - | | |
| G26 | PR6B | 2 | | C (LVDS)* |
| G25 | PR6A | 2 | | T (LVDS)* |
| G30 | PR5B | 2 | | C |
| F30 | PR5A | 2 | | T |
| VCCIO | VCCIO2 | 2 | | |
| F26 | PR4B | 2 | | C (LVDS)* |
| F27 | PR4A | 2 | | T (LVDS)* |
| F29 | PR3B | 2 | | C |
| GND | GNDIO2 | - | | |
| F28 | PR3A | 2 | | T |
| H29 | PR2B | 2 | VREF2_2 | C (LVDS)* |
| H30 | PR2A | 2 | VREF1_2 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| B26 | PT100B | 1 | VREF2_1 | C |
| A26 | PT100A | 1 | VREF1_1 | T |
| GND | GNDIO1 | - | | |
| C25 | PT99B | 1 | | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| D25 | PT99A | 1 | | T |
| J22 | PT98B | 1 | | C |
| J21 | PT98A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| B25 | PT97B | 1 | | C |
| A25 | PT97A | 1 | | T |
| E24 | PT96B | 1 | | C |
| F24 | PT96A | 1 | | T |
| GND | GNDIO1 | - | | |
| F23 | PT95B | 1 | | C |
| H22 | PT95A | 1 | | T |
| D24 | PT94B | 1 | | C |
| C24 | PT94A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| E23 | PT93B | 1 | | C |
| G23 | PT93A | 1 | | T |
| B24 | PT92B | 1 | | C |
| A24 | PT92A | 1 | | T |
| C27 | PT91B | 1 | | C |
| GND | GNDIO1 | - | | |
| D27 | PT91A | 1 | | T |
| C26 | PT90B | 1 | | C |
| D26 | PT90A | 1 | | T |
| A27 | PT89B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | |
| B27 | PT89A | 1 | | T |
| A28 | PT88B | 1 | | C |
| B28 | PT88A | 1 | | T |
| A29 | PT87B | 1 | | C |
| B29 | PT87A | 1 | | T |
| GND | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | |
| H21 | PT80B | 1 | | C |
| F22 | PT80A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| B23 | PT79B | 1 | | C |
| A23 | PT79A | 1 | | T |
| G24 | PT78B | 1 | | C |
| E22 | PT78A | 1 | | T |
| GND | GNDIO1 | - | | |
| D22 | PT77B | 1 | | C |
| C22 | PT77A | 1 | | T |
| G22 | PT76B | 1 | | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| E21 | PT76A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| B22 | PT75B | 1 | | C |
| A22 | PT75A | 1 | | T |
| H20 | PT74B | 1 | | C |
| F21 | PT74A | 1 | | T |
| F20 | PT73B | 1 | | C |
| GND | GNDIO1 | - | | |
| H19 | PT73A | 1 | | T |
| D21 | PT72B | 1 | | C |
| C21 | PT72A | 1 | | T |
| E20 | PT71B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | |
| G21 | PT71A | 1 | | T |
| B21 | PT70B | 1 | | C |
| A21 | PT70A | 1 | | T |
| F19 | PT69B | 1 | | C |
| G20 | PT69A | 1 | | T |
| E19 | PT68B | 1 | | C |
| GND | GNDIO1 | - | | |
| G19 | PT68A | 1 | | T |
| D20 | PT67B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | |
| C20 | PT67A | 1 | | T |
| B20 | PT66B | 1 | | C |
| A20 | PT66A | 1 | | T |
| F18 | PT65B | 1 | | C |
| H18 | PT65A | 1 | | T |
| D19 | PT64B | 1 | | C |
| C19 | PT64A | 1 | | T |
| GND | GNDIO1 | - | | |
| G18 | PT63B | 1 | | C |
| E18 | PT63A | 1 | | T |
| H17 | PT62B | 1 | | C |
| F17 | PT62A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| G17 | PT61B | 1 | | C |
| E17 | PT61A | 1 | | T |
| B19 | PT60B | 1 | | C |
| A19 | PT60A | 1 | | T |
| GND | GNDIO1 | - | | |
| D17 | PT59B | 1 | | C |
| B18 | PT59A | 1 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| C17 | PT58B | 1 | | C |
| A18 | PT58A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| H16 | PT57B | 1 | PCLKC1_0 | C |
| F16 | PT57A | 1 | PCLKT1_0 | T |
| K16 | XRES | 1 | | |
| E16 | PT55B | 0 | PCLKC0_0 | C |
| GND | GNDIO0 | - | | |
| G16 | PT55A | 0 | PCLKT0_0 | T |
| B17 | PT54B | 0 | | C |
| A17 | PT54A | 0 | | T |
| J15 | PT53B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| J16 | PT53A | 0 | | T |
| C16 | PT52B | 0 | | C |
| D16 | PT52A | 0 | | T |
| F15 | PT51B | 0 | | C |
| H15 | PT51A | 0 | | T |
| E15 | PT50B | 0 | | C |
| GND | GNDIO0 | - | | |
| G15 | PT50A | 0 | | T |
| C15 | PT49B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| D15 | PT49A | 0 | | T |
| B16 | PT48B | 0 | | C |
| A16 | PT48A | 0 | | T |
| E14 | PT47B | 0 | | C |
| G14 | PT47A | 0 | | T |
| B15 | PT46B | 0 | | C |
| A15 | PT46A | 0 | | T |
| GND | GNDIO0 | - | | |
| H14 | PT45B | 0 | | C |
| F14 | PT45A | 0 | | T |
| D14 | PT44B | 0 | | C |
| C14 | PT44A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| G13 | PT43B | 0 | | C |
| E13 | PT43A | 0 | | T |
| B14 | PT42B | 0 | | C |
| A14 | PT42A | 0 | | T |
| GND | GNDIO0 | - | | |
| H13 | PT41B | 0 | | C |
| F13 | PT41A | 0 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| G12 | PT40B | 0 | | C |
| E12 | PT40A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| B13 | PT39B | 0 | | C |
| A13 | PT39A | 0 | | T |
| H12 | PT38B | 0 | | C |
| F12 | PT38A | 0 | | T |
| C12 | PT37B | 0 | | C |
| GND | GNDIO0 | - | | |
| D12 | PT37A | 0 | | T |
| B12 | PT36B | 0 | | C |
| A12 | PT36A | 0 | | T |
| E11 | PT35B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| G11 | PT35A | 0 | | T |
| F11 | PT34B | 0 | | C |
| H11 | PT34A | 0 | | T |
| C11 | PT33B | 0 | | C |
| D11 | PT33A | 0 | | T |
| B11 | PT32B | 0 | | C |
| GND | GNDIO0 | - | | |
| A11 | PT32A | 0 | | T |
| E10 | PT31B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| G10 | PT31A | 0 | | T |
| F10 | PT30B | 0 | | C |
| H10 | PT30A | 0 | | T |
| D10 | PT29B | 0 | | C |
| C10 | PT29A | 0 | | T |
| GND | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | |
| A7 | PT16B | 0 | | C |
| B7 | PT16A | 0 | | T |
| A6 | PT15B | 0 | | C |
| B6 | PT15A | 0 | | T |
| C7 | PT14B | 0 | | C |
| GND | GNDIO0 | - | | |
| D7 | PT14A | 0 | | T |
| D8 | PT13B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| E7 | PT13A | 0 | | T |
| C6 | PT12B | 0 | | C |
| D6 | PT12A | 0 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| C5 | PT11B | 0 | | C |
| D5 | PT11A | 0 | | T |
| E9 | PT10B | 0 | | C |
| G9 | PT10A | 0 | | T |
| GND | GNDIO0 | - | | |
| B10 | PT9B | 0 | | C |
| A10 | PT9A | 0 | | T |
| D9 | PT8B | 0 | | C |
| C9 | PT8A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| F9 | PT7B | 0 | | C |
| H9 | PT7A | 0 | | T |
| B9 | PT6B | 0 | | C |
| A9 | PT6A | 0 | | T |
| GND | GNDIO0 | - | | |
| E8 | PT5B | 0 | | C |
| G8 | PT5A | 0 | | T |
| A8 | PT4B | 0 | | C |
| B8 | PT4A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| F8 | PT3B | 0 | | C |
| F7 | PT3A | 0 | | T |
| J10 | PT2B | 0 | VREF2_0 | C |
| J9 | PT2A | 0 | VREF1_0 | T |
| AA11 | VCC | - | | |
| AA20 | VCC | - | | |
| K11 | VCC | - | | |
| K21 | VCC | - | | |
| K22 | VCC | - | | |
| L11 | VCC | - | | |
| L12 | VCC | - | | |
| L13 | VCC | - | | |
| L18 | VCC | - | | |
| L19 | VCC | - | | |
| L20 | VCC | - | | |
| M11 | VCC | - | | |
| M20 | VCC | - | | |
| N11 | VCC | - | | |
| N20 | VCC | - | | |
| V11 | VCC | - | | |
| V20 | VCC | - | | |
| W11 | VCC | - | | |
| W20 | VCC | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| Y10 | VCC | - | | |
| Y11 | VCC | - | | |
| Y12 | VCC | - | | |
| Y13 | VCC | - | | |
| Y18 | VCC | - | | |
| Y19 | VCC | - | | |
| Y20 | VCC | - | | |
| J13 | VCCIO0 | 0 | | |
| J14 | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | |
| K13 | VCCIO0 | 0 | | |
| K14 | VCCIO0 | 0 | | |
| K15 | VCCIO0 | 0 | | |
| J17 | VCCIO1 | 1 | | |
| J18 | VCCIO1 | 1 | | |
| J20 | VCCIO1 | 1 | | |
| K17 | VCCIO1 | 1 | | |
| K18 | VCCIO1 | 1 | | |
| K20 | VCCIO1 | 1 | | |
| L21 | VCCIO2 | 2 | | |
| M21 | VCCIO2 | 2 | | |
| M22 | VCCIO2 | 2 | | |
| N21 | VCCIO2 | 2 | | |
| N22 | VCCIO2 | 2 | | |
| R21 | VCCIO2 | 2 | | |
| U21 | VCCIO3 | 3 | | |
| U22 | VCCIO3 | 3 | | |
| V21 | VCCIO3 | 3 | | |
| V22 | VCCIO3 | 3 | | |
| W21 | VCCIO3 | 3 | | |
| Y22 | VCCIO3 | 3 | | |
| AA16 | VCCIO4 | 4 | | |
| AA17 | VCCIO4 | 4 | | |
| AA18 | VCCIO4 | 4 | | |
| AA19 | VCCIO4 | 4 | | |
| AB17 | VCCIO4 | 4 | | |
| AB18 | VCCIO4 | 4 | | |
| AA12 | VCCIO5 | 5 | | |
| AA13 | VCCIO5 | 5 | | |
| AA14 | VCCIO5 | 5 | | |
| AB12 | VCCIO5 | 5 | | |
| AB13 | VCCIO5 | 5 | | |
| AB14 | VCCIO5 | 5 | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| U10 | VCCIO6 | 6 | | |
| U9 | VCCIO6 | 6 | | |
| V10 | VCCIO6 | 6 | | |
| W10 | VCCIO6 | 6 | | |
| W9 | VCCIO6 | 6 | | |
| Y9 | VCCIO6 | 6 | | |
| L10 | VCCIO7 | 7 | | |
| L9 | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | |
| N10 | VCCIO7 | 7 | | |
| P10 | VCCIO7 | 7 | | |
| R10 | VCCIO7 | 7 | | |
| AA21 | VCCIO8 | 8 | | |
| Y21 | VCCIO8 | 8 | | |
| AA15 | VCCAUX | - | | |
| AB11 | VCCAUX | - | | |
| AB19 | VCCAUX | - | | |
| AB20 | VCCAUX | - | | |
| J11 | VCCAUX | - | | |
| J12 | VCCAUX | - | | |
| J19 | VCCAUX | - | | |
| K19 | VCCAUX | - | | |
| L22 | VCCAUX | - | | |
| M9 | VCCAUX | - | | |
| N9 | VCCAUX | - | | |
| P21 | VCCAUX | - | | |
| P9 | VCCAUX | - | | |
| T10 | VCCAUX | - | | |
| T21 | VCCAUX | - | | |
| V9 | VCCAUX | - | | |
| W22 | VCCAUX | - | | |
| A1 | GND | - | | |
| A30 | GND | - | | |
| AC28 | GND | - | | |
| AC3 | GND | - | | |
| AH13 | GND | - | | |
| AH18 | GND | - | | |
| AH23 | GND | - | | |
| AH28 | GND | - | | |
| AH3 | GND | - | | |
| AH8 | GND | - | | |
| AK1 | GND | - | | |
| AK30 | GND | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| C13 | GND | - | | |
| C18 | GND | - | | |
| C23 | GND | - | | |
| C28 | GND | - | | |
| C3 | GND | - | | |
| C8 | GND | - | | |
| H28 | GND | - | | |
| H3 | GND | - | | |
| L14 | GND | - | | |
| L15 | GND | - | | |
| L16 | GND | - | | |
| L17 | GND | - | | |
| M12 | GND | - | | |
| M13 | GND | - | | |
| M14 | GND | - | | |
| M15 | GND | - | | |
| M16 | GND | - | | |
| M17 | GND | - | | |
| M18 | GND | - | | |
| M19 | GND | - | | |
| N12 | GND | - | | |
| N13 | GND | - | | |
| N14 | GND | - | | |
| N15 | GND | - | | |
| N16 | GND | - | | |
| N17 | GND | - | | |
| N18 | GND | - | | |
| N19 | GND | - | | |
| N28 | GND | - | | |
| N3 | GND | - | | |
| P11 | GND | - | | |
| P12 | GND | - | | |
| P13 | GND | - | | |
| P14 | GND | - | | |
| P15 | GND | - | | |
| P16 | GND | - | | |
| P17 | GND | - | | |
| P18 | GND | - | | |
| P19 | GND | - | | |
| P20 | GND | - | | |
| R11 | GND | - | | |
| R12 | GND | - | | |
| R13 | GND | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| R14 | GND | - | | |
| R15 | GND | - | | |
| R16 | GND | - | | |
| R17 | GND | - | | |
| R18 | GND | - | | |
| R19 | GND | - | | |
| R20 | GND | - | | |
| T11 | GND | - | | |
| T12 | GND | - | | |
| T13 | GND | - | | |
| T14 | GND | - | | |
| T15 | GND | - | | |
| T16 | GND | - | | |
| T17 | GND | - | | |
| T18 | GND | - | | |
| T19 | GND | - | | |
| T20 | GND | - | | |
| U11 | GND | - | | |
| U12 | GND | - | | |
| U13 | GND | - | | |
| U14 | GND | - | | |
| U15 | GND | - | | |
| U16 | GND | - | | |
| U17 | GND | - | | |
| U18 | GND | - | | |
| U19 | GND | - | | |
| U20 | GND | - | | |
| V12 | GND | - | | |
| V13 | GND | - | | |
| V14 | GND | - | | |
| V15 | GND | - | | |
| V16 | GND | - | | |
| V17 | GND | - | | |
| V18 | GND | - | | |
| V19 | GND | - | | |
| V28 | GND | - | | |
| V3 | GND | - | | |
| W12 | GND | - | | |
| W13 | GND | - | | |
| W14 | GND | - | | |
| W15 | GND | - | | |
| W16 | GND | - | | |
| W17 | GND | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| W18 | GND | - | | |
| W19 | GND | - | | |
| Y14 | GND | - | | |
| Y15 | GND | - | | |
| Y16 | GND | - | | |
| Y17 | GND | - | | |
| A2 | NC | - | | |
| A3 | NC | - | | |
| A4 | NC | - | | |
| A5 | NC | - | | |
| AB28 | NC | - | | |
| AC4 | NC | - | | |
| AD23 | NC | - | | |
| AE1 | NC | - | | |
| AE2 | NC | - | | |
| AE29 | NC | - | | |
| AE3 | NC | - | | |
| AE30 | NC | - | | |
| AE4 | NC | - | | |
| AE5 | NC | - | | |
| AE6 | NC | - | | |
| AF1 | NC | - | | |
| AF2 | NC | - | | |
| AF23 | NC | - | | |
| AF26 | NC | - | | |
| AF27 | NC | - | | |
| AF28 | NC | - | | |
| AF29 | NC | - | | |
| AF3 | NC | - | | |
| AF30 | NC | - | | |
| AF4 | NC | - | | |
| AF5 | NC | - | | |
| AG1 | NC | - | | |
| AG13 | NC | - | | |
| AG16 | NC | - | | |
| AG18 | NC | - | | |
| AG2 | NC | - | | |
| AG26 | NC | - | | |
| AG27 | NC | - | | |
| AG28 | NC | - | | |
| AG29 | NC | - | | |
| AG3 | NC | - | | |
| AG30 | NC | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| AG4 | NC | - | | |
| AG8 | NC | - | | |
| AH1 | NC | - | | |
| AH16 | NC | - | | |
| AH2 | NC | - | | |
| AH26 | NC | - | | |
| AH27 | NC | - | | |
| AH29 | NC | - | | |
| AH30 | NC | - | | |
| AH4 | NC | - | | |
| AJ1 | NC | - | | |
| AJ2 | NC | - | | |
| AJ27 | NC | - | | |
| AJ28 | NC | - | | |
| AJ29 | NC | - | | |
| AJ3 | NC | - | | |
| AJ30 | NC | - | | |
| AK2 | NC | - | | |
| AK27 | NC | - | | |
| AK28 | NC | - | | |
| AK29 | NC | - | | |
| AK3 | NC | - | | |
| B1 | NC | - | | |
| B2 | NC | - | | |
| B3 | NC | - | | |
| B30 | NC | - | | |
| B4 | NC | - | | |
| B5 | NC | - | | |
| C1 | NC | - | | |
| C2 | NC | - | | |
| C29 | NC | - | | |
| C30 | NC | - | | |
| C4 | NC | - | | |
| D13 | NC | - | | |
| D18 | NC | - | | |
| D23 | NC | - | | |
| D28 | NC | - | | |
| D29 | NC | - | | |
| D3 | NC | - | | |
| D30 | NC | - | | |
| D4 | NC | - | | |
| E25 | NC | - | | |
| E26 | NC | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| E27 | NC | - | | |
| E28 | NC | - | | |
| E29 | NC | - | | |
| E3 | NC | - | | |
| E30 | NC | - | | |
| E4 | NC | - | | |
| E5 | NC | - | | |
| E6 | NC | - | | |
| F25 | NC | - | | |
| F5 | NC | - | | |
| F6 | NC | - | | |
| G6 | NC | - | | |
| G7 | NC | - | | |
| K10 | NC | - | | |
| K9 | NC | - | | |
| N27 | NC | - | | |
| N4 | NC | - | | |
| R1 | NC | - | | |
| R2 | NC | - | | |
| V27 | NC | - | | |
| V4 | NC | - | | |
| P22 | VCCPLL | - | | |
| P8 | VCCPLL | - | | |
| T22 | VCCPLL | - | | |
| Y7 | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A2 | PL2A | 7 | LDQ6 | T (LVDS)* | PL2A | 7 | LDQ6 | T (LVDS)* |
| B2 | PL2B | 7 | LDQ6 | C (LVDS)* | PL2B | 7 | LDQ6 | C(LVDS)* |
| D3 | PL3A | 7 | LDQ6 | T | PL3A | 7 | LDQ6 | T |
| C2 | PL3B | 7 | LDQ6 | C | PL3B | 7 | LDQ6 | C |
| E4 | PL4A | 7 | LDQ6 | T (LVDS)* | PL4A | 7 | LDQ6 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E5 | PL4B | 7 | LDQ6 | C (LVDS)* | PL4B | 7 | LDQ6 | C(LVDS)* |
| B1 | PL5A | 7 | LDQ6 | T | PL5A | 7 | LDQ6 | T |
| C1 | PL5B | 7 | LDQ6 | C | PL5B | 7 | LDQ6 | C |
| D2 | PL6A | 7 | LDQS6 | T (LVDS)* | PL6A | 7 | LDQS6 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| D1 | PL6B | 7 | LDQ6 | C (LVDS)* | PL6B | 7 | LDQ6 | C(LVDS)* |
| E1 | PL7A | 7 | LDQ6 | T | PL7A | 7 | LDQ6 | T |
| F1 | PL7B | 7 | LDQ6 | C | PL7B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F3 | PL8A | 7 | LDQ6 | T (LVDS)* | PL8A | 7 | LDQ6 | T (LVDS)* |
| F2 | PL8B | 7 | LDQ6 | C (LVDS)* | PL8B | 7 | LDQ6 | C(LVDS)* |
| F6 | PL9A | 7 | VREF2_7/LDQ6 | T | PL9A | 7 | VREF2_7/LDQ6 | T |
| F5 | PL9B | 7 | VREF1_7/LDQ6 | C | PL9B | 7 | VREF1_7/LDQ6 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| G4 | PL11A | 7 | LUM0_SPLLT_IN_A | T (LVDS)* | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* |
| G3 | PL11B | 7 | LUM0_SPLLC_IN_A | C (LVDS)* | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C(LVDS)* |
| G1 | PL12A | 7 | LUM0_SPLLT_FB_A | T | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T |
| G2 | PL12B | 7 | LUM0_SPLLC_FB_A | C | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C |
| H1 | PL13A | 7 | | T (LVDS)* | PL13A | 7 | LDQ15 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J1 | PL13B | 7 | | C (LVDS)* | PL13B | 7 | LDQ15 | C(LVDS)* |
| H2 | PL14A | 7 | | T | PL14A | 7 | LDQ15 | T |
| H3 | PL14B | 7 | | C | PL14B | 7 | LDQ15 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G6 | PL24A | 7 | LDQ22 | T (LVDS)* | PL34A | 7 | LDQ32 | T (LVDS)* |
| H6 | PL24B | 7 | LDQ22 | C (LVDS)* | PL34B | 7 | LDQ32 | C(LVDS)* |
| J2 | PL25A | 7 | PCLKT7_0/LDQ22 | T | PL35A | 7 | PCLKT7_0/LDQ32 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| K1 | PL25B | 7 | PCLKC7_0/LDQ22 | C | PL35B | 7 | PCLKC7_0/LDQ32 | C |
| H4 | PL27A | 6 | PCLKT6_0 | T (LVDS)* | PL37A | 6 | PCLKT6_0 | T (LVDS)* |
| H5 | PL27B | 6 | PCLKC6_0 | C (LVDS)* | PL37B | 6 | PCLKC6_0 | C(LVDS)* |
| J4 | PL28A | 6 | VREF2_6 | T | PL38A | 6 | VREF2_6 | T |
| K4 | PL28B | 6 | VREF1_6 | C | PL38B | 6 | VREF1_6 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| J6 | PL31A | 6 | LLM1_SPLLT_IN_A | T (LVDS)* | PL41A | 6 | LLM2_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| J5 | PL31B | 6 | LLM1_SPLLC_IN_A | C (LVDS)* | PL41B | 6 | LLM2_SPLLC_IN_A | C(LVDS)* |
| K3 | PL32A | 6 | LLM1_SPLLT_FB_A | T | PL42A | 6 | LLM2_SPLLT_FB_A | T |
| K2 | PL32B | 6 | LLM1_SPLLC_FB_A | C | PL42B | 6 | LLM2_SPLLC_FB_A | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| L1 | PL42A | 6 | LLM0_GPLLT_IN_A | T (LVDS)* | PL57A | 6 | LLM0_GPLLT_IN_A**/LDQS57*** | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| L2 | PL42B | 6 | LLM0_GPLLC_IN_A | C (LVDS)* | PL57B | 6 | LLM0_GPLLC_IN_A**/LDQ57 | C(LVDS)* |
| L3 | PL43A | 6 | LLM0_GPLLT_FB_A | T | PL58A | 6 | LLM0_GPLLT_FB_A/LDQ57 | T |
| L4 | PL43B | 6 | LLM0_GPLLC_FB_A | C | PL58B | 6 | LLM0_GPLLC_FB_A/LDQ57 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| M1 | PL44A | 6 | LLM0_GDLLT_IN_A | T (LVDS)* | PL59A | 6 | LLM0_GDLLT_IN_A**/LDQ57 | T (LVDS)* |
| N1 | PL44B | 6 | LLM0_GDLLC_IN_A | C (LVDS)* | PL59B | 6 | LLM0_GDLLC_IN_A**/LDQ57 | C(LVDS)* |
| N2 | PL45A | 6 | LLM0_GDLLT_FB_A | T | PL60A | 6 | LLM0_GDLLT_FB_A/LDQ57 | T |
| N3 | PL45B | 6 | LLM0_GDLLC_FB_A | C | PL60B | 6 | LLM0_GDLLC_FB_A/LDQ57 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| M4 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| K6 | TCK | - | | | TCK | - | | |
| L5 | TDI | - | | | TDI | - | | |
| N4 | TMS | - | | | TMS | - | | |
| N6 | TDO | - | | | TDO | - | | |
| K7 | VCCJ | - | | | VCCJ | - | | |
| M5 | PB2A | 5 | BDQ6 | T | PB2A | 5 | BDQ6 | T |
| N5 | PB2B | 5 | BDQ6 | C | PB2B | 5 | BDQ6 | C |
| L6 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| M6 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| P3 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P4 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| P2 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| P1 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| R1 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| R2 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| R3 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| T2 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| R4 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T3 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| T4 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| T5 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| T6 | PB16A | 5 | VREF2_5/BDQ15 | T | PB34A | 5 | VREF2_5/BDQ33 | T |
| R6 | PB16B | 5 | VREF1_5/BDQ15 | C | PB34B | 5 | VREF1_5/BDQ33 | C |
| P6 | PB17A | 5 | PCLKT5_0/BDQ15 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| P7 | PB17B | 5 | PCLKC5_0/BDQ15 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T7 | PB22A | 4 | PCLKT4_0/BDQ24 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T8 | PB22B | 4 | PCLKC4_0/BDQ24 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| L7 | PB23A | 4 | VREF2_4/BDQ24 | T | PB41A | 4 | VREF2_4/BDQ42 | T |
| L8 | PB23B | 4 | VREF1_4/BDQ24 | C | PB41B | 4 | VREF1_4/BDQ42 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| P8 | PB29A | 4 | BDQ33 | T | PB47A | 4 | BDQ51 | T |
| N8 | PB29B | 4 | BDQ33 | C | PB47B | 4 | BDQ51 | C |
| R7 | PB30A | 4 | BDQ33 | T | PB48A | 4 | BDQ51 | T |
| R8 | PB30B | 4 | BDQ33 | C | PB48B | 4 | BDQ51 | C |
| N7 | PB31A | 4 | BDQ33 | T | PB49A | 4 | BDQ51 | T |
| M8 | PB31B | 4 | BDQ33 | C | PB49B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| R9 | PB32A | 4 | BDQ33 | T | PB50A | 4 | BDQ51 | T |
| T9 | PB32B | 4 | BDQ33 | C | PB50B | 4 | BDQ51 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| T10 | PB33A | 4 | BDQS33 | T | PB51A | 4 | BDQS51 | T |
| R10 | PB33B | 4 | BDQ33 | C | PB51B | 4 | BDQ51 | C |
| N9 | PB34A | 4 | BDQ33 | T | PB52A | 4 | BDQ51 | T |
| P10 | PB34B | 4 | BDQ33 | C | PB52B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| L9 | PB47A | 4 | BDQ51 | T | PB65A | 4 | BDQ69 | T |
| M9 | PB47B | 4 | BDQ51 | C | PB65B | 4 | BDQ69 | C |
| T11 | PB49A | 4 | BDQ51 | T | PB67A | 4 | BDQ69 | T |
| R11 | PB49B | 4 | BDQ51 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T12 | PB50A | 4 | BDQ51 | T | PB68A | 4 | BDQ69 | T |
| T13 | PB50B | 4 | BDQ51 | C | PB68B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| P11 | PB51A | 4 | BDQS51 | T | PB69A | 4 | BDQS69 | T |
| N10 | PB51B | 4 | BDQ51 | C | PB69B | 4 | BDQ69 | C |
| T14 | PB52A | 4 | BDQ51 | T | PB70A | 4 | BDQ69 | T |
| R13 | PB52B | 4 | BDQ51 | C | PB70B | 4 | BDQ69 | C |
| R15 | PB53A | 4 | BDQ51 | T | PB71A | 4 | BDQ69 | T |
| R16 | PB53B | 4 | BDQ51 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| R14 | PB54A | 4 | BDQ51 | T | PB72A | 4 | BDQ69 | T |
| P15 | PB54B | 4 | BDQ51 | C | PB72B | 4 | BDQ69 | C |
| P16 | PB55A | 4 | BDQ51 | T | PB73A | 4 | BDQ69 | T |
| P14 | PB55B | 4 | BDQ51 | C | PB73B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| L11 | CFG2 | 8 | | | CFG2 | 8 | | |
| L10 | CFG1 | 8 | | | CFG1 | 8 | | |
| P13 | CFG0 | 8 | | | CFG0 | 8 | | |
| N12 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N11 | CCLK | 8 | | | CCLK | 8 | | |
| M11 | INITN | 8 | | | INITN | 8 | | |
| N13 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| M12 | PR53B | 8 | WRITEN | C | PR68B | 8 | WRITEN | C |
| M13 | PR53A | 8 | CS1N | T | PR68A | 8 | CS1N | T |
| N14 | PR52B | 8 | CSN | C | PR67B | 8 | CSN | C |
| N15 | PR52A | 8 | D0/SPIFASTN | T | PR67A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| N16 | PR51B | 8 | D1 | C | PR66B | 8 | D1 | C |
| M16 | PR51A | 8 | D2 | T | PR66A | 8 | D2 | T |
| L12 | PR50B | 8 | D3 | C | PR65B | 8 | D3 | C |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| L13 | PR50A | 8 | D4 | T | PR65A | 8 | D4 | T |
| L16 | PR49B | 8 | D5 | C | PR64B | 8 | D5 | C |
| K16 | PR49A | 8 | D6 | T | PR64A | 8 | D6 | T |
| L14 | PR48B | 8 | D7/SPID0*** | C | PR63B | 8 | D7/SPID0*** | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| L15 | PR48A | 8 | DI/CSSPI0N | T | PR63A | 8 | DI/CSSPI0N | T |
| K13 | PR47B | 8 | DOUT/CSON/CSSPI1N | C | PR62B | 8 | DOUT/CSON/CSSPI1N | C |
| K14 | PR47A | 8 | BUSY/SISPI | T | PR62A | 8 | BUSY/SISPI | T |
| K11 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| K15 | PR45B | 3 | RLM0_GDLLC_FB_A | C | PR60B | 3 | RLM0_GDLLC_FB_A/RDQ57 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| J16 | PR45A | 3 | RLM0_GDLLT_FB_A | T | PR60A | 3 | RLM0_GDLLT_FB_A/RDQ57 | T |
| H16 | PR44B | 3 | RLM0_GDLLC_IN_A | C (LVDS)* | PR59B | 3 | RLM0_GDLLC_IN_A**/RDQ57 | C(LVDS)* |
| J15 | PR44A | 3 | RLM0_GDLLT_IN_A | T (LVDS)* | PR59A | 3 | RLM0_GDLLT_IN_A**/RDQ57 | T (LVDS)* |
| J14 | PR43B | 3 | RLM0_GPLLC_IN_A | C | PR58B | 3 | RLM0_GPLLC_IN_A**/RDQ57 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| J13 | PR43A | 3 | RLM0_GPLLT_IN_A | T | PR58A | 3 | RLM0_GPLLT_IN_A**/RDQ57 | T |
| H13 | PR42B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR57B | 3 | RLM0_GPLLC_FB_A/RDQ57 | C(LVDS)* |
| H12 | PR42A | 3 | RLM0_GPLLT_FB_A | T (LVDS)* | PR57A | 3 | RLM0_GPLLT_FB_A/RDQS57*** | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| G16 | PR32B | 3 | RLM1_SPLLC_FB_A | C | PR42B | 3 | RLM2_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| H15 | PR32A | 3 | RLM1_SPLLT_FB_A | T | PR42A | 3 | RLM2_SPLLT_FB_A | T |
| E16 | PR31B | 3 | RLM1_SPLLC_IN_A | C (LVDS)* | PR41B | 3 | RLM2_SPLLC_IN_A | C(LVDS)* |
| F15 | PR31A | 3 | RLM1_SPLLT_IN_A | T (LVDS)* | PR41A | 3 | RLM2_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| F16 | PR28B | 3 | VREF2_3 | C | PR38B | 3 | VREF2_3 | C |
| G15 | PR28A | 3 | VREF1_3 | T | PR38A | 3 | VREF1_3 | T |
| J11 | PR27B | 3 | PCLKC3_0 | C (LVDS)* | PR37B | 3 | PCLKC3_0 | C(LVDS)* |
| J12 | PR27A | 3 | PCLKT3_0 | T (LVDS)* | PR37A | 3 | PCLKT3_0 | T (LVDS)* |
| G14 | PR25B | 2 | PCLKC2_0/RDQ22 | C | PR35B | 2 | PCLKC2_0/RDQ32 | C |
| G13 | PR25A | 2 | PCLKT2_0/RDQ22 | T | PR35A | 2 | PCLKT2_0/RDQ32 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F14 | PR24B | 2 | RDQ22 | C (LVDS)* | PR34B | 2 | RDQ32 | C(LVDS)* |
| F13 | PR24A | 2 | RDQ22 | T (LVDS)* | PR34A | 2 | RDQ32 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| H11 | PR14B | 2 | | C | PR14B | 2 | RDQ15 | C |
| G11 | PR14A | 2 | | T | PR14A | 2 | RDQ15 | T |
| E13 | PR13B | 2 | | C (LVDS)* | PR13B | 2 | RDQ15 | C(LVDS)* |
| F12 | PR13A | 2 | | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F11 | PR12B | 2 | RUM0_SPLLC_FB_A | C | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| E12 | PR12A | 2 | RUM0_SPLLT_FB_A | T | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| D16 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C(LVDS)* |
| D15 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| C16 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| B16 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F4 | XRES | - | | | XRES | - | | |
| C15 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A14 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B15 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B14 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C12 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A11 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A12 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B11 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C11 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B10 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C10 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A10 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C14 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B13 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C13 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A13 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B9 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| D8 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D9 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C9 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A5 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| C5 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B5 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C4 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A8 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C8 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B8 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C7 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B7 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| A6 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A7 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C6 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B4 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B3 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A4 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C3 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G10 | VCCPLL | - | | | VCCPLL | - | | |
| G7 | VCC | - | | | VCC | - | | |
| G9 | VCC | - | | | VCC | - | | |
| H7 | VCC | - | | | VCC | - | | |
| J10 | VCC | - | | | VCC | - | | |
| K10 | VCC | - | | | VCC | - | | |
| K8 | VCC | - | | | VCC | - | | |
| E7 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E10 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E14 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G12 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K12 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M14 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M10 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| P12 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| M7 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P5 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| K5 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| M3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| E3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G5 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T15 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| G8 | VCCAUX | - | | | VCCAUX | - | | |
| H10 | VCCAUX | - | | | VCCAUX | - | | |
| J7 | VCCAUX | - | | | VCCAUX | - | | |
| K9 | VCCAUX | - | | | VCCAUX | - | | |
| A1 | GND | - | | | GND | - | | |
| A15 | GND | - | | | GND | - | | |
| A16 | GND | - | | | GND | - | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A3 | GND | - | | | GND | - | | |
| A9 | GND | - | | | GND | - | | |
| B12 | GND | - | | | GND | - | | |
| B6 | GND | - | | | GND | - | | |
| E15 | GND | - | | | GND | - | | |
| E2 | GND | - | | | GND | - | | |
| H14 | GND | - | | | GND | - | | |
| H8 | GND | - | | | GND | - | | |
| H9 | GND | - | | | GND | - | | |
| J3 | GND | - | | | GND | - | | |
| J8 | GND | - | | | GND | - | | |
| J9 | GND | - | | | GND | - | | |
| M15 | GND | - | | | GND | - | | |
| M2 | GND | - | | | GND | - | | |
| P9 | GND | - | | | GND | - | | |
| R12 | GND | - | | | GND | - | | |
| R5 | GND | - | | | GND | - | | |
| T1 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| D10 | NC | - | | | NC | - | | |
| D11 | NC | - | | | NC | - | | |
| D12 | NC | - | | | NC | - | | |
| D13 | NC | - | | | NC | - | | |
| D14 | NC | - | | | NC | - | | |
| D4 | NC | - | | | NC | - | | |
| D5 | NC | - | | | NC | - | | |
| D6 | NC | - | | | NC | - | | |
| D7 | NC | - | | | NC | - | | |
| E11 | NC | - | | | NC | - | | |
| E6 | NC | - | | | NC | - | | |
| E8 | NC | - | | | NC | - | | |
| E9 | NC | - | | | NC | - | | |
| F10 | NC | - | | | NC | - | | |
| F7 | NC | - | | | NC | - | | |
| F8 | NC | - | | | NC | - | | |
| F9 | NC | - | | | NC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D1 | PL2A | 7 | LDQ6 | T (LVDS)* | PL2A | 7 | LDQ6 | T (LVDS)* |
| E1 | PL2B | 7 | LDQ6 | C (LVDS)* | PL2B | 7 | LDQ6 | C (LVDS)* |
| F1 | PL3A | 7 | LDQ6 | T | PL3A | 7 | LDQ6 | T |
| F2 | PL3B | 7 | LDQ6 | C | PL3B | 7 | LDQ6 | C |
| F5 | PL4A | 7 | LDQ6 | T (LVDS)* | PL4A | 7 | LDQ6 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G6 | PL4B | 7 | LDQ6 | C (LVDS)* | PL4B | 7 | LDQ6 | C (LVDS)* |
| F4 | PL5A | 7 | LDQ6 | T | PL5A | 7 | LDQ6 | T |
| F3 | PL5B | 7 | LDQ6 | C | PL5B | 7 | LDQ6 | C |
| G1 | PL6A | 7 | LDQS6 | T (LVDS)* | PL6A | 7 | LDQS6 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| G2 | PL6B | 7 | LDQ6 | C (LVDS)* | PL6B | 7 | LDQ6 | C (LVDS)* |
| H1 | PL7A | 7 | LDQ6 | T | PL7A | 7 | LDQ6 | T |
| H2 | PL7B | 7 | LDQ6 | C | PL7B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H7 | PL8A | 7 | LDQ6 | T (LVDS)* | PL8A | 7 | LDQ6 | T (LVDS)* |
| H6 | PL8B | 7 | LDQ6 | C (LVDS)* | PL8B | 7 | LDQ6 | C (LVDS)* |
| G3 | PL9A | 7 | VREF2_7/LDQ6 | T | PL9A | 7 | VREF2_7/LDQ6 | T |
| H3 | PL9B | 7 | VREF1_7/LDQ6 | C | PL9B | 7 | VREF1_7/LDQ6 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| H5 | PL11A | 7 | LUM0_SPLLT_IN_A | T (LVDS)* | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* |
| H4 | PL11B | 7 | LUM0_SPLLC_IN_A | C (LVDS)* | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* |
| J1 | PL12A | 7 | LUM0_SPLLT_FB_A | T | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T |
| J2 | PL12B | 7 | LUM0_SPLLC_FB_A | C | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C |
| J3 | PL13A | 7 | | T (LVDS)* | PL13A | 7 | LDQ15 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J4 | PL13B | 7 | | C (LVDS)* | PL13B | 7 | LDQ15 | C (LVDS)* |
| J7 | PL14A | 7 | | T | PL14A | 7 | LDQ15 | T |
| J6 | PL14B | 7 | | C | PL14B | 7 | LDQ15 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K1 | PL18A | 7 | LUM1_SPLLT_IN_A/LDQ22 | T (LVDS)* | PL28A | 7 | LUM1_SPLLT_IN_A/LDQ32 | T (LVDS)* |
| K2 | PL18B | 7 | LUM1_SPLLC_IN_A/LDQ22 | C (LVDS)* | PL28B | 7 | LUM1_SPLLC_IN_A/LDQ32 | C (LVDS)* |
| J5 | PL19A | 7 | LUM1_SPLLT_FB_A/LDQ22 | T | PL29A | 7 | LUM1_SPLLT_FB_A/LDQ32 | T |
| K5 | PL19B | 7 | LUM1_SPLLC_FB_A/LDQ22 | C | PL29B | 7 | LUM1_SPLLC_FB_A/LDQ32 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K7 | PL20A | 7 | LDQ22 | T (LVDS)* | PL30A | 7 | LDQ32 | T (LVDS)* |
| K6 | PL20B | 7 | LDQ22 | C (LVDS)* | PL30B | 7 | LDQ32 | C (LVDS)* |
| L6 | PL21A | 7 | LDQ22 | T | PL31A | 7 | LDQ32 | T |
| L7 | PL21B | 7 | LDQ22 | C | PL31B | 7 | LDQ32 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| L1 | PL22A | 7 | LDQS22 | T (LVDS)* | PL32A | 7 | LDQS32 | T (LVDS)* |
| L2 | PL22B | 7 | LDQ22 | C (LVDS)* | PL32B | 7 | LDQ32 | C (LVDS)* |
| M7 | PL23A | 7 | LDQ22 | T | PL33A | 7 | LDQ32 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L5 | PL23B | 7 | LDQ22 | C | PL33B | 7 | LDQ32 | C |
| L3 | PL24A | 7 | LDQ22 | T (LVDS)* | PL34A | 7 | LDQ32 | T (LVDS)* |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L4 | PL24B | 7 | LDQ22 | C (LVDS)* | PL34B | 7 | LDQ32 | C (LVDS)* |
| M1 | PL25A | 7 | PCLKT7_0/LDQ22 | T | PL35A | 7 | PCLKT7_0/LDQ32 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M2 | PL25B | 7 | PCLKC7_0/LDQ22 | C | PL35B | 7 | PCLKC7_0/LDQ32 | C |
| M6 | PL27A | 6 | PCLKT6_0 | T (LVDS)* | PL37A | 6 | PCLKT6_0 | T (LVDS)* |
| M5 | PL27B | 6 | PCLKC6_0 | C (LVDS)* | PL37B | 6 | PCLKC6_0 | C (LVDS)* |
| M3 | PL28A | 6 | VREF2_6 | T | PL38A | 6 | VREF2_6 | T |
| M4 | PL28B | 6 | VREF1_6 | C | PL38B | 6 | VREF1_6 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| N7 | PL31A | 6 | LLM1_SPLLT_IN_A | T (LVDS)* | PL41A | 6 | LLM2_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| N6 | PL31B | 6 | LLM1_SPLLC_IN_A | C (LVDS)* | PL41B | 6 | LLM2_SPLLC_IN_A | C (LVDS)* |
| N1 | PL32A | 6 | LLM1_SPLLT_FB_A | T | PL42A | 6 | LLM2_SPLLT_FB_A | T |
| N2 | PL32B | 6 | LLM1_SPLLC_FB_A | C | PL42B | 6 | LLM2_SPLLC_FB_A | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| P6 | PL38A | 6 | LDQS38**** | T (LVDS)* | PL48A | 6 | LDQS48**** | T (LVDS)* |
| N5 | PL38B | 6 | LDQ38 | C (LVDS)* | PL48B | 6 | LDQ48 | C (LVDS)* |
| P1 | PL39A | 6 | LDQ38 | T | PL49A | 6 | LDQ48 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P2 | PL39B | 6 | LDQ38 | C | PL49B | 6 | LDQ48 | C |
| P3 | PL40A | 6 | LDQ38 | T (LVDS)* | PL50A | 6 | LDQ48 | T (LVDS)* |
| P4 | PL40B | 6 | LDQ38 | C (LVDS)* | PL50B | 6 | LDQ48 | C (LVDS)* |
| P5 | PL41A | 6 | LDQ38 | T | PL51A | 6 | LDQ48 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| P7 | PL41B | 6 | LDQ38 | C | PL51B | 6 | LDQ48 | C |
| R1 | PL42A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* | PL57A | 6 | LLM0_GPLLT_IN_A**/LDQS57**** | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| R2 | PL42B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* | PL57B | 6 | LLM0_GPLLC_IN_A**/LDQ57 | C (LVDS)* |
| R3 | PL43A | 6 | LLM0_GPLLT_FB_A | T | PL58A | 6 | LLM0_GPLLT_FB_A/LDQ57 | T |
| R4 | PL43B | 6 | LLM0_GPLLC_FB_A | C | PL58B | 6 | LLM0_GPLLC_FB_A/LDQ57 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R6 | PL44A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* | PL59A | 6 | LLM0_GDLLT_IN_A**/LDQ57 | T (LVDS)* |
| R5 | PL44B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* | PL59B | 6 | LLM0_GDLLC_IN_A**/LDQ57 | C (LVDS)* |
| T1 | PL45A | 6 | LLM0_GDLLT_FB_A | T | PL60A | 6 | LLM0_GDLLT_FB_A/LDQ57 | T |
| T2 | PL45B | 6 | LLM0_GDLLC_FB_A | C | PL60B | 6 | LLM0_GDLLC_FB_A/LDQ57 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| R7 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| T6 | PL47A | 6 | LDQ51 | T (LVDS)* | PL62A | 6 | LDQ66 | T (LVDS)* |
| T7 | PL47B | 6 | LDQ51 | C (LVDS)* | PL62B | 6 | LDQ66 | C (LVDS)* |
| U1 | PL48A | 6 | LDQ51 | T | PL63A | 6 | LDQ66 | T |
| U2 | PL48B | 6 | LDQ51 | C | PL63B | 6 | LDQ66 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T3 | PL49A | 6 | LDQ51 | T (LVDS)* | PL64A | 6 | LDQ66 | T (LVDS)* |
| U3 | PL49B | 6 | LDQ51 | C (LVDS)* | PL64B | 6 | LDQ66 | C (LVDS)* |
| U6 | PL50A | 6 | LDQ51 | T | NC | - | | |
| U5 | PL50B | 6 | LDQ51 | C | PL65B | 6 | LDQ66 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| V5 | PL51A | 6 | LDQS51 | T (LVDS)* | PL66A | 6 | LDQS66 | T (LVDS)* |
| U4 | PL51B | 6 | LDQ51 | C (LVDS)* | PL66B | 6 | LDQ66 | C (LVDS)* |
| V1 | PL52A | 6 | LDQ51 | T | PL67A | 6 | LDQ66 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V3 | PL52B | 6 | LDQ51 | C | PL67B | 6 | LDQ66 | C |
| W1 | PL53A | 6 | LDQ51 | T (LVDS)* | PL68A | 6 | LDQ66 | T (LVDS)* |
| Y1 | PL53B | 6 | LDQ51 | C (LVDS)* | PL68B | 6 | LDQ66 | C (LVDS)* |
| AA1 | PL54A | 6 | LDQ51 | T | PL69A | 6 | LDQ66 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA2 | PL54B | 6 | LDQ51 | C | PL69B | 6 | LDQ66 | C |
| V4 | TCK | - | | | TCK | - | | |
| Y2 | TDI | - | | | TDI | - | | |
| Y3 | TMS | - | | | TMS | - | | |
| W3 | TDO | - | | | TDO | - | | |
| W4 | VCCJ | - | | | VCCJ | - | | |
| W5 | PB2A | 5 | BDQ6 | T | PB2A | 5 | BDQ6 | T |
| Y4 | PB2B | 5 | BDQ6 | C | PB2B | 5 | BDQ6 | C |
| W6 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| V6 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| AA3 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AB2 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| T8 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| U7 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| U8 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| T9 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| V8 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| W8 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| Y6 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y5 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| AB3 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| AB4 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| AB5 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AA6 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| V9 | PB13A | 5 | BDQ15 | T | PB31A | 5 | BDQ33 | T |
| U9 | PB13B | 5 | BDQ15 | C | PB31B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| - | - | - | | | GNDIO5 | - | | |
| U10 | PB14A | 5 | BDQ15 | T | PB32A | 5 | BDQ33 | T |
| T10 | PB14B | 5 | BDQ15 | C | PB32B | 5 | BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| W9 | PB15A | 5 | BDQS15**** | T | PB33A | 5 | BDQS33**** | T |
| Y8 | PB15B | 5 | BDQ15 | C | PB33B | 5 | BDQ33 | C |
| AA7 | PB16A | 5 | VREF2_5/BDQ15 | T | PB34A | 5 | VREF2_5/BDQ33 | T |
| Y7 | PB16B | 5 | VREF1_5/BDQ15 | C | PB34B | 5 | VREF1_5/BDQ33 | C |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AB6 | PB17A | 5 | PCLKT5_0/BDQ15 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| AB7 | PB17B | 5 | PCLKC5_0/BDQ15 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AA8 | PB22A | 4 | PCLKT4_0/BDQ24 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AB8 | PB22B | 4 | PCLKC4_0/BDQ24 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| AA9 | PB23A | 4 | VREF2_4/BDQ24 | T | PB41A | 4 | VREF2_4/BDQ42 | T |
| Y9 | PB23B | 4 | VREF1_4/BDQ24 | C | PB41B | 4 | VREF1_4/BDQ42 | C |
| AB9 | PB24A | 4 | BDQS24**** | T | PB42A | 4 | BDQS42**** | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AB10 | PB24B | 4 | BDQ24 | C | PB42B | 4 | BDQ42 | C |
| AA10 | PB25A | 4 | BDQ24 | T | PB43A | 4 | BDQ42 | T |
| Y11 | PB25B | 4 | BDQ24 | C | PB43B | 4 | BDQ42 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| V10 | PB29A | 4 | BDQ33 | T | PB47A | 4 | BDQ51 | T |
| U11 | PB29B | 4 | BDQ33 | C | PB47B | 4 | BDQ51 | C |
| V11 | PB30A | 4 | BDQ33 | T | PB48A | 4 | BDQ51 | T |
| W11 | PB30B | 4 | BDQ33 | C | PB48B | 4 | BDQ51 | C |
| AA11 | PB31A | 4 | BDQ33 | T | PB49A | 4 | BDQ51 | T |
| AB11 | PB31B | 4 | BDQ33 | C | PB49B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T11 | PB32A | 4 | BDQ33 | T | PB50A | 4 | BDQ51 | T |
| U12 | PB32B | 4 | BDQ33 | C | PB50B | 4 | BDQ51 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA12 | PB33A | 4 | BDQS33 | T | PB51A | 4 | BDQS51 | T |
| Y12 | PB33B | 4 | BDQ33 | C | PB51B | 4 | BDQ51 | C |
| V12 | PB34A | 4 | BDQ33 | T | PB52A | 4 | BDQ51 | T |
| W12 | PB34B | 4 | BDQ33 | C | PB52B | 4 | BDQ51 | C |
| AB12 | PB35A | 4 | BDQ33 | T | PB53A | 4 | BDQ51 | T |
| AA13 | PB35B | 4 | BDQ33 | C | PB53B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T12 | PB36A | 4 | BDQ33 | T | PB54A | 4 | BDQ51 | T |
| U13 | PB36B | 4 | BDQ33 | C | PB54B | 4 | BDQ51 | C |
| V13 | PB37A | 4 | BDQ33 | T | PB55A | 4 | BDQ51 | T |
| T13 | PB37B | 4 | BDQ33 | C | PB55B | 4 | BDQ51 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AB13 | PB38A | 4 | BDQ42 | T | PB56A | 4 | BDQ60 | T |
| AB14 | PB38B | 4 | BDQ42 | C | PB56B | 4 | BDQ60 | C |
| U14 | PB39A | 4 | BDQ42 | T | PB57A | 4 | BDQ60 | T |
| T14 | PB39B | 4 | BDQ42 | C | PB57B | 4 | BDQ60 | C |
| AA14 | PB40A | 4 | BDQ42 | T | PB58A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y14 | PB40B | 4 | BDQ42 | C | PB58B | 4 | BDQ60 | C |
| W14 | PB41A | 4 | BDQ42 | T | PB59A | 4 | BDQ60 | T |
| V14 | PB41B | 4 | BDQ42 | C | PB59B | 4 | BDQ60 | C |
| AB15 | PB42A | 4 | BDQS42 | T | PB60A | 4 | BDQS60 | T |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA15 | PB42B | 4 | BDQ42 | C | PB60B | 4 | BDQ60 | C |
| V15 | PB43A | 4 | BDQ42 | T | PB61A | 4 | BDQ60 | T |
| U15 | PB43B | 4 | BDQ42 | C | PB61B | 4 | BDQ60 | C |
| AB16 | PB44A | 4 | BDQ42 | T | PB62A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA16 | PB44B | 4 | BDQ42 | C | PB62B | 4 | BDQ60 | C |
| AB17 | PB45A | 4 | BDQ42 | T | PB63A | 4 | BDQ60 | T |
| AA17 | PB45B | 4 | BDQ42 | C | PB63B | 4 | BDQ60 | C |
| Y15 | PB46A | 4 | BDQ42 | T | PB64A | 4 | BDQ60 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W15 | PB46B | 4 | BDQ42 | C | PB64B | 4 | BDQ60 | C |
| AB20 | PB47A | 4 | BDQ51 | T | PB65A | 4 | BDQ69 | T |
| AB21 | PB47B | 4 | BDQ51 | C | PB65B | 4 | BDQ69 | C |
| AA21 | PB48A | 4 | BDQ51 | T | PB66A | 4 | BDQ69 | T |
| AA20 | PB48B | 4 | BDQ51 | C | PB66B | 4 | BDQ69 | C |
| AB19 | PB49A | 4 | BDQ51 | T | PB67A | 4 | BDQ69 | T |
| AB18 | PB49B | 4 | BDQ51 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y22 | PB50A | 4 | BDQ51 | T | PB68A | 4 | BDQ69 | T |
| Y21 | PB50B | 4 | BDQ51 | C | PB68B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| Y17 | PB51A | 4 | BDQS51 | T | PB69A | 4 | BDQS69 | T |
| Y18 | PB51B | 4 | BDQ51 | C | PB69B | 4 | BDQ69 | C |
| Y16 | PB52A | 4 | BDQ51 | T | PB70A | 4 | BDQ69 | T |
| W17 | PB52B | 4 | BDQ51 | C | PB70B | 4 | BDQ69 | C |
| Y19 | PB53A | 4 | BDQ51 | T | PB71A | 4 | BDQ69 | T |
| Y20 | PB53B | 4 | BDQ51 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W19 | PB54A | 4 | BDQ51 | T | PB72A | 4 | BDQ69 | T |
| W18 | PB54B | 4 | BDQ51 | C | PB72B | 4 | BDQ69 | C |
| V17 | PB55A | 4 | BDQ51 | T | PB73A | 4 | BDQ69 | T |
| V18 | PB55B | 4 | BDQ51 | C | PB73B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W20 | CFG2 | 8 | | | CFG2 | 8 | | |
| V20 | CFG1 | 8 | | | CFG1 | 8 | | |
| V19 | CFG0 | 8 | | | CFG0 | 8 | | |
| V22 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| W22 | CCLK | 8 | | | CCLK | 8 | | |
| U18 | INITN | 8 | | | INITN | 8 | | |
| U22 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| U20 | PR53B | 8 | WRITEN*** | C | PR68B | 8 | WRITEN*** | C |
| U21 | PR53A | 8 | CS1N*** | T | PR68A | 8 | CS1N*** | T |
| U17 | PR52B | 8 | CSN*** | C | PR67B | 8 | CSN*** | C |
| U16 | PR52A | 8 | D0/SPIFASTN*** | T | PR67A | 8 | D0/SPIFASTN*** | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| T16 | PR51B | 8 | D1*** | C | PR66B | 8 | D1*** | C |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T17 | PR51A | 8 | D2*** | T | PR66A | 8 | D2*** | T |
| T22 | PR50B | 8 | D3*** | C | PR65B | 8 | D3*** | C |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| R22 | PR50A | 8 | D4*** | T | PR65A | 8 | D4*** | T |
| T15 | PR49B | 8 | D5*** | C | PR64B | 8 | D5*** | C |
| R17 | PR49A | 8 | D6*** | T | PR64A | 8 | D6*** | T |
| T20 | PR48B | 8 | D7/SPID0*** | C | PR63B | 8 | D7/SPID0*** | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| T21 | PR48A | 8 | DI/CSSPI0N*** | T | PR63A | 8 | DI/CSSPI0N*** | T |
| R21 | PR47B | 8 | DOUT/CSON/CSSPI1N*** | C | PR62B | 8 | DOUT/CSON/CSSPI1N*** | C |
| R20 | PR47A | 8 | BUSY/SISPI*** | T | PR62A | 8 | BUSY/SISPI*** | T |
| R16 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| R18 | PR45B | 3 | RLM0_GDLLC_FB_A | C | PR60B | 3 | RLM0_GDLLC_FB_A/RDQ57 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| R19 | PR45A | 3 | RLM0_GDLLT_FB_A | T | PR60A | 3 | RLM0_GDLLT_FB_A/RDQ57 | T |
| P22 | PR44B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR59B | 3 | RLM0_GDLLC_IN_A**/RDQ57 | C (LVDS)* |
| P21 | PR44A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR59A | 3 | RLM0_GDLLT_IN_A**/RDQ57 | T (LVDS)* |
| P16 | PR43B | 3 | RLM0_GPLLC_IN_A** | C | PR58B | 3 | RLM0_GPLLC_IN_A**/RDQ57 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| P17 | PR43A | 3 | RLM0_GPLLT_IN_A** | T | PR58A | 3 | RLM0_GPLLT_IN_A**/RDQ57 | T |
| P20 | PR42B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR57B | 3 | RLM0_GPLLC_FB_A/RDQ57 | C (LVDS)* |
| P19 | PR42A | 3 | RLM0_GPLLT_FB_A | T (LVDS)* | PR57A | 3 | RLM0_GPLLT_FB_A/RDQS57**** | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| - | - | - | | | VCCIO3 | 3 | | |
| P18 | PR41B | 3 | RDQ38 | C | PR51B | 3 | RDQ48 | C |
| N16 | PR41A | 3 | RDQ38 | T | PR51A | 3 | RDQ48 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| N22 | PR40B | 3 | RDQ38 | C (LVDS)* | PR50B | 3 | RDQ48 | C (LVDS)* |
| N21 | PR40A | 3 | RDQ38 | T (LVDS)* | PR50A | 3 | RDQ48 | T (LVDS)* |
| N17 | PR39B | 3 | RDQ38 | C | PR49B | 3 | RDQ48 | C |
| N18 | PR39A | 3 | RDQ38 | T | PR49A | 3 | RDQ48 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M22 | PR38B | 3 | RDQ38 | C (LVDS)* | PR48B | 3 | RDQ48 | C (LVDS)* |
| M21 | PR38A | 3 | RDQS38 | T (LVDS)* | PR48A | 3 | RDQS48 | T (LVDS)* |
| M16 | PR37B | 3 | RDQ38 | C | PR47B | 3 | RDQ48 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| M17 | PR37A | 3 | RDQ38 | T | PR47A | 3 | RDQ48 | T |
| M20 | PR36B | 3 | RDQ38 | C (LVDS)* | PR46B | 3 | RDQ48 | C (LVDS)* |
| M19 | PR36A | 3 | RDQ38 | T (LVDS)* | PR46A | 3 | RDQ48 | T (LVDS)* |
| M18 | PR35B | 3 | RDQ38 | C | PR45B | 3 | RDQ48 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| L16 | PR35A | 3 | RDQ38 | T | PR45A | 3 | RDQ48 | T |
| L22 | PR34B | 3 | RDQ38 | C (LVDS)* | PR44B | 3 | RDQ48 | C (LVDS)* |
| L21 | PR34A | 3 | RDQ38 | T (LVDS)* | PR44A | 3 | RDQ48 | T (LVDS)* |
| K22 | PR32B | 3 | RLM1_SPLLC_FB_A | C | PR42B | 3 | RLM2_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| K21 | PR32A | 3 | RLM1_SPLLT_FB_A | T | PR42A | 3 | RLM2_SPLLT_FB_A | T |
| L17 | PR31B | 3 | RLM1_SPLLC_IN_A | C (LVDS)* | PR41B | 3 | RLM2_SPLLC_IN_A | C (LVDS)* |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L18 | PR31A | 3 | RLM1_SPLLT_IN_A | T (LVDS)* | PR41A | 3 | RLM2_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| L20 | PR30B | 3 | | C | PR40B | 3 | | C |
| L19 | PR30A | 3 | | T | PR40A | 3 | | T |
| K16 | PR29B | 3 | | C (LVDS)* | PR39B | 3 | | C (LVDS)* |
| K17 | PR29A | 3 | | T (LVDS)* | PR39A | 3 | | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| J16 | PR28B | 3 | VREF2_3 | C | PR38B | 3 | VREF2_3 | C |
| K18 | PR28A | 3 | VREF1_3 | T | PR38A | 3 | VREF1_3 | T |
| J22 | PR27B | 3 | PCLKC3_0 | C (LVDS)* | PR37B | 3 | PCLKC3_0 | C (LVDS)* |
| J21 | PR27A | 3 | PCLKT3_0 | T (LVDS)* | PR37A | 3 | PCLKT3_0 | T (LVDS)* |
| H22 | PR25B | 2 | PCLKC2_0/RDQ22 | C | PR35B | 2 | PCLKC2_0/RDQ32 | C |
| H21 | PR25A | 2 | PCLKT2_0/RDQ22 | T | PR35A | 2 | PCLKT2_0/RDQ32 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| J17 | PR24B | 2 | RDQ22 | C (LVDS)* | PR34B | 2 | RDQ32 | C (LVDS)* |
| J18 | PR24A | 2 | RDQ22 | T (LVDS)* | PR34A | 2 | RDQ32 | T (LVDS)* |
| J20 | PR23B | 2 | RDQ22 | C | PR33B | 2 | RDQ32 | C |
| J19 | PR23A | 2 | RDQ22 | T | PR33A | 2 | RDQ32 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H16 | PR22B | 2 | RDQ22 | C (LVDS)* | PR32B | 2 | RDQ32 | C (LVDS)* |
| H17 | PR22A | 2 | RDQS22 | T (LVDS)* | PR32A | 2 | RDQS32 | T (LVDS)* |
| G22 | PR21B | 2 | RDQ22 | C | PR31B | 2 | RDQ32 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| G21 | PR21A | 2 | RDQ22 | T | PR31A | 2 | RDQ32 | T |
| H20 | PR20B | 2 | RDQ22 | C (LVDS)* | PR30B | 2 | RDQ32 | C (LVDS)* |
| H19 | PR20A | 2 | RDQ22 | T (LVDS)* | PR30A | 2 | RDQ32 | T (LVDS)* |
| G16 | PR19B | 2 | RUM1_SPLLC_FB_A/RDQ22 | C | PR29B | 2 | RUM1_SPLLC_FB_A/RDQ32 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H18 | PR19A | 2 | RUM1_SPLLT_FB_A/RDQ22 | T | PR29A | 2 | RUM1_SPLLT_FB_A/RDQ32 | T |
| F22 | PR18B | 2 | RUM1_SPLLC_IN_A/RDQ22 | C (LVDS)* | PR28B | 2 | RUM1_SPLLC_IN_A/RDQ32 | C (LVDS)* |
| F21 | PR18A | 2 | RUM1_SPLLT_IN_A/RDQ22 | T (LVDS)* | PR28A | 2 | RUM1_SPLLT_IN_A/RDQ32 | T (LVDS)* |
| GNDIO | GNDIO2 | - | | | - | - | | |
| G20 | PR16B | 2 | | C | PR26B | 2 | RDQ23 | C |
| VCCIO | VCCIO2 | 2 | | | - | - | | |
| F20 | PR16A | 2 | | T | PR26A | 2 | RDQ23 | T |
| - | - | - | | | GNDIO2 | - | | |
| G17 | PR15B | 2 | | C (LVDS)* | PR25B | 2 | RDQ23 | C (LVDS)* |
| F17 | PR15A | 2 | | T (LVDS)* | PR25A | 2 | RDQ23 | T (LVDS)* |
| - | - | - | | | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR14B | 2 | | C | PR14B | 2 | RDQ15 | C |
| D22 | PR14A | 2 | | T | PR14A | 2 | RDQ15 | T |
| E20 | PR13B | 2 | | C (LVDS)* | PR13B | 2 | RDQ15 | C (LVDS)* |
| D20 | PR13A | 2 | | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| D19 | PR12B | 2 | RUM0_SPLLC_FB_A | C | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| E19 | PR12A | 2 | RUM0_SPLLT_FB_A | T | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| F18 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F19 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| E18 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| D18 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | - | - | | |
| F16 | XRES | - | | | XRES | - | | |
| C22 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A21 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B22 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B21 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C19 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A18 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A19 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B18 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C18 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B17 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C17 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A17 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C21 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B20 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C20 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A20 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B16 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| E17 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D17 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C16 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A12 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| C12 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B12 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C11 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A15 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C15 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B15 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C14 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B14 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| A13 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A14 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C13 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B11 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B10 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A11 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C10 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E13 | PT28B | 1 | | C | PT46B | 1 | | C |
| D12 | PT28A | 1 | | T | PT46A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A9 | PT27B | 1 | | C | PT45B | 1 | | C |
| A8 | PT27A | 1 | | T | PT45A | 1 | | T |
| A7 | PT26B | 1 | | C | PT44B | 1 | | C |
| A6 | PT26A | 1 | | T | PT44A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E12 | PT25B | 1 | | C | PT43B | 1 | | C |
| F12 | PT25A | 1 | | T | PT43A | 1 | | T |
| A5 | PT24B | 1 | | C | PT42B | 1 | | C |
| A4 | PT24A | 1 | | T | PT42A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| B7 | PT23B | 1 | | C | PT41B | 1 | | C |
| B8 | PT23A | 1 | | T | PT41A | 1 | | T |
| G11 | PT22B | 1 | | C | PT40B | 1 | | C |
| E11 | PT22A | 1 | | T | PT40A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D11 | PT21B | 1 | VREF2_1 | C | PT39B | 1 | VREF2_1 | C |
| D10 | PT21A | 1 | VREF1_1 | T | PT39A | 1 | VREF1_1 | T |
| F11 | PT20A | 1 | PCLKT1_0 | T | PT38A | 1 | PCLKT1_0 | T |
| G10 | PT20B | 1 | PCLKC1_0 | C | PT38B | 1 | PCLKC1_0 | C |
| G9 | PT19B | 0 | PCLKC0_0 | C | PT37B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| F9 | PT19A | 0 | PCLKT0_0 | T | PT37A | 0 | PCLKT0_0 | T |
| C9 | PT18B | 0 | VREF2_0 | C | PT36B | 0 | VREF2_0 | C |
| D9 | PT18A | 0 | VREF1_0 | T | PT36A | 0 | VREF1_0 | T |
| A2 | PT17B | 0 | | C | PT35B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| A3 | PT17A | 0 | | T | PT35A | 0 | | T |
| B3 | PT16B | 0 | | C | PT34B | 0 | | C |
| C4 | PT16A | 0 | | T | PT34A | 0 | | T |
| E10 | PT15B | 0 | | C | PT33B | 0 | | C |
| F10 | PT15A | 0 | | T | PT33A | 0 | | T |
| C7 | PT14B | 0 | | C | PT32B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| B6 | PT14A | 0 | | T | PT32A | 0 | | T |
| C6 | PT13B | 0 | | C | PT31B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C5 | PT13A | 0 | | T | PT31A | 0 | | T |
| C8 | PT12B | 0 | | C | PT30B | 0 | | C |
| D8 | PT12A | 0 | | T | PT30A | 0 | | T |
| E8 | PT11B | 0 | | C | PT29B | 0 | | C |
| E9 | PT11A | 0 | | T | PT29A | 0 | | T |
| - | - | - | | | GNDIO0 | - | | |
| - | - | - | | | VCCIO0 | 0 | | |
| F8 | PT10B | 0 | | C | PT10B | 0 | | C |
| G8 | PT10A | 0 | | T | PT10A | 0 | | T |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| F7 | PT9B | 0 | | C | PT9B | 0 | | C |
| G7 | PT9A | 0 | | T | PT9A | 0 | | T |
| C3 | PT8B | 0 | | C | PT8B | 0 | | C |
| D4 | PT8A | 0 | | T | PT8A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F6 | PT7B | 0 | | C | PT7B | 0 | | C |
| E6 | PT7A | 0 | | T | PT7A | 0 | | T |
| E5 | PT6B | 0 | | C | PT6B | 0 | | C |
| D6 | PT6A | 0 | | T | PT6A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| D3 | PT5B | 0 | | C | PT5B | 0 | | C |
| E3 | PT5A | 0 | | T | PT5A | 0 | | T |
| D5 | PT4B | 0 | | C | PT4B | 0 | | C |
| E4 | PT4A | 0 | | T | PT4A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C2 | PT3B | 0 | | C | PT3B | 0 | | C |
| B2 | PT3A | 0 | | T | PT3A | 0 | | T |
| B1 | PT2B | 0 | | C | PT2B | 0 | | C |
| C1 | PT2A | 0 | | T | PT2A | 0 | | T |
| R8 | VCCPLL | - | | | VCCPLL | - | | |
| H15 | VCCPLL | - | | | VCCPLL | - | | |
| H8 | VCCPLL | - | | | VCCPLL | - | | |
| R15 | VCCPLL | - | | | VCCPLL | - | | |
| J10 | VCC | - | | | VCC | - | | |
| J11 | VCC | - | | | VCC | - | | |
| J12 | VCC | - | | | VCC | - | | |
| J13 | VCC | - | | | VCC | - | | |
| K14 | VCC | - | | | VCC | - | | |
| K9 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L9 | VCC | - | | | VCC | - | | |
| M14 | VCC | - | | | VCC | - | | |
| M9 | VCC | - | | | VCC | - | | |
| N14 | VCC | - | | | VCC | - | | |
| N9 | VCC | - | | | VCC | - | | |
| P10 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P12 | VCC | - | | | VCC | - | | |
| P13 | VCC | - | | | VCC | - | | |
| B5 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E7 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D13 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K19 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N19 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| P15 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| R14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W13 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA5 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| R9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V7 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| W10 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| N4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T5 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| E2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G5 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AA22 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| U19 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| H11 | VCCAUX | - | | | VCCAUX | - | | |
| H12 | VCCAUX | - | | | VCCAUX | - | | |
| L15 | VCCAUX | - | | | VCCAUX | - | | |
| L8 | VCCAUX | - | | | VCCAUX | - | | |
| M15 | VCCAUX | - | | | VCCAUX | - | | |
| M8 | VCCAUX | - | | | VCCAUX | - | | |
| R11 | VCCAUX | - | | | VCCAUX | - | | |
| R12 | VCCAUX | - | | | VCCAUX | - | | |
| A1 | GND | - | | | GND | - | | |
| A10 | GND | - | | | GND | - | | |
| A16 | GND | - | | | GND | - | | |
| A22 | GND | - | | | GND | - | | |
| AA19 | GND | - | | | GND | - | | |
| AA4 | GND | - | | | GND | - | | |
| AB1 | GND | - | | | GND | - | | |
| AB22 | GND | - | | | GND | - | | |
| B13 | GND | - | | | GND | - | | |
| B19 | GND | - | | | GND | - | | |
| B4 | GND | - | | | GND | - | | |
| D16 | GND | - | | | GND | - | | |
| D2 | GND | - | | | GND | - | | |
| D21 | GND | - | | | GND | - | | |
| D7 | GND | - | | | GND | - | | |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G19 | GND | - | | | GND | - | | |
| G4 | GND | - | | | GND | - | | |
| H10 | GND | - | | | GND | - | | |
| H13 | GND | - | | | GND | - | | |
| J14 | GND | - | | | GND | - | | |
| J9 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K12 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K15 | GND | - | | | GND | - | | |
| K20 | GND | - | | | GND | - | | |
| K3 | GND | - | | | GND | - | | |
| K8 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |
| L12 | GND | - | | | GND | - | | |
| L13 | GND | - | | | GND | - | | |
| M10 | GND | - | | | GND | - | | |
| M11 | GND | - | | | GND | - | | |
| M12 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N11 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N20 | GND | - | | | GND | - | | |
| N3 | GND | - | | | GND | - | | |
| N8 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P9 | GND | - | | | GND | - | | |
| R10 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| T19 | GND | - | | | GND | - | | |
| T4 | GND | - | | | GND | - | | |
| W16 | GND | - | | | GND | - | | |
| W2 | GND | - | | | GND | - | | |
| W21 | GND | - | | | GND | - | | |
| W7 | GND | - | | | GND | - | | |
| Y10 | GND | - | | | GND | - | | |
| Y13 | GND | - | | | GND | - | | |
| D15 | NC | - | | | NC | - | | |
| G14 | NC | - | | | NC | - | | |
| G15 | NC | - | | | NC | - | | |
| D14 | NC | - | | | NC | - | | |
| E15 | NC | - | | | NC | - | | |
| E14 | NC | - | | | NC | - | | |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F15 | NC | - | | | NC | - | | |
| F14 | NC | - | | | NC | - | | |
| F13 | NC | - | | | NC | - | | |
| G12 | NC | - | | | NC | - | | |
| G13 | NC | - | | | NC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated sysCONFIG pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| D1 | PL2A | 7 | LDQ6 | T (LVDS)* |
| E1 | PL2B | 7 | LDQ6 | C (LVDS)* |
| F1 | PL3A | 7 | LDQ6 | T |
| F2 | PL3B | 7 | LDQ6 | C |
| F5 | PL4A | 7 | LDQ6 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | |
| G6 | PL4B | 7 | LDQ6 | C (LVDS)* |
| F4 | PL5A | 7 | LDQ6 | T |
| F3 | PL5B | 7 | LDQ6 | C |
| G1 | PL6A | 7 | LDQS6 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | |
| G2 | PL6B | 7 | LDQ6 | C (LVDS)* |
| H1 | PL7A | 7 | LDQ6 | T |
| H2 | PL7B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | |
| H7 | PL8A | 7 | LDQ6 | T (LVDS)* |
| H6 | PL8B | 7 | LDQ6 | C (LVDS)* |
| G3 | PL9A | 7 | VREF2_7/LDQ6 | T |
| H3 | PL9B | 7 | VREF1_7/LDQ6 | C |
| GNDIO | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| H5 | PL11A | 7 | LUM0_SPLLT_IN_A | T (LVDS)* |
| H4 | PL11B | 7 | LUM0_SPLLC_IN_A | C (LVDS)* |
| J1 | PL12A | 7 | LUM0_SPLLT_FB_A | T |
| J2 | PL12B | 7 | LUM0_SPLLC_FB_A | C |
| GNDIO | GNDIO7 | - | | |
| J3 | PL13A | 7 | | T (LVDS)* |
| J4 | PL13B | 7 | | C (LVDS)* |
| J7 | PL14A | 7 | | T |
| VCCIO | VCCIO7 | 7 | | |
| J6 | PL14B | 7 | | C |
| GNDIO | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| K1 | PL32A | 7 | LUM3_SPLLT_IN_A/LDQ36 | T (LVDS)* |
| K2 | PL32B | 7 | LUM3_SPLLC_IN_A/LDQ36 | C (LVDS)* |
| J5 | PL33A | 7 | LUM3_SPLLT_FB_A/LDQ36 | T |
| K5 | PL33B | 7 | LUM3_SPLLC_FB_A/LDQ36 | C |
| VCCIO | VCCIO7 | 7 | | |
| K7 | PL34A | 7 | LDQ36 | T (LVDS)* |
| K6 | PL34B | 7 | LDQ36 | C (LVDS)* |
| L6 | PL35A | 7 | LDQ36 | T |
| L7 | PL35B | 7 | LDQ36 | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| GNDIO | GNDIO7 | - | | |
| L1 | PL36A | 7 | LDQS36 | T (LVDS)* |
| L2 | PL36B | 7 | LDQ36 | C (LVDS)* |
| M7 | PL37A | 7 | LDQ36 | T |
| VCCIO | VCCIO7 | 7 | | |
| L5 | PL37B | 7 | LDQ36 | C |
| L3 | PL38A | 7 | LDQ36 | T (LVDS)* |
| L4 | PL38B | 7 | LDQ36 | C (LVDS)* |
| M1 | PL39A | 7 | PCLKT7_0/LDQ36 | T |
| GNDIO | GNDIO7 | - | | |
| M2 | PL39B | 7 | PCLKC7_0/LDQ36 | C |
| M6 | PL41A | 6 | PCLKT6_0 | T (LVDS)* |
| M5 | PL41B | 6 | PCLKC6_0 | C (LVDS)* |
| M3 | PL42A | 6 | VREF2_6 | T |
| M4 | PL42B | 6 | VREF1_6 | C |
| VCCIO | VCCIO6 | 6 | | |
| N7 | PL45A | 6 | LLM3_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| N6 | PL45B | 6 | LLM3_SPLLC_IN_A | C (LVDS)* |
| N1 | PL46A | 6 | LLM3_SPLLT_FB_A | T |
| N2 | PL46B | 6 | LLM3_SPLLC_FB_A | C |
| VCCIO | VCCIO6 | 6 | | |
| GNDIO | GNDIO6 | - | | |
| P6 | PL52A | 6 | LDQS52**** | T (LVDS)* |
| N5 | PL52B | 6 | LDQ52 | C (LVDS)* |
| P1 | PL53A | 6 | LDQ52 | T |
| VCCIO | VCCIO6 | 6 | | |
| P2 | PL53B | 6 | LDQ52 | C |
| P3 | PL54A | 6 | LDQ52 | T (LVDS)* |
| P4 | PL54B | 6 | LDQ52 | C (LVDS)* |
| P5 | PL55A | 6 | LDQ52 | T |
| GNDIO | GNDIO6 | - | | |
| P7 | PL55B | 6 | LDQ52 | C |
| VCCIO | VCCIO6 | 6 | | |
| GNDIO | GNDIO6 | - | | |
| R1 | PL62A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| R2 | PL62B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* |
| R3 | PL63A | 6 | LLM0_GPLLT_FB_A | T |
| R4 | PL63B | 6 | LLM0_GPLLC_FB_A | C |
| VCCIO | VCCIO6 | 6 | | |
| R6 | PL64A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* |
| R5 | PL64B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| T1 | PL65A | 6 | LLM0_GDLLT_FB_A | T |
| T2 | PL65B | 6 | LLM0_GDLLC_FB_A | C |
| GNDIO | GNDIO6 | - | | |
| R7 | LLM0_PLLCAP | 6 | | |
| T6 | PL67A | 6 | LDQ71 | T (LVDS)* |
| T7 | PL67B | 6 | LDQ71 | C (LVDS)* |
| U1 | PL68A | 6 | LDQ71 | T |
| U2 | PL68B | 6 | LDQ71 | C |
| VCCIO | VCCIO6 | 6 | | |
| T3 | PL69A | 6 | LDQ71 | T (LVDS)* |
| U3 | PL69B | 6 | LDQ71 | C (LVDS)* |
| U6 | PL70A | 6 | LDQ71 | T |
| U5 | PL70B | 6 | LDQ71 | C |
| GNDIO | GNDIO6 | - | | |
| V5 | PL71A | 6 | LDQS71 | T (LVDS)* |
| U4 | PL71B | 6 | LDQ71 | C (LVDS)* |
| V1 | PL72A | 6 | LDQ71 | T |
| VCCIO | VCCIO6 | 6 | | |
| V3 | PL72B | 6 | LDQ71 | C |
| W1 | PL73A | 6 | LDQ71 | T (LVDS)* |
| Y1 | PL73B | 6 | LDQ71 | C (LVDS)* |
| AA1 | PL74A | 6 | LDQ71 | T |
| GNDIO | GNDIO6 | - | | |
| AA2 | PL74B | 6 | LDQ71 | C |
| V4 | TCK | - | | |
| Y2 | TDI | - | | |
| Y3 | TMS | - | | |
| W3 | TDO | - | | |
| W4 | VCCJ | - | | |
| W5 | PB2A | 5 | BDQ6 | T |
| Y4 | PB2B | 5 | BDQ6 | C |
| W6 | PB3A | 5 | BDQ6 | T |
| V6 | PB3B | 5 | BDQ6 | C |
| AA3 | PB4A | 5 | BDQ6 | T |
| AB2 | PB4B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | |
| T8 | PB5A | 5 | BDQ6 | T |
| U7 | PB5B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | |
| U8 | PB6A | 5 | BDQS6 | T |
| T9 | PB6B | 5 | BDQ6 | C |
| V8 | PB7A | 5 | BDQ6 | T |
| W8 | PB7B | 5 | BDQ6 | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| Y6 | PB8A | 5 | BDQ6 | T |
| Y5 | PB8B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | |
| AB3 | PB9A | 5 | BDQ6 | T |
| AB4 | PB9B | 5 | BDQ6 | C |
| AB5 | PB10A | 5 | BDQ6 | T |
| AA6 | PB10B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | |
| VCCIO | VCCIO5 | 5 | | |
| V9 | PB40A | 5 | BDQ42 | T |
| U9 | PB40B | 5 | BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | |
| U10 | PB41A | 5 | BDQ42 | T |
| T10 | PB41B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | |
| W9 | PB42A | 5 | BDQS42**** | T |
| Y8 | PB42B | 5 | BDQ42 | C |
| AA7 | PB43A | 5 | VREF2_5/BDQ42 | T |
| Y7 | PB43B | 5 | VREF1_5/BDQ42 | C |
| AB6 | PB44A | 5 | PCLKT5_0/BDQ42 | T |
| AB7 | PB44B | 5 | PCLKC5_0/BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | |
| AA8 | PB49A | 4 | PCLKT4_0/BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | |
| AB8 | PB49B | 4 | PCLKC4_0/BDQ51 | C |
| AA9 | PB50A | 4 | VREF2_4/BDQ51 | T |
| Y9 | PB50B | 4 | VREF1_4/BDQ51 | C |
| AB9 | PB51A | 4 | BDQS51**** | T |
| GNDIO | GNDIO4 | - | | |
| AB10 | PB51B | 4 | BDQ51 | C |
| AA10 | PB52A | 4 | BDQ51 | T |
| Y11 | PB52B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | |
| V10 | PB56A | 4 | BDQ60 | T |
| U11 | PB56B | 4 | BDQ60 | C |
| V11 | PB57A | 4 | BDQ60 | T |
| W11 | PB57B | 4 | BDQ60 | C |
| AA11 | PB58A | 4 | BDQ60 | T |
| AB11 | PB58B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | |
| T11 | PB59A | 4 | BDQ60 | T |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| U12 | PB59B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | |
| AA12 | PB60A | 4 | BDQS60 | T |
| Y12 | PB60B | 4 | BDQ60 | C |
| V12 | PB61A | 4 | BDQ60 | T |
| W12 | PB61B | 4 | BDQ60 | C |
| AB12 | PB62A | 4 | BDQ60 | T |
| AA13 | PB62B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | |
| T12 | PB63A | 4 | BDQ60 | T |
| U13 | PB63B | 4 | BDQ60 | C |
| V13 | PB64A | 4 | BDQ60 | T |
| T13 | PB64B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | |
| AB13 | PB65A | 4 | BDQ69 | T |
| AB14 | PB65B | 4 | BDQ69 | C |
| U14 | PB66A | 4 | BDQ69 | T |
| T14 | PB66B | 4 | BDQ69 | C |
| AA14 | PB67A | 4 | BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | |
| Y14 | PB67B | 4 | BDQ69 | C |
| W14 | PB68A | 4 | BDQ69 | T |
| V14 | PB68B | 4 | BDQ69 | C |
| AB15 | PB69A | 4 | BDQS69 | T |
| GNDIO | GNDIO4 | - | | |
| AA15 | PB69B | 4 | BDQ69 | C |
| V15 | PB70A | 4 | BDQ69 | T |
| U15 | PB70B | 4 | BDQ69 | C |
| AB16 | PB71A | 4 | BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | |
| AA16 | PB71B | 4 | BDQ69 | C |
| AB17 | PB72A | 4 | BDQ69 | T |
| AA17 | PB72B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | |
| W20 | CFG2 | 8 | | |
| V20 | CFG1 | 8 | | |
| V19 | CFG0 | 8 | | |
| V22 | PROGRAMN | 8 | | |
| W22 | CCLK | 8 | | |
| U18 | INITN | 8 | | |
| U22 | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | |
| U20 | WRITEN*** | 8 | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| U21 | CS1N*** | 8 | | |
| U17 | CSN*** | 8 | | |
| U16 | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | |
| T16 | D1*** | 8 | | |
| T17 | D2*** | 8 | | |
| T22 | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | |
| R22 | D4*** | 8 | | |
| T15 | D5*** | 8 | | |
| R17 | D6*** | 8 | | |
| T20 | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | |
| T21 | DI/CSSPI0N*** | 8 | | |
| R21 | DOUT/CSON/CSSPI1N*** | 8 | | |
| R20 | BUSY/SISPI*** | 8 | | |
| R16 | RLM0_PLLCAP | 3 | | |
| R18 | PR65B | 3 | RLM0_GDLLC_FB_A | C |
| GNDIO | GNDIO3 | - | | |
| R19 | PR65A | 3 | RLM0_GDLLT_FB_A | T |
| P22 | PR64B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* |
| P21 | PR64A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* |
| P16 | PR63B | 3 | RLM0_GPLLC_IN_A** | C |
| VCCIO | VCCIO3 | 3 | | |
| P17 | PR63A | 3 | RLM0_GPLLT_IN_A** | T |
| P20 | PR62B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* |
| P19 | PR62A | 3 | RLM0_GPLLT_FB_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | |
| P18 | PR55B | 3 | RDQ52 | C |
| N16 | PR55A | 3 | RDQ52 | T |
| GNDIO | GNDIO3 | - | | |
| N22 | PR54B | 3 | RDQ52 | C (LVDS)* |
| N21 | PR54A | 3 | RDQ52 | T (LVDS)* |
| N17 | PR53B | 3 | RDQ52 | C |
| N18 | PR53A | 3 | RDQ52 | T |
| VCCIO | VCCIO3 | 3 | | |
| M22 | PR52B | 3 | RDQ52 | C (LVDS)* |
| M21 | PR52A | 3 | RDQS52 | T (LVDS)* |
| M16 | PR51B | 3 | RDQ52 | C |
| GNDIO | GNDIO3 | - | | |
| M17 | PR51A | 3 | RDQ52 | T |
| M20 | PR50B | 3 | RDQ52 | C (LVDS)* |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| M19 | PR50A | 3 | RDQ52 | T (LVDS)* |
| M18 | PR49B | 3 | RDQ52 | C |
| VCCIO | VCCIO3 | 3 | | |
| L16 | PR49A | 3 | RDQ52 | T |
| L22 | PR48B | 3 | RDQ52 | C (LVDS)* |
| L21 | PR48A | 3 | RDQ52 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| K22 | PR46B | 3 | RLM3_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | |
| K21 | PR46A | 3 | RLM3_SPLLT_FB_A | T |
| L17 | PR45B | 3 | RLM3_SPLLC_IN_A | C (LVDS)* |
| L18 | PR45A | 3 | RLM3_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| L20 | PR44B | 3 | | C |
| L19 | PR44A | 3 | | T |
| K16 | PR43B | 3 | | C (LVDS)* |
| K17 | PR43A | 3 | | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| J16 | PR42B | 3 | VREF2_3 | C |
| K18 | PR42A | 3 | VREF1_3 | T |
| J22 | PR41B | 3 | PCLKC3_0 | C (LVDS)* |
| J21 | PR41A | 3 | PCLKT3_0 | T (LVDS)* |
| H22 | PR39B | 2 | PCLKC2_0/RDQ36 | C |
| H21 | PR39A | 2 | PCLKT2_0/RDQ36 | T |
| GNDIO | GNDIO2 | - | | |
| J17 | PR38B | 2 | RDQ36 | C (LVDS)* |
| J18 | PR38A | 2 | RDQ36 | T (LVDS)* |
| J20 | PR37B | 2 | RDQ36 | C |
| J19 | PR37A | 2 | RDQ36 | T |
| VCCIO | VCCIO2 | 2 | | |
| H16 | PR36B | 2 | RDQ36 | C (LVDS)* |
| H17 | PR36A | 2 | RDQS36 | T (LVDS)* |
| G22 | PR35B | 2 | RDQ36 | C |
| GNDIO | GNDIO2 | - | | |
| G21 | PR35A | 2 | RDQ36 | T |
| H20 | PR34B | 2 | RDQ36 | C (LVDS)* |
| H19 | PR34A | 2 | RDQ36 | T (LVDS)* |
| G16 | PR33B | 2 | RUM3_SPLLC_FB_A/RDQ36 | C |
| VCCIO | VCCIO2 | 2 | | |
| H18 | PR33A | 2 | RUM3_SPLLT_FB_A/RDQ36 | T |
| F22 | PR32B | 2 | RUM3_SPLLC_IN_A/RDQ36 | C (LVDS)* |
| F21 | PR32A | 2 | RUM3_SPLLT_IN_A/RDQ36 | T (LVDS)* |
| G20 | PR30B | 2 | RDQ27 | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| F20 | PR30A | 2 | RDQ27 | T |
| GNDIO | GNDIO2 | - | | |
| G17 | PR29B | 2 | RDQ27 | C (LVDS)* |
| F17 | PR29A | 2 | RDQ27 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | |
| E22 | PR14B | 2 | | C |
| D22 | PR14A | 2 | | T |
| VCCIO | VCCIO2 | - | | |
| E20 | PR13B | 2 | | C (LVDS)* |
| D20 | PR13A | 2 | | T (LVDS)* |
| D19 | PR12B | 2 | RUM0_SPLLC_FB_A | C |
| GNDIO | GNDIO2 | - | | |
| E19 | PR12A | 2 | RUM0_SPLLT_FB_A | T |
| F18 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* |
| F19 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* |
| VCCIO | VCCIO2 | - | | |
| E18 | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | |
| D18 | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | |
| F16 | XRES | - | | |
| C22 | URC_SQ_VCCRX0 | 12 | | |
| A21 | URC_SQ_HDINP0 | 12 | | T |
| B22 | URC_SQ_VCCIB0 | 12 | | |
| B21 | URC_SQ_HDINN0 | 12 | | C |
| C19 | URC_SQ_VCCTX0 | 12 | | |
| A18 | URC_SQ_HDOUTP0 | 12 | | T |
| A19 | URC_SQ_VCCOB0 | 12 | | |
| B18 | URC_SQ_HDOUTN0 | 12 | | C |
| C18 | URC_SQ_VCCTX1 | 12 | | |
| B17 | URC_SQ_HDOUTN1 | 12 | | C |
| C17 | URC_SQ_VCCOB1 | 12 | | |
| A17 | URC_SQ_HDOUTP1 | 12 | | T |
| C21 | URC_SQ_VCCRX1 | 12 | | |
| B20 | URC_SQ_HDINN1 | 12 | | C |
| C20 | URC_SQ_VCCIB1 | 12 | | |
| A20 | URC_SQ_HDINP1 | 12 | | T |
| B16 | URC_SQ_VCCAUX33 | 12 | | |
| E17 | URC_SQ_REFCLKN | 12 | | C |
| D17 | URC_SQ_REFCLKP | 12 | | T |
| C16 | URC_SQ_VCCP | 12 | | |
| A12 | URC_SQ_HDINP2 | 12 | | T |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| C12 | URC_SQ_VCCIB2 | 12 | | |
| B12 | URC_SQ_HDINN2 | 12 | | C |
| C11 | URC_SQ_VCCRX2 | 12 | | |
| A15 | URC_SQ_HDOUTP2 | 12 | | T |
| C15 | URC_SQ_VCCOB2 | 12 | | |
| B15 | URC_SQ_HDOUTN2 | 12 | | C |
| C14 | URC_SQ_VCCTX2 | 12 | | |
| B14 | URC_SQ_HDOUTN3 | 12 | | C |
| A13 | URC_SQ_VCCOB3 | 12 | | |
| A14 | URC_SQ_HDOUTP3 | 12 | | T |
| C13 | URC_SQ_VCCTX3 | 12 | | |
| B11 | URC_SQ_HDINN3 | 12 | | C |
| B10 | URC_SQ_VCCIB3 | 12 | | |
| A11 | URC_SQ_HDINP3 | 12 | | T |
| C10 | URC_SQ_VCCRX3 | 12 | | |
| GNDIO | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | |
| E13 | PT55B | 1 | | C |
| D12 | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| A9 | PT54B | 1 | | C |
| A8 | PT54A | 1 | | T |
| A7 | PT53B | 1 | | C |
| A6 | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| E12 | PT52B | 1 | | C |
| F12 | PT52A | 1 | | T |
| A5 | PT51B | 1 | | C |
| A4 | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| B7 | PT50B | 1 | | C |
| B8 | PT50A | 1 | | T |
| G11 | PT49B | 1 | | C |
| E11 | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| D11 | PT48B | 1 | VREF2_1 | C |
| D10 | PT48A | 1 | VREF1_1 | T |
| G10 | PT47B | 1 | PCLKC1_0 | C |
| F11 | PT47A | 1 | PCLKT1_0 | T |
| G9 | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | |
| F9 | PT46A | 0 | PCLKT0_0 | T |
| C9 | PT45B | 0 | VREF2_0 | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| D9 | PT45A | 0 | VREF1_0 | T |
| A2 | PT44B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| A3 | PT44A | 0 | | T |
| B3 | PT43B | 0 | | C |
| C4 | PT43A | 0 | | T |
| E10 | PT42B | 0 | | C |
| F10 | PT42A | 0 | | T |
| C7 | PT41B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| B6 | PT41A | 0 | | T |
| C6 | PT40B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| C5 | PT40A | 0 | | T |
| C8 | PT39B | 0 | | C |
| D8 | PT39A | 0 | | T |
| E8 | PT38B | 0 | | C |
| E9 | PT38A | 0 | | T |
| GNDIO | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | |
| F8 | PT10B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| G8 | PT10A | 0 | | T |
| F7 | PT9B | 0 | | C |
| G7 | PT9A | 0 | | T |
| C3 | PT8B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| D4 | PT8A | 0 | | T |
| F6 | PT7B | 0 | | C |
| E6 | PT7A | 0 | | T |
| E5 | PT6B | 0 | | C |
| D6 | PT6A | 0 | | T |
| D3 | PT5B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| E3 | PT5A | 0 | | T |
| D5 | PT4B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| E4 | PT4A | 0 | | T |
| C2 | PT3B | 0 | | C |
| B2 | PT3A | 0 | | T |
| B1 | PT2B | 0 | | C |
| C1 | PT2A | 0 | | T |
| J10 | VCC | - | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| J11 | VCC | - | | |
| J12 | VCC | - | | |
| J13 | VCC | - | | |
| K14 | VCC | - | | |
| K9 | VCC | - | | |
| L14 | VCC | - | | |
| L9 | VCC | - | | |
| M14 | VCC | - | | |
| M9 | VCC | - | | |
| N14 | VCC | - | | |
| N9 | VCC | - | | |
| P10 | VCC | - | | |
| P11 | VCC | - | | |
| P12 | VCC | - | | |
| P13 | VCC | - | | |
| B5 | VCCIO0 | 0 | | |
| B9 | VCCIO0 | 0 | | |
| E7 | VCCIO0 | 0 | | |
| H9 | VCCIO0 | 0 | | |
| D13 | VCCIO1 | 1 | | |
| E16 | VCCIO1 | 1 | | |
| H14 | VCCIO1 | 1 | | |
| E21 | VCCIO2 | 2 | | |
| G18 | VCCIO2 | 2 | | |
| J15 | VCCIO2 | 2 | | |
| K19 | VCCIO2 | 2 | | |
| N19 | VCCIO3 | 3 | | |
| P15 | VCCIO3 | 3 | | |
| T18 | VCCIO3 | 3 | | |
| V21 | VCCIO3 | 3 | | |
| AA18 | VCCIO4 | 4 | | |
| R14 | VCCIO4 | 4 | | |
| V16 | VCCIO4 | 4 | | |
| W13 | VCCIO4 | 4 | | |
| AA5 | VCCIO5 | 5 | | |
| R9 | VCCIO5 | 5 | | |
| V7 | VCCIO5 | 5 | | |
| W10 | VCCIO5 | 5 | | |
| N4 | VCCIO6 | 6 | | |
| P8 | VCCIO6 | 6 | | |
| T5 | VCCIO6 | 6 | | |
| V2 | VCCIO6 | 6 | | |
| E2 | VCCIO7 | 7 | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| G5 | VCCIO7 | 7 | | |
| J8 | VCCIO7 | 7 | | |
| K4 | VCCIO7 | 7 | | |
| AA22 | VCCIO8 | 8 | | |
| U19 | VCCIO8 | 8 | | |
| H11 | VCCAUX | - | | |
| H12 | VCCAUX | - | | |
| L15 | VCCAUX | - | | |
| L8 | VCCAUX | - | | |
| M15 | VCCAUX | - | | |
| M8 | VCCAUX | - | | |
| R11 | VCCAUX | - | | |
| R12 | VCCAUX | - | | |
| A1 | GND | - | | |
| A10 | GND | - | | |
| A16 | GND | - | | |
| A22 | GND | - | | |
| AA19 | GND | - | | |
| AA4 | GND | - | | |
| AB1 | GND | - | | |
| AB22 | GND | - | | |
| B13 | GND | - | | |
| B19 | GND | - | | |
| B4 | GND | - | | |
| D16 | GND | - | | |
| D2 | GND | - | | |
| D21 | GND | - | | |
| D7 | GND | - | | |
| G19 | GND | - | | |
| G4 | GND | - | | |
| H10 | GND | - | | |
| H13 | GND | - | | |
| J14 | GND | - | | |
| J9 | GND | - | | |
| K10 | GND | - | | |
| K11 | GND | - | | |
| K12 | GND | - | | |
| K13 | GND | - | | |
| K15 | GND | - | | |
| K20 | GND | - | | |
| K3 | GND | - | | |
| K8 | GND | - | | |
| L10 | GND | - | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| L11 | GND | - | | |
| L12 | GND | - | | |
| L13 | GND | - | | |
| M10 | GND | - | | |
| M11 | GND | - | | |
| M12 | GND | - | | |
| M13 | GND | - | | |
| N10 | GND | - | | |
| N11 | GND | - | | |
| N12 | GND | - | | |
| N13 | GND | - | | |
| N15 | GND | - | | |
| N20 | GND | - | | |
| N3 | GND | - | | |
| N8 | GND | - | | |
| P14 | GND | - | | |
| P9 | GND | - | | |
| R10 | GND | - | | |
| R13 | GND | - | | |
| T19 | GND | - | | |
| T4 | GND | - | | |
| W16 | GND | - | | |
| W2 | GND | - | | |
| W21 | GND | - | | |
| W7 | GND | - | | |
| Y10 | GND | - | | |
| Y13 | GND | - | | |
| Y15 | NC | - | | |
| W15 | NC | - | | |
| AB20 | NC | - | | |
| AB21 | NC | - | | |
| AA21 | NC | - | | |
| AA20 | NC | - | | |
| AB19 | NC | - | | |
| AB18 | NC | - | | |
| Y22 | NC | - | | |
| Y21 | NC | - | | |
| Y17 | NC | - | | |
| Y18 | NC | - | | |
| Y16 | NC | - | | |
| W17 | NC | - | | |
| Y19 | NC | - | | |
| Y20 | NC | - | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| W19 | NC | - | | |
| W18 | NC | - | | |
| V17 | NC | - | | |
| V18 | NC | - | | |
| D15 | NC | - | | |
| G14 | NC | - | | |
| G15 | NC | - | | |
| D14 | NC | - | | |
| E15 | NC | - | | |
| E14 | NC | - | | |
| F15 | NC | - | | |
| F14 | NC | - | | |
| F13 | NC | - | | |
| G12 | NC | - | | |
| G13 | NC | - | | |
| H8 | VCCPLL | - | | |
| H15 | VCCPLL | - | | |
| R8 | VCCPLL | - | | |
| R15 | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C2 | PL2A | 7 | LDQ6 | T (LVDS)* | PL2A | 7 | LDQ6 | T* |
| C1 | PL2B | 7 | LDQ6 | C (LVDS)* | PL2B | 7 | LDQ6 | C* |
| F6 | PL3A | 7 | LDQ6 | T | PL3A | 7 | LDQ6 | T |
| H9 | PL3B | 7 | LDQ6 | C | PL3B | 7 | LDQ6 | C |
| D3 | PL4A | 7 | LDQ6 | T (LVDS)* | PL4A | 7 | LDQ6 | T* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| D2 | PL4B | 7 | LDQ6 | C (LVDS)* | PL4B | 7 | LDQ6 | C* |
| F5 | PL5A | 7 | LDQ6 | T | PL5A | 7 | LDQ6 | T |
| H8 | PL5B | 7 | LDQ6 | C | PL5B | 7 | LDQ6 | C |
| E3 | PL6A | 7 | LDQS6 | T (LVDS)* | PL6A | 7 | LDQS6 | T* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| E2 | PL6B | 7 | LDQ6 | C (LVDS)* | PL6B | 7 | LDQ6 | C* |
| J9 | PL7A | 7 | LDQ6 | T | PL7A | 7 | LDQ6 | T |
| E4 | PL7B | 7 | LDQ6 | C | PL7B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E1 | PL8A | 7 | LDQ6 | T (LVDS)* | PL8A | 7 | LDQ6 | T* |
| D1 | PL8B | 7 | LDQ6 | C (LVDS)* | PL8B | 7 | LDQ6 | C* |
| J8 | PL9A | 7 | VREF2_7/LDQ6 | T | PL9A | 7 | VREF2_7/LDQ6 | T |
| F4 | PL9B | 7 | VREF1_7/LDQ6 | C | PL9B | 7 | VREF1_7/LDQ6 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| - | - | - | | | VCCIO7 | 7 | | |
| F3 | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* | PL11A | 7 | LUM0_SPLLT_IN_A | T* |
| F1 | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* | PL11B | 7 | LUM0_SPLLC_IN_A | C* |
| G6 | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T | PL12A | 7 | LUM0_SPLLT_FB_A | T |
| K9 | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C | PL12B | 7 | LUM0_SPLLC_FB_A | C |
| - | - | - | | | GNDIO7 | - | | |
| G5 | PL13A | 7 | LDQ15 | T (LVDS)* | PL13A | 7 | | T* |
| VCCIO | VCCIO7 | 7 | | | - | - | | |
| G4 | PL13B | 7 | LDQ15 | C (LVDS)* | PL13B | 7 | | C* |
| H5 | PL14A | 7 | LDQ15 | T | PL14A | 7 | | T |
| - | - | - | | | VCCIO7 | 7 | | |
| H6 | PL14B | 7 | LDQ15 | C | PL14B | 7 | | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| J7 | PL16A | 7 | LDQ15 | T | PL19A | 7 | | T |
| H4 | PL16B | 7 | LDQ15 | C | PL19B | 7 | | C |
| H3 | PL17A | 7 | LDQ15 | T (LVDS)* | PL20A | 7 | | T* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G3 | PL17B | 7 | LDQ15 | C (LVDS)* | PL20B | 7 | | C* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| G1 | PL19A | 7 | LDQ23 | T (LVDS)* | PL23A | 7 | LDQ27 | T* |
| H1 | PL19B | 7 | LDQ23 | C (LVDS)* | PL23B | 7 | LDQ27 | C* |
| J3 | PL20A | 7 | LDQ23 | T | PL24A | 7 | LDQ27 | T |
| J4 | PL20B | 7 | LDQ23 | C | PL24B | 7 | LDQ27 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H2 | PL21A | 7 | LDQ23 | T (LVDS)* | PL25A | 7 | LDQ27 | T* |
| J2 | PL21B | 7 | LDQ23 | C (LVDS)* | PL25B | 7 | LDQ27 | C* |
| K7 | PL22A | 7 | LDQ23 | T | PL26A | 7 | LDQ27 | T |
| J6 | PL22B | 7 | LDQ23 | C | PL26B | 7 | LDQ27 | C |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| K5 | PL23A | 7 | LDQS23 | T (LVDS)* | PL27A | 7 | LDQS27 | T* |
| L5 | PL23B | 7 | LDQ23 | C (LVDS)* | PL27B | 7 | LDQ27 | C* |
| K4 | PL24A | 7 | LDQ23 | T | PL28A | 7 | LDQ27 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L4 | PL24B | 7 | LDQ23 | C | PL28B | 7 | LDQ27 | C |
| K3 | PL25A | 7 | LDQ23 | T (LVDS)* | PL29A | 7 | LDQ27 | T* |
| L3 | PL25B | 7 | LDQ23 | C (LVDS)* | PL29B | 7 | LDQ27 | C* |
| J1 | PL26A | 7 | LDQ23 | T | PL30A | 7 | LDQ27 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| K2 | PL26B | 7 | LDQ23 | C | PL30B | 7 | LDQ27 | C |
| K1 | PL28A | 7 | LUM1_SPLLT_IN_A/LDQ32 | T (LVDS)* | PL32A | 7 | LUM3_SPLLT_IN_A/LDQ36 | T* |
| L1 | PL28B | 7 | LUM1_SPLLC_IN_A/LDQ32 | C (LVDS)* | PL32B | 7 | LUM3_SPLLC_IN_A/LDQ36 | C* |
| K8 | PL29A | 7 | LUM1_SPLLT_FB_A/LDQ32 | T | PL33A | 7 | LUM3_SPLLT_FB_A/LDQ36 | T |
| M5 | PL29B | 7 | LUM1_SPLLC_FB_A/LDQ32 | C | PL33B | 7 | LUM3_SPLLC_FB_A/LDQ36 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M4 | PL30A | 7 | LDQ32 | T (LVDS)* | PL34A | 7 | LDQ36 | T* |
| M3 | PL30B | 7 | LDQ32 | C (LVDS)* | PL34B | 7 | LDQ36 | C* |
| L8 | PL31A | 7 | LDQ32 | T | PL35A | 7 | LDQ36 | T |
| M6 | PL31B | 7 | LDQ32 | C | PL35B | 7 | LDQ36 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M1 | PL32A | 7 | LDQS32 | T (LVDS)* | PL36A | 7 | LDQS36 | T* |
| N1 | PL32B | 7 | LDQ32 | C (LVDS)* | PL36B | 7 | LDQ36 | C* |
| N3 | PL33A | 7 | LDQ32 | T | PL37A | 7 | LDQ36 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N2 | PL33B | 7 | LDQ32 | C | PL37B | 7 | LDQ36 | C |
| N5 | PL34A | 7 | LDQ32 | T (LVDS)* | PL38A | 7 | LDQ36 | T* |
| N4 | PL34B | 7 | LDQ32 | C (LVDS)* | PL38B | 7 | LDQ36 | C* |
| M7 | PL35A | 7 | PCLKT7_0/LDQ32 | T | PL39A | 7 | PCLKT7_0/LDQ36 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M8 | PL35B | 7 | PCLKC7_0/LDQ32 | C | PL39B | 7 | PCLKC7_0/LDQ36 | C |
| P3 | PL37A | 6 | PCLKT6_0 | T (LVDS)* | PL41A | 6 | PCLKT6_0 | T* |
| P2 | PL37B | 6 | PCLKC6_0 | C (LVDS)* | PL41B | 6 | PCLKC6_0 | C* |
| P5 | PL38A | 6 | VREF2_6 | T | PL42A | 6 | VREF2_6 | T |
| N6 | PL38B | 6 | VREF1_6 | C | PL42B | 6 | VREF1_6 | C |
| P4 | PL39A | 6 | | T (LVDS)* | PL43A | 6 | | T* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R3 | PL39B | 6 | | C (LVDS)* | PL43B | 6 | | C* |
| P6 | PL40A | 6 | | T | PL44A | 6 | | T |
| N7 | NC | - | | | PL44B | 6 | | C |
| P1 | PL41A | 6 | LLM2_SPLLT_IN_A | T (LVDS)* | PL45A | 6 | LLM3_SPLLT_IN_A | T* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| R1 | PL41B | 6 | LLM2_SPLLC_IN_A | C (LVDS)* | PL45B | 6 | LLM3_SPLLC_IN_A | C* |
| N8 | PL42A | 6 | LLM2_SPLLT_FB_A | T | PL46A | 6 | LLM3_SPLLT_FB_A | T |
| R5 | PL42B | 6 | LLM2_SPLLC_FB_A | C | PL46B | 6 | LLM3_SPLLC_FB_A | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T3 | PL44A | 6 | LDQ48 | T (LVDS)* | PL48A | 6 | LDQ52 | T* |
| T4 | PL44B | 6 | LDQ48 | C (LVDS)* | PL48B | 6 | LDQ52 | C* |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| P8 | PL45A | 6 | LDQ48 | T | PL49A | 6 | LDQ52 | T |
| R6 | PL45B | 6 | LDQ48 | C | PL49B | 6 | LDQ52 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T1 | PL46A | 6 | LDQ48 | T (LVDS)* | PL50A | 6 | LDQ52 | T* |
| U1 | PL46B | 6 | LDQ48 | C (LVDS)* | PL50B | 6 | LDQ52 | C* |
| R7 | PL47A | 6 | LDQ48 | T | PL51A | 6 | LDQ52 | T |
| T5 | PL47B | 6 | LDQ48 | C | PL51B | 6 | LDQ52 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| U3 | PL48A | 6 | LDQS48 | T (LVDS)* | PL52A | 6 | LDQS52 | T* |
| U4 | PL48B | 6 | LDQ48 | C (LVDS)* | PL52B | 6 | LDQ52 | C* |
| U5 | PL49A | 6 | LDQ48 | T | PL53A | 6 | LDQ52 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U6 | PL49B | 6 | LDQ48 | C | PL53B | 6 | LDQ52 | C |
| U2 | PL50A | 6 | LDQ48 | T (LVDS)* | PL54A | 6 | LDQ52 | T* |
| V1 | PL50B | 6 | LDQ48 | C (LVDS)* | PL54B | 6 | LDQ52 | C* |
| W2 | PL51A | 6 | LDQ48 | T | PL55A | 6 | LDQ52 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| V2 | PL51B | 6 | LDQ48 | C | PL55B | 6 | LDQ52 | C |
| V4 | PL55A | 6 | LDQ57 | T (LVDS)* | PL59A | 6 | | T* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V3 | PL55B | 6 | LDQ57 | C (LVDS)* | PL59B | 6 | | C* |
| - | - | - | | | GNDIO6 | - | | |
| W4 | PL57A | 6 | LLM0_GPLLT_IN_A**/LDQS57**** | T (LVDS)* | PL62A | 6 | LLM0_GPLLT_IN_A | T* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| W3 | PL57B | 6 | LLM0_GPLLC_IN_A**/LDQ57 | C (LVDS)* | PL62B | 6 | LLM0_GPLLC_IN_A | C* |
| W1 | PL58A | 6 | LLM0_GPLLT_FB_A/LDQ57 | T | PL63A | 6 | LLM0_GPLLT_FB_A | T |
| Y1 | PL58B | 6 | LLM0_GPLLC_FB_A/LDQ57 | C | PL63B | 6 | LLM0_GPLLC_FB_A | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AA1 | PL59A | 6 | LLM0_GDLLT_IN_A**/LDQ57 | T (LVDS)* | PL64A | 6 | LLM0_GDLLT_IN_A | T* |
| AB1 | PL59B | 6 | LLM0_GDLLC_IN_A**/LDQ57 | C (LVDS)* | PL64B | 6 | LLM0_GDLLC_IN_A | C* |
| U7 | PL60A | 6 | LLM0_GDLLT_FB_A/LDQ57 | T | PL65A | 6 | LLM0_GDLLT_FB_A | T |
| V6 | PL60B | 6 | LLM0_GDLLC_FB_A/LDQ57 | C | PL65B | 6 | LLM0_GDLLC_FB_A | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| T8 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| W5 | PL62A | 6 | LDQ66 | T (LVDS)* | PL67A | 6 | LDQ71 | T* |
| Y4 | PL62B | 6 | LDQ66 | C (LVDS)* | PL67B | 6 | LDQ71 | C* |
| U8 | PL63A | 6 | LDQ66 | T | PL68A | 6 | LDQ71 | T |
| W6 | PL63B | 6 | LDQ66 | C | PL68B | 6 | LDQ71 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y3 | PL64A | 6 | LDQ66 | T (LVDS)* | PL69A | 6 | LDQ71 | T* |
| AA3 | PL64B | 6 | LDQ66 | C (LVDS)* | PL69B | 6 | LDQ71 | C* |
| V7 | NC | - | | | PL70A | 6 | LDQ71 | T |
| Y5 | PL65B | 6 | LDQ66 | C | PL70B | 6 | LDQ71 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AB2 | PL66A | 6 | LDQS66 | T (LVDS)* | PL71A | 6 | LDQS71 | T* |
| AA4 | PL66B | 6 | LDQ66 | C (LVDS)* | PL71B | 6 | LDQ71 | C* |
| Y6 | PL67A | 6 | LDQ66 | T | PL72A | 6 | LDQ71 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U9 | PL67B | 6 | LDQ66 | C | PL72B | 6 | LDQ71 | C |
| AA5 | PL68A | 6 | LDQ66 | T (LVDS)* | PL73A | 6 | LDQ71 | T* |
| AA6 | PL68B | 6 | LDQ66 | C (LVDS)* | PL73B | 6 | LDQ71 | C* |
| Y7 | PL69A | 6 | LDQ66 | T | PL74A | 6 | LDQ71 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| V9 | PL69B | 6 | LDQ66 | C | PL74B | 6 | LDQ71 | C |
| AC3 | TCK | - | | | TCK | - | | |
| W8 | TDI | - | | | TDI | - | | |
| AC4 | TMS | - | | | TMS | - | | |
| V8 | TDO | - | | | TDO | - | | |
| AA7 | VCCJ | - | | | VCCJ | - | | |
| AB6 | PB2A | 5 | BDQ6 | T | PB2A | 5 | BDQ6 | T |
| Y8 | PB2B | 5 | BDQ6 | C | PB2B | 5 | BDQ6 | C |
| AD1 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| AD2 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| AC5 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| AA8 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC6 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| W9 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| AB7 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| Y9 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AD3 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| AD4 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA9 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| W10 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC7 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| Y10 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| AE2 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| AD5 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AE4 | PB11A | 5 | BDQ15 | T | PB11A | 5 | BDQ15 | T |
| AE3 | PB11B | 5 | BDQ15 | C | PB11B | 5 | BDQ15 | C |
| W11 | PB12A | 5 | BDQ15 | T | PB12A | 5 | BDQ15 | T |
| AB8 | PB12B | 5 | BDQ15 | C | PB12B | 5 | BDQ15 | C |
| AE5 | PB13A | 5 | BDQ15 | T | PB13A | 5 | BDQ15 | T |
| AD6 | PB13B | 5 | BDQ15 | C | PB13B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA10 | PB14A | 5 | BDQ15 | T | PB14A | 5 | BDQ15 | T |
| AC8 | PB14B | 5 | BDQ15 | C | PB14B | 5 | BDQ15 | C |
| W12 | PB15A | 5 | BDQS15 | T | PB15A | 5 | BDQS15 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AC9 | PB15B | 5 | BDQ15 | C | PB15B | 5 | BDQ15 | C |
| W13 | PB16A | 5 | BDQ15 | T | PB16A | 5 | BDQ15 | T |
| AB10 | PB16B | 5 | BDQ15 | C | PB16B | 5 | BDQ15 | C |
| AF3 | PB17A | 5 | BDQ15 | T | PB17A | 5 | BDQ15 | T |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AF4 | PB17B | 5 | BDQ15 | C | PB17B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AF5 | PB18A | 5 | BDQ15 | T | PB18A | 5 | BDQ15 | T |
| AF6 | PB18B | 5 | BDQ15 | C | PB18B | 5 | BDQ15 | C |
| Y12 | PB19A | 5 | BDQ15 | T | PB19A | 5 | BDQ15 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AB11 | PB19B | 5 | BDQ15 | C | PB19B | 5 | BDQ15 | C |
| - | - | - | | | VCCIO5 | 5 | | |
| - | - | - | | | GNDIO5 | - | | |
| AD7 | PB20A | 5 | BDQ24 | T | PB29A | 5 | BDQ33 | T |
| AF7 | PB20B | 5 | BDQ24 | C | PB29B | 5 | BDQ33 | C |
| AD8 | PB21A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| AA12 | PB21B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| AE8 | PB22A | 5 | BDQ24 | T | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AF8 | PB22B | 5 | BDQ24 | C | PB31B | 5 | BDQ33 | C |
| AD9 | PB23A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| AC10 | PB23B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| AC11 | PB24A | 5 | BDQS24 | T | PB33A | 5 | BDQS33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AB12 | PB24B | 5 | BDQ24 | C | PB33B | 5 | BDQ33 | C |
| AD10 | PB25A | 5 | BDQ24 | T | PB34A | 5 | BDQ33 | T |
| Y13 | PB25B | 5 | BDQ24 | C | PB34B | 5 | BDQ33 | C |
| AF9 | PB26A | 5 | BDQ24 | T | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE9 | PB26B | 5 | BDQ24 | C | PB35B | 5 | BDQ33 | C |
| AF10 | PB27A | 5 | BDQ24 | T | PB36A | 5 | BDQ33 | T |
| AE10 | PB27B | 5 | BDQ24 | C | PB36B | 5 | BDQ33 | C |
| AD11 | PB28A | 5 | BDQ24 | T | PB37A | 5 | BDQ33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AF11 | PB28B | 5 | BDQ24 | C | PB37B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AA13 | PB33A | 5 | BDQS33**** | T | PB42A | 5 | BDQS42**** | T |
| AB13 | PB33B | 5 | BDQ33 | C | PB42B | 5 | BDQ42 | C |
| W14 | PB34A | 5 | VREF2_5/BDQ33 | T | PB43A | 5 | VREF2_5/BDQ42 | T |
| AC12 | PB34B | 5 | VREF1_5/BDQ33 | C | PB43B | 5 | VREF1_5/BDQ42 | C |
| AF12 | PB35A | 5 | PCLKT5_0/BDQ33 | T | PB44A | 5 | PCLKT5_0/BDQ42 | T |
| AD12 | PB35B | 5 | PCLKC5_0/BDQ33 | C | PB44B | 5 | PCLKC5_0/BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AC13 | PB40A | 4 | PCLKT4_0/BDQ42 | T | PB49A | 4 | PCLKT4_0/BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y14 | PB40B | 4 | PCLKC4_0/BDQ42 | C | PB49B | 4 | PCLKC4_0/BDQ51 | C |
| AB20 | PB57A | 4 | BDQ60 | T | PB50A | 4 | VREF2_4/BDQ51 | T |
| AC14 | PB41B | 4 | VREF1_4/BDQ42 | C | PB50B | 4 | VREF1_4/BDQ51 | C |
| AB14 | PB42A | 4 | BDQS42**** | T | PB51A | 4 | BDQS51**** | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA14 | PB42B | 4 | BDQ42 | C | PB51B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W17 | PB65A | 4 | BDQ69 | T | PB56A | 4 | BDQ60 | T |
| AA19 | PB65B | 4 | BDQ69 | C | PB56B | 4 | BDQ60 | C |
| AC15 | PB48A | 4 | BDQ51 | T | PB57A | 4 | BDQ60 | T |
| Y18 | PB68B | 4 | BDQ69 | C | PB57B | 4 | BDQ60 | C |
| AB15 | PB49A | 4 | BDQ51 | T | PB58A | 4 | BDQ60 | T |
| AC16 | PB49B | 4 | BDQ51 | C | PB58B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA17 | PB60A | 4 | BDQS60**** | T | PB59A | 4 | BDQ60 | T |
| AB16 | PB50B | 4 | BDQ51 | C | PB59B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA15 | PB51A | 4 | BDQS51**** | T | PB60A | 4 | BDQS60 | T |
| W16 | PB59B | 4 | BDQ60 | C | PB60B | 4 | BDQ60 | C |
| Y15 | PB52A | 4 | BDQ51 | T | PB61A | 4 | BDQ60 | T |
| AC17 | PB52B | 4 | BDQ51 | C | PB61B | 4 | BDQ60 | C |
| AA18 | PB61A | 4 | BDQ60 | T | PB62A | 4 | BDQ60 | T |
| Y17 | PB61B | 4 | BDQ60 | C | PB62B | 4 | BDQ60 | C |
| - | - | - | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | - | - | | |
| W15 | PB54A | 4 | BDQ51 | T | PB63A | 4 | BDQ60 | T |
| AB17 | PB54B | 4 | BDQ51 | C | PB63B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V17 | PB73A | 4 | BDQ69 | T | PB72A | 4 | BDQ69 | T |
| AA20 | PB73B | 4 | BDQ69 | C | PB72B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AD13 | VCC | - | | | LRC_SQ_VCCRX3 | 13 | | |
| AF14 | PB47A | 4 | BDQ51 | T | LRC_SQ_HDINP3 | 13 | | T |
| AE13 | NC | - | | | LRC_SQ_VCCIB3 | 13 | | |
| AE14 | PB41A | 4 | VREF2_4/BDQ42 | T | LRC_SQ_HDINN3 | 13 | | C |
| AD16 | VCC | - | | | LRC_SQ_VCCTX3 | 13 | | |
| AF17 | PB51B | 4 | BDQ51 | C | LRC_SQ_HDOUTP3 | 13 | | T |
| AF16 | NC | - | | | LRC_SQ_VCCOB3 | 13 | | |
| AE17 | PB50A | 4 | BDQ51 | T | LRC_SQ_HDOUTN3 | 13 | | C |
| AD17 | VCC | - | | | LRC_SQ_VCCTX2 | 13 | | |
| AE18 | PB53B | 4 | BDQ51 | C | LRC_SQ_HDOUTN2 | 13 | | C |
| AD18 | NC | - | | | LRC_SQ_VCCOB2 | 13 | | |
| AF18 | PB53A | 4 | BDQ51 | T | LRC_SQ_HDOUTP2 | 13 | | T |
| AD14 | VCC | - | | | LRC_SQ_VCCRX2 | 13 | | |
| AE15 | PB48B | 4 | BDQ51 | C | LRC_SQ_HDINN2 | 13 | | C |
| AD15 | NC | - | | | LRC_SQ_VCCIB2 | 13 | | |
| AF15 | PB47B | 4 | BDQ51 | C | LRC_SQ_HDINP2 | 13 | | T |
| AD19 | VCC | - | | | LRC_SQ_VCCP | 13 | | |
| AC19 | PB57B | 4 | BDQ60 | C | LRC_SQ_REFCLKP | 13 | | T |
| AB19 | PB59A | 4 | BDQ60 | T | LRC_SQ_REFCLKN | 13 | | C |
| AE19 | VCCAUX | - | | | LRC_SQ_VCCAUX33 | 13 | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AF23 | PB64A | 4 | BDQ60 | T | LRC_SQ_HDINP1 | 13 | | T |
| AD23 | NC | - | | | LRC_SQ_VCCIB1 | 13 | | |
| AE23 | PB66B | 4 | BDQ69 | C | LRC_SQ_HDINN1 | 13 | | C |
| AD24 | VCC | - | | | LRC_SQ_VCCRX1 | 13 | | |
| AF20 | PB55A | 4 | BDQ51 | T | LRC_SQ_HDOUTP1 | 13 | | T |
| AD20 | NC | - | | | LRC_SQ_VCCOB1 | 13 | | |
| AE20 | PB55B | 4 | BDQ51 | C | LRC_SQ_HDOUTN1 | 13 | | C |
| AD21 | VCC | - | | | LRC_SQ_VCCTX1 | 13 | | |
| AE21 | PB63B | 4 | BDQ60 | C | LRC_SQ_HDOUTN0 | 13 | | C |
| AF22 | NC | - | | | LRC_SQ_VCCOB0 | 13 | | |
| AF21 | PB62A | 4 | BDQ60 | T | LRC_SQ_HDOUTP0 | 13 | | T |
| AD22 | VCC | - | | | LRC_SQ_VCCTX0 | 13 | | |
| AE24 | PB67B | 4 | BDQ69 | C | LRC_SQ_HDINN0 | 13 | | C |
| AE25 | NC | - | | | LRC_SQ_VCCIB0 | 13 | | |
| AF24 | PB67A | 4 | BDQ69 | T | LRC_SQ_HDINP0 | 13 | | T |
| AD25 | VCC | - | | | LRC_SQ_VCCRX0 | 13 | | |
| AA21 | CFG2 | 8 | | | CFG2 | 8 | | |
| AA22 | CFG1 | 8 | | | CFG1 | 8 | | |
| AB23 | CFG0 | 8 | | | CFG0 | 8 | | |
| AC26 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| AB24 | CCLK | 8 | | | CCLK | 8 | | |
| AA23 | INITN | 8 | | | INITN | 8 | | |
| AB25 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| Y19 | PR68B | 8 | WRITEN*** | C | WRITEN*** | 8 | | |
| Y21 | PR68A | 8 | CS1N*** | T | CS1N*** | 8 | | |
| AB26 | PR67B | 8 | CSN*** | C | CSN*** | 8 | | |
| Y22 | PR67A | 8 | D0/SPIFASTN*** | T | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | | 8 | | |
| W19 | PR66B | 8 | D1*** | C | D1*** | 8 | | |
| Y20 | PR66A | 8 | D2*** | T | D2*** | 8 | | |
| W22 | PR65B | 8 | D3*** | C | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | | | - | | |
| W18 | PR65A | 8 | D4*** | T | D4*** | 8 | | |
| Y23 | PR64B | 8 | D5*** | C | D5*** | 8 | | |
| AA24 | PR64A | 8 | D6*** | T | D6*** | 8 | | |
| W21 | PR63B | 8 | D7/SPID0*** | C | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| V20 | PR63A | 8 | DI/CSSPI0N*** | T | DI/CSSPI0N*** | 8 | | |
| W23 | PR62B | 8 | DOUT/CSON/CSSPI1N*** | C | DOUT/CSON/ CSSPI1N*** | 8 | | |
| Y24 | PR62A | 8 | BUSY/SISPI*** | T | BUSY/SISPI*** | 8 | | |
| V19 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| V21 | PR60B | 3 | RLM0_GDLLC_FB_A | C | PR65B | 3 | RLM0_GDLLC_FB_A | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| U19 | PR60A | 3 | RLM0_GDLLT_FB_A/RDQ57 | T | PR65A | 3 | RLM0_GDLLT_FB_A | T |
| AA26 | PR59B | 3 | RLM0_GDLLC_IN_A**/RDQ57 | C (LVDS)* | PR64B | 3 | RLM0_GDLLC_IN_A | C* |
| Y26 | PR59A | 3 | RLM0_GDLLT_IN_A**/RDQ57 | T (LVDS)* | PR64A | 3 | RLM0_GDLLT_IN_A | T* |
| V23 | PR58B | 3 | RLM0_GPLLC_IN_A**/RDQ57 | C | PR63B | 3 | RLM0_GPLLC_IN_A | C |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U20 | PR58A | 3 | RLM0_GPLLT_IN_A**/RDQ57 | T | PR63A | 3 | RLM0_GPLLT_IN_A | T |
| W24 | PR57B | 3 | RLM0_GPLLC_FB_A/RDQ57 | C (LVDS)* | PR62B | 3 | RLM0_GPLLC_FB_A | C* |
| V24 | PR57A | 3 | RLM0_GPLLT_FB_A/RDQS57 | T (LVDS)* | PR62A | 3 | RLM0_GPLLT_FB_A | T* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| U21 | PR56A | 3 | RDQ57 | T | PR60A | 3 | | T |
| W25 | PR55B | 3 | RDQ57 | C (LVDS)* | PR59B | 3 | | C* |
| W26 | PR55A | 3 | RDQ57 | T (LVDS)* | PR59A | 3 | | T* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U18 | PR54B | 3 | RDQ57 | C | PR58B | 3 | | C |
| U22 | PR54A | 3 | RDQ57 | T | PR58A | 3 | | T |
| V25 | PR53B | 3 | RDQ57 | C (LVDS)* | PR57B | 3 | | C* |
| V26 | PR53A | 3 | RDQ57 | T (LVDS)* | PR57A | 3 | | T* |
| U24 | PR51B | 3 | RDQ48 | C | PR55B | 3 | RDQ52 | C |
| T24 | PR51A | 3 | RDQ48 | T | PR55A | 3 | RDQ52 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| T22 | PR50B | 3 | RDQ48 | C (LVDS)* | PR54B | 3 | RDQ52 | C* |
| T23 | PR50A | 3 | RDQ48 | T (LVDS)* | PR54A | 3 | RDQ52 | T* |
| U25 | PR49B | 3 | RDQ48 | C | PR53B | 3 | RDQ52 | C |
| U26 | PR49A | 3 | RDQ48 | T | PR53A | 3 | RDQ52 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T19 | PR48B | 3 | RDQ48 | C (LVDS)* | PR52B | 3 | RDQ52 | C* |
| R19 | PR48A | 3 | RDQS48 | T (LVDS)* | PR52A | 3 | RDQS52 | T* |
| R21 | PR47B | 3 | RDQ48 | C | PR51B | 3 | RDQ52 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| R20 | PR47A | 3 | RDQ48 | T | PR51A | 3 | RDQ52 | T |
| T26 | PR46B | 3 | RDQ48 | C (LVDS)* | PR50B | 3 | RDQ52 | C* |
| R26 | PR46A | 3 | RDQ48 | T (LVDS)* | PR50A | 3 | RDQ52 | T* |
| P21 | PR45B | 3 | RDQ48 | C | PR49B | 3 | RDQ52 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| P19 | PR45A | 3 | RDQ48 | T | PR49A | 3 | RDQ52 | T |
| R23 | PR44B | 3 | RDQ48 | C (LVDS)* | PR48B | 3 | RDQ52 | C* |
| R24 | PR44A | 3 | RDQ48 | T (LVDS)* | PR48A | 3 | RDQ52 | T* |
| - | - | - | | | GNDIO3 | - | | |
| R22 | PR42B | 3 | RLM2_SPLLC_FB_A | C | PR46B | 3 | RLM3_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| N19 | PR42A | 3 | RLM2_SPLLT_FB_A | T | PR46A | 3 | RLM3_SPLLT_FB_A | T |
| P23 | PR41B | 3 | RLM2_SPLLC_IN_A | C (LVDS)* | PR45B | 3 | RLM3_SPLLC_IN_A | C* |
| P24 | PR41A | 3 | RLM2_SPLLT_IN_A | T (LVDS)* | PR45A | 3 | RLM3_SPLLT_IN_A | T* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| N21 | PR40B | 3 | | C | PR44B | 3 | | C |
| P22 | PR40A | 3 | | T | PR44A | 3 | | T |
| N20 | PR39B | 3 | | C (LVDS)* | PR43B | 3 | | C* |
| N22 | PR39A | 3 | | T (LVDS)* | PR43A | 3 | | T* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| P25 | PR38B | 3 | VREF2_3 | C | PR42B | 3 | VREF2_3 | C |
| P26 | PR38A | 3 | VREF1_3 | T | PR42A | 3 | VREF1_3 | T |
| M21 | PR37B | 3 | PCLKC3_0 | C (LVDS)* | PR41B | 3 | PCLKC3_0 | C* |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N23 | PR37A | 3 | PCLKT3_0 | T (LVDS)* | PR41A | 3 | PCLKT3_0 | T* |
| N24 | PR35B | 2 | PCLKC2_0/RDQ32 | C | PR39B | 2 | PCLKC2_0/RDQ36 | C |
| N25 | PR35A | 2 | PCLKT2_0/RDQ32 | T | PR39A | 2 | PCLKT2_0/RDQ36 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| M22 | PR34B | 2 | RDQ32 | C (LVDS)* | PR38B | 2 | RDQ36 | C* |
| M24 | PR34A | 2 | RDQ32 | T (LVDS)* | PR38A | 2 | RDQ36 | T* |
| M23 | PR33B | 2 | RDQ32 | C | PR37B | 2 | RDQ36 | C |
| N26 | PR33A | 2 | RDQ32 | T | PR37A | 2 | RDQ36 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L22 | PR32B | 2 | RDQ32 | C (LVDS)* | PR36B | 2 | RDQ36 | C* |
| L24 | PR32A | 2 | RDQS32 | T (LVDS)* | PR36A | 2 | RDQS36 | T* |
| L23 | PR31B | 2 | RDQ32 | C | PR35B | 2 | RDQ36 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| M20 | PR31A | 2 | RDQ32 | T | PR35A | 2 | RDQ36 | T |
| M26 | PR30B | 2 | RDQ32 | C (LVDS)* | PR34B | 2 | RDQ36 | C* |
| L26 | PR30A | 2 | RDQ32 | T (LVDS)* | PR34A | 2 | RDQ36 | T* |
| K22 | PR29B | 2 | RUM1_SPLLC_FB_A/RDQ32 | C | PR33B | 2 | RUM3_SPLLC_FB_A/RDQ36 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M19 | PR29A | 2 | RUM1_SPLLT_FB_A/RDQ32 | T | PR33A | 2 | RUM3_SPLLT_FB_A/RDQ36 | T |
| K25 | PR28B | 2 | RUM1_SPLLC_IN_A/RDQ32 | C (LVDS)* | PR32B | 2 | RUM3_SPLLC_IN_A/RDQ36 | C* |
| K26 | PR28A | 2 | RUM1_SPLLT_IN_A/RDQ32 | T (LVDS)* | PR32A | 2 | RUM3_SPLLT_IN_A/RDQ36 | T* |
| K24 | PR26B | 2 | RDQ23 | C | PR30B | 2 | RDQ27 | C |
| K23 | PR26A | 2 | RDQ23 | T | PR30A | 2 | RDQ27 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| L19 | PR25B | 2 | RDQ23 | C (LVDS)* | PR29B | 2 | RDQ27 | C* |
| K21 | PR25A | 2 | RDQ23 | T (LVDS)* | PR29A | 2 | RDQ27 | T* |
| J23 | PR24B | 2 | RDQ23 | C | PR28B | 2 | RDQ27 | C |
| J24 | PR24A | 2 | RDQ23 | T | PR28A | 2 | RDQ27 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K20 | PR23B | 2 | RDQ23 | C (LVDS)* | PR27B | 2 | RDQ27 | C* |
| J21 | PR23A | 2 | RDQS23 | T (LVDS)* | PR27A | 2 | RDQS27 | T* |
| H21 | PR22B | 2 | RDQ23 | C | PR26B | 2 | RDQ27 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| K18 | PR22A | 2 | RDQ23 | T | PR26A | 2 | RDQ27 | T |
| H22 | PR21B | 2 | RDQ23 | C (LVDS)* | PR25B | 2 | RDQ27 | C* |
| J20 | PR21A | 2 | RDQ23 | T (LVDS)* | PR25A | 2 | RDQ27 | T* |
| J25 | PR20B | 2 | RDQ23 | C | PR24B | 2 | RDQ27 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J26 | PR20A | 2 | RDQ23 | T | PR24A | 2 | RDQ27 | T |
| G21 | PR19B | 2 | RDQ23 | C (LVDS)* | PR23B | 2 | RDQ27 | C* |
| J19 | PR19A | 2 | RDQ23 | T (LVDS)* | PR23A | 2 | RDQ27 | T* |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| H23 | PR18B | 2 | RDQ15 | C | PR21B | 2 | | C |
| H24 | PR18A | 2 | RDQ15 | T | PR21A | 2 | | T |
| H25 | PR17B | 2 | RDQ15 | C (LVDS)* | PR20B | 2 | | C* |
| H26 | PR17A | 2 | RDQ15 | T (LVDS)* | PR20A | 2 | | T* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G22 | PR16B | 2 | RDQ15 | C | PR19B | 2 | | C |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K19 | PR16A | 2 | RDQ15 | T | PR19A | 2 | | T |
| G24 | PR15B | 2 | RDQ15 | C (LVDS)* | PR18B | 2 | | C* |
| G23 | PR15A | 2 | RDQS15 | T (LVDS)* | PR18A | 2 | | T* |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| J18 | PR14B | 2 | RDQ15 | C | PR14B | 2 | | C |
| F22 | PR14A | 2 | RDQ15 | T | PR14A | 2 | | T |
| - | - | - | | | VCCIO2 | 2 | | |
| F23 | PR13B | 2 | RDQ15 | C (LVDS)* | PR13B | 2 | | C* |
| F24 | PR13A | 2 | RDQ15 | T (LVDS)* | PR13A | 2 | | T* |
| VCCIO | VCCIO2 | 2 | | | - | - | | |
| H20 | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C | PR12B | 2 | RUM0_SPLLC_FB_A | C |
| - | - | - | | | GNDIO2 | - | | |
| F21 | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T | PR12A | 2 | RUM0_SPLLT_FB_A | T |
| G26 | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A | C* |
| F26 | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A | T* |
| - | - | - | | | VCCIO2 | 2 | | |
| E24 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| E23 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO2 | 2 | | |
| H19 | XRES | - | | | XRES | - | | |
| C25 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A24 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B25 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B24 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C22 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A21 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A22 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B21 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C21 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B20 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C20 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A20 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C24 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B23 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C23 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A23 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B19 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| E19 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D19 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C19 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A15 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C15 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B15 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C14 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A18 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C18 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B18 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C17 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B17 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| A16 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A17 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C16 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B14 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B13 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A14 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C13 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |
| - | - | - | | | GNDIO1 | - | | |
| - | - | - | | | VCCIO1 | 1 | | |
| E17 | PT46B | 1 | | C | PT55B | 1 | | C |
| D17 | PT46A | 1 | | T | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| F17 | PT45B | 1 | | C | PT54B | 1 | | C |
| D16 | PT45A | 1 | | T | PT54A | 1 | | T |
| F19 | PT44B | 1 | | C | PT53B | 1 | | C |
| F18 | PT44A | 1 | | T | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E16 | PT43B | 1 | | C | PT52B | 1 | | C |
| D15 | PT43A | 1 | | T | PT52A | 1 | | T |
| G18 | PT42B | 1 | | C | PT51B | 1 | | C |
| E15 | PT42A | 1 | | T | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| G17 | PT41B | 1 | | C | PT50B | 1 | | C |
| E14 | PT41A | 1 | | T | PT50A | 1 | | T |
| D14 | PT40B | 1 | | C | PT49B | 1 | | C |
| D13 | PT40A | 1 | | T | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F15 | PT39B | 1 | VREF2_1 | C | PT48B | 1 | VREF2_1 | C |
| E12 | PT39A | 1 | VREF1_1 | T | PT48A | 1 | VREF1_1 | T |
| H17 | PT38B | 1 | PCLKC1_0 | C | PT47B | 1 | PCLKC1_0 | C |
| E13 | PT38A | 1 | PCLKT1_0 | T | PT47A | 1 | PCLKT1_0 | T |
| C12 | PT37B | 0 | PCLKC0_0 | C | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| G15 | PT37A | 0 | PCLKT0_0 | T | PT46A | 0 | PCLKT0_0 | T |
| C11 | PT36B | 0 | VREF2_0 | C | PT45B | 0 | VREF2_0 | C |
| F14 | PT36A | 0 | VREF1_0 | T | PT45A | 0 | VREF1_0 | T |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A12 | PT35B | 0 | | C | PT44B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| A11 | PT35A | 0 | | T | PT44A | 0 | | T |
| D12 | PT34B | 0 | | C | PT43B | 0 | | C |
| H16 | PT34A | 0 | | T | PT43A | 0 | | T |
| H18 | PT33B | 0 | | C | PT42B | 0 | | C |
| H15 | PT33A | 0 | | T | PT42A | 0 | | T |
| A10 | PT32B | 0 | | C | PT41B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| B10 | PT32A | 0 | | T | PT41A | 0 | | T |
| D11 | PT31B | 0 | | C | PT40B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G14 | PT31A | 0 | | T | PT40A | 0 | | T |
| E11 | PT30B | 0 | | C | PT39B | 0 | | C |
| F13 | PT30A | 0 | | T | PT39A | 0 | | T |
| D10 | PT29B | 0 | | C | PT38B | 0 | | C |
| H14 | PT29A | 0 | | T | PT38A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| A9 | PT24B | 0 | | C | PT24B | 0 | | C |
| C10 | PT23B | 0 | | C | PT23B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| E8 | PT23A | 0 | | T | PT23A | 0 | | T |
| B9 | PT22B | 0 | | C | PT22B | 0 | | C |
| A8 | PT22A | 0 | | T | PT22A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F12 | PT21B | 0 | | C | PT21B | 0 | | C |
| E10 | PT21A | 0 | | T | PT21A | 0 | | T |
| G13 | PT20B | 0 | | C | PT20B | 0 | | C |
| C9 | PT20A | 0 | | T | PT20A | 0 | | T |
| B8 | PT19B | 0 | | C | PT19B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| A7 | PT19A | 0 | | T | PT19A | 0 | | T |
| D9 | PT18B | 0 | | C | PT18B | 0 | | C |
| H13 | PT18A | 0 | | T | PT18A | 0 | | T |
| D6 | PT17B | 0 | | C | PT17B | 0 | | C |
| C7 | PT17A | 0 | | T | PT17A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C8 | PT16B | 0 | | C | PT16B | 0 | | C |
| G12 | PT16A | 0 | | T | PT16A | 0 | | T |
| D8 | PT15B | 0 | | C | PT15B | 0 | | C |
| H12 | PT15A | 0 | | T | PT15A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| A6 | PT14B | 0 | | C | PT14B | 0 | | C |
| A5 | PT14A | 0 | | T | PT14A | 0 | | T |
| A4 | PT13B | 0 | | C | PT13B | 0 | | C |
| A3 | PT13A | 0 | | T | PT13A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C6 | PT12B | 0 | | C | PT12B | 0 | | C |
| F10 | PT12A | 0 | | T | PT12A | 0 | | T |
| D7 | PT11B | 0 | | C | PT11B | 0 | | C |
| H11 | PT11A | 0 | | T | PT11A | 0 | | T |
| D5 | PT10B | 0 | | C | PT10B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| E6 | PT10A | 0 | | T | PT10A | 0 | | T |
| G10 | PT9B | 0 | | C | PT9B | 0 | | C |
| F9 | PT9A | 0 | | T | PT9A | 0 | | T |
| H10 | PT8B | 0 | | C | PT8B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E7 | PT8A | 0 | | T | PT8A | 0 | | T |
| B3 | PT7B | 0 | | C | PT7B | 0 | | C |
| C5 | PT7A | 0 | | T | PT7A | 0 | | T |
| B2 | PT6B | 0 | | C | PT6B | 0 | | C |
| C4 | PT6A | 0 | | T | PT6A | 0 | | T |
| G9 | PT5B | 0 | | C | PT5B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| F7 | PT5A | 0 | | T | PT5A | 0 | | T |
| C3 | PT4B | 0 | | C | PT4B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D4 | PT4A | 0 | | T | PT4A | 0 | | T |
| J10 | PT3B | 0 | | C | PT3B | 0 | | C |
| F8 | PT3A | 0 | | T | PT3A | 0 | | T |
| G8 | PT2B | 0 | | C | PT2B | 0 | | C |
| G7 | PT2A | 0 | | T | PT2A | 0 | | T |
| L12 | VCC | - | | | VCC | - | | |
| L13 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L15 | VCC | - | | | VCC | - | | |
| M11 | VCC | - | | | VCC | - | | |
| M12 | VCC | - | | | VCC | - | | |
| M15 | VCC | - | | | VCC | - | | |
| M16 | VCC | - | | | VCC | - | | |
| N11 | VCC | - | | | VCC | - | | |
| N16 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P16 | VCC | - | | | VCC | - | | |
| R11 | VCC | - | | | VCC | - | | |
| R12 | VCC | - | | | VCC | - | | |
| R15 | VCC | - | | | VCC | - | | |
| R16 | VCC | - | | | VCC | - | | |
| T12 | VCC | - | | | VCC | - | | |
| T13 | VCC | - | | | VCC | - | | |
| T14 | VCC | - | | | VCC | - | | |
| T15 | VCC | - | | | VCC | - | | |
| B12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B7 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F11 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J13 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 1 | | |
| D18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M17 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| P18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R17 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| Y25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V13 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE7 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| U12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P9 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T6 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| G2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AC24 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| U17 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| J11 | VCCAUX | - | | | VCCAUX | - | | |
| J12 | VCCAUX | - | | | VCCAUX | - | | |
| J15 | VCCAUX | - | | | VCCAUX | - | | |
| J16 | VCCAUX | - | | | VCCAUX | - | | |
| L18 | VCCAUX | - | | | VCCAUX | - | | |
| L9 | VCCAUX | - | | | VCCAUX | - | | |
| M18 | VCCAUX | - | | | VCCAUX | - | | |
| M9 | VCCAUX | - | | | VCCAUX | - | | |
| R18 | VCCAUX | - | | | VCCAUX | - | | |
| R9 | VCCAUX | - | | | VCCAUX | - | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T18 | VCCAUX | - | | | VCCAUX | - | | |
| T9 | VCCAUX | - | | | VCCAUX | - | | |
| V11 | VCCAUX | - | | | VCCAUX | - | | |
| V12 | VCCAUX | - | | | VCCAUX | - | | |
| V15 | VCCAUX | - | | | VCCAUX | - | | |
| V16 | VCCAUX | - | | | VCCAUX | - | | |
| A13 | GND | - | | | GND | - | | |
| A19 | GND | - | | | GND | - | | |
| A2 | GND | - | | | GND | - | | |
| A25 | GND | - | | | GND | - | | |
| AA2 | GND | - | | | GND | - | | |
| AA25 | GND | - | | | GND | - | | |
| AB18 | GND | - | | | GND | - | | |
| AB22 | GND | - | | | GND | - | | |
| AB5 | GND | - | | | GND | - | | |
| AB9 | GND | - | | | GND | - | | |
| AE1 | GND | - | | | GND | - | | |
| AE11 | GND | - | | | GND | - | | |
| AE16 | GND | - | | | GND | - | | |
| AE22 | GND | - | | | GND | - | | |
| AE26 | GND | - | | | GND | - | | |
| AE6 | GND | - | | | GND | - | | |
| AF13 | GND | - | | | GND | - | | |
| AF19 | GND | - | | | GND | - | | |
| AF2 | GND | - | | | GND | - | | |
| AF25 | GND | - | | | GND | - | | |
| B1 | GND | - | | | GND | - | | |
| B11 | GND | - | | | GND | - | | |
| B16 | GND | - | | | GND | - | | |
| B22 | GND | - | | | GND | - | | |
| B26 | GND | - | | | GND | - | | |
| B6 | GND | - | | | GND | - | | |
| E18 | GND | - | | | GND | - | | |
| E22 | GND | - | | | GND | - | | |
| E5 | GND | - | | | GND | - | | |
| E9 | GND | - | | | GND | - | | |
| F2 | GND | - | | | GND | - | | |
| F25 | GND | - | | | GND | - | | |
| G11 | GND | - | | | GND | - | | |
| G16 | GND | - | | | GND | - | | |
| J22 | GND | - | | | GND | - | | |
| J5 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K14 | GND | - | | | GND | - | | |
| K16 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L16 | GND | - | | | GND | - | | |
| L17 | GND | - | | | GND | - | | |
| L2 | GND | - | | | GND | - | | |
| L20 | GND | - | | | GND | - | | |
| L25 | GND | - | | | GND | - | | |
| L7 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M14 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N14 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| P10 | GND | - | | | GND | - | | |
| P12 | GND | - | | | GND | - | | |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T2 | GND | - | | | GND | - | | |
| T20 | GND | - | | | GND | - | | |
| T25 | GND | - | | | GND | - | | |
| T7 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| V22 | GND | - | | | GND | - | | |
| V5 | GND | - | | | GND | - | | |
| Y11 | GND | - | | | GND | - | | |
| Y16 | GND | - | | | GND | - | | |
| AB3 | NC | - | | | NC | - | | |
| AB4 | NC | - | | | NC | - | | |
| AC1 | NC | - | | | NC | - | | |
| AC2 | NC | - | | | NC | - | | |
| B4 | NC | - | | | NC | - | | |
| B5 | NC | - | | | NC | - | | |
| C26 | NC | - | | | NC | - | | |
| D20 | NC | - | | | NC | - | | |
| D21 | NC | - | | | NC | - | | |
| D22 | NC | - | | | NC | - | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D23 | NC | - | | | NC | - | | |
| D24 | NC | - | | | NC | - | | |
| D25 | NC | - | | | NC | - | | |
| D26 | NC | - | | | NC | - | | |
| E20 | NC | - | | | NC | - | | |
| E21 | NC | - | | | NC | - | | |
| E25 | NC | - | | | NC | - | | |
| E26 | NC | - | | | NC | - | | |
| F20 | NC | - | | | NC | - | | |
| G20 | NC | - | | | NC | - | | |
| K10 | NC | - | | | NC | - | | |
| K17 | NC | - | | | NC | - | | |
| R4 | NC | - | | | NC | - | | |
| U10 | NC | - | | | NC | - | | |
| U23 | NC | - | | | NC | - | | |
| V10 | NC | - | | | NC | - | | |
| W7 | NC | - | | | NC | - | | |
| AB21 | PB69B | 4 | BDQ69 | C | NC | - | | |
| AC20 | PB58A | 4 | BDQ60 | T | NC | - | | |
| AC21 | PB63A | 4 | BDQ60 | T | NC | - | | |
| AC22 | PB69A | 4 | BDQS69**** | T | NC | - | | |
| AC23 | PB71A | 4 | BDQ69 | T | NC | - | | |
| AC25 | PB71B | 4 | BDQ69 | C | NC | - | | |
| AD26 | PB70B | 4 | BDQ69 | C | NC | - | | |
| W20 | PB72B | 4 | BDQ69 | C | NC | - | | |
| H7 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| K6 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| P7 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| R8 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| V18 | R_VCCPLL | - | | | R_VCCPLL | - | | |
| P20 | R_VCCPLL | - | | | R_VCCPLL | - | | |
| J17 | R_VCCPLL | - | | | R_VCCPLL | - | | |
| G19 | R_VCCPLL | - | | | R_VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D2 | PL9A | 7 | VREF2_7/LDQ6 | T | PL9A | 7 | VREF2_7 | T |
| D3 | PL9B | 7 | VREF1_7/LDQ6 | C | PL9B | 7 | VREF1_7 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| J8 | PL11A | 7 | LUM0_SPLLT_IN_A | T (LVDS)* | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* |
| H7 | PL11B | 7 | LUM0_SPLLC_IN_A | C (LVDS)* | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* |
| E3 | PL12A | 7 | LUM0_SPLLT_FB_A | T | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T |
| E4 | PL12B | 7 | LUM0_SPLLC_FB_A | C | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C |
| GNDIO | GNDIO7 | - | | | - | - | | |
| G6 | PL13A | 7 | | T (LVDS)* | PL13A | 7 | LDQ15 | T (LVDS)* |
| F5 | PL13B | 7 | | C (LVDS)* | PL13B | 7 | LDQ15 | C (LVDS)* |
| E2 | PL14A | 7 | | T | PL14A | 7 | LDQ15 | T |
| D1 | PL14B | 7 | | C | PL14B | 7 | LDQ15 | C |
| - | - | - | | | GNDIO7 | - | | |
| G5 | NC | - | | | PL15A | 7 | LDQS15 | T (LVDS)* |
| G4 | NC | - | | | PL15B | 7 | LDQ15 | C (LVDS)* |
| K7 | NC | - | | | PL16A | 7 | LDQ15 | T |
| K8 | NC | - | | | PL16B | 7 | LDQ15 | C |
| E1 | NC | - | | | PL17A | 7 | LDQ15 | T (LVDS)* |
| F2 | NC | - | | | PL17B | 7 | LDQ15 | C (LVDS)* |
| F1 | NC | - | | | PL18A | 7 | LDQ15 | T |
| - | - | - | | | GNDIO7 | - | | |
| G3 | NC | - | | | PL18B | 7 | LDQ15 | C |
| H5 | PL15A | 7 | | T (LVDS)* | PL21A | 7 | | T (LVDS)* |
| H4 | PL15B | 7 | | C (LVDS)* | PL21B | 7 | | C (LVDS)* |
| J5 | PL16A | 7 | | T | PL22A | 7 | | T |
| J4 | PL16B | 7 | | C | PL22B | 7 | | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| G2 | NC | - | | | PL24A | 7 | LDQ28 | T (LVDS)* |
| G1 | NC | - | | | PL24B | 7 | LDQ28 | C (LVDS)* |
| L9 | NC | - | | | PL25A | 7 | LDQ28 | T |
| L7 | NC | - | | | PL25B | 7 | LDQ28 | C |
| K6 | NC | - | | | PL26A | 7 | LDQ28 | T (LVDS)* |
| K5 | NC | - | | | PL26B | 7 | LDQ28 | C (LVDS)* |
| L8 | NC | - | | | PL27A | 7 | LDQ28 | T |
| L6 | NC | - | | | PL27B | 7 | LDQ28 | C |
| - | - | - | | | GNDIO7 | - | | |
| H3 | PL18A | 7 | | T (LVDS)* | PL28A | 7 | LDQS28 | T (LVDS)* |
| H2 | PL18B | 7 | | C (LVDS)* | PL28B | 7 | LDQ28 | C (LVDS)* |
| N8 | PL19A | 7 | | T | PL29A | 7 | LDQ28 | T |
| M9 | PL19B | 7 | | C | PL29B | 7 | LDQ28 | C |
| J3 | PL20A | 7 | | T (LVDS)* | PL30A | 7 | LDQ28 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | - | - | | |
| J2 | PL20B | 7 | | C (LVDS)* | PL30B | 7 | LDQ28 | C (LVDS)* |
| H1 | PL21A | 7 | | T | PL31A | 7 | LDQ28 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| J1 | PL21B | 7 | | C | PL31B | 7 | LDQ28 | C |
| - | - | - | | | - | - | | |
| - | - | - | | | - | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L5 | PL23A | 7 | LDQ27 | T (LVDS)* | PL33A | 7 | LDQ37 | T (LVDS)* |
| L4 | PL23B | 7 | LDQ27 | C (LVDS)* | PL33B | 7 | LDQ37 | C (LVDS)* |
| N9 | PL24A | 7 | LDQ27 | T | PL34A | 7 | LDQ37 | T |
| N7 | PL24B | 7 | LDQ27 | C | PL34B | 7 | LDQ37 | C |
| K2 | PL25A | 7 | LDQ27 | T (LVDS)* | PL35A | 7 | LDQ37 | T (LVDS)* |
| K1 | PL25B | 7 | LDQ27 | C (LVDS)* | PL35B | 7 | LDQ37 | C (LVDS)* |
| P9 | PL26A | 7 | LDQ27 | T | PL36A | 7 | LDQ37 | T |
| P7 | PL26B | 7 | LDQ27 | C | PL36B | 7 | LDQ37 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M6 | PL27A | 7 | LDQS27 | T (LVDS)* | PL37A | 7 | LDQS37 | T (LVDS)* |
| M5 | PL27B | 7 | LDQ27 | C (LVDS)* | PL37B | 7 | LDQ37 | C (LVDS)* |
| N5 | PL28A | 7 | LDQ27 | T | PL38A | 7 | LDQ37 | T |
| N6 | PL28B | 7 | LDQ27 | C | PL38B | 7 | LDQ37 | C |
| M4 | PL29A | 7 | LDQ27 | T (LVDS)* | PL39A | 7 | LDQ37 | T (LVDS)* |
| M3 | PL29B | 7 | LDQ27 | C (LVDS)* | PL39B | 7 | LDQ37 | C (LVDS)* |
| P6 | PL30A | 7 | LDQ27 | T | PL40A | 7 | LDQ37 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| P8 | PL30B | 7 | LDQ27 | C | PL40B | 7 | LDQ37 | C |
| L3 | PL32A | 7 | LUM3_SPLLT_IN_A/LDQ36 | T (LVDS)* | PL42A | 7 | LUM3_SPLLT_IN_A/LDQ46 | T (LVDS)* |
| L2 | PL32B | 7 | LUM3_SPLLC_IN_A/LDQ36 | C (LVDS)* | PL42B | 7 | LUM3_SPLLC_IN_A/LDQ46 | C (LVDS)* |
| P5 | PL33A | 7 | LUM3_SPLLT_FB_A/LDQ36 | T | PL43A | 7 | LUM3_SPLLT_FB_A/LDQ46 | T |
| P4 | PL33B | 7 | LUM3_SPLLC_FB_A/LDQ36 | C | PL43B | 7 | LUM3_SPLLC_FB_A/LDQ46 | C |
| L1 | PL34A | 7 | LDQ36 | T (LVDS)* | PL44A | 7 | LDQ46 | T (LVDS)* |
| M2 | PL34B | 7 | LDQ36 | C (LVDS)* | PL44B | 7 | LDQ46 | C (LVDS)* |
| R5 | PL35A | 7 | LDQ36 | T | PL45A | 7 | LDQ46 | T |
| R4 | PL35B | 7 | LDQ36 | C | PL45B | 7 | LDQ46 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M1 | PL36A | 7 | LDQS36 | T (LVDS)* | PL46A | 7 | LDQS46 | T (LVDS)* |
| N2 | PL36B | 7 | LDQ36 | C (LVDS)* | PL46B | 7 | LDQ46 | C (LVDS)* |
| R8 | PL37A | 7 | LDQ36 | T | PL47A | 7 | LDQ46 | T |
| T9 | PL37B | 7 | LDQ36 | C | PL47B | 7 | LDQ46 | C |
| P3 | PL38A | 7 | LDQ36 | T (LVDS)* | PL48A | 7 | LDQ46 | T (LVDS)* |
| P2 | PL38B | 7 | LDQ36 | C (LVDS)* | PL48B | 7 | LDQ46 | C (LVDS)* |
| N1 | PL39A | 7 | PCLKT7_0/LDQ36 | T | PL49A | 7 | PCLKT7_0/LDQ46 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| P1 | PL39B | 7 | PCLKC7_0/LDQ36 | C | PL49B | 7 | PCLKC7_0/LDQ46 | C |
| T5 | PL41A | 6 | PCLKT6_0 | T (LVDS)* | PL51A | 6 | PCLKT6_0/LDQ55 | T (LVDS)* |
| T4 | PL41B | 6 | PCLKC6_0 | C (LVDS)* | PL51B | 6 | PCLKC6_0/LDQ55 | C (LVDS)* |
| U7 | PL42A | 6 | VREF2_6 | T | PL52A | 6 | VREF2_6/LDQ55 | T |
| T8 | PL42B | 6 | VREF1_6 | C | PL52B | 6 | VREF1_6/LDQ55 | C |
| R3 | PL43A | 6 | | T (LVDS)* | PL53A | 6 | LDQ55 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R2 | PL43B | 6 | | C (LVDS)* | PL53B | 6 | LDQ55 | C (LVDS)* |
| R1 | PL44A | 6 | | T | PL54A | 6 | LDQ55 | T |
| T1 | PL44B | 6 | | C | PL54B | 6 | LDQ55 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| - | - | - | | | VCCIO6 | 6 | | |
| T3 | PL45A | 6 | LLM3_SPLLT_IN_A | T (LVDS)* | PL57A | 6 | LLM3_SPLLT_IN_A/LDQ55 | T (LVDS)* |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T2 | PL45B | 6 | LLM3_SPLLC_IN_A | C (LVDS)* | PL57B | 6 | LLM3_SPLLC_IN_A/LDQ55 | C (LVDS)* |
| U9 | PL46A | 6 | LLM3_SPLLT_FB_A | T | PL58A | 6 | LLM3_SPLLT_FB_A/LDQ55 | T |
| U8 | PL46B | 6 | LLM3_SPLLC_FB_A | C | PL58B | 6 | LLM3_SPLLC_FB_A/LDQ55 | C |
| VCCIO | VCCIO6 | 6 | | | GNDIO6 | - | | |
| U5 | PL48A | 6 | LDQ52 | T (LVDS)* | PL60A | 6 | LDQ64 | T (LVDS)* |
| U4 | PL48B | 6 | LDQ52 | C (LVDS)* | PL60B | 6 | LDQ64 | C (LVDS)* |
| V9 | PL49A | 6 | LDQ52 | T | PL61A | 6 | LDQ64 | T |
| V7 | PL49B | 6 | LDQ52 | C | PL61B | 6 | LDQ64 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U3 | PL50A | 6 | LDQ52 | T (LVDS)* | PL62A | 6 | LDQ64 | T (LVDS)* |
| U2 | PL50B | 6 | LDQ52 | C (LVDS)* | PL62B | 6 | LDQ64 | C (LVDS)* |
| V8 | PL51A | 6 | LDQ52 | T | PL63A | 6 | LDQ64 | T |
| U6 | PL51B | 6 | LDQ52 | C | PL63B | 6 | LDQ64 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| U1 | PL52A | 6 | LDQS52 | T (LVDS)* | PL64A | 6 | LDQS64 | T (LVDS)* |
| V2 | PL52B | 6 | LDQ52 | C (LVDS)* | PL64B | 6 | LDQ64 | C (LVDS)* |
| V5 | PL53A | 6 | LDQ52 | T | PL65A | 6 | LDQ64 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V6 | PL53B | 6 | LDQ52 | C | PL65B | 6 | LDQ64 | C |
| V1 | PL54A | 6 | LDQ52 | T (LVDS)* | PL66A | 6 | LDQ64 | T (LVDS)* |
| W1 | PL54B | 6 | LDQ52 | C (LVDS)* | PL66B | 6 | LDQ64 | C (LVDS)* |
| W5 | PL55A | 6 | LDQ52 | T | PL67A | 6 | LDQ64 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| W6 | PL55B | 6 | LDQ52 | C | PL67B | 6 | LDQ64 | C |
| W3 | PL57A | 6 | | T (LVDS)* | PL69A | 6 | LDQ73 | T (LVDS)* |
| W4 | PL57B | 6 | | C (LVDS)* | PL69B | 6 | LDQ73 | C (LVDS)* |
| W2 | PL58A | 6 | | T | PL70A | 6 | LDQ73 | T |
| Y4 | PL58B | 6 | | C | PL70B | 6 | LDQ73 | C |
| Y1 | PL59A | 6 | | T (LVDS)* | PL71A | 6 | LDQ73 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | PL59B | 6 | | C (LVDS)* | PL71B | 6 | LDQ73 | C (LVDS)* |
| Y5 | PL60A | 6 | | T | PL72A | 6 | LDQ73 | T |
| Y6 | PL60B | 6 | | C | PL72B | 6 | LDQ73 | C |
| AA1 | NC | - | | | PL73A | 6 | LDQS73 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA2 | NC | - | | | PL73B | 6 | LDQ73 | C (LVDS)* |
| Y3 | NC | - | | | PL74A | 6 | LDQ73 | T |
| AB1 | NC | - | | | PL74B | 6 | LDQ73 | C |
| - | - | - | | | VCCIO6 | 6 | | |
| Y9 | NC | - | | | PL75A | 6 | LDQ73 | T (LVDS)* |
| Y8 | NC | - | | | PL75B | 6 | LDQ73 | C (LVDS)* |
| Y7 | NC | - | | | PL76A | 6 | LDQ73 | T |
| AA7 | NC | - | | | PL76B | 6 | LDQ73 | C |
| - | - | - | | | GNDIO6 | - | | |
| - | - | - | | | - | - | | |
| AB2 | NC | - | | | PL78A | 6 | LDQ82 | T (LVDS)* |
| AB3 | NC | - | | | PL78B | 6 | LDQ82 | C (LVDS)* |
| AA5 | NC | - | | | PL79A | 6 | LDQ82 | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA6 | NC | - | | | PL79B | 6 | LDQ82 | C |
| AB4 | NC | - | | | PL80A | 6 | LDQ82 | T (LVDS)* |
| - | - | - | | | VCCIO6 | 6 | | |
| AB5 | NC | - | | | PL80B | 6 | LDQ82 | C (LVDS)* |
| AA8 | NC | - | | | PL81A | 6 | LDQ82 | T |
| AA9 | NC | - | | | PL81B | 6 | LDQ82 | C |
| AC1 | PL62A | 6 | LLM0_GPLLT_IN_A** | T (LVDS)* | PL82A | 6 | LLM0_GPLLT_IN_A**/LDQS82 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AC2 | PL62B | 6 | LLM0_GPLLC_IN_A** | C (LVDS)* | PL82B | 6 | LLM0_GPLLC_IN_A**/LDQ82 | C (LVDS)* |
| AC4 | PL63A | 6 | LLM0_GPLLT_FB_A | T | PL83A | 6 | LLM0_GPLLT_FB_A/LDQ82 | T |
| AC3 | PL63B | 6 | LLM0_GPLLC_FB_A | C | PL83B | 6 | LLM0_GPLLC_FB_A/LDQ82 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AC7 | PL64A | 6 | LLM0_GDLLT_IN_A** | T (LVDS)* | PL84A | 6 | LLM0_GDLLT_IN_A**/LDQ82 | T (LVDS)* |
| AC6 | PL64B | 6 | LLM0_GDLLC_IN_A** | C (LVDS)* | PL84B | 6 | LLM0_GDLLC_IN_A**/LDQ82 | C (LVDS)* |
| AC5 | PL65A | 6 | LLM0_GDLLT_FB_A | T | PL85A | 6 | LLM0_GDLLT_FB_A/LDQ82 | T |
| AD3 | PL65B | 6 | LLM0_GDLLC_FB_A | C | PL85B | 6 | LLM0_GDLLC_FB_A/LDQ82 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AB8 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| AD2 | PL67A | 6 | LDQ71 | T (LVDS)* | PL87A | 6 | | T |
| AD1 | PL67B | 6 | LDQ71 | C (LVDS)* | PL87B | 6 | | C |
| AE2 | TCK | - | | | TCK | - | | |
| AE1 | TDI | - | | | TDI | - | | |
| AF2 | TMS | - | | | TMS | - | | |
| AF1 | TDO | - | | | TDO | - | | |
| AG1 | VCCJ | - | | | VCCJ | - | | |
| AH1 | VCC | - | | | LLC_SQ_VCCRX3 | 14 | | |
| AK2 | PB11A | 5 | BDQ15 | T | LLC_SQ_HDINP3 | 14 | | T |
| AJ1 | NC | - | | | LLC_SQ_VCCIB3 | 14 | | |
| AJ2 | PB11B | 5 | BDQ15 | C | LLC_SQ_HDINN3 | 14 | | C |
| AH4 | VCC | - | | | LLC_SQ_VCCTX3 | 14 | | |
| AK5 | PB13A | 5 | BDQ15 | T | LLC_SQ_HDOUTP3 | 14 | | T |
| AK4 | NC | - | | | LLC_SQ_VCCOB3 | 14 | | |
| AJ5 | PB13B | 5 | BDQ15 | C | LLC_SQ_HDOUTN3 | 14 | | C |
| AH5 | VCC | - | | | LLC_SQ_VCCTX2 | 14 | | |
| AJ6 | PB14B | 5 | BDQ15 | C | LLC_SQ_HDOUTN2 | 14 | | C |
| AH6 | NC | - | | | LLC_SQ_VCCOB2 | 14 | | |
| AK6 | PB14A | 5 | BDQ15 | T | LLC_SQ_HDOUTP2 | 14 | | T |
| AH2 | VCC | - | | | LLC_SQ_VCCRX2 | 14 | | |
| AJ3 | PB12B | 5 | BDQ15 | C | LLC_SQ_HDINN2 | 14 | | C |
| AH3 | NC | - | | | LLC_SQ_VCCIB2 | 14 | | |
| AK3 | PB12A | 5 | BDQ15 | T | LLC_SQ_HDINP2 | 14 | | T |
| AH7 | VCC | - | | | LLC_SQ_VCCP | 14 | | |
| AG7 | PB15A | 5 | BDQS15 | T | LLC_SQ_REFCLKP | 14 | | T |
| AF7 | PB15B | 5 | BDQ15 | C | LLC_SQ_REFCLKN | 14 | | C |
| AJ7 | VCCAUX | - | | | LLC_SQ_VCCAUX33 | 14 | | |
| AK11 | PB18A | 5 | BDQ15 | T | LLC_SQ_HDINP1 | 14 | | T |
| AH11 | NC | - | | | LLC_SQ_VCCIB1 | 14 | | |
| AJ11 | PB18B | 5 | BDQ15 | C | LLC_SQ_HDINN1 | 14 | | C |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AH12 | VCC | - | | | LLC_SQ_VCCRX1 | 14 | | |
| AK8 | PB16A | 5 | BDQ15 | T | LLC_SQ_HDOUTP1 | 14 | | T |
| AH8 | NC | - | | | LLC_SQ_VCCOB1 | 14 | | |
| AJ8 | PB16B | 5 | BDQ15 | C | LLC_SQ_HDOUTN1 | 14 | | C |
| AH9 | VCC | - | | | LLC_SQ_VCCTX1 | 14 | | |
| AJ9 | PB17B | 5 | BDQ15 | C | LLC_SQ_HDOUTN0 | 14 | | C |
| AK10 | NC | - | | | LLC_SQ_VCCOB0 | 14 | | |
| AK9 | PB17A | 5 | BDQ15 | T | LLC_SQ_HDOUTP0 | 14 | | T |
| AH10 | VCC | - | | | LLC_SQ_VCCTX0 | 14 | | |
| AJ12 | PB19B | 5 | BDQ15 | C | LLC_SQ_HDINN0 | 14 | | C |
| AJ13 | NC | - | | | LLC_SQ_VCCIB0 | 14 | | |
| AK12 | PB19A | 5 | BDQ15 | T | LLC_SQ_HDINP0 | 14 | | T |
| AH13 | VCC | - | | | LLC_SQ_VCCRX0 | 14 | | |
| AF10 | PB3A | 5 | BDQ6 | T | PB30A | 5 | BDQ33 | T |
| AE8 | PB3B | 5 | BDQ6 | C | PB30B | 5 | BDQ33 | C |
| AE11 | PB4A | 5 | BDQ6 | T | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AD9 | PB4B | 5 | BDQ6 | C | PB31B | 5 | BDQ33 | C |
| AE10 | PB5A | 5 | BDQ6 | T | PB32A | 5 | BDQ33 | T |
| AD10 | PB5B | 5 | BDQ6 | C | PB32B | 5 | BDQ33 | C |
| AE13 | PB6A | 5 | BDQS6 | T | PB33A | 5 | BDQS33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AC12 | PB6B | 5 | BDQ6 | C | PB33B | 5 | BDQ33 | C |
| AG2 | PB7A | 5 | BDQ6 | T | PB34A | 5 | BDQ33 | T |
| AG3 | PB7B | 5 | BDQ6 | C | PB34B | 5 | BDQ33 | C |
| AD13 | PB8A | 5 | BDQ6 | T | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC13 | PB8B | 5 | BDQ6 | C | PB35B | 5 | BDQ33 | C |
| AE14 | PB9A | 5 | BDQ6 | T | PB36A | 5 | BDQ33 | T |
| AC14 | PB9B | 5 | BDQ6 | C | PB36B | 5 | BDQ33 | C |
| AF3 | PB10A | 5 | BDQ6 | T | PB37A | 5 | BDQ33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AF4 | PB10B | 5 | BDQ6 | C | PB37B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | - | - | | |
| AG4 | PB20A | 5 | BDQ24 | T | PB38A | 5 | BDQ42 | T |
| AG5 | PB20B | 5 | BDQ24 | C | PB38B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | | - | - | | |
| VCCIO | VCCIO5 | 5 | | | - | - | | |
| AD11 | PB24A | 5 | BDQS24**** | T | PB39A | 5 | BDQ42 | T |
| AF13 | PB24B | 5 | BDQ24 | C | PB39B | 5 | BDQ42 | C |
| AF12 | PB25A | 5 | BDQ24 | T | PB40A | 5 | BDQ42 | T |
| - | - | - | | | VCCIO5 | 5 | | |
| AD14 | PB25B | 5 | BDQ24 | C | PB40B | 5 | BDQ42 | C |
| AG8 | PB26A | 5 | BDQ24 | T | PB41A | 5 | BDQ42 | T |
| AF8 | PB26B | 5 | BDQ24 | C | PB41B | 5 | BDQ42 | C |
| AE15 | PB27A | 5 | BDQ24 | T | PB42A | 5 | BDQS42**** | T |
| - | - | - | | | GNDIO5 | - | | |
| VCCIO | VCCIO5 | 5 | | | - | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AC15 | PB27B | 5 | BDQ24 | C | PB42B | 5 | BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AD15 | PB38A | 5 | BDQ42 | T | PB47A | 5 | BDQ51 | T |
| AF15 | PB38B | 5 | BDQ42 | C | PB47B | 5 | BDQ51 | C |
| AG10 | PB39A | 5 | BDQ42 | T | PB48A | 5 | BDQ51 | T |
| AG9 | PB39B | 5 | BDQ42 | C | PB48B | 5 | BDQ51 | C |
| AH14 | PB40A | 5 | BDQ42 | T | PB49A | 5 | BDQ51 | T |
| AG12 | PB40B | 5 | BDQ42 | C | PB49B | 5 | BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG15 | PB41A | 5 | BDQ42 | T | PB50A | 5 | BDQ51 | T |
| AG13 | PB41B | 5 | BDQ42 | C | PB50B | 5 | BDQ51 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AF16 | PB42A | 5 | BDQS42 | T | PB51A | 5 | BDQS51 | T |
| AH15 | PB42B | 5 | BDQ42 | C | PB51B | 5 | BDQ51 | C |
| AC16 | PB43A | 5 | VREF2_5/BDQ42 | T | PB52A | 5 | VREF2_5/BDQ51 | T |
| AE16 | PB43B | 5 | VREF1_5/BDQ42 | C | PB52B | 5 | VREF1_5/BDQ51 | C |
| AG11 | PB44A | 5 | PCLKT5_0/BDQ42 | T | PB53A | 5 | PCLKT5_0/BDQ51 | T |
| AF11 | PB44B | 5 | PCLKC5_0/BDQ42 | C | PB53B | 5 | PCLKC5_0/BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AJ14 | PB49A | 4 | PCLKT4_0/BDQ51 | T | PB58A | 4 | PCLKT4_0/BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AK14 | PB49B | 4 | PCLKC4_0/BDQ51 | C | PB58B | 4 | PCLKC4_0/BDQ60 | C |
| AK15 | PB50A | 4 | VREF2_4/BDQ51 | T | PB59A | 4 | VREF2_4/BDQ60 | T |
| AK16 | PB50B | 4 | VREF1_4/BDQ51 | C | PB59B | 4 | VREF1_4/BDQ60 | C |
| AF18 | PB51A | 4 | BDQS51 | T | PB60A | 4 | BDQS60 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AD16 | PB51B | 4 | BDQ51 | C | PB60B | 4 | BDQ60 | C |
| AJ15 | PB52A | 4 | BDQ51 | T | PB61A | 4 | BDQ60 | T |
| AG16 | PB52B | 4 | BDQ51 | C | PB61B | 4 | BDQ60 | C |
| AE17 | PB53A | 4 | BDQ51 | T | PB62A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC17 | PB53B | 4 | BDQ51 | C | PB62B | 4 | BDQ60 | C |
| AH16 | PB54A | 4 | BDQ51 | T | PB63A | 4 | BDQ60 | T |
| AK17 | PB54B | 4 | BDQ51 | C | PB63B | 4 | BDQ60 | C |
| AG20 | PB55A | 4 | BDQ51 | T | PB64A | 4 | BDQ60 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AG21 | PB55B | 4 | BDQ51 | C | PB64B | 4 | BDQ60 | C |
| AG18 | PB56A | 4 | BDQ60 | T | PB65A | 4 | BDQ69 | T |
| AJ16 | PB56B | 4 | BDQ60 | C | PB65B | 4 | BDQ69 | C |
| AF21 | PB57A | 4 | BDQ60 | T | PB66A | 4 | BDQ69 | T |
| AG22 | PB57B | 4 | BDQ60 | C | PB66B | 4 | BDQ69 | C |
| AD17 | PB58A | 4 | BDQ60 | T | PB67A | 4 | BDQ69 | T |
| AF19 | PB58B | 4 | BDQ60 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AH17 | PB62A | 4 | BDQ60 | T | PB71A | 4 | BDQ69 | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AJ17 | PB62B | 4 | BDQ60 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AF26 | PB64A | 4 | BDQ60 | T | PB73A | 4 | BDQ69 | T |
| AE25 | PB64B | 4 | BDQ60 | C | PB73B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AD24 | PB65A | 4 | BDQ69 | T | PB74A | 4 | BDQ78 | T |
| AE24 | PB65B | 4 | BDQ69 | C | PB74B | 4 | BDQ78 | C |
| AD18 | PB66A | 4 | BDQ69 | T | PB75A | 4 | BDQ78 | T |
| AC18 | PB66B | 4 | BDQ69 | C | PB75B | 4 | BDQ78 | C |
| AE18 | PB67A | 4 | BDQ69 | T | PB76A | 4 | BDQ78 | T |
| AG19 | PB67B | 4 | BDQ69 | C | PB76B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AC19 | PB69A | 4 | BDQS69 | T | PB78A | 4 | BDQS78 | T |
| AD20 | PB69B | 4 | BDQ69 | C | PB78B | 4 | BDQ78 | C |
| AB18 | PB70A | 4 | BDQ69 | T | PB79A | 4 | BDQ78 | T |
| AC20 | PB70B | 4 | BDQ69 | C | PB79B | 4 | BDQ78 | C |
| AE20 | PB71A | 4 | BDQ69 | T | PB80A | 4 | BDQ78 | T |
| AE21 | PB71B | 4 | BDQ69 | C | PB80B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC23 | PB72A | 4 | BDQ69 | T | PB81A | 4 | BDQ78 | T |
| AD23 | PB72B | 4 | BDQ69 | C | PB81B | 4 | BDQ78 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AH18 | LRC_SQ_VCCRX3 | 13 | | | LRC_SQ_VCCRX3 | 13 | | |
| AK19 | LRC_SQ_HDINP3 | 13 | | T | LRC_SQ_HDINP3 | 13 | | T |
| AJ18 | LRC_SQ_VCCIB3 | 13 | | | LRC_SQ_VCCIB3 | 13 | | |
| AJ19 | LRC_SQ_HDINN3 | 13 | | C | LRC_SQ_HDINN3 | 13 | | C |
| AH21 | LRC_SQ_VCCTX3 | 13 | | | LRC_SQ_VCCTX3 | 13 | | |
| AK22 | LRC_SQ_HDOUTP3 | 13 | | T | LRC_SQ_HDOUTP3 | 13 | | T |
| AK21 | LRC_SQ_VCCOB3 | 13 | | | LRC_SQ_VCCOB3 | 13 | | |
| AJ22 | LRC_SQ_HDOUTN3 | 13 | | C | LRC_SQ_HDOUTN3 | 13 | | C |
| AH22 | LRC_SQ_VCCTX2 | 13 | | | LRC_SQ_VCCTX2 | 13 | | |
| AJ23 | LRC_SQ_HDOUTN2 | 13 | | C | LRC_SQ_HDOUTN2 | 13 | | C |
| AH23 | LRC_SQ_VCCOB2 | 13 | | | LRC_SQ_VCCOB2 | 13 | | |
| AK23 | LRC_SQ_HDOUTP2 | 13 | | T | LRC_SQ_HDOUTP2 | 13 | | T |
| AH19 | LRC_SQ_VCCRX2 | 13 | | | LRC_SQ_VCCRX2 | 13 | | |
| AJ20 | LRC_SQ_HDINN2 | 13 | | C | LRC_SQ_HDINN2 | 13 | | C |
| AH20 | LRC_SQ_VCCIB2 | 13 | | | LRC_SQ_VCCIB2 | 13 | | |
| AK20 | LRC_SQ_HDINP2 | 13 | | T | LRC_SQ_HDINP2 | 13 | | T |
| AH24 | LRC_SQ_VCCP | 13 | | | LRC_SQ_VCCP | 13 | | |
| AG24 | LRC_SQ_REFCLKP | 13 | | T | LRC_SQ_REFCLKP | 13 | | T |
| AF24 | LRC_SQ_REFCLKN | 13 | | C | LRC_SQ_REFCLKN | 13 | | C |
| AJ24 | LRC_SQ_VCCAUX33 | 13 | | | LRC_SQ_VCCAUX33 | 13 | | |
| AK28 | LRC_SQ_HDINP1 | 13 | | T | LRC_SQ_HDINP1 | 13 | | T |
| AH28 | LRC_SQ_VCCIB1 | 13 | | | LRC_SQ_VCCIB1 | 13 | | |
| AJ28 | LRC_SQ_HDINN1 | 13 | | C | LRC_SQ_HDINN1 | 13 | | C |
| AH29 | LRC_SQ_VCCRX1 | 13 | | | LRC_SQ_VCCRX1 | 13 | | |
| AK25 | LRC_SQ_HDOUTP1 | 13 | | T | LRC_SQ_HDOUTP1 | 13 | | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AH25 | LRC_SQ_VCCOB1 | 13 | | | LRC_SQ_VCCOB1 | 13 | | |
| AJ25 | LRC_SQ_HDOUTN1 | 13 | | C | LRC_SQ_HDOUTN1 | 13 | | C |
| AH26 | LRC_SQ_VCCTX1 | 13 | | | LRC_SQ_VCCTX1 | 13 | | |
| AJ26 | LRC_SQ_HDOUTN0 | 13 | | C | LRC_SQ_HDOUTN0 | 13 | | C |
| AK27 | LRC_SQ_VCCOB0 | 13 | | | LRC_SQ_VCCOB0 | 13 | | |
| AK26 | LRC_SQ_HDOUTP0 | 13 | | T | LRC_SQ_HDOUTP0 | 13 | | T |
| AH27 | LRC_SQ_VCCTX0 | 13 | | | LRC_SQ_VCCTX0 | 13 | | |
| AJ29 | LRC_SQ_HDINN0 | 13 | | C | LRC_SQ_HDINN0 | 13 | | C |
| AJ30 | LRC_SQ_VCCIB0 | 13 | | | LRC_SQ_VCCIB0 | 13 | | |
| AK29 | LRC_SQ_HDINP0 | 13 | | T | LRC_SQ_HDINP0 | 13 | | T |
| AH30 | LRC_SQ_VCCRX0 | 13 | | | LRC_SQ_VCCRX0 | 13 | | |
| AG27 | CFG2 | 8 | | | CFG2 | 8 | | |
| AD25 | CFG1 | 8 | | | CFG1 | 8 | | |
| AG28 | CFG0 | 8 | | | CFG0 | 8 | | |
| AG30 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| AG29 | CCLK | 8 | | | CCLK | 8 | | |
| AC24 | INITN | 8 | | | INITN | 8 | | |
| AF27 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| AF28 | WRITEN*** | 8 | | | WRITEN*** | 8 | | |
| AE26 | CS1N*** | 8 | | | CS1N*** | 8 | | |
| AB23 | CSN*** | 8 | | | CSN*** | 8 | | |
| AF29 | D0/SPIFASTN*** | 8 | | | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AF30 | D1*** | 8 | | | D1*** | 8 | | |
| AD26 | D2*** | 8 | | | D2*** | 8 | | |
| AE29 | D3*** | 8 | | | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| AE30 | D4*** | 8 | | | D4*** | 8 | | |
| AD29 | D5*** | 8 | | | D5*** | 8 | | |
| AC25 | D6*** | 8 | | | D6*** | 8 | | |
| AD30 | D7/SPID0*** | 8 | | | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AA22 | DI/CSSPI0N*** | 8 | | | DI/CSSPI0N*** | 8 | | |
| AC26 | DOUT/CSON/ CSSPI1N*** | 8 | | | DOUT/CSON/ CSSPI1N*** | 8 | | |
| AA23 | BUSY/SISPI*** | 8 | | | BUSY/SISPI*** | 8 | | |
| AB22 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| AC27 | PR65B | 3 | RLM0_GDLLC_FB_A | C | PR85B | 3 | RLM0_GDLLC_FB_A/RDQ82 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AC28 | PR65A | 3 | RLM0_GDLLT_FB_A | T | PR85A | 3 | RLM0_GDLLT_FB_A/RDQ82 | T |
| AC29 | PR64B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR84B | 3 | RLM0_GDLLC_IN_A**/RDQ82 | C (LVDS)* |
| AC30 | PR64A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR84A | 3 | RLM0_GDLLT_IN_A**/RDQ82 | T (LVDS)* |
| AB30 | PR63B | 3 | RLM0_GPLLC_IN_A** | C | PR83B | 3 | RLM0_GPLLC_IN_A**/RDQ82 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA30 | PR63A | 3 | RLM0_GPLLT_IN_A** | T | PR83A | 3 | RLM0_GPLLT_IN_A**/RDQ82 | T |
| AB29 | PR62B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR82B | 3 | RLM0_GPLLC_FB_A/RDQ82 | C (LVDS)* |
| AB28 | PR62A | 3 | RLM0_GPLLT_FB_A | T (LVDS)* | PR82A | 3 | RLM0_GPLLT_FB_A/RDQS82 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| Y22 | PR60B | 3 | | C | PR81B | 3 | RDQ82 | C |
| Y23 | PR60A | 3 | | T | PR81A | 3 | RDQ82 | T |
| AB26 | NC | - | | | PR80B | 3 | RDQ82 | C (LVDS)* |
| AB27 | NC | - | | | PR80A | 3 | RDQ82 | T (LVDS)* |
| - | - | - | | | VCCIO3 | 3 | | |
| Y24 | NC | - | | | PR79B | 3 | RDQ82 | C |
| Y25 | NC | - | | | PR79A | 3 | RDQ82 | T |
| AA29 | NC | - | | | PR78B | 3 | RDQ82 | C (LVDS)* |
| Y28 | NC | - | | | PR78A | 3 | RDQ82 | T (LVDS)* |
| Y30 | NC | - | | | PR76B | 3 | RDQ73 | C |
| Y29 | NC | - | | | PR76A | 3 | RDQ73 | T |
| - | - | - | | | GNDIO3 | - | | |
| - | - | - | | | - | - | | |
| W22 | NC | - | | | PR75B | 3 | RDQ73 | C (LVDS)* |
| V22 | NC | - | | | PR75A | 3 | RDQ73 | T (LVDS)* |
| Y27 | NC | - | | | PR74B | 3 | RDQ73 | C |
| - | - | - | | | VCCIO3 | 3 | | |
| Y26 | NC | - | | | PR74A | 3 | RDQ73 | T |
| W30 | NC | - | | | PR73B | 3 | RDQ73 | C (LVDS)* |
| W29 | NC | - | | | PR73A | 3 | RDQS73 | T (LVDS)* |
| - | - | - | | | GNDIO3 | - | | |
| W25 | NC | - | | | PR72B | 3 | RDQ73 | C |
| W26 | NC | - | | | PR72A | 3 | RDQ73 | T |
| U29 | PR59B | 3 | | C (LVDS)* | PR71B | 3 | RDQ73 | C (LVDS)* |
| V29 | PR59A | 3 | | T (LVDS)* | PR71A | 3 | RDQ73 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V30 | PR58B | 3 | | C | PR70B | 3 | RDQ73 | C |
| U30 | PR58A | 3 | | T | PR70A | 3 | RDQ73 | T |
| W27 | PR57B | 3 | | C (LVDS)* | PR69B | 3 | RDQ73 | C (LVDS)* |
| W28 | PR57A | 3 | | T (LVDS)* | PR69A | 3 | RDQ73 | T (LVDS)* |
| V24 | PR55B | 3 | RDQ52 | C | PR67B | 3 | RDQ64 | C |
| V25 | PR55A | 3 | RDQ52 | T | PR67A | 3 | RDQ64 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| U28 | PR54B | 3 | RDQ52 | C (LVDS)* | PR66B | 3 | RDQ64 | C (LVDS)* |
| U27 | PR54A | 3 | RDQ52 | T (LVDS)* | PR66A | 3 | RDQ64 | T (LVDS)* |
| U23 | PR53B | 3 | RDQ52 | C | PR65B | 3 | RDQ64 | C |
| V23 | PR53A | 3 | RDQ52 | T | PR65A | 3 | RDQ64 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V26 | PR52B | 3 | RDQ52 | C (LVDS)* | PR64B | 3 | RDQ64 | C (LVDS)* |
| U26 | PR52A | 3 | RDQS52 | T (LVDS)* | PR64A | 3 | RDQS64 | T (LVDS)* |
| U25 | PR51B | 3 | RDQ52 | C | PR63B | 3 | RDQ64 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| U24 | PR51A | 3 | RDQ52 | T | PR63A | 3 | RDQ64 | T |
| T30 | PR50B | 3 | RDQ52 | C (LVDS)* | PR62B | 3 | RDQ64 | C (LVDS)* |
| R30 | PR50A | 3 | RDQ52 | T (LVDS)* | PR62A | 3 | RDQ64 | T (LVDS)* |
| T23 | PR49B | 3 | RDQ52 | C | PR61B | 3 | RDQ64 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T22 | PR49A | 3 | RDQ52 | T | PR61A | 3 | RDQ64 | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T29 | PR48B | 3 | RDQ52 | C (LVDS)* | PR60B | 3 | RDQ64 | C (LVDS)* |
| T28 | PR48A | 3 | RDQ52 | T (LVDS)* | PR60A | 3 | RDQ64 | T (LVDS)* |
| R23 | PR46B | 3 | RLM3_SPLLC_FB_A | C | PR58B | 3 | RLM3_SPLLC_FB_A/RDQ55 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | - | - | | |
| R22 | PR46A | 3 | RLM3_SPLLT_FB_A | T | PR58A | 3 | RLM3_SPLLT_FB_A/RDQ55 | T |
| P30 | PR45B | 3 | RLM3_SPLLC_IN_A | C (LVDS)* | PR57B | 3 | RLM3_SPLLC_IN_A/RDQ55 | C (LVDS)* |
| R29 | PR45A | 3 | RLM3_SPLLT_IN_A | T (LVDS)* | PR57A | 3 | RLM3_SPLLT_IN_A/RDQ55 | T (LVDS)* |
| T27 | PR44B | 3 | | C | PR56B | 3 | RDQ55 | C |
| - | - | - | | | VCCIO3 | 3 | | |
| T26 | PR44A | 3 | | T | PR56A | 3 | RDQ55 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| N30 | PR43B | 3 | | C (LVDS)* | PR53B | 3 | RDQ55 | C (LVDS)* |
| N29 | PR43A | 3 | | T (LVDS)* | PR53A | 3 | RDQ55 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R27 | PR42B | 3 | VREF2_3 | C | PR52B | 3 | VREF2_3/RDQ55 | C |
| R28 | PR42A | 3 | VREF1_3 | T | PR52A | 3 | VREF1_3/RDQ55 | T |
| P29 | PR41B | 3 | PCLKC3_0 | C (LVDS)* | PR51B | 3 | PCLKC3_0/RDQ55 | C (LVDS)* |
| P28 | PR41A | 3 | PCLKT3_0 | T (LVDS)* | PR51A | 3 | PCLKT3_0/RDQ55 | T (LVDS)* |
| M30 | PR39B | 2 | PCLKC2_0/RDQ36 | C | PR49B | 2 | PCLKC2_0/RDQ46 | C |
| M29 | PR39A | 2 | PCLKT2_0/RDQ36 | T | PR49A | 2 | PCLKT2_0/RDQ46 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| P23 | PR38B | 2 | RDQ36 | C (LVDS)* | PR48B | 2 | RDQ46 | C (LVDS)* |
| P24 | PR38A | 2 | RDQ36 | T (LVDS)* | PR48A | 2 | RDQ46 | T (LVDS)* |
| R26 | PR37B | 2 | RDQ36 | C | PR47B | 2 | RDQ46 | C |
| P27 | PR37A | 2 | RDQ36 | T | PR47A | 2 | RDQ46 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| P25 | PR36B | 2 | RDQ36 | C (LVDS)* | PR46B | 2 | RDQ46 | C (LVDS)* |
| P26 | PR36A | 2 | RDQS36 | T (LVDS)* | PR46A | 2 | RDQS46 | T (LVDS)* |
| K30 | PR35B | 2 | RDQ36 | C | PR45B | 2 | RDQ46 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| K29 | PR35A | 2 | RDQ36 | T | PR45A | 2 | RDQ46 | T |
| N22 | PR34B | 2 | RDQ36 | C (LVDS)* | PR44B | 2 | RDQ46 | C (LVDS)* |
| P22 | PR34A | 2 | RDQ36 | T (LVDS)* | PR44A | 2 | RDQ46 | T (LVDS)* |
| J30 | PR33B | 2 | RUM3_SPLLC_FB_A/RDQ36 | C | PR43B | 2 | RUM3_SPLLC_FB_A/RDQ46 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J29 | PR33A | 2 | RUM3_SPLLT_FB_A/RDQ36 | T | PR43A | 2 | RUM3_SPLLT_FB_A/RDQ46 | T |
| N24 | PR32B | 2 | RUM3_SPLLC_IN_A/RDQ36 | C (LVDS)* | PR42B | 2 | RUM3_SPLLC_IN_A/RDQ46 | C (LVDS)* |
| N23 | PR32A | 2 | RUM3_SPLLT_IN_A/RDQ36 | T (LVDS)* | PR42A | 2 | RUM3_SPLLT_IN_A/RDQ46 | T (LVDS)* |
| N25 | PR30B | 2 | RDQ27 | C | PR40B | 2 | RDQ37 | C |
| N26 | PR30A | 2 | RDQ27 | T | PR40A | 2 | RDQ37 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| M27 | PR29B | 2 | RDQ27 | C (LVDS)* | PR39B | 2 | RDQ37 | C (LVDS)* |
| M28 | PR29A | 2 | RDQ27 | T (LVDS)* | PR39A | 2 | RDQ37 | T (LVDS)* |
| H30 | PR28B | 2 | RDQ27 | C | PR38B | 2 | RDQ37 | C |
| G30 | PR28A | 2 | RDQ27 | T | PR38A | 2 | RDQ37 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M25 | PR27B | 2 | RDQ27 | C (LVDS)* | PR37B | 2 | RDQ37 | C (LVDS)* |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M26 | PR27A | 2 | RDQS27 | T (LVDS)* | PR37A | 2 | RDQS37 | T (LVDS)* |
| L30 | PR26B | 2 | RDQ27 | C | PR36B | 2 | RDQ37 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| L29 | PR26A | 2 | RDQ27 | T | PR36A | 2 | RDQ37 | T |
| L28 | PR25B | 2 | RDQ27 | C (LVDS)* | PR35B | 2 | RDQ37 | C (LVDS)* |
| L27 | PR25A | 2 | RDQ27 | T (LVDS)* | PR35A | 2 | RDQ37 | T (LVDS)* |
| H29 | PR24B | 2 | RDQ27 | C | PR34B | 2 | RDQ37 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G29 | PR24A | 2 | RDQ27 | T | PR34A | 2 | RDQ37 | T |
| L22 | PR23B | 2 | RDQ27 | C (LVDS)* | PR33B | 2 | RDQ37 | C (LVDS)* |
| M22 | PR23A | 2 | RDQ27 | T (LVDS)* | PR33A | 2 | RDQ37 | T (LVDS)* |
| F30 | PR21B | 2 | | C | PR31B | 2 | RDQ28 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| F29 | PR21A | 2 | | T | PR31A | 2 | RDQ28 | T |
| - | - | - | | | - | - | | |
| - | - | - | | | - | - | | |
| E30 | PR20B | 2 | | C (LVDS)* | PR30B | 2 | RDQ28 | C (LVDS)* |
| E29 | PR20A | 2 | | T (LVDS)* | PR30A | 2 | RDQ28 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | - | - | | |
| L25 | PR19B | 2 | | C | PR29B | 2 | RDQ28 | C |
| L26 | PR19A | 2 | | T | PR29A | 2 | RDQ28 | T |
| - | - | - | | | VCCIO2 | 2 | | |
| H28 | PR18B | 2 | | C (LVDS)* | PR28B | 2 | RDQ28 | C (LVDS)* |
| J28 | PR18A | 2 | | T (LVDS)* | PR28A | 2 | RDQS28 | T (LVDS)* |
| G28 | PR16B | 2 | | C | PR27B | 2 | RDQ28 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| G27 | PR16A | 2 | | T | PR27A | 2 | RDQ28 | T |
| L24 | NC | - | | | PR26B | 2 | RDQ28 | C (LVDS)* |
| L23 | NC | - | | | PR26A | 2 | RDQ28 | T (LVDS)* |
| D30 | NC | - | | | PR25B | 2 | RDQ28 | C |
| - | - | - | | | VCCIO2 | 2 | | |
| D29 | NC | - | | | PR25A | 2 | RDQ28 | T |
| K24 | NC | - | | | PR24B | 2 | RDQ28 | C (LVDS)* |
| K25 | NC | - | | | PR24A | 2 | RDQ28 | T (LVDS)* |
| J27 | NC | - | | | PR22B | 2 | | C |
| - | - | - | | | GNDIO2 | - | | |
| K26 | NC | - | | | PR22A | 2 | | T |
| K23 | PR15B | 2 | | C (LVDS)* | PR21B | 2 | | C (LVDS)* |
| K22 | PR15A | 2 | | T (LVDS)* | PR21A | 2 | | T (LVDS)* |
| J22 | PR14B | 2 | | C | PR20B | 2 | | C |
| VCCIO | VCCIO2 | - | | | VCCIO2 | 2 | | |
| J23 | PR14A | 2 | | T | PR20A | 2 | | T |
| - | - | - | | | GNDIO2 | - | | |
| - | - | - | | | - | - | | |
| J26 | NC | - | | | PR17B | 2 | RDQ15 | C (LVDS)* |
| H26 | NC | - | | | PR17A | 2 | RDQ15 | T (LVDS)* |
| H27 | NC | - | | | PR16B | 2 | RDQ15 | C |
| G26 | NC | - | | | PR16A | 2 | RDQ15 | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| - | - | - | | | VCCIO2 | 2 | | |
| H23 | NC | - | | | PR15B | 2 | RDQ15 | C (LVDS)* |
| H24 | NC | - | | | PR15A | 2 | RDQS15 | T (LVDS)* |
| D28 | NC | - | | | PR14B | 2 | RDQ15 | C |
| - | - | - | | | GNDIO2 | - | | |
| E28 | NC | - | | | PR14A | 2 | RDQ15 | T |
| G24 | PR13B | 2 | | C (LVDS)* | PR13B | 2 | RDQ15 | C (LVDS)* |
| H25 | PR13A | 2 | | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| D27 | PR12B | 2 | RUM0_SPLLC_FB_A | C | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| GNDIO | GNDIO2 | - | | | VCCIO2 | 2 | | |
| E27 | PR12A | 2 | RUM0_SPLLT_FB_A | T | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| F26 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* |
| G25 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| F24 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| VCCIO | VCCIO2 | - | | | - | - | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| F25 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G23 | XRES | - | | | XRES | 1 | | |
| C30 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A29 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B30 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B29 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C27 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A26 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A27 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B26 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C26 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B25 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C25 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A25 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C29 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B28 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C28 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A28 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B24 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| E24 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D24 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C24 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A20 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| C20 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B20 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C19 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A23 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C23 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B23 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C22 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B22 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A21 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A22 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C21 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B19 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B18 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A19 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C18 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |
| D23 | PT73B | 1 | | C | PT82B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E21 | PT73A | 1 | | T | PT82A | 1 | | T |
| D26 | PT72B | 1 | | C | PT81B | 1 | | C |
| E26 | PT72A | 1 | | T | PT81A | 1 | | T |
| E23 | PT71B | 1 | | C | PT80B | 1 | | C |
| - | - | - | | | VCCIO1 | 1 | | |
| G22 | PT71A | 1 | | T | PT80A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | - | - | | |
| D22 | PT70B | 1 | | C | PT79B | 1 | | C |
| F21 | PT70A | 1 | | T | PT79A | 1 | | T |
| G18 | PT69B | 1 | | C | PT78B | 1 | | C |
| H18 | PT69A | 1 | | T | PT78A | 1 | | T |
| D20 | PT68B | 1 | | C | PT77B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| D21 | PT68A | 1 | | T | PT77A | 1 | | T |
| E20 | PT67B | 1 | | C | PT76B | 1 | | C |
| E19 | PT67A | 1 | | T | PT76A | 1 | | T |
| D19 | PT66B | 1 | | C | PT75B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E18 | PT66A | 1 | | T | PT75A | 1 | | T |
| D18 | PT65B | 1 | | C | PT74B | 1 | | C |
| C17 | PT65A | 1 | | T | PT74A | 1 | | T |
| A17 | PT64B | 1 | | C | PT73B | 1 | | C |
| B17 | PT64A | 1 | | T | PT73A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J18 | NC | - | | | PT66B | 1 | | C |
| J19 | NC | - | | | PT66A | 1 | | T |
| H17 | NC | - | | | PT65B | 1 | | C |
| J17 | NC | - | | | PT65A | 1 | | T |
| F18 | NC | - | | | PT64B | 1 | | C |
| F17 | NC | - | | | PT64A | 1 | | T |
| - | - | - | | | GNDIO1 | - | | |
| A16 | PT54B | 1 | | C | PT63B | 1 | | C |
| B16 | PT54A | 1 | | T | PT63A | 1 | | T |
| G17 | PT53B | 1 | | C | PT62B | 1 | | C |
| G16 | PT53A | 1 | | T | PT62A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H16 | PT52B | 1 | | C | PT61B | 1 | | C |
| F16 | PT52A | 1 | | T | PT61A | 1 | | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J16 | PT51B | 1 | | C | PT60B | 1 | | C |
| G15 | PT51A | 1 | | T | PT60A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| C16 | PT50B | 1 | | C | PT59B | 1 | | C |
| D16 | PT50A | 1 | | T | PT59A | 1 | | T |
| J15 | PT49B | 1 | | C | PT58B | 1 | | C |
| H15 | PT49A | 1 | | T | PT58A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A15 | PT48B | 1 | VREF2_1 | C | PT57B | 1 | VREF2_1 | C |
| B15 | PT48A | 1 | VREF1_1 | T | PT57A | 1 | VREF1_1 | T |
| F15 | PT47B | 1 | PCLKC1_0 | C | PT56B | 1 | PCLKC1_0 | C |
| E16 | PT47A | 1 | PCLKT1_0 | T | PT56A | 1 | PCLKT1_0 | T |
| C15 | PT46B | 0 | PCLKC0_0 | C | PT55B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| D15 | PT46A | 0 | PCLKT0_0 | T | PT55A | 0 | PCLKT0_0 | T |
| C14 | PT45B | 0 | VREF2_0 | C | PT54B | 0 | VREF2_0 | C |
| E15 | PT45A | 0 | VREF1_0 | T | PT54A | 0 | VREF1_0 | T |
| G14 | PT44B | 0 | | C | PT53B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J14 | PT44A | 0 | | T | PT53A | 0 | | T |
| F14 | PT43B | 0 | | C | PT52B | 0 | | C |
| H14 | PT43A | 0 | | T | PT52A | 0 | | T |
| A14 | PT42B | 0 | | C | PT51B | 0 | | C |
| B14 | PT42A | 0 | | T | PT51A | 0 | | T |
| D13 | PT41B | 0 | | C | PT50B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| F13 | PT41A | 0 | | T | PT50A | 0 | | T |
| G13 | PT40B | 0 | | C | PT49B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J11 | PT40A | 0 | | T | PT49A | 0 | | T |
| D4 | PT38B | 0 | | C | PT47B | 0 | | C |
| D5 | PT38A | 0 | | T | PT47A | 0 | | T |
| E5 | PT37B | 0 | | C | PT46B | 0 | | C |
| F6 | PT37A | 0 | | T | PT46A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F7 | PT34B | 0 | | C | PT43B | 0 | | C |
| D8 | PT34A | 0 | | T | PT43A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| J13 | PT32B | 0 | | C | PT41B | 0 | | C |
| G11 | PT32A | 0 | | T | PT41A | 0 | | T |
| H13 | PT31B | 0 | | C | PT40B | 0 | | C |
| H12 | PT31A | 0 | | T | PT40A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E8 | PT30B | 0 | | C | PT39B | 0 | | C |
| D9 | PT30A | 0 | | T | PT39A | 0 | | T |
| D12 | PT28B | 0 | | C | PT37B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E13 | PT28A | 0 | | T | PT37A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| J12 | PT5B | 0 | | C | PT31B | 0 | | C |
| GNDIO | GNDIO0 | - | | | - | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H10 | PT5A | 0 | | T | PT31A | 0 | | T |
| E12 | PT4B | 0 | | C | PT30B | 0 | | C |
| D11 | PT4A | 0 | | T | PT30A | 0 | | T |
| H11 | PT3B | 0 | | C | PT29B | 0 | | C |
| F11 | PT3A | 0 | | T | PT29A | 0 | | T |
| C13 | VCC | - | | | ULC_SQ_VCCRX0 | 11 | | |
| A12 | PT19A | 0 | | T | ULC_SQ_HDINP0 | 11 | | T |
| B13 | NC | - | | | ULC_SQ_VCCIB0 | 11 | | |
| B12 | PT19B | 0 | | C | ULC_SQ_HDINN0 | 11 | | C |
| C10 | VCC | - | | | ULC_SQ_VCCTX0 | 11 | | |
| A9 | PT17A | 0 | | T | ULC_SQ_HDOUTP0 | 11 | | T |
| A10 | NC | - | | | ULC_SQ_VCCOB0 | 11 | | |
| B9 | PT17B | 0 | | C | ULC_SQ_HDOUTN0 | 11 | | C |
| C9 | VCC | - | | | ULC_SQ_VCCTX1 | 11 | | |
| B8 | PT18B | 0 | | C | ULC_SQ_HDOUTN1 | 11 | | C |
| C8 | NC | - | | | ULC_SQ_VCCOB1 | 11 | | |
| A8 | PT18A | 0 | | T | ULC_SQ_HDOUTP1 | 11 | | T |
| C12 | VCC | - | | | ULC_SQ_VCCRX1 | 11 | | |
| B11 | PT16B | 0 | | C | ULC_SQ_HDINN1 | 11 | | C |
| C11 | NC | - | | | ULC_SQ_VCCIB1 | 11 | | |
| A11 | PT16A | 0 | | T | ULC_SQ_HDINP1 | 11 | | T |
| B7 | VCCAUX | - | | | ULC_SQ_VCCAUX33 | 11 | | |
| E7 | PT15B | 0 | | C | ULC_SQ_REFCLKN | 11 | | C |
| D7 | PT15A | 0 | | T | ULC_SQ_REFCLKP | 11 | | T |
| C7 | VCC | - | | | ULC_SQ_VCCP | 11 | | |
| A3 | PT12A | 0 | | T | ULC_SQ_HDINP2 | 11 | | T |
| C3 | NC | - | | | ULC_SQ_VCCIB2 | 11 | | |
| B3 | PT12B | 0 | | C | ULC_SQ_HDINN2 | 11 | | C |
| C2 | VCC | - | | | ULC_SQ_VCCRX2 | 11 | | |
| A6 | PT14A | 0 | | T | ULC_SQ_HDOUTP2 | 11 | | T |
| C6 | NC | - | | | ULC_SQ_VCCOB2 | 11 | | |
| B6 | PT14B | 0 | | C | ULC_SQ_HDOUTN2 | 11 | | C |
| C5 | VCC | - | | | ULC_SQ_VCCTX2 | 11 | | |
| B5 | PT13B | 0 | | C | ULC_SQ_HDOUTN3 | 11 | | C |
| A4 | NC | - | | | ULC_SQ_VCCOB3 | 11 | | |
| A5 | PT13A | 0 | | T | ULC_SQ_HDOUTP3 | 11 | | T |
| C4 | VCC | - | | | ULC_SQ_VCCTX3 | 11 | | |
| B2 | PT11B | 0 | | C | ULC_SQ_HDINN3 | 11 | | C |
| B1 | NC | - | | | ULC_SQ_VCCIB3 | 11 | | |
| A2 | PT11A | 0 | | T | ULC_SQ_HDINP3 | 11 | | T |
| C1 | VCC | - | | | ULC_SQ_VCCRX3 | 11 | | |
| L12 | VCC | - | | | VCC | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L13 | VCC | - | | | VCC | - | | |
| L18 | VCC | - | | | VCC | - | | |
| L19 | VCC | - | | | VCC | - | | |
| M11 | VCC | - | | | VCC | - | | |
| M12 | VCC | - | | | VCC | - | | |
| M13 | VCC | - | | | VCC | - | | |
| M14 | VCC | - | | | VCC | - | | |
| M15 | VCC | - | | | VCC | - | | |
| M16 | VCC | - | | | VCC | - | | |
| M17 | VCC | - | | | VCC | - | | |
| M18 | VCC | - | | | VCC | - | | |
| M19 | VCC | - | | | VCC | - | | |
| M20 | VCC | - | | | VCC | - | | |
| N11 | VCC | - | | | VCC | - | | |
| N12 | VCC | - | | | VCC | - | | |
| N19 | VCC | - | | | VCC | - | | |
| N20 | VCC | - | | | VCC | - | | |
| P12 | VCC | - | | | VCC | - | | |
| P19 | VCC | - | | | VCC | - | | |
| R12 | VCC | - | | | VCC | - | | |
| R19 | VCC | - | | | VCC | - | | |
| T12 | VCC | - | | | VCC | - | | |
| T19 | VCC | - | | | VCC | - | | |
| U12 | VCC | - | | | VCC | - | | |
| U19 | VCC | - | | | VCC | - | | |
| V11 | VCC | - | | | VCC | - | | |
| V12 | VCC | - | | | VCC | - | | |
| V19 | VCC | - | | | VCC | - | | |
| V20 | VCC | - | | | VCC | - | | |
| W11 | VCC | - | | | VCC | - | | |
| W12 | VCC | - | | | VCC | - | | |
| W13 | VCC | - | | | VCC | - | | |
| W14 | VCC | - | | | VCC | - | | |
| W15 | VCC | - | | | VCC | - | | |
| W16 | VCC | - | | | VCC | - | | |
| W17 | VCC | - | | | VCC | - | | |
| W18 | VCC | - | | | VCC | - | | |
| W19 | VCC | - | | | VCC | - | | |
| W20 | VCC | - | | | VCC | - | | |
| Y12 | VCC | - | | | VCC | - | | |
| Y13 | VCC | - | | | VCC | - | | |
| Y18 | VCC | - | | | VCC | - | | |
| Y19 | VCC | - | | | VCC | - | | |
| D14 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E6 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K13 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D17 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E22 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E25 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F19 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K19 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F28 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K28 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M24 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N28 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| P21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| R25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| AA28 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AB25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AE28 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V28 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| W21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| W24 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA19 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AE19 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AF22 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AG17 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AG25 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA13 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AF9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG14 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG6 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AB6 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AE3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T6 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| F3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| P10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| R6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AA25 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AD28 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AA10 | VCCAUX | - | | | VCCAUX | - | | |
| AA11 | VCCAUX | - | | | VCCAUX | - | | |
| AA20 | VCCAUX | - | | | VCCAUX | - | | |
| AA21 | VCCAUX | - | | | VCCAUX | - | | |
| K10 | VCCAUX | - | | | VCCAUX | - | | |
| K11 | VCCAUX | - | | | VCCAUX | - | | |
| K20 | VCCAUX | - | | | VCCAUX | - | | |
| K21 | VCCAUX | - | | | VCCAUX | - | | |
| L10 | VCCAUX | - | | | VCCAUX | - | | |
| L11 | VCCAUX | - | | | VCCAUX | - | | |
| L20 | VCCAUX | - | | | VCCAUX | - | | |
| L21 | VCCAUX | - | | | VCCAUX | - | | |
| Y10 | VCCAUX | - | | | VCCAUX | - | | |
| Y11 | VCCAUX | - | | | VCCAUX | - | | |
| Y20 | VCCAUX | - | | | VCCAUX | - | | |
| Y21 | VCCAUX | - | | | VCCAUX | - | | |
| A1 | GND | - | | | GND | - | | |
| A13 | GND | - | | | GND | - | | |
| A18 | GND | - | | | GND | - | | |
| A24 | GND | - | | | GND | - | | |
| A30 | GND | - | | | GND | - | | |
| A7 | GND | - | | | GND | - | | |
| AA14 | GND | - | | | GND | - | | |
| AA15 | GND | - | | | GND | - | | |
| AA16 | GND | - | | | GND | - | | |
| AA17 | GND | - | | | GND | - | | |
| AA24 | GND | - | | | GND | - | | |
| AA27 | GND | - | | | GND | - | | |
| AA4 | GND | - | | | GND | - | | |
| AB24 | GND | - | | | GND | - | | |
| AB7 | GND | - | | | GND | - | | |
| AD12 | GND | - | | | GND | - | | |
| AD19 | GND | - | | | GND | - | | |
| AD27 | GND | - | | | GND | - | | |
| AE22 | GND | - | | | GND | - | | |
| AE27 | GND | - | | | GND | - | | |
| AE4 | GND | - | | | GND | - | | |
| AE9 | GND | - | | | GND | - | | |
| AF14 | GND | - | | | GND | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AF17 | GND | - | | | GND | - | | |
| AF25 | GND | - | | | GND | - | | |
| AF6 | GND | - | | | GND | - | | |
| AJ10 | GND | - | | | GND | - | | |
| AJ21 | GND | - | | | GND | - | | |
| AJ27 | GND | - | | | GND | - | | |
| AJ4 | GND | - | | | GND | - | | |
| AK1 | GND | - | | | GND | - | | |
| AK13 | GND | - | | | GND | - | | |
| AK18 | GND | - | | | GND | - | | |
| AK24 | GND | - | | | GND | - | | |
| AK30 | GND | - | | | GND | - | | |
| AK7 | GND | - | | | GND | - | | |
| B10 | GND | - | | | GND | - | | |
| B21 | GND | - | | | GND | - | | |
| B27 | GND | - | | | GND | - | | |
| B4 | GND | - | | | GND | - | | |
| D25 | GND | - | | | GND | - | | |
| D6 | GND | - | | | GND | - | | |
| E14 | GND | - | | | GND | - | | |
| E17 | GND | - | | | GND | - | | |
| F22 | GND | - | | | GND | - | | |
| F27 | GND | - | | | GND | - | | |
| F4 | GND | - | | | GND | - | | |
| F9 | GND | - | | | GND | - | | |
| G12 | GND | - | | | GND | - | | |
| G19 | GND | - | | | GND | - | | |
| J24 | GND | - | | | GND | - | | |
| J7 | GND | - | | | GND | - | | |
| K14 | GND | - | | | GND | - | | |
| K15 | GND | - | | | GND | - | | |
| K16 | GND | - | | | GND | - | | |
| K17 | GND | - | | | GND | - | | |
| K27 | GND | - | | | GND | - | | |
| K4 | GND | - | | | GND | - | | |
| L14 | GND | - | | | GND | - | | |
| L15 | GND | - | | | GND | - | | |
| L16 | GND | - | | | GND | - | | |
| L17 | GND | - | | | GND | - | | |
| M23 | GND | - | | | GND | - | | |
| M8 | GND | - | | | GND | - | | |
| N14 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N16 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| N27 | GND | - | | | GND | - | | |
| N4 | GND | - | | | GND | - | | |
| P11 | GND | - | | | GND | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P16 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| P18 | GND | - | | | GND | - | | |
| P20 | GND | - | | | GND | - | | |
| R10 | GND | - | | | GND | - | | |
| R11 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| R15 | GND | - | | | GND | - | | |
| R16 | GND | - | | | GND | - | | |
| R17 | GND | - | | | GND | - | | |
| R18 | GND | - | | | GND | - | | |
| R20 | GND | - | | | GND | - | | |
| R21 | GND | - | | | GND | - | | |
| R24 | GND | - | | | GND | - | | |
| R7 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T13 | GND | - | | | GND | - | | |
| T14 | GND | - | | | GND | - | | |
| T15 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T18 | GND | - | | | GND | - | | |
| T20 | GND | - | | | GND | - | | |
| T21 | GND | - | | | GND | - | | |
| T24 | GND | - | | | GND | - | | |
| T7 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U15 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| U18 | GND | - | | | GND | - | | |
| U20 | GND | - | | | GND | - | | |
| V14 | GND | - | | | GND | - | | |
| V15 | GND | - | | | GND | - | | |
| V16 | GND | - | | | GND | - | | |
| V17 | GND | - | | | GND | - | | |
| V27 | GND | - | | | GND | - | | |
| V4 | GND | - | | | GND | - | | |
| W23 | GND | - | | | GND | - | | |
| W8 | GND | - | | | GND | - | | |
| Y14 | GND | - | | | GND | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| Y15 | GND | - | | | GND | - | | |
| Y16 | GND | - | | | GND | - | | |
| Y17 | GND | - | | | GND | - | | |
| AA26 | NC | - | | | NC | - | | |
| AB10 | PL73B | 6 | LDQ71 | C (LVDS)* | NC | - | | |
| AB11 | NC | - | | | NC | - | | |
| AB12 | NC | - | | | NC | - | | |
| AB13 | NC | - | | | NC | - | | |
| AB14 | NC | - | | | NC | - | | |
| AB15 | NC | - | | | NC | - | | |
| AB16 | NC | - | | | NC | - | | |
| AB17 | NC | - | | | NC | - | | |
| AB19 | NC | - | | | NC | - | | |
| AB20 | NC | - | | | NC | - | | |
| AB21 | NC | - | | | NC | - | | |
| AB9 | PL73A | 6 | LDQ71 | T (LVDS)* | NC | - | | |
| AC10 | PL74B | 6 | LDQ71 | C | NC | - | | |
| AC11 | NC | - | | | NC | - | | |
| AC21 | NC | - | | | NC | - | | |
| AC22 | NC | - | | | NC | - | | |
| AC8 | PL70B | 6 | LDQ71 | C | NC | - | | |
| AC9 | PL74A | 6 | LDQ71 | T | NC | - | | |
| AD21 | NC | - | | | NC | - | | |
| AD22 | NC | - | | | NC | - | | |
| AD4 | PL68A | 6 | LDQ71 | T | NC | - | | |
| AD5 | PL68B | 6 | LDQ71 | C | NC | - | | |
| AD6 | PL71A | 6 | LDQS71 | T (LVDS)* | NC | - | | |
| AD7 | PL72A | 6 | LDQ71 | T | NC | - | | |
| AD8 | PL72B | 6 | LDQ71 | C | NC | - | | |
| AE23 | NC | - | | | NC | - | | |
| AE5 | PL69A | 6 | LDQ71 | T (LVDS)* | NC | - | | |
| AE6 | PL70A | 6 | LDQ71 | T | NC | - | | |
| AE7 | PL71B | 6 | LDQ71 | C (LVDS)* | NC | - | | |
| AF20 | NC | - | | | NC | - | | |
| AF23 | NC | - | | | NC | - | | |
| AF5 | PL69B | 6 | LDQ71 | C (LVDS)* | NC | - | | |
| AG23 | NC | - | | | NC | - | | |
| AG26 | NC | - | | | NC | - | | |
| D10 | PT10A | 0 | | T | NC | - | | |
| E10 | PT9B | 0 | | C | NC | - | | |
| E11 | PT10B | 0 | | C | NC | - | | |
| F10 | PT9A | 0 | | T | NC | - | | |
| F20 | NC | - | | | NC | - | | |
| F23 | NC | - | | | NC | - | | |
| F8 | PL6B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| G10 | NC | - | | | NC | - | | |
| G20 | NC | - | | | NC | - | | |
| G21 | NC | - | | | NC | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G7 | PL8A | 7 | LDQ6 | T (LVDS)* | NC | - | | |
| G8 | PL6A | 7 | LDQS6**** | T (LVDS)* | NC | - | | |
| G9 | PL5A | 7 | LDQ6 | T | NC | - | | |
| H19 | NC | - | | | NC | - | | |
| H20 | NC | - | | | NC | - | | |
| H21 | NC | - | | | NC | - | | |
| H22 | NC | - | | | NC | - | | |
| H6 | PL8B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| H8 | PL5B | 7 | LDQ6 | C | NC | - | | |
| H9 | PL2A | 7 | LDQ6 | T (LVDS)* | NC | - | | |
| J10 | PL2B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| J20 | NC | - | | | NC | - | | |
| J21 | NC | - | | | NC | - | | |
| J9 | PL4A | 7 | LDQ6 | T (LVDS)* | NC | - | | |
| K9 | PL4B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| R9 | NC | - | | | NC | - | | |
| U22 | NC | - | | | NC | - | | |
| W9 | NC | - | | | NC | - | | |
| N13 | VCCPLL | - | | | VCCPLL | - | | |
| N18 | VCCPLL | - | | | VCCPLL | - | | |
| V13 | VCCPLL | - | | | VCCPLL | - | | |
| V18 | VCCPLL | - | | | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** These sysCONFIG pins are dedicated I/O pins for configuration. The outpus are actively driven during normal device operation.
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| D2 | PL9A | 7 | VREF2_7 | T |
| D3 | PL9B | 7 | VREF1_7 | C |
| GNDIO | GNDIO7 | - | | |
| J8 | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* |
| H7 | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* |
| E3 | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T |
| E4 | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C |
| G6 | PL13A | 7 | LDQ15 | T (LVDS)* |
| F5 | PL13B | 7 | LDQ15 | C (LVDS)* |
| E2 | PL14A | 7 | LDQ15 | T |
| D1 | PL14B | 7 | LDQ15 | C |
| GNDIO | GNDIO7 | - | | |
| G5 | PL15A | 7 | LDQS15 | T (LVDS)* |
| G4 | PL15B | 7 | LDQ15 | C (LVDS)* |
| K7 | PL16A | 7 | LDQ15 | T |
| K8 | PL16B | 7 | LDQ15 | C |
| E1 | PL17A | 7 | LDQ15 | T (LVDS)* |
| F2 | PL17B | 7 | LDQ15 | C (LVDS)* |
| F1 | PL18A | 7 | LDQ15 | T |
| GNDIO | GNDIO7 | - | | |
| G3 | PL18B | 7 | LDQ15 | C |
| GNDIO | GNDIO7 | - | | |
| H5 | PL25A | 7 | LDQ23 | T (LVDS)* |
| H4 | PL25B | 7 | LDQ23 | C (LVDS)* |
| J5 | PL26A | 7 | LDQ23 | T |
| J4 | PL26B | 7 | LDQ23 | C |
| GNDIO | GNDIO7 | - | | |
| G2 | PL28A | 7 | LDQ32 | T (LVDS)* |
| G1 | PL28B | 7 | LDQ32 | C (LVDS)* |
| L9 | PL29A | 7 | LDQ32 | T |
| L7 | PL29B | 7 | LDQ32 | C |
| K6 | PL30A | 7 | LDQ32 | T (LVDS)* |
| K5 | PL30B | 7 | LDQ32 | C (LVDS)* |
| L8 | PL31A | 7 | LDQ32 | T |
| L6 | PL31B | 7 | LDQ32 | C |
| GNDIO | GNDIO7 | - | | |
| H3 | PL32A | 7 | LDQS32 | T (LVDS)* |
| H2 | PL32B | 7 | LDQ32 | C (LVDS)* |
| N8 | PL33A | 7 | LDQ32 | T |
| M9 | PL33B | 7 | LDQ32 | C |
| J3 | PL34A | 7 | LDQ32 | T (LVDS)* |
| - | - | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| J2 | PL34B | 7 | LDQ32 | C (LVDS)* |
| H1 | PL35A | 7 | LDQ32 | T |
| GNDIO | GNDIO7 | - | | |
| J1 | PL35B | 7 | LDQ32 | C |
| GNDIO | GNDIO7 | - | | |
| L5 | PL41A | 7 | LDQ45 | T (LVDS)* |
| L4 | PL41B | 7 | LDQ45 | C (LVDS)* |
| N9 | PL42A | 7 | LDQ45 | T |
| N7 | PL42B | 7 | LDQ45 | C |
| K2 | PL43A | 7 | LDQ45 | T (LVDS)* |
| K1 | PL43B | 7 | LDQ45 | C (LVDS)* |
| P9 | PL44A | 7 | LDQ45 | T |
| P7 | PL44B | 7 | LDQ45 | C |
| GNDIO | GNDIO7 | - | | |
| M6 | PL45A | 7 | LDQS45 | T (LVDS)* |
| M5 | PL45B | 7 | LDQ45 | C (LVDS)* |
| N5 | PL46A | 7 | LDQ45 | T |
| N6 | PL46B | 7 | LDQ45 | C |
| M4 | PL47A | 7 | LDQ45 | T (LVDS)* |
| M3 | PL47B | 7 | LDQ45 | C (LVDS)* |
| P6 | PL48A | 7 | LDQ45 | T |
| GNDIO | GNDIO7 | - | | |
| P8 | PL48B | 7 | LDQ45 | C |
| L3 | PL50A | 7 | LUM3_SPLLT_IN_A/LDQ54 | T (LVDS)* |
| L2 | PL50B | 7 | LUM3_SPLLC_IN_A/LDQ54 | C (LVDS)* |
| P5 | PL51A | 7 | LUM3_SPLLT_FB_A/LDQ54 | T |
| P4 | PL51B | 7 | LUM3_SPLLC_FB_A/LDQ54 | C |
| L1 | PL52A | 7 | LDQ54 | T (LVDS)* |
| M2 | PL52B | 7 | LDQ54 | C (LVDS)* |
| R5 | PL53A | 7 | LDQ54 | T |
| R4 | PL53B | 7 | LDQ54 | C |
| GNDIO | GNDIO7 | - | | |
| M1 | PL54A | 7 | LDQS54 | T (LVDS)* |
| N2 | PL54B | 7 | LDQ54 | C (LVDS)* |
| R8 | PL55A | 7 | LDQ54 | T |
| T9 | PL55B | 7 | LDQ54 | C |
| P3 | PL56A | 7 | LDQ54 | T (LVDS)* |
| P2 | PL56B | 7 | LDQ54 | C (LVDS)* |
| N1 | PL57A | 7 | PCLKT7_0/LDQ54 | T |
| GNDIO | GNDIO7 | - | | |
| P1 | PL57B | 7 | PCLKC7_0/LDQ54 | C |
| T5 | PL59A | 6 | PCLKT6_0/LDQ63 | T (LVDS)* |
| T4 | PL59B | 6 | PCLKC6_0/LDQ63 | C (LVDS)* |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| U7 | PL60A | 6 | VREF2_6/LDQ63 | T |
| T8 | PL60B | 6 | VREF1_6/LDQ63 | C |
| R3 | PL61A | 6 | LDQ63 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| R2 | PL61B | 6 | LDQ63 | C (LVDS)* |
| R1 | PL62A | 6 | LDQ63 | T |
| T1 | PL62B | 6 | LDQ63 | C |
| GNDIO | GNDIO6 | - | | |
| VCCIO | VCCIO6 | 6 | | |
| T3 | PL65A | 6 | LLM4_SPLLT_IN_A/LDQ63 | T (LVDS)* |
| T2 | PL65B | 6 | LLM4_SPLLC_IN_A/LDQ63 | C (LVDS)* |
| U9 | PL66A | 6 | LLM4_SPLLT_FB_A/LDQ63 | T |
| U8 | PL66B | 6 | LLM4_SPLLC_FB_A/LDQ63 | C |
| GNDIO | GNDIO6 | - | | |
| U5 | PL68A | 6 | LDQ72 | T (LVDS)* |
| U4 | PL68B | 6 | LDQ72 | C (LVDS)* |
| V9 | PL69A | 6 | LDQ72 | T |
| V7 | PL69B | 6 | LDQ72 | C |
| VCCIO | VCCIO6 | 6 | | |
| U3 | PL70A | 6 | LDQ72 | T (LVDS)* |
| U2 | PL70B | 6 | LDQ72 | C (LVDS)* |
| V8 | PL71A | 6 | LDQ72 | T |
| U6 | PL71B | 6 | LDQ72 | C |
| GNDIO | GNDIO6 | - | | |
| U1 | PL72A | 6 | LDQS72 | T (LVDS)* |
| V2 | PL72B | 6 | LDQ72 | C (LVDS)* |
| V5 | PL73A | 6 | LDQ72 | T |
| VCCIO | VCCIO6 | 6 | | |
| V6 | PL73B | 6 | LDQ72 | C |
| V1 | PL74A | 6 | LDQ72 | T (LVDS)* |
| W1 | PL74B | 6 | LDQ72 | C (LVDS)* |
| W5 | PL75A | 6 | LDQ72 | T |
| GNDIO | GNDIO6 | - | | |
| W6 | PL75B | 6 | LDQ72 | C |
| W3 | PL77A | 6 | LDQ81 | T (LVDS)* |
| W4 | PL77B | 6 | LDQ81 | C (LVDS)* |
| W2 | PL78A | 6 | LDQ81 | T |
| Y4 | PL78B | 6 | LDQ81 | C |
| Y1 | PL79A | 6 | LDQ81 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| Y2 | PL79B | 6 | LDQ81 | C (LVDS)* |
| Y5 | PL80A | 6 | LDQ81 | T |
| Y6 | PL80B | 6 | LDQ81 | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AA1 | PL81A | 6 | LDQS81 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| AA2 | PL81B | 6 | LDQ81 | C (LVDS)* |
| Y3 | PL82A | 6 | LDQ81 | T |
| AB1 | PL82B | 6 | LDQ81 | C |
| VCCIO | VCCIO6 | 6 | | |
| Y9 | PL83A | 6 | LDQ81 | T (LVDS)* |
| Y8 | PL83B | 6 | LDQ81 | C (LVDS)* |
| Y7 | PL84A | 6 | LDQ81 | T |
| AA7 | PL84B | 6 | LDQ81 | C |
| GNDIO | GNDIO6 | - | | |
| VCCIO | VCCIO6 | 6 | | |
| AB2 | PL95A | 6 | LDQ99 | T (LVDS)* |
| AB3 | PL95B | 6 | LDQ99 | C (LVDS)* |
| AA5 | PL96A | 6 | LDQ99 | T |
| AA6 | PL96B | 6 | LDQ99 | C |
| AB4 | PL97A | 6 | LDQ99 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| AB5 | PL97B | 6 | LDQ99 | C (LVDS)* |
| AA8 | PL98A | 6 | LDQ99 | T |
| AA9 | PL98B | 6 | LDQ99 | C |
| AC1 | PL99A | 6 | LLM0_GPLLT_IN_A**/LDQS99 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| AC2 | PL99B | 6 | LLM0_GPLLC_IN_A**/LDQ99 | C (LVDS)* |
| AC4 | PL100A | 6 | LLM0_GPLLT_FB_A/LDQ99 | T |
| AC3 | PL100B | 6 | LLM0_GPLLC_FB_A/LDQ99 | C |
| VCCIO | VCCIO6 | 6 | | |
| AC7 | PL101A | 6 | LLM0_GDLLT_IN_A**/LDQ99 | T (LVDS)* |
| AC6 | PL101B | 6 | LLM0_GDLLC_IN_A**/LDQ99 | C (LVDS)* |
| AC5 | PL102A | 6 | LLM0_GDLLT_FB_A/LDQ99 | T |
| AD3 | PL102B | 6 | LLM0_GDLLC_FB_A/LDQ99 | C |
| GNDIO | GNDIO6 | - | | |
| AB8 | LLM0_PLLCAP | 6 | | |
| AD2 | PL104A | 6 | | T |
| AD1 | PL104B | 6 | | C |
| AE2 | TCK | - | | |
| AE1 | TDI | - | | |
| AF2 | TMS | - | | |
| AF1 | TDO | - | | |
| AG1 | VCCJ | - | | |
| AH1 | LLC_SQ_VCCRX3 | 14 | | |
| AK2 | LLC_SQ_HDINP3 | 14 | | T |
| AJ1 | LLC_SQ_VCCIB3 | 14 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| AJ2 | LLC_SQ_HDINN3 | 14 | | C |
| AH4 | LLC_SQ_VCCTX3 | 14 | | |
| AK5 | LLC_SQ_HDOUTP3 | 14 | | T |
| AK4 | LLC_SQ_VCCOB3 | 14 | | |
| AJ5 | LLC_SQ_HDOUTN3 | 14 | | C |
| AH5 | LLC_SQ_VCCTX2 | 14 | | |
| AJ6 | LLC_SQ_HDOUTN2 | 14 | | C |
| AH6 | LLC_SQ_VCCOB2 | 14 | | |
| AK6 | LLC_SQ_HDOUTP2 | 14 | | T |
| AH2 | LLC_SQ_VCCRX2 | 14 | | |
| AJ3 | LLC_SQ_HDINN2 | 14 | | C |
| AH3 | LLC_SQ_VCCIB2 | 14 | | |
| AK3 | LLC_SQ_HDINP2 | 14 | | T |
| AH7 | LLC_SQ_VCCP | 14 | | |
| AG7 | LLC_SQ_REFCLKP | 14 | | T |
| AF7 | LLC_SQ_REFCLKN | 14 | | C |
| AJ7 | LLC_SQ_VCCAUX33 | 14 | | |
| AK11 | LLC_SQ_HDINP1 | 14 | | T |
| AH11 | LLC_SQ_VCCIB1 | 14 | | |
| AJ11 | LLC_SQ_HDINN1 | 14 | | C |
| AH12 | LLC_SQ_VCCRX1 | 14 | | |
| AK8 | LLC_SQ_HDOUTP1 | 14 | | T |
| AH8 | LLC_SQ_VCCOB1 | 14 | | |
| AJ8 | LLC_SQ_HDOUTN1 | 14 | | C |
| AH9 | LLC_SQ_VCCTX1 | 14 | | |
| AJ9 | LLC_SQ_HDOUTN0 | 14 | | C |
| AK10 | LLC_SQ_VCCOB0 | 14 | | |
| AK9 | LLC_SQ_HDOUTP0 | 14 | | T |
| AH10 | LLC_SQ_VCCTX0 | 14 | | |
| AJ12 | LLC_SQ_HDINN0 | 14 | | C |
| AJ13 | LLC_SQ_VCCIB0 | 14 | | |
| AK12 | LLC_SQ_HDINP0 | 14 | | T |
| AH13 | LLC_SQ_VCCRX0 | 14 | | |
| AF10 | PB30A | 5 | BDQ33 | T |
| AE8 | PB30B | 5 | BDQ33 | C |
| AE11 | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | |
| AD9 | PB31B | 5 | BDQ33 | C |
| AE10 | PB32A | 5 | BDQ33 | T |
| AD10 | PB32B | 5 | BDQ33 | C |
| AE13 | PB33A | 5 | BDQS33 | T |
| GNDIO | GNDIO5 | - | | |
| AC12 | PB33B | 5 | BDQ33 | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AG2 | PB34A | 5 | BDQ33 | T |
| AG3 | PB34B | 5 | BDQ33 | C |
| AD13 | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | |
| AC13 | PB35B | 5 | BDQ33 | C |
| AE14 | PB36A | 5 | BDQ33 | T |
| AC14 | PB36B | 5 | BDQ33 | C |
| AF3 | PB37A | 5 | BDQ33 | T |
| GNDIO | GNDIO5 | - | | |
| AF4 | PB37B | 5 | BDQ33 | C |
| - | - | - | | |
| AG4 | PB38A | 5 | BDQ42 | T |
| AG5 | PB38B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | |
| - | - | - | | |
| AD11 | PB48A | 5 | BDQ51 | T |
| AF13 | PB48B | 5 | BDQ51 | C |
| AF12 | PB49A | 5 | BDQ51 | T |
| VCCIO | VCCIO5 | 5 | | |
| AD14 | PB49B | 5 | BDQ51 | C |
| AG8 | PB50A | 5 | BDQ51 | T |
| AF8 | PB50B | 5 | BDQ51 | C |
| AE15 | PB51A | 5 | BDQS51**** | T |
| GNDIO | GNDIO5 | - | | |
| - | - | - | | |
| AC15 | PB51B | 5 | BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | |
| AD15 | PB56A | 5 | BDQ60 | T |
| AF15 | PB56B | 5 | BDQ60 | C |
| AG10 | PB57A | 5 | BDQ60 | T |
| AG9 | PB57B | 5 | BDQ60 | C |
| AH14 | PB58A | 5 | BDQ60 | T |
| AG12 | PB58B | 5 | BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | |
| AG15 | PB59A | 5 | BDQ60 | T |
| AG13 | PB59B | 5 | BDQ60 | C |
| GNDIO | GNDIO5 | - | | |
| AF16 | PB60A | 5 | BDQS60 | T |
| AH15 | PB60B | 5 | BDQ60 | C |
| AC16 | PB61A | 5 | VREF2_5/BDQ60 | T |
| AE16 | PB61B | 5 | VREF1_5/BDQ60 | C |
| AG11 | PB62A | 5 | PCLKT5_0/BDQ60 | T |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AF11 | PB62B | 5 | PCLKC5_0/BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | |
| AJ14 | PB67A | 4 | PCLKT4_0/BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK14 | PB67B | 4 | PCLKC4_0/BDQ69 | C |
| AK15 | PB68A | 4 | VREF2_4/BDQ69 | T |
| AK16 | PB68B | 4 | VREF1_4/BDQ69 | C |
| AF18 | PB69A | 4 | BDQS69 | T |
| GNDIO | GNDIO4 | - | | |
| AD16 | PB69B | 4 | BDQ69 | C |
| AJ15 | PB70A | 4 | BDQ69 | T |
| AG16 | PB70B | 4 | BDQ69 | C |
| AE17 | PB71A | 4 | BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | |
| AC17 | PB71B | 4 | BDQ69 | C |
| AH16 | PB72A | 4 | BDQ69 | T |
| AK17 | PB72B | 4 | BDQ69 | C |
| AG20 | PB73A | 4 | BDQ69 | T |
| GNDIO | GNDIO4 | - | | |
| AG21 | PB73B | 4 | BDQ69 | C |
| AG18 | PB74A | 4 | BDQ78 | T |
| AJ16 | PB74B | 4 | BDQ78 | C |
| AF21 | PB75A | 4 | BDQ78 | T |
| AG22 | PB75B | 4 | BDQ78 | C |
| AD17 | PB76A | 4 | BDQ78 | T |
| AF19 | PB76B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | |
| AH17 | PB80A | 4 | BDQ78 | T |
| AJ17 | PB80B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | |
| AF26 | PB82A | 4 | BDQ78 | T |
| AE25 | PB82B | 4 | BDQ78 | C |
| GNDIO | GNDIO4 | - | | |
| AD24 | PB92A | 4 | BDQ96 | T |
| AE24 | PB92B | 4 | BDQ96 | C |
| AD18 | PB93A | 4 | BDQ96 | T |
| AC18 | PB93B | 4 | BDQ96 | C |
| AE18 | PB94A | 4 | BDQ96 | T |
| AG19 | PB94B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AC19 | PB96A | 4 | BDQS96 | T |
| AD20 | PB96B | 4 | BDQ96 | C |
| AB18 | PB97A | 4 | BDQ96 | T |
| AC20 | PB97B | 4 | BDQ96 | C |
| AE20 | PB98A | 4 | BDQ96 | T |
| AE21 | PB98B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | |
| AC23 | PB99A | 4 | BDQ96 | T |
| AD23 | PB99B | 4 | BDQ96 | C |
| GNDIO | GNDIO4 | - | | |
| AH18 | LRC_SQ_VCCRX3 | 13 | | |
| AK19 | LRC_SQ_HDINP3 | 13 | | T |
| AJ18 | LRC_SQ_VCCIB3 | 13 | | |
| AJ19 | LRC_SQ_HDINN3 | 13 | | C |
| AH21 | LRC_SQ_VCCTX3 | 13 | | |
| AK22 | LRC_SQ_HDOUTP3 | 13 | | T |
| AK21 | LRC_SQ_VCCOB3 | 13 | | |
| AJ22 | LRC_SQ_HDOUTN3 | 13 | | C |
| AH22 | LRC_SQ_VCCTX2 | 13 | | |
| AJ23 | LRC_SQ_HDOUTN2 | 13 | | C |
| AH23 | LRC_SQ_VCCOB2 | 13 | | |
| AK23 | LRC_SQ_HDOUTP2 | 13 | | T |
| AH19 | LRC_SQ_VCCRX2 | 13 | | |
| AJ20 | LRC_SQ_HDINN2 | 13 | | C |
| AH20 | LRC_SQ_VCCIB2 | 13 | | |
| AK20 | LRC_SQ_HDINP2 | 13 | | T |
| AH24 | LRC_SQ_VCCP | 13 | | |
| AG24 | LRC_SQ_REFCLKP | 13 | | T |
| AF24 | LRC_SQ_REFCLKN | 13 | | C |
| AJ24 | LRC_SQ_VCCAUX33 | 13 | | |
| AK28 | LRC_SQ_HDINP1 | 13 | | T |
| AH28 | LRC_SQ_VCCIB1 | 13 | | |
| AJ28 | LRC_SQ_HDINN1 | 13 | | C |
| AH29 | LRC_SQ_VCCRX1 | 13 | | |
| AK25 | LRC_SQ_HDOUTP1 | 13 | | T |
| AH25 | LRC_SQ_VCCOB1 | 13 | | |
| AJ25 | LRC_SQ_HDOUTN1 | 13 | | C |
| AH26 | LRC_SQ_VCCTX1 | 13 | | |
| AJ26 | LRC_SQ_HDOUTN0 | 13 | | C |
| AK27 | LRC_SQ_VCCOB0 | 13 | | |
| AK26 | LRC_SQ_HDOUTP0 | 13 | | T |
| AH27 | LRC_SQ_VCCTX0 | 13 | | |
| AJ29 | LRC_SQ_HDINN0 | 13 | | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AJ30 | LRC_SQ_VCCIB0 | 13 | | |
| AK29 | LRC_SQ_HDINP0 | 13 | | T |
| AH30 | LRC_SQ_VCCRX0 | 13 | | |
| AG27 | CFG2 | 8 | | |
| AD25 | CFG1 | 8 | | |
| AG28 | CFG0 | 8 | | |
| AG30 | PROGRAMN | 8 | | |
| AG29 | CCLK | 8 | | |
| AC24 | INITN | 8 | | |
| AF27 | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | |
| AF28 | WRITEN*** | 8 | | |
| AE26 | CS1N*** | 8 | | |
| AB23 | CSN*** | 8 | | |
| AF29 | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | |
| AF30 | D1*** | 8 | | |
| AD26 | D2*** | 8 | | |
| AE29 | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | |
| AE30 | D4*** | 8 | | |
| AD29 | D5*** | 8 | | |
| AC25 | D6*** | 8 | | |
| AD30 | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | |
| AA22 | DI/CSSPI0N*** | 8 | | |
| AC26 | DOUT/CSON/CSSPI1N*** | 8 | | |
| AA23 | BUSY/SISPI*** | 8 | | |
| AB22 | RLM0_PLLCAP | 3 | | |
| AC27 | PR102B | 3 | RLM0_GDLLC_FB_A/RDQ99 | C |
| GNDIO | GNDIO3 | - | | |
| AC28 | PR102A | 3 | RLM0_GDLLT_FB_A/RDQ99 | T |
| AC29 | PR101B | 3 | RLM0_GDLLC_IN_A**/RDQ99 | C (LVDS)* |
| AC30 | PR101A | 3 | RLM0_GDLLT_IN_A**/RDQ99 | T (LVDS)* |
| AB30 | PR100B | 3 | RLM0_GPLLC_IN_A**/RDQ99 | C |
| VCCIO | VCCIO3 | 3 | | |
| AA30 | PR100A | 3 | RLM0_GPLLT_IN_A**/RDQ99 | T |
| AB29 | PR99B | 3 | RLM0_GPLLC_FB_A/RDQ99 | C (LVDS)* |
| AB28 | PR99A | 3 | RLM0_GPLLT_FB_A/RDQS99 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| Y22 | PR98B | 3 | RDQ99 | C |
| Y23 | PR98A | 3 | RDQ99 | T |
| AB26 | PR97B | 3 | RDQ99 | C (LVDS)* |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AB27 | PR97A | 3 | RDQ99 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| Y24 | PR96B | 3 | RDQ99 | C |
| Y25 | PR96A | 3 | RDQ99 | T |
| AA29 | PR95B | 3 | RDQ99 | C (LVDS)* |
| Y28 | PR95A | 3 | RDQ99 | T (LVDS)* |
| Y30 | PR93B | 3 | RDQ90 | C |
| Y29 | PR93A | 3 | RDQ90 | T |
| GNDIO | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | |
| W22 | PR83B | 3 | RDQ81 | C (LVDS)* |
| V22 | PR83A | 3 | RDQ81 | T (LVDS)* |
| Y27 | PR82B | 3 | RDQ81 | C |
| VCCIO | VCCIO3 | 3 | | |
| Y26 | PR82A | 3 | RDQ81 | T |
| W30 | PR81B | 3 | RDQ81 | C (LVDS)* |
| W29 | PR81A | 3 | RDQS81 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| W25 | PR80B | 3 | RDQ81 | C |
| W26 | PR80A | 3 | RDQ81 | T |
| U29 | PR79B | 3 | RDQ81 | C (LVDS)* |
| V29 | PR79A | 3 | RDQ81 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| V30 | PR78B | 3 | RDQ81 | C |
| U30 | PR78A | 3 | RDQ81 | T |
| W27 | PR77B | 3 | RDQ81 | C (LVDS)* |
| W28 | PR77A | 3 | RDQ81 | T (LVDS)* |
| V24 | PR75B | 3 | RDQ72 | C |
| V25 | PR75A | 3 | RDQ72 | T |
| GNDIO | GNDIO3 | - | | |
| U28 | PR74B | 3 | RDQ72 | C (LVDS)* |
| U27 | PR74A | 3 | RDQ72 | T (LVDS)* |
| U23 | PR73B | 3 | RDQ72 | C |
| V23 | PR73A | 3 | RDQ72 | T |
| VCCIO | VCCIO3 | 3 | | |
| V26 | PR72B | 3 | RDQ72 | C (LVDS)* |
| U26 | PR72A | 3 | RDQS72 | T (LVDS)* |
| U25 | PR71B | 3 | RDQ72 | C |
| GNDIO | GNDIO3 | - | | |
| U24 | PR71A | 3 | RDQ72 | T |
| T30 | PR70B | 3 | RDQ72 | C (LVDS)* |
| R30 | PR70A | 3 | RDQ72 | T (LVDS)* |
| T23 | PR69B | 3 | RDQ72 | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| VCCIO | VCCIO3 | 3 | | |
| T22 | PR69A | 3 | RDQ72 | T |
| T29 | PR68B | 3 | RDQ72 | C (LVDS)* |
| T28 | PR68A | 3 | RDQ72 | T (LVDS)* |
| R23 | PR66B | 3 | RLM4_SPLLC_FB_A/RDQ63 | C |
| GNDIO | GNDIO3 | - | | |
| - | - | - | | |
| R22 | PR66A | 3 | RLM4_SPLLT_FB_A/RDQ63 | T |
| P30 | PR65B | 3 | RLM4_SPLLC_IN_A/RDQ63 | C (LVDS)* |
| R29 | PR65A | 3 | RLM4_SPLLT_IN_A/RDQ63 | T (LVDS)* |
| T27 | PR64B | 3 | RDQ63 | C |
| VCCIO | VCCIO3 | 3 | | |
| T26 | PR64A | 3 | RDQ63 | T |
| GNDIO | GNDIO3 | - | | |
| N30 | PR61B | 3 | RDQ63 | C (LVDS)* |
| N29 | PR61A | 3 | RDQ63 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| R27 | PR60B | 3 | VREF2_3/RDQ63 | C |
| R28 | PR60A | 3 | VREF1_3/RDQ63 | T |
| P29 | PR59B | 3 | PCLKC3_0/RDQ63 | C (LVDS)* |
| P28 | PR59A | 3 | PCLKT3_0/RDQ63 | T (LVDS)* |
| M30 | PR57B | 2 | PCLKC2_0/RDQ54 | C |
| M29 | PR57A | 2 | PCLKT2_0/RDQ54 | T |
| GNDIO | GNDIO2 | - | | |
| P23 | PR56B | 2 | RDQ54 | C (LVDS)* |
| P24 | PR56A | 2 | RDQ54 | T (LVDS)* |
| R26 | PR55B | 2 | RDQ54 | C |
| P27 | PR55A | 2 | RDQ54 | T |
| VCCIO | VCCIO2 | 2 | | |
| P25 | PR54B | 2 | RDQ54 | C (LVDS)* |
| P26 | PR54A | 2 | RDQS54 | T (LVDS)* |
| K30 | PR53B | 2 | RDQ54 | C |
| GNDIO | GNDIO2 | - | | |
| K29 | PR53A | 2 | RDQ54 | T |
| N22 | PR52B | 2 | RDQ54 | C (LVDS)* |
| P22 | PR52A | 2 | RDQ54 | T (LVDS)* |
| J30 | PR51B | 2 | RUM3_SPLLC_FB_A/RDQ54 | C |
| VCCIO | VCCIO2 | 2 | | |
| J29 | PR51A | 2 | RUM3_SPLLT_FB_A/RDQ54 | T |
| N24 | PR50B | 2 | RUM3_SPLLC_IN_A/RDQ54 | C (LVDS)* |
| N23 | PR50A | 2 | RUM3_SPLLT_IN_A/RDQ54 | T (LVDS)* |
| N25 | PR48B | 2 | RDQ45 | C |
| N26 | PR48A | 2 | RDQ45 | T |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| GNDIO | GNDIO2 | - | | |
| M27 | PR47B | 2 | RDQ45 | C (LVDS)* |
| M28 | PR47A | 2 | RDQ45 | T (LVDS)* |
| H30 | PR46B | 2 | RDQ45 | C |
| G30 | PR46A | 2 | RDQ45 | T |
| VCCIO | VCCIO2 | 2 | | |
| M25 | PR45B | 2 | RDQ45 | C (LVDS)* |
| M26 | PR45A | 2 | RDQS45 | T (LVDS)* |
| L30 | PR44B | 2 | RDQ45 | C |
| GNDIO | GNDIO2 | - | | |
| L29 | PR44A | 2 | RDQ45 | T |
| L28 | PR43B | 2 | RDQ45 | C (LVDS)* |
| L27 | PR43A | 2 | RDQ45 | T (LVDS)* |
| H29 | PR42B | 2 | RDQ45 | C |
| VCCIO | VCCIO2 | 2 | | |
| G29 | PR42A | 2 | RDQ45 | T |
| L22 | PR41B | 2 | RDQ45 | C (LVDS)* |
| M22 | PR41A | 2 | RDQ45 | T (LVDS)* |
| F30 | PR40B | 2 | | C |
| GNDIO | GNDIO2 | - | | |
| F29 | PR40A | 2 | | T |
| VCCIO | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | |
| E30 | PR34B | 2 | RDQ32 | C (LVDS)* |
| E29 | PR34A | 2 | RDQ32 | T (LVDS)* |
| - | - | - | | |
| L25 | PR33B | 2 | RDQ32 | C |
| L26 | PR33A | 2 | RDQ32 | T |
| VCCIO | VCCIO2 | 2 | | |
| H28 | PR32B | 2 | RDQ32 | C (LVDS)* |
| J28 | PR32A | 2 | RDQS32 | T (LVDS)* |
| G28 | PR31B | 2 | RDQ32 | C |
| GNDIO | GNDIO2 | - | | |
| G27 | PR31A | 2 | RDQ32 | T |
| L24 | PR30B | 2 | RDQ32 | C (LVDS)* |
| L23 | PR30A | 2 | RDQ32 | T (LVDS)* |
| D30 | PR29B | 2 | RDQ32 | C |
| VCCIO | VCCIO2 | 2 | | |
| D29 | PR29A | 2 | RDQ32 | T |
| K24 | PR28B | 2 | RDQ32 | C (LVDS)* |
| K25 | PR28A | 2 | RDQ32 | T (LVDS)* |
| J27 | PR26B | 2 | RDQ23 | C |
| GNDIO | GNDIO2 | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| K26 | PR26A | 2 | RDQ23 | T |
| K23 | PR25B | 2 | RDQ23 | C (LVDS)* |
| K22 | PR25A | 2 | RDQ23 | T (LVDS)* |
| J22 | PR24B | 2 | RDQ23 | C |
| VCCIO | VCCIO2 | 2 | | |
| J23 | PR24A | 2 | RDQ23 | T |
| GNDIO | GNDIO2 | - | | |
| VCCIO | VCCIO2 | 2 | | |
| J26 | PR17B | 2 | RDQ15 | C (LVDS)* |
| H26 | PR17A | 2 | RDQ15 | T (LVDS)* |
| H27 | PR16B | 2 | RDQ15 | C |
| G26 | PR16A | 2 | RDQ15 | T |
| VCCIO | VCCIO2 | 2 | | |
| H23 | PR15B | 2 | RDQ15 | C (LVDS)* |
| H24 | PR15A | 2 | RDQS15 | T (LVDS)* |
| D28 | PR14B | 2 | RDQ15 | C |
| GNDIO | GNDIO2 | - | | |
| E28 | PR14A | 2 | RDQ15 | T |
| G24 | PR13B | 2 | RDQ15 | C (LVDS)* |
| H25 | PR13A | 2 | RDQ15 | T (LVDS)* |
| D27 | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| VCCIO | VCCIO2 | 2 | | |
| E27 | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| F26 | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* |
| G25 | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| F24 | PR9B | 2 | VREF2_2 | C |
| - | - | - | | |
| GNDIO | GNDIO2 | - | | |
| F25 | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | |
| G23 | XRES | 1 | | |
| C30 | URC_SQ_VCCRX0 | 12 | | |
| A29 | URC_SQ_HDINP0 | 12 | | T |
| B30 | URC_SQ_VCCIB0 | 12 | | |
| B29 | URC_SQ_HDINN0 | 12 | | C |
| C27 | URC_SQ_VCCTX0 | 12 | | |
| A26 | URC_SQ_HDOUTP0 | 12 | | T |
| A27 | URC_SQ_VCCOB0 | 12 | | |
| B26 | URC_SQ_HDOUTN0 | 12 | | C |
| C26 | URC_SQ_VCCTX1 | 12 | | |
| B25 | URC_SQ_HDOUTN1 | 12 | | C |
| C25 | URC_SQ_VCCOB1 | 12 | | |
| A25 | URC_SQ_HDOUTP1 | 12 | | T |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| C29 | URC_SQ_VCCRX1 | 12 | | |
| B28 | URC_SQ_HDINN1 | 12 | | C |
| C28 | URC_SQ_VCCIB1 | 12 | | |
| A28 | URC_SQ_HDINP1 | 12 | | T |
| B24 | URC_SQ_VCCAUX33 | 12 | | |
| E24 | URC_SQ_REFCLKN | 12 | | C |
| D24 | URC_SQ_REFCLKP | 12 | | T |
| C24 | URC_SQ_VCCP | 12 | | |
| A20 | URC_SQ_HDINP2 | 12 | | T |
| C20 | URC_SQ_VCCIB2 | 12 | | |
| B20 | URC_SQ_HDINN2 | 12 | | C |
| C19 | URC_SQ_VCCRX2 | 12 | | |
| A23 | URC_SQ_HDOUTP2 | 12 | | T |
| C23 | URC_SQ_VCCOB2 | 12 | | |
| B23 | URC_SQ_HDOUTN2 | 12 | | C |
| C22 | URC_SQ_VCCTX2 | 12 | | |
| B22 | URC_SQ_HDOUTN3 | 12 | | C |
| A21 | URC_SQ_VCCOB3 | 12 | | |
| A22 | URC_SQ_HDOUTP3 | 12 | | T |
| C21 | URC_SQ_VCCTX3 | 12 | | |
| B19 | URC_SQ_HDINN3 | 12 | | C |
| B18 | URC_SQ_VCCIB3 | 12 | | |
| A19 | URC_SQ_HDINP3 | 12 | | T |
| C18 | URC_SQ_VCCRX3 | 12 | | |
| D23 | PT100B | 1 | | C |
| GNDIO | GNDIO1 | - | | |
| E21 | PT100A | 1 | | T |
| D26 | PT99B | 1 | | C |
| E26 | PT99A | 1 | | T |
| E23 | PT98B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | |
| G22 | PT98A | 1 | | T |
| - | - | - | | |
| D22 | PT97B | 1 | | C |
| F21 | PT97A | 1 | | T |
| G18 | PT96B | 1 | | C |
| H18 | PT96A | 1 | | T |
| D20 | PT95B | 1 | | C |
| GNDIO | GNDIO1 | - | | |
| D21 | PT95A | 1 | | T |
| E20 | PT94B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | |
| E19 | PT94A | 1 | | T |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| D19 | PT93B | 1 | | C |
| E18 | PT93A | 1 | | T |
| D18 | PT92B | 1 | | C |
| C17 | PT92A | 1 | | T |
| A17 | PT91B | 1 | | C |
| B17 | PT91A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | |
| J18 | PT75B | 1 | | C |
| J19 | PT75A | 1 | | T |
| H17 | PT74B | 1 | | C |
| J17 | PT74A | 1 | | T |
| F18 | PT73B | 1 | | C |
| F17 | PT73A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| A16 | PT72B | 1 | | C |
| B16 | PT72A | 1 | | T |
| G17 | PT71B | 1 | | C |
| G16 | PT71A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| H16 | PT70B | 1 | | C |
| F16 | PT70A | 1 | | T |
| J16 | PT69B | 1 | | C |
| G15 | PT69A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| C16 | PT68B | 1 | | C |
| D16 | PT68A | 1 | | T |
| J15 | PT67B | 1 | | C |
| H15 | PT67A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| A15 | PT66B | 1 | VREF2_1 | C |
| B15 | PT66A | 1 | VREF1_1 | T |
| F15 | PT65B | 1 | PCLKC1_0 | C |
| E16 | PT65A | 1 | PCLKT1_0 | T |
| C15 | PT64B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | |
| D15 | PT64A | 0 | PCLKT0_0 | T |
| C14 | PT63B | 0 | VREF2_0 | C |
| E15 | PT63A | 0 | VREF1_0 | T |
| G14 | PT62B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| J14 | PT62A | 0 | | T |
| F14 | PT61B | 0 | | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| H14 | PT61A | 0 | | T |
| A14 | PT60B | 0 | | C |
| B14 | PT60A | 0 | | T |
| D13 | PT59B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| F13 | PT59A | 0 | | T |
| G13 | PT58B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| J11 | PT58A | 0 | | T |
| D4 | PT57B | 0 | | |
| D5 | PT56A | 0 | | |
| E5 | PT55B | 0 | | C |
| F6 | PT55A | 0 | | T |
| GNDIO | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | |
| F7 | PT52B | 0 | | C |
| D8 | PT52A | 0 | | T |
| GNDIO | GNDIO0 | - | | |
| J13 | PT50B | 0 | | C |
| G11 | PT50A | 0 | | T |
| H13 | PT49B | 0 | | C |
| H12 | PT49A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| E8 | PT48B | 0 | | C |
| D9 | PT48A | 0 | | T |
| D12 | PT46B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| E13 | PT46A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| GNDIO | GNDIO0 | - | | |
| J12 | PT31B | 0 | | C |
| - | - | - | | |
| VCCIO | VCCIO0 | 0 | | |
| H10 | PT31A | 0 | | T |
| E12 | PT30B | 0 | | C |
| D11 | PT30A | 0 | | T |
| H11 | PT29B | 0 | | C |
| F11 | PT29A | 0 | | T |
| C13 | ULC_SQ_VCCRX0 | 11 | | |
| A12 | ULC_SQ_HDINP0 | 11 | | T |
| B13 | ULC_SQ_VCCIB0 | 11 | | |
| B12 | ULC_SQ_HDINN0 | 11 | | C |
| C10 | ULC_SQ_VCCTX0 | 11 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| A9 | ULC_SQ_HDOUTP0 | 11 | | T |
| A10 | ULC_SQ_VCCOB0 | 11 | | |
| B9 | ULC_SQ_HDOUTN0 | 11 | | C |
| C9 | ULC_SQ_VCCTX1 | 11 | | |
| B8 | ULC_SQ_HDOUTN1 | 11 | | C |
| C8 | ULC_SQ_VCCOB1 | 11 | | |
| A8 | ULC_SQ_HDOUTP1 | 11 | | T |
| C12 | ULC_SQ_VCCRX1 | 11 | | |
| B11 | ULC_SQ_HDINN1 | 11 | | C |
| C11 | ULC_SQ_VCCIB1 | 11 | | |
| A11 | ULC_SQ_HDINP1 | 11 | | T |
| B7 | ULC_SQ_VCCAUX33 | 11 | | |
| E7 | ULC_SQ_REFCLKN | 11 | | C |
| D7 | ULC_SQ_REFCLKP | 11 | | T |
| C7 | ULC_SQ_VCCP | 11 | | |
| A3 | ULC_SQ_HDINP2 | 11 | | T |
| C3 | ULC_SQ_VCCIB2 | 11 | | |
| B3 | ULC_SQ_HDINN2 | 11 | | C |
| C2 | ULC_SQ_VCCRX2 | 11 | | |
| A6 | ULC_SQ_HDOUTP2 | 11 | | T |
| C6 | ULC_SQ_VCCOB2 | 11 | | |
| B6 | ULC_SQ_HDOUTN2 | 11 | | C |
| C5 | ULC_SQ_VCCTX2 | 11 | | |
| B5 | ULC_SQ_HDOUTN3 | 11 | | C |
| A4 | ULC_SQ_VCCOB3 | 11 | | |
| A5 | ULC_SQ_HDOUTP3 | 11 | | T |
| C4 | ULC_SQ_VCCTX3 | 11 | | |
| B2 | ULC_SQ_HDINN3 | 11 | | C |
| B1 | ULC_SQ_VCCIB3 | 11 | | |
| A2 | ULC_SQ_HDINP3 | 11 | | T |
| C1 | ULC_SQ_VCCRX3 | 11 | | |
| L12 | VCC | - | | |
| L13 | VCC | - | | |
| L18 | VCC | - | | |
| L19 | VCC | - | | |
| M11 | VCC | - | | |
| M12 | VCC | - | | |
| M13 | VCC | - | | |
| M14 | VCC | - | | |
| M15 | VCC | - | | |
| M16 | VCC | - | | |
| M17 | VCC | - | | |
| M18 | VCC | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| M19 | VCC | - | | |
| M20 | VCC | - | | |
| N11 | VCC | - | | |
| N12 | VCC | - | | |
| N19 | VCC | - | | |
| N20 | VCC | - | | |
| P12 | VCC | - | | |
| P19 | VCC | - | | |
| R12 | VCC | - | | |
| R19 | VCC | - | | |
| T12 | VCC | - | | |
| T19 | VCC | - | | |
| U12 | VCC | - | | |
| U19 | VCC | - | | |
| V11 | VCC | - | | |
| V12 | VCC | - | | |
| V19 | VCC | - | | |
| V20 | VCC | - | | |
| W11 | VCC | - | | |
| W12 | VCC | - | | |
| W13 | VCC | - | | |
| W14 | VCC | - | | |
| W15 | VCC | - | | |
| W16 | VCC | - | | |
| W17 | VCC | - | | |
| W18 | VCC | - | | |
| W19 | VCC | - | | |
| W20 | VCC | - | | |
| Y12 | VCC | - | | |
| Y13 | VCC | - | | |
| Y18 | VCC | - | | |
| Y19 | VCC | - | | |
| D14 | VCCIO0 | 0 | | |
| E6 | VCCIO0 | 0 | | |
| E9 | VCCIO0 | 0 | | |
| F12 | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | |
| K13 | VCCIO0 | 0 | | |
| D17 | VCCIO1 | 1 | | |
| E22 | VCCIO1 | 1 | | |
| E25 | VCCIO1 | 1 | | |
| F19 | VCCIO1 | 1 | | |
| K18 | VCCIO1 | 1 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| K19 | VCCIO1 | 1 | | |
| F28 | VCCIO2 | 2 | | |
| J25 | VCCIO2 | 2 | | |
| K28 | VCCIO2 | 2 | | |
| M21 | VCCIO2 | 2 | | |
| M24 | VCCIO2 | 2 | | |
| N21 | VCCIO2 | 2 | | |
| N28 | VCCIO2 | 2 | | |
| P21 | VCCIO2 | 2 | | |
| R25 | VCCIO2 | 2 | | |
| AA28 | VCCIO3 | 3 | | |
| AB25 | VCCIO3 | 3 | | |
| AE28 | VCCIO3 | 3 | | |
| T25 | VCCIO3 | 3 | | |
| U21 | VCCIO3 | 3 | | |
| V21 | VCCIO3 | 3 | | |
| V28 | VCCIO3 | 3 | | |
| W21 | VCCIO3 | 3 | | |
| W24 | VCCIO3 | 3 | | |
| AA18 | VCCIO4 | 4 | | |
| AA19 | VCCIO4 | 4 | | |
| AE19 | VCCIO4 | 4 | | |
| AF22 | VCCIO4 | 4 | | |
| AG17 | VCCIO4 | 4 | | |
| AG25 | VCCIO4 | 4 | | |
| AA12 | VCCIO5 | 5 | | |
| AA13 | VCCIO5 | 5 | | |
| AE12 | VCCIO5 | 5 | | |
| AF9 | VCCIO5 | 5 | | |
| AG14 | VCCIO5 | 5 | | |
| AG6 | VCCIO5 | 5 | | |
| AA3 | VCCIO6 | 6 | | |
| AB6 | VCCIO6 | 6 | | |
| AE3 | VCCIO6 | 6 | | |
| T6 | VCCIO6 | 6 | | |
| U10 | VCCIO6 | 6 | | |
| V10 | VCCIO6 | 6 | | |
| V3 | VCCIO6 | 6 | | |
| W10 | VCCIO6 | 6 | | |
| W7 | VCCIO6 | 6 | | |
| F3 | VCCIO7 | 7 | | |
| J6 | VCCIO7 | 7 | | |
| K3 | VCCIO7 | 7 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| M10 | VCCIO7 | 7 | | |
| M7 | VCCIO7 | 7 | | |
| N10 | VCCIO7 | 7 | | |
| N3 | VCCIO7 | 7 | | |
| P10 | VCCIO7 | 7 | | |
| R6 | VCCIO7 | 7 | | |
| AA25 | VCCIO8 | 8 | | |
| AD28 | VCCIO8 | 8 | | |
| AA10 | VCCAUX | - | | |
| AA11 | VCCAUX | - | | |
| AA20 | VCCAUX | - | | |
| AA21 | VCCAUX | - | | |
| K10 | VCCAUX | - | | |
| K11 | VCCAUX | - | | |
| K20 | VCCAUX | - | | |
| K21 | VCCAUX | - | | |
| L10 | VCCAUX | - | | |
| L11 | VCCAUX | - | | |
| L20 | VCCAUX | - | | |
| L21 | VCCAUX | - | | |
| Y10 | VCCAUX | - | | |
| Y11 | VCCAUX | - | | |
| Y20 | VCCAUX | - | | |
| Y21 | VCCAUX | - | | |
| A1 | GND | - | | |
| A13 | GND | - | | |
| A18 | GND | - | | |
| A24 | GND | - | | |
| A30 | GND | - | | |
| A7 | GND | - | | |
| AA14 | GND | - | | |
| AA15 | GND | - | | |
| AA16 | GND | - | | |
| AA17 | GND | - | | |
| AA24 | GND | - | | |
| AA27 | GND | - | | |
| AA4 | GND | - | | |
| AB24 | GND | - | | |
| AB7 | GND | - | | |
| AD12 | GND | - | | |
| AD19 | GND | - | | |
| AD27 | GND | - | | |
| AE22 | GND | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AE27 | GND | - | | |
| AE4 | GND | - | | |
| AE9 | GND | - | | |
| AF14 | GND | - | | |
| AF17 | GND | - | | |
| AF25 | GND | - | | |
| AF6 | GND | - | | |
| AJ10 | GND | - | | |
| AJ21 | GND | - | | |
| AJ27 | GND | - | | |
| AJ4 | GND | - | | |
| AK1 | GND | - | | |
| AK13 | GND | - | | |
| AK18 | GND | - | | |
| AK24 | GND | - | | |
| AK30 | GND | - | | |
| AK7 | GND | - | | |
| B10 | GND | - | | |
| B21 | GND | - | | |
| B27 | GND | - | | |
| B4 | GND | - | | |
| D25 | GND | - | | |
| D6 | GND | - | | |
| E14 | GND | - | | |
| E17 | GND | - | | |
| F22 | GND | - | | |
| F27 | GND | - | | |
| F4 | GND | - | | |
| F9 | GND | - | | |
| G12 | GND | - | | |
| G19 | GND | - | | |
| J24 | GND | - | | |
| J7 | GND | - | | |
| K14 | GND | - | | |
| K15 | GND | - | | |
| K16 | GND | - | | |
| K17 | GND | - | | |
| K27 | GND | - | | |
| K4 | GND | - | | |
| L14 | GND | - | | |
| L15 | GND | - | | |
| L16 | GND | - | | |
| L17 | GND | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| M23 | GND | - | | |
| M8 | GND | - | | |
| N14 | GND | - | | |
| N15 | GND | - | | |
| N16 | GND | - | | |
| N17 | GND | - | | |
| N27 | GND | - | | |
| N4 | GND | - | | |
| P11 | GND | - | | |
| P13 | GND | - | | |
| P14 | GND | - | | |
| P15 | GND | - | | |
| P16 | GND | - | | |
| P17 | GND | - | | |
| P18 | GND | - | | |
| P20 | GND | - | | |
| R10 | GND | - | | |
| R11 | GND | - | | |
| R13 | GND | - | | |
| R14 | GND | - | | |
| R15 | GND | - | | |
| R16 | GND | - | | |
| R17 | GND | - | | |
| R18 | GND | - | | |
| R20 | GND | - | | |
| R21 | GND | - | | |
| R24 | GND | - | | |
| R7 | GND | - | | |
| T10 | GND | - | | |
| T11 | GND | - | | |
| T13 | GND | - | | |
| T14 | GND | - | | |
| T15 | GND | - | | |
| T16 | GND | - | | |
| T17 | GND | - | | |
| T18 | GND | - | | |
| T20 | GND | - | | |
| T21 | GND | - | | |
| T24 | GND | - | | |
| T7 | GND | - | | |
| U11 | GND | - | | |
| U13 | GND | - | | |
| U14 | GND | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| U15 | GND | - | | |
| U16 | GND | - | | |
| U17 | GND | - | | |
| U18 | GND | - | | |
| U20 | GND | - | | |
| V14 | GND | - | | |
| V15 | GND | - | | |
| V16 | GND | - | | |
| V17 | GND | - | | |
| V27 | GND | - | | |
| V4 | GND | - | | |
| W23 | GND | - | | |
| W8 | GND | - | | |
| Y14 | GND | - | | |
| Y15 | GND | - | | |
| Y16 | GND | - | | |
| Y17 | GND | - | | |
| AA26 | NC | - | | |
| AB10 | NC | - | | |
| AB11 | NC | - | | |
| AB12 | NC | - | | |
| AB13 | NC | - | | |
| AB14 | NC | - | | |
| AB15 | NC | - | | |
| AB16 | NC | - | | |
| AB17 | NC | - | | |
| AB19 | NC | - | | |
| AB20 | NC | - | | |
| AB21 | NC | - | | |
| AB9 | NC | - | | |
| AC10 | NC | - | | |
| AC11 | NC | - | | |
| AC21 | NC | - | | |
| AC22 | NC | - | | |
| AC8 | NC | - | | |
| AC9 | NC | - | | |
| AD21 | NC | - | | |
| AD22 | NC | - | | |
| AD4 | NC | - | | |
| AD5 | NC | - | | |
| AD6 | NC | - | | |
| AD7 | NC | - | | |
| AD8 | NC | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AE23 | NC | - | | |
| AE5 | NC | - | | |
| AE6 | NC | - | | |
| AE7 | NC | - | | |
| AF20 | NC | - | | |
| AF23 | NC | - | | |
| AF5 | NC | - | | |
| AG23 | NC | - | | |
| AG26 | NC | - | | |
| D10 | NC | - | | |
| E10 | NC | - | | |
| E11 | NC | - | | |
| F10 | NC | - | | |
| F20 | NC | - | | |
| F23 | NC | - | | |
| F8 | NC | - | | |
| G10 | NC | - | | |
| G20 | NC | - | | |
| G21 | NC | - | | |
| G7 | NC | - | | |
| G8 | NC | - | | |
| G9 | NC | - | | |
| H19 | NC | - | | |
| H20 | NC | - | | |
| H21 | NC | - | | |
| H22 | NC | - | | |
| H6 | NC | - | | |
| H8 | NC | - | | |
| H9 | NC | - | | |
| J10 | NC | - | | |
| J20 | NC | - | | |
| J21 | NC | - | | |
| J9 | NC | - | | |
| K9 | NC | - | | |
| R9 | NC | - | | |
| U22 | NC | - | | |
| W9 | NC | - | | |
| N13 | VCCPLL | - | | |
| N18 | VCCPLL | - | | |
| V13 | VCCPLL | - | | |

# LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| V18 | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** These sysCONFIG pins are dedicated I/O pins for configuration. The outpus are actively driven during normal device operation.
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F4 | PL9A | 7 | VREF2_7 | T | PL9A | 7 | VREF2_7 | T |
| F3 | PL9B | 7 | VREF1_7 | C | PL9B | 7 | VREF1_7 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| E1 | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* |
| E2 | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* |
| K9 | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T |
| H7 | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F1 | PL13A | 7 | LDQ15 | T (LVDS)* | PL13A | 7 | LDQ15 | T (LVDS)* |
| F2 | PL13B | 7 | LDQ15 | C (LVDS)* | PL13B | 7 | LDQ15 | C (LVDS)* |
| J8 | PL14A | 7 | LDQ15 | T | PL14A | 7 | LDQ15 | T |
| H6 | PL14B | 7 | LDQ15 | C | PL14B | 7 | LDQ15 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| G2 | PL15A | 7 | LDQS15 | T (LVDS)* | PL15A | 7 | LDQS15 | T (LVDS)* |
| G1 | PL15B | 7 | LDQ15 | C (LVDS)* | PL15B | 7 | LDQ15 | C (LVDS)* |
| J7 | PL16A | 7 | LDQ15 | T | PL16A | 7 | LDQ15 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L8 | PL16B | 7 | LDQ15 | C | PL16B | 7 | LDQ15 | C |
| L9 | PL17A | 7 | LDQ15 | T (LVDS)* | PL17A | 7 | LDQ15 | T (LVDS)* |
| L10 | PL17B | 7 | LDQ15 | C (LVDS)* | PL17B | 7 | LDQ15 | C (LVDS)* |
| H5 | PL18A | 7 | LDQ15 | T | PL18A | 7 | LDQ15 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| J6 | PL18B | 7 | LDQ15 | C | PL18B | 7 | LDQ15 | C |
| H2 | NC | - | | | PL19A | 7 | LDQ23 | T (LVDS)* |
| H1 | NC | - | | | PL19B | 7 | LDQ23 | C (LVDS)* |
| G5 | NC | - | | | PL20A | 7 | LDQ23 | T |
| G6 | NC | - | | | PL20B | 7 | LDQ23 | C |
| M9 | NC | - | | | PL21A | 7 | LDQ23 | T (LVDS)* |
| - | - | - | | | VCCIO7 | 7 | | |
| M10 | NC | - | | | PL21B | 7 | LDQ23 | C (LVDS)* |
| H3 | NC | - | | | PL22A | 7 | LDQ23 | T |
| H4 | NC | - | | | PL22B | 7 | LDQ23 | C |
| J2 | PL19A | 7 | | T (LVDS)* | PL23A | 7 | LDQS23 | T (LVDS)* |
| - | - | - | | | GNDIO7 | - | | |
| J1 | PL19B | 7 | | C (LVDS)* | PL23B | 7 | LDQ23 | C (LVDS)* |
| K2 | PL20A | 7 | | T | PL24A | 7 | LDQ23 | T |
| K1 | PL20B | 7 | | C | PL24B | 7 | LDQ23 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J4 | PL21A | 7 | | T (LVDS)* | PL25A | 7 | LDQ23 | T (LVDS)* |
| J3 | PL21B | 7 | | C (LVDS)* | PL25B | 7 | LDQ23 | C (LVDS)* |
| J5 | PL22A | 7 | | T | PL26A | 7 | LDQ23 | T |
| K5 | PL22B | 7 | | C | PL26B | 7 | LDQ23 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| L2 | PL24A | 7 | LDQ28 | T (LVDS)* | PL28A | 7 | LDQ32 | T (LVDS)* |
| L1 | PL24B | 7 | LDQ28 | C (LVDS)* | PL28B | 7 | LDQ32 | C (LVDS)* |
| L7 | PL25A | 7 | LDQ28 | T | PL29A | 7 | LDQ32 | T |
| K6 | PL25B | 7 | LDQ28 | C | PL29B | 7 | LDQ32 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M2 | PL26A | 7 | LDQ28 | T (LVDS)* | PL30A | 7 | LDQ32 | T (LVDS)* |
| M1 | PL26B | 7 | LDQ28 | C (LVDS)* | PL30B | 7 | LDQ32 | C (LVDS)* |
| L6 | PL27A | 7 | LDQ28 | T | PL31A | 7 | LDQ32 | T |
| L5 | PL27B | 7 | LDQ28 | C | PL31B | 7 | LDQ32 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| L3 | PL28A | 7 | LDQS28 | T (LVDS)* | PL32A | 7 | LDQS32 | T (LVDS)* |
| L4 | PL28B | 7 | LDQ28 | C (LVDS)* | PL32B | 7 | LDQ32 | C (LVDS)* |
| M3 | PL29A | 7 | LDQ28 | T | PL33A | 7 | LDQ32 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M4 | PL29B | 7 | LDQ28 | C | PL33B | 7 | LDQ32 | C |
| N1 | PL30A | 7 | LDQ28 | T (LVDS)* | PL34A | 7 | LDQ32 | T (LVDS)* |
| N2 | PL30B | 7 | LDQ28 | C (LVDS)* | PL34B | 7 | LDQ32 | C (LVDS)* |
| M5 | PL31A | 7 | LDQ28 | T | PL35A | 7 | LDQ32 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| N6 | PL31B | 7 | LDQ28 | C | PL35B | 7 | LDQ32 | C |
| P3 | NC | - | | | PL37A | 7 | | T (LVDS)* |
| - | - | - | | | GNDIO7 | - | | |
| P4 | NC | - | | | PL37B | 7 | | C (LVDS)* |
| P9 | NC | - | | | PL38A | 7 | | T |
| M7 | NC | - | | | PL38B | 7 | | C |
| - | - | - | | | VCCIO7 | 7 | | |
| P1 | NC | - | | | PL39A | 7 | | T (LVDS)* |
| P2 | NC | - | | | PL39B | 7 | | C (LVDS)* |
| N7 | NC | - | | | PL40A | 7 | | T |
| P7 | NC | - | | | PL40B | 7 | | C |
| - | - | - | | | GNDIO7 | - | | |
| P5 | PL33A | 7 | LDQ37 | T (LVDS)* | PL41A | 7 | LDQ45 | T (LVDS)* |
| N5 | PL33B | 7 | LDQ37 | C (LVDS)* | PL41B | 7 | LDQ45 | C (LVDS)* |
| P8 | PL34A | 7 | LDQ37 | T | PL42A | 7 | LDQ45 | T |
| P6 | PL34B | 7 | LDQ37 | C | PL42B | 7 | LDQ45 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| R3 | PL35A | 7 | LDQ37 | T (LVDS)* | PL43A | 7 | LDQ45 | T (LVDS)* |
| R4 | PL35B | 7 | LDQ37 | C (LVDS)* | PL43B | 7 | LDQ45 | C (LVDS)* |
| R10 | PL36A | 7 | LDQ37 | T | PL44A | 7 | LDQ45 | T |
| P11 | PL36B | 7 | LDQ37 | C | PL44B | 7 | LDQ45 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| R7 | PL37A | 7 | LDQS37 | T (LVDS)* | PL45A | 7 | LDQS45 | T (LVDS)* |
| R8 | PL37B | 7 | LDQ37 | C (LVDS)* | PL45B | 7 | LDQ45 | C (LVDS)* |
| R5 | PL38A | 7 | LDQ37 | T | PL46A | 7 | LDQ45 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T5 | PL38B | 7 | LDQ37 | C | PL46B | 7 | LDQ45 | C |
| R1 | PL39A | 7 | LDQ37 | T (LVDS)* | PL47A | 7 | LDQ45 | T (LVDS)* |
| R2 | PL39B | 7 | LDQ37 | C (LVDS)* | PL47B | 7 | LDQ45 | C (LVDS)* |
| R11 | PL40A | 7 | LDQ37 | T | PL48A | 7 | LDQ45 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| T10 | PL40B | 7 | LDQ37 | C | PL48B | 7 | LDQ45 | C |
| T1 | PL42A | 7 | LUM3_SPLLT_IN_A/LDQ46 | T (LVDS)* | PL50A | 7 | LUM3_SPLLT_IN_A/LDQ54 | T (LVDS)* |
| T2 | PL42B | 7 | LUM3_SPLLC_IN_A/LDQ46 | C (LVDS)* | PL50B | 7 | LUM3_SPLLC_IN_A/LDQ54 | C (LVDS)* |
| U10 | PL43A | 7 | LUM3_SPLLT_FB_A/LDQ46 | T | PL51A | 7 | LUM3_SPLLT_FB_A/LDQ54 | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U8 | PL43B | 7 | LUM3_SPLLC_FB_A/LDQ46 | C | PL51B | 7 | LUM3_SPLLC_FB_A/LDQ54 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T6 | PL44A | 7 | LDQ46 | T (LVDS)* | PL52A | 7 | LDQ54 | T (LVDS)* |
| R6 | PL44B | 7 | LDQ46 | C (LVDS)* | PL52B | 7 | LDQ54 | C (LVDS)* |
| U9 | PL45A | 7 | LDQ46 | T | PL53A | 7 | LDQ54 | T |
| T7 | PL45B | 7 | LDQ46 | C | PL53B | 7 | LDQ54 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| U5 | PL46A | 7 | LDQS46 | T (LVDS)* | PL54A | 7 | LDQS54 | T (LVDS)* |
| U6 | PL46B | 7 | LDQ46 | C (LVDS)* | PL54B | 7 | LDQ54 | C (LVDS)* |
| U7 | PL47A | 7 | LDQ46 | T | PL55A | 7 | LDQ54 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| V9 | PL47B | 7 | LDQ46 | C | PL55B | 7 | LDQ54 | C |
| V11 | PL48A | 7 | LDQ46 | T (LVDS)* | PL56A | 7 | LDQ54 | T (LVDS)* |
| V10 | PL48B | 7 | LDQ46 | C (LVDS)* | PL56B | 7 | LDQ54 | C (LVDS)* |
| U4 | PL49A | 7 | PCLKT7_0/LDQ46 | T | PL57A | 7 | PCLKT7_0/LDQ54 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| U3 | PL49B | 7 | PCLKC7_0/LDQ46 | C | PL57B | 7 | PCLKC7_0/LDQ54 | C |
| U2 | PL51A | 6 | PCLKT6_0/LDQ55 | T (LVDS)* | PL59A | 6 | PCLKT6_0/LDQ63 | T (LVDS)* |
| U1 | PL51B | 6 | PCLKC6_0/LDQ55 | C (LVDS)* | PL59B | 6 | PCLKC6_0/LDQ63 | C (LVDS)* |
| V5 | PL52A | 6 | VREF2_6/LDQ55 | T | PL60A | 6 | VREF2_6/LDQ63 | T |
| V6 | PL52B | 6 | VREF1_6/LDQ55 | C | PL60B | 6 | VREF1_6/LDQ63 | C |
| V7 | PL53A | 6 | LDQ55 | T (LVDS)* | PL61A | 6 | LDQ63 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V8 | PL53B | 6 | LDQ55 | C (LVDS)* | PL61B | 6 | LDQ63 | C (LVDS)* |
| V4 | PL54A | 6 | LDQ55 | T | PL62A | 6 | LDQ63 | T |
| V3 | PL54B | 6 | LDQ55 | C | PL62B | 6 | LDQ63 | C |
| V2 | PL55A | 6 | LDQS55 | T (LVDS)* | PL63A | 6 | LDQS63 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| V1 | PL55B | 6 | LDQ55 | C (LVDS)* | PL63B | 6 | LDQ63 | C (LVDS)* |
| W7 | PL56A | 6 | LDQ55 | T | PL64A | 6 | LDQ63 | T |
| W5 | PL56B | 6 | LDQ55 | C | PL64B | 6 | LDQ63 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W2 | PL57A | 6 | LLM3_SPLLT_IN_A/LDQ55 | T (LVDS)* | PL65A | 6 | LLM4_SPLLT_IN_A/LDQ63 | T (LVDS)* |
| W1 | PL57B | 6 | LLM3_SPLLC_IN_A/LDQ55 | C (LVDS)* | PL65B | 6 | LLM4_SPLLC_IN_A/LDQ63 | C (LVDS)* |
| Y6 | PL58A | 6 | LLM3_SPLLT_FB_A/LDQ55 | T | PL66A | 6 | LLM4_SPLLT_FB_A/LDQ63 | T |
| W6 | PL58B | 6 | LLM3_SPLLC_FB_A/LDQ55 | C | PL66B | 6 | LLM4_SPLLC_FB_A/LDQ63 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| Y1 | PL60A | 6 | LDQ64 | T (LVDS)* | PL68A | 6 | LDQ72 | T (LVDS)* |
| Y2 | PL60B | 6 | LDQ64 | C (LVDS)* | PL68B | 6 | LDQ72 | C (LVDS)* |
| Y7 | PL61A | 6 | LDQ64 | T | PL69A | 6 | LDQ72 | T |
| Y5 | PL61B | 6 | LDQ64 | C | PL69B | 6 | LDQ72 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W10 | PL62A | 6 | LDQ64 | T (LVDS)* | PL70A | 6 | LDQ72 | T (LVDS)* |
| Y8 | PL62B | 6 | LDQ64 | C (LVDS)* | PL70B | 6 | LDQ72 | C (LVDS)* |
| Y4 | PL63A | 6 | LDQ64 | T | PL71A | 6 | LDQ72 | T |
| Y3 | PL63B | 6 | LDQ64 | C | PL71B | 6 | LDQ72 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA1 | PL64A | 6 | LDQS64 | T (LVDS)* | PL72A | 6 | LDQS72 | T (LVDS)* |
| AA2 | PL64B | 6 | LDQ64 | C (LVDS)* | PL72B | 6 | LDQ72 | C (LVDS)* |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA8 | PL65A | 6 | LDQ64 | T | PL73A | 6 | LDQ72 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y9 | PL65B | 6 | LDQ64 | C | PL73B | 6 | LDQ72 | C |
| AA6 | PL66A | 6 | LDQ64 | T (LVDS)* | PL74A | 6 | LDQ72 | T (LVDS)* |
| AA7 | PL66B | 6 | LDQ64 | C (LVDS)* | PL74B | 6 | LDQ72 | C (LVDS)* |
| AA4 | PL67A | 6 | LDQ64 | T | PL75A | 6 | LDQ72 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA3 | PL67B | 6 | LDQ64 | C | PL75B | 6 | LDQ72 | C |
| AA9 | PL69A | 6 | LDQ73 | T (LVDS)* | PL77A | 6 | LDQ81 | T (LVDS)* |
| AA10 | PL69B | 6 | LDQ73 | C (LVDS)* | PL77B | 6 | LDQ81 | C (LVDS)* |
| AA5 | PL70A | 6 | LDQ73 | T | PL78A | 6 | LDQ81 | T |
| AB6 | PL70B | 6 | LDQ73 | C | PL78B | 6 | LDQ81 | C |
| AB1 | PL71A | 6 | LDQ73 | T (LVDS)* | PL79A | 6 | LDQ81 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AB2 | PL71B | 6 | LDQ73 | C (LVDS)* | PL79B | 6 | LDQ81 | C (LVDS)* |
| AC8 | PL72A | 6 | LDQ73 | T | PL80A | 6 | LDQ81 | T |
| AB10 | PL72B | 6 | LDQ73 | C | PL80B | 6 | LDQ81 | C |
| AC1 | PL73A | 6 | LDQS73 | T (LVDS)* | PL81A | 6 | LDQS81 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AC2 | PL73B | 6 | LDQ73 | C (LVDS)* | PL81B | 6 | LDQ81 | C (LVDS)* |
| AB7 | PL74A | 6 | LDQ73 | T | PL82A | 6 | LDQ81 | T |
| AB5 | PL74B | 6 | LDQ73 | C | PL82B | 6 | LDQ81 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AC3 | PL75A | 6 | LDQ73 | T (LVDS)* | PL83A | 6 | LDQ81 | T (LVDS)* |
| AC4 | PL75B | 6 | LDQ73 | C (LVDS)* | PL83B | 6 | LDQ81 | C (LVDS)* |
| AC10 | PL76A | 6 | LDQ73 | T | PL84A | 6 | LDQ81 | T |
| AC9 | PL76B | 6 | LDQ73 | C | PL84B | 6 | LDQ81 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AC7 | NC | - | | | PL86A | 6 | LDQ90 | T (LVDS)* |
| AC5 | NC | - | | | PL86B | 6 | LDQ90 | C (LVDS)* |
| AC6 | NC | - | | | PL87A | 6 | LDQ90 | T |
| AD5 | NC | - | | | PL87B | 6 | LDQ90 | C |
| - | - | - | | | VCCIO6 | 6 | | |
| AD4 | NC | - | | | PL88A | 6 | LDQ90 | T (LVDS)* |
| AD3 | NC | - | | | PL88B | 6 | LDQ90 | C (LVDS)* |
| AD10 | NC | - | | | PL89A | 6 | LDQ90 | T |
| AD8 | NC | - | | | PL89B | 6 | LDQ90 | C |
| - | - | - | | | GNDIO6 | - | | |
| AD2 | NC | - | | | PL90A | 6 | LDQS90 | T (LVDS)* |
| AD1 | NC | - | | | PL90B | 6 | LDQ90 | C (LVDS)* |
| AD9 | NC | - | | | PL91A | 6 | LDQ90 | T |
| - | - | - | | | VCCIO6 | 6 | | |
| AC11 | NC | - | | | PL91B | 6 | LDQ90 | C |
| AD6 | NC | - | | | PL92A | 6 | LDQ90 | T (LVDS)* |
| AD7 | NC | - | | | PL92B | 6 | LDQ90 | C (LVDS)* |
| AE1 | NC | - | | | PL93A | 6 | LDQ90 | T |
| - | - | - | | | GNDIO6 | - | | |
| AE2 | NC | - | | | PL93B | 6 | LDQ90 | C |
| AF2 | PL78A | 6 | LDQ82 | T (LVDS)* | PL95A | 6 | LDQ99 | T (LVDS)* |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AF1 | PL78B | 6 | LDQ82 | C (LVDS)* | PL95B | 6 | LDQ99 | C (LVDS)* |
| AE5 | PL79A | 6 | LDQ82 | T | PL96A | 6 | LDQ99 | T |
| AE6 | PL79B | 6 | LDQ82 | C | PL96B | 6 | LDQ99 | C |
| AF4 | PL80A | 6 | LDQ82 | T (LVDS)* | PL97A | 6 | LDQ99 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AF3 | PL80B | 6 | LDQ82 | C (LVDS)* | PL97B | 6 | LDQ99 | C (LVDS)* |
| AF5 | PL81A | 6 | LDQ82 | T | PL98A | 6 | LDQ99 | T |
| AF6 | PL81B | 6 | LDQ82 | C | PL98B | 6 | LDQ99 | C |
| AG1 | PL82A | 6 | LLM0_GPLLT_IN_A**/LDQS82 | T (LVDS)* | PL99A | 6 | LLM0_GPLLT_IN_A**/ LDQS99 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AG2 | PL82B | 6 | LLM0_GPLLC_IN_A**/LDQ82 | C (LVDS)* | PL99B | 6 | LLM0_GPLLC_IN_A**/LDQ99 | C (LVDS)* |
| AE9 | PL83A | 6 | LLM0_GPLLT_FB_A/LDQ82 | T | PL100A | 6 | LLM0_GPLLT_FB_A/LDQ99 | T |
| AF7 | PL83B | 6 | LLM0_GPLLC_FB_A/LDQ82 | C | PL100B | 6 | LLM0_GPLLC_FB_A/LDQ99 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AH1 | PL84A | 6 | LLM0_GDLLT_IN_A**/LDQ82 | T (LVDS)* | PL101A | 6 | LLM0_GDLLT_IN_A**/LDQ99 | T (LVDS)* |
| AH2 | PL84B | 6 | LLM0_GDLLC_IN_A**/LDQ82 | C (LVDS)* | PL101B | 6 | LLM0_GDLLC_IN_A**/ LDQ99 | C (LVDS)* |
| AG5 | PL85A | 6 | LLM0_GDLLT_FB_A/LDQ82 | T | PL102A | 6 | LLM0_GDLLT_FB_A/LDQ99 | T |
| AG4 | PL85B | 6 | LLM0_GDLLC_FB_A/LDQ82 | C | PL102B | 6 | LLM0_GDLLC_FB_A/LDQ99 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AG6 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| AJ1 | PL87A | 6 | | T | PL104A | 6 | | T |
| AJ2 | PL87B | 6 | | C | PL104B | 6 | | C |
| AK2 | TCK | - | | | TCK | - | | |
| AK1 | TDI | - | | | TDI | - | | |
| AL1 | TMS | - | | | TMS | - | | |
| AF10 | TDO | - | | | TDO | - | | |
| AK3 | VCCJ | - | | | VCCJ | - | | |
| AN2 | LLC_SQ_VCCRX3 | 14 | | | LLC_SQ_VCCRX3 | 14 | | |
| AM2 | LLC_SQ_HDINP3 | 14 | | T | LLC_SQ_HDINP3 | 14 | | T |
| AN1 | LLC_SQ_VCCIB3 | 14 | | | LLC_SQ_VCCIB3 | 14 | | |
| AM3 | LLC_SQ_HDINN3 | 14 | | C | LLC_SQ_HDINN3 | 14 | | C |
| AN3 | LLC_SQ_VCCTX3 | 14 | | | LLC_SQ_VCCTX3 | 14 | | |
| AP2 | LLC_SQ_HDOUTP3 | 14 | | T | LLC_SQ_HDOUTP3 | 14 | | T |
| AM1 | LLC_SQ_VCCOB3 | 14 | | | LLC_SQ_VCCOB3 | 14 | | |
| AP3 | LLC_SQ_HDOUTN3 | 14 | | C | LLC_SQ_HDOUTN3 | 14 | | C |
| AN4 | LLC_SQ_VCCTX2 | 14 | | | LLC_SQ_VCCTX2 | 14 | | |
| AP4 | LLC_SQ_HDOUTN2 | 14 | | C | LLC_SQ_HDOUTN2 | 14 | | C |
| AL3 | LLC_SQ_VCCOB2 | 14 | | | LLC_SQ_VCCOB2 | 14 | | |
| AP5 | LLC_SQ_HDOUTP2 | 14 | | T | LLC_SQ_HDOUTP2 | 14 | | T |
| AN5 | LLC_SQ_VCCRX2 | 14 | | | LLC_SQ_VCCRX2 | 14 | | |
| AM4 | LLC_SQ_HDINN2 | 14 | | C | LLC_SQ_HDINN2 | 14 | | C |
| AL4 | LLC_SQ_VCCIB2 | 14 | | | LLC_SQ_VCCIB2 | 14 | | |
| AM5 | LLC_SQ_HDINP2 | 14 | | T | LLC_SQ_HDINP2 | 14 | | T |
| AL6 | LLC_SQ_VCCP | 14 | | | LLC_SQ_VCCP | 14 | | |
| AL5 | LLC_SQ_REFCLKP | 14 | | T | LLC_SQ_REFCLKP | 14 | | T |
| AK5 | LLC_SQ_REFCLKN | 14 | | C | LLC_SQ_REFCLKN | 14 | | C |
| AK6 | LLC_SQ_VCCAUX33 | 14 | | | LLC_SQ_VCCAUX33 | 14 | | |
| AM6 | LLC_SQ_HDINP1 | 14 | | T | LLC_SQ_HDINP1 | 14 | | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AL8 | LLC_SQ_VCCIB1 | 14 | | | LLC_SQ_VCCIB1 | 14 | | |
| AM7 | LLC_SQ_HDINN1 | 14 | | C | LLC_SQ_HDINN1 | 14 | | C |
| AN6 | LLC_SQ_VCCRX1 | 14 | | | LLC_SQ_VCCRX1 | 14 | | |
| AP6 | LLC_SQ_HDOUTP1 | 14 | | T | LLC_SQ_HDOUTP1 | 14 | | T |
| AK7 | LLC_SQ_VCCOB1 | 14 | | | LLC_SQ_VCCOB1 | 14 | | |
| AP7 | LLC_SQ_HDOUTN1 | 14 | | C | LLC_SQ_HDOUTN1 | 14 | | C |
| AN7 | LLC_SQ_VCCTX1 | 14 | | | LLC_SQ_VCCTX1 | 14 | | |
| AP8 | LLC_SQ_HDOUTN0 | 14 | | C | LLC_SQ_HDOUTN0 | 14 | | C |
| AL9 | LLC_SQ_VCCOB0 | 14 | | | LLC_SQ_VCCOB0 | 14 | | |
| AP9 | LLC_SQ_HDOUTP0 | 14 | | T | LLC_SQ_HDOUTP0 | 14 | | T |
| AN8 | LLC_SQ_VCCTX0 | 14 | | | LLC_SQ_VCCTX0 | 14 | | |
| AM8 | LLC_SQ_HDINN0 | 14 | | C | LLC_SQ_HDINN0 | 14 | | C |
| AN9 | LLC_SQ_VCCIB0 | 14 | | | LLC_SQ_VCCIB0 | 14 | | |
| AM9 | LLC_SQ_HDINP0 | 14 | | T | LLC_SQ_HDINP0 | 14 | | T |
| AL7 | LLC_SQ_VCCRX0 | 14 | | | LLC_SQ_VCCRX0 | 14 | | |
| - | - | - | | | VCCIO5 | 5 | | |
| AJ12 | NC | - | | | PB32A | 5 | BDQ33 | T |
| AH12 | NC | - | | | PB32B | 5 | BDQ33 | C |
| - | - | - | | | GNDIO5 | - | | |
| - | - | - | | | VCCIO5 | 5 | | |
| AL13 | NC | - | | | PB36A | 5 | BDQ33 | T |
| AK13 | NC | - | | | PB36B | 5 | BDQ33 | C |
| - | - | - | | | GNDIO5 | - | | |
| AE14 | NC | - | | | PB38A | 5 | BDQ42 | T |
| AG13 | NC | - | | | PB38B | 5 | BDQ42 | C |
| AN14 | PB30A | 5 | BDQ33 | T | PB39A | 5 | BDQ42 | T |
| AP14 | PB30B | 5 | BDQ33 | C | PB39B | 5 | BDQ42 | C |
| AH14 | PB31A | 5 | BDQ33 | T | PB40A | 5 | BDQ42 | T |
| AJ15 | PB31B | 5 | BDQ33 | C | PB40B | 5 | BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AL14 | PB33A | 5 | BDQS33 | T | PB42A | 5 | BDQS42 | T |
| AM14 | PB33B | 5 | BDQ33 | C | PB42B | 5 | BDQ42 | C |
| AF14 | PB35A | 5 | BDQ33 | T | PB44A | 5 | BDQ42 | T |
| AF13 | PB35B | 5 | BDQ33 | C | PB44B | 5 | BDQ42 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE15 | PB36A | 5 | BDQ33 | T | PB45A | 5 | BDQ42 | T |
| AG14 | PB36B | 5 | BDQ33 | C | PB45B | 5 | BDQ42 | C |
| AH15 | PB37A | 5 | BDQ33 | T | PB46A | 5 | BDQ42 | T |
| AK15 | PB37B | 5 | BDQ33 | C | PB46B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AL15 | PB38A | 5 | BDQ42 | T | PB47A | 5 | BDQ51 | T |
| AM15 | PB38B | 5 | BDQ42 | C | PB47B | 5 | BDQ51 | C |
| AK16 | PB39A | 5 | BDQ42 | T | PB48A | 5 | BDQ51 | T |
| AJ16 | PB39B | 5 | BDQ42 | C | PB48B | 5 | BDQ51 | C |
| AN15 | PB40A | 5 | BDQ42 | T | PB49A | 5 | BDQ51 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AP15 | PB40B | 5 | BDQ42 | C | PB49B | 5 | BDQ51 | C |
| AG15 | PB42A | 5 | BDQS42 | T | PB51A | 5 | BDQS51 | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AE16 | PB42B | 5 | BDQ42 | C | PB51B | 5 | BDQ51 | C |
| AF15 | PB44A | 5 | BDQ42 | T | PB53A | 5 | BDQ51 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AD16 | PB44B | 5 | BDQ42 | C | PB53B | 5 | BDQ51 | C |
| AK17 | PB45A | 5 | BDQ42 | T | PB54A | 5 | BDQ51 | T |
| AH16 | PB45B | 5 | BDQ42 | C | PB54B | 5 | BDQ51 | C |
| AN16 | PB46A | 5 | BDQ42 | T | PB55A | 5 | BDQ51 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AP16 | PB46B | 5 | BDQ42 | C | PB55B | 5 | BDQ51 | C |
| AL17 | PB47A | 5 | BDQ51 | T | PB56A | 5 | BDQ60 | T |
| AM17 | PB47B | 5 | BDQ51 | C | PB56B | 5 | BDQ60 | C |
| AN17 | PB48A | 5 | BDQ51 | T | PB57A | 5 | BDQ60 | T |
| AP17 | PB48B | 5 | BDQ51 | C | PB57B | 5 | BDQ60 | C |
| AD17 | PB49A | 5 | BDQ51 | T | PB58A | 5 | BDQ60 | T |
| AE17 | PB49B | 5 | BDQ51 | C | PB58B | 5 | BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AL18 | PB50A | 5 | BDQ51 | T | PB59A | 5 | BDQ60 | T |
| AM18 | PB50B | 5 | BDQ51 | C | PB59B | 5 | BDQ60 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AP18 | PB51A | 5 | BDQS51 | T | PB60A | 5 | BDQS60 | T |
| AN18 | PB51B | 5 | BDQ51 | C | PB60B | 5 | BDQ60 | C |
| AG17 | PB52A | 5 | VREF2_5/BDQ51 | T | PB61A | 5 | VREF2_5/BDQ60 | T |
| AJ17 | PB52B | 5 | VREF1_5/BDQ51 | C | PB61B | 5 | VREF1_5/BDQ60 | C |
| AF17 | PB53A | 5 | PCLKT5_0/BDQ51 | T | PB62A | 5 | PCLKT5_0/BDQ60 | T |
| AH17 | PB53B | 5 | PCLKC5_0/BDQ51 | C | PB62B | 5 | PCLKC5_0/BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AF18 | PB58A | 4 | PCLKT4_0/BDQ60 | T | PB67A | 4 | PCLKT4_0/BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AD18 | PB58B | 4 | PCLKC4_0/BDQ60 | C | PB67B | 4 | PCLKC4_0/BDQ69 | C |
| AP19 | PB59A | 4 | VREF2_4/BDQ60 | T | PB68A | 4 | VREF2_4/BDQ69 | T |
| AN19 | PB59B | 4 | VREF1_4/BDQ60 | C | PB68B | 4 | VREF1_4/BDQ69 | C |
| AP20 | PB60A | 4 | BDQS60 | T | PB69A | 4 | BDQS69 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AM20 | PB60B | 4 | BDQ60 | C | PB69B | 4 | BDQ69 | C |
| AN20 | PB61A | 4 | BDQ60 | T | PB70A | 4 | BDQ69 | T |
| AM21 | PB61B | 4 | BDQ60 | C | PB70B | 4 | BDQ69 | C |
| AG18 | PB62A | 4 | BDQ60 | T | PB71A | 4 | BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AE18 | PB62B | 4 | BDQ60 | C | PB71B | 4 | BDQ69 | C |
| AJ18 | PB63A | 4 | BDQ60 | T | PB72A | 4 | BDQ69 | T |
| AH18 | PB63B | 4 | BDQ60 | C | PB72B | 4 | BDQ69 | C |
| AK18 | PB64A | 4 | BDQ60 | T | PB73A | 4 | BDQ69 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AK19 | PB64B | 4 | BDQ60 | C | PB73B | 4 | BDQ69 | C |
| AP21 | PB65A | 4 | BDQ69 | T | PB74A | 4 | BDQ78 | T |
| AN21 | PB65B | 4 | BDQ69 | C | PB74B | 4 | BDQ78 | C |
| AL20 | PB66A | 4 | BDQ69 | T | PB75A | 4 | BDQ78 | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AK20 | PB66B | 4 | BDQ69 | C | PB75B | 4 | BDQ78 | C |
| AN22 | PB67A | 4 | BDQ69 | T | PB76A | 4 | BDQ78 | T |
| AL21 | PB67B | 4 | BDQ69 | C | PB76B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AH19 | PB69A | 4 | BDQS69 | T | PB78A | 4 | BDQS78 | T |
| AJ20 | PB69B | 4 | BDQ69 | C | PB78B | 4 | BDQ78 | C |
| AD20 | PB71A | 4 | BDQ69 | T | PB80A | 4 | BDQ78 | T |
| AF20 | PB71B | 4 | BDQ69 | C | PB80B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AJ19 | PB72A | 4 | BDQ69 | T | PB81A | 4 | BDQ78 | T |
| AH20 | PB72B | 4 | BDQ69 | C | PB81B | 4 | BDQ78 | C |
| AE20 | PB73A | 4 | BDQ69 | T | PB82A | 4 | BDQ78 | T |
| AG20 | PB73B | 4 | BDQ69 | C | PB82B | 4 | BDQ78 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AH22 | NC | - | | | PB89A | 4 | BDQ87 | T |
| - | - | - | | | VCCIO4 | 4 | | |
| AH21 | NC | - | | | PB89B | 4 | BDQ87 | C |
| AG22 | NC | - | | | PB90A | 4 | BDQ87 | T |
| AG21 | NC | - | | | PB90B | 4 | BDQ87 | C |
| - | - | - | | | GNDIO4 | - | | |
| AM22 | PB74A | 4 | BDQ78 | T | PB92A | 4 | BDQ96 | T |
| AL22 | PB74B | 4 | BDQ78 | C | PB92B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AP23 | PB77A | 4 | BDQ78 | T | PB95A | 4 | BDQ96 | T |
| AN23 | PB77B | 4 | BDQ78 | C | PB95B | 4 | BDQ96 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AM24 | PB78A | 4 | BDQS78 | T | PB96A | 4 | BDQS96 | T |
| AL24 | PB78B | 4 | BDQ78 | C | PB96B | 4 | BDQ96 | C |
| AK22 | PB79A | 4 | BDQ78 | T | PB97A | 4 | BDQ96 | T |
| AJ22 | PB79B | 4 | BDQ78 | C | PB97B | 4 | BDQ96 | C |
| AL23 | PB80A | 4 | BDQ78 | T | PB98A | 4 | BDQ96 | T |
| AK23 | PB80B | 4 | BDQ78 | C | PB98B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AJ23 | PB81A | 4 | BDQ78 | T | PB99A | 4 | BDQ96 | T |
| AH23 | PB81B | 4 | BDQ78 | C | PB99B | 4 | BDQ96 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AL28 | LRC_SQ_VCCRX3 | 13 | | | LRC_SQ_VCCRX3 | 13 | | |
| AM26 | LRC_SQ_HDINP3 | 13 | | T | LRC_SQ_HDINP3 | 13 | | T |
| AN26 | LRC_SQ_VCCIB3 | 13 | | | LRC_SQ_VCCIB3 | 13 | | |
| AM27 | LRC_SQ_HDINN3 | 13 | | C | LRC_SQ_HDINN3 | 13 | | C |
| AN27 | LRC_SQ_VCCTX3 | 13 | | | LRC_SQ_VCCTX3 | 13 | | |
| AP26 | LRC_SQ_HDOUTP3 | 13 | | T | LRC_SQ_HDOUTP3 | 13 | | T |
| AL26 | LRC_SQ_VCCOB3 | 13 | | | LRC_SQ_VCCOB3 | 13 | | |
| AP27 | LRC_SQ_HDOUTN3 | 13 | | C | LRC_SQ_HDOUTN3 | 13 | | C |
| AN28 | LRC_SQ_VCCTX2 | 13 | | | LRC_SQ_VCCTX2 | 13 | | |
| AP28 | LRC_SQ_HDOUTN2 | 13 | | C | LRC_SQ_HDOUTN2 | 13 | | C |
| AK28 | LRC_SQ_VCCOB2 | 13 | | | LRC_SQ_VCCOB2 | 13 | | |
| AP29 | LRC_SQ_HDOUTP2 | 13 | | T | LRC_SQ_HDOUTP2 | 13 | | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AN29 | LRC_SQ_VCCRX2 | 13 | | | LRC_SQ_VCCRX2 | 13 | | |
| AM28 | LRC_SQ_HDINN2 | 13 | | C | LRC_SQ_HDINN2 | 13 | | C |
| AL27 | LRC_SQ_VCCIB2 | 13 | | | LRC_SQ_VCCIB2 | 13 | | |
| AM29 | LRC_SQ_HDINP2 | 13 | | T | LRC_SQ_HDINP2 | 13 | | T |
| AL29 | LRC_SQ_VCCP | 13 | | | LRC_SQ_VCCP | 13 | | |
| AL30 | LRC_SQ_REFCLKP | 13 | | T | LRC_SQ_REFCLKP | 13 | | T |
| AK30 | LRC_SQ_REFCLKN | 13 | | C | LRC_SQ_REFCLKN | 13 | | C |
| AK29 | LRC_SQ_VCCAUX33 | 13 | | | LRC_SQ_VCCAUX33 | 13 | | |
| AM30 | LRC_SQ_HDINP1 | 13 | | T | LRC_SQ_HDINP1 | 13 | | T |
| AL31 | LRC_SQ_VCCIB1 | 13 | | | LRC_SQ_VCCIB1 | 13 | | |
| AM31 | LRC_SQ_HDINN1 | 13 | | C | LRC_SQ_HDINN1 | 13 | | C |
| AN30 | LRC_SQ_VCCRX1 | 13 | | | LRC_SQ_VCCRX1 | 13 | | |
| AP30 | LRC_SQ_HDOUTP1 | 13 | | T | LRC_SQ_HDOUTP1 | 13 | | T |
| AL32 | LRC_SQ_VCCOB1 | 13 | | | LRC_SQ_VCCOB1 | 13 | | |
| AP31 | LRC_SQ_HDOUTN1 | 13 | | C | LRC_SQ_HDOUTN1 | 13 | | C |
| AN31 | LRC_SQ_VCCTX1 | 13 | | | LRC_SQ_VCCTX1 | 13 | | |
| AP32 | LRC_SQ_HDOUTN0 | 13 | | C | LRC_SQ_HDOUTN0 | 13 | | C |
| AM34 | LRC_SQ_VCCOB0 | 13 | | | LRC_SQ_VCCOB0 | 13 | | |
| AP33 | LRC_SQ_HDOUTP0 | 13 | | T | LRC_SQ_HDOUTP0 | 13 | | T |
| AN32 | LRC_SQ_VCCTX0 | 13 | | | LRC_SQ_VCCTX0 | 13 | | |
| AM32 | LRC_SQ_HDINN0 | 13 | | C | LRC_SQ_HDINN0 | 13 | | C |
| AN34 | LRC_SQ_VCCIB0 | 13 | | | LRC_SQ_VCCIB0 | 13 | | |
| AM33 | LRC_SQ_HDINP0 | 13 | | T | LRC_SQ_HDINP0 | 13 | | T |
| AN33 | LRC_SQ_VCCRX0 | 13 | | | LRC_SQ_VCCRX0 | 13 | | |
| AH28 | CFG2 | 8 | | | CFG2 | 8 | | |
| AD24 | CFG1 | 8 | | | CFG1 | 8 | | |
| AJ29 | CFG0 | 8 | | | CFG0 | 8 | | |
| AF25 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| AJ28 | CCLK | 8 | | | CCLK | 8 | | |
| AE25 | INITN | 8 | | | INITN | 8 | | |
| AK31 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| AE24 | WRITEN*** | 8 | | | WRITEN*** | 8 | | |
| AJ30 | CS1N*** | 8 | | | CS1N*** | 8 | | |
| AD25 | CSN*** | 8 | | | CSN*** | 8 | | |
| AG29 | D0/SPIFASTN*** | 8 | | | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AG28 | D1*** | 8 | | | D1*** | 8 | | |
| AG30 | D2*** | 8 | | | D2*** | 8 | | |
| AH29 | D3*** | 8 | | | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| AF26 | D4*** | 8 | | | D4*** | 8 | | |
| AH30 | D5*** | 8 | | | D5*** | 8 | | |
| AE26 | D6*** | 8 | | | D6*** | 8 | | |
| AJ31 | D7/SPID0*** | 8 | | | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AG27 | DI/CSSPI0N*** | 8 | | | DI/CSSPI0N*** | 8 | | |
| AK32 | DOUT/CSON/ CSSPI1N*** | 8 | | | DOUT/CSON/ CSSPI1N*** | 8 | | |
| AK33 | BUSY/SISPI*** | 8 | | | BUSY/SISPI*** | 8 | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AF27 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| AF28 | PR85B | 3 | RLM0_GDLLC_FB_A | C | PR102B | 3 | RLM0_GDLLC_FB_A/RDQ99 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AD26 | PR85A | 3 | RLM0_GDLLT_FB_A | T | PR102A | 3 | RLM0_GDLLT_FB_A/RDQ99 | T |
| AJ32 | PR84B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR101B | 3 | RLM0_GDLLC_IN_A**/ RDQ99 | C (LVDS)* |
| AJ33 | PR84A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR101A | 3 | RLM0_GDLLT_IN_A**/ RDQ99 | T (LVDS)* |
| AJ34 | PR83B | 3 | RLM0_GPLLC_IN_A** | C | PR100B | 3 | RLM0_GPLLC_IN_A**/ RDQ99 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AK34 | PR83A | 3 | RLM0_GPLLT_IN_A** | T | PR100A | 3 | RLM0_GPLLT_IN_A**/ RDQ99 | T |
| AH33 | PR82B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR99B | 3 | RLM0_GPLLC_FB_A/RDQ99 | C (LVDS)* |
| AH34 | PR82A | 3 | RLM0_GPLLT_FB_A/RDQS82**** | T (LVDS)* | PR99A | 3 | RLM0_GPLLT_FB_A/ RDQS99 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AF29 | PR81B | 3 | RDQ82 | C | PR98B | 3 | RDQ99 | C |
| AF31 | PR81A | 3 | RDQ82 | T | PR98A | 3 | RDQ99 | T |
| AG33 | PR80B | 3 | RDQ82 | C (LVDS)* | PR97B | 3 | RDQ99 | C (LVDS)* |
| AG34 | PR80A | 3 | RDQ82 | T (LVDS)* | PR97A | 3 | RDQ99 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AF30 | PR79B | 3 | RDQ82 | C | PR96B | 3 | RDQ99 | C |
| AF32 | PR79A | 3 | RDQ82 | T | PR96A | 3 | RDQ99 | T |
| AE29 | PR78B | 3 | RDQ82 | C (LVDS)* | PR95B | 3 | RDQ99 | C (LVDS)* |
| AE30 | PR78A | 3 | RDQ82 | T (LVDS)* | PR95A | 3 | RDQ99 | T (LVDS)* |
| AF33 | NC | - | | | PR93B | 3 | RDQ90 | C |
| AF34 | NC | - | | | PR93A | 3 | RDQ90 | T |
| - | - | - | | | GNDIO3 | - | | |
| AC27 | NC | - | | | PR92B | 3 | RDQ90 | C (LVDS)* |
| AC28 | NC | - | | | PR92A | 3 | RDQ90 | T (LVDS)* |
| AD29 | NC | - | | | PR91B | 3 | RDQ90 | C |
| AD30 | NC | - | | | PR91A | 3 | RDQ90 | T |
| - | - | - | | | VCCIO3 | 3 | | |
| AE33 | NC | - | | | PR90B | 3 | RDQ90 | C (LVDS)* |
| AE34 | NC | - | | | PR90A | 3 | RDQS90 | T (LVDS)* |
| AD32 | NC | - | | | PR89B | 3 | RDQ90 | C |
| - | - | - | | | GNDIO3 | - | | |
| AD31 | NC | - | | | PR89A | 3 | RDQ90 | T |
| AB25 | NC | - | | | PR88B | 3 | RDQ90 | C (LVDS)* |
| AC25 | NC | - | | | PR88A | 3 | RDQ90 | T (LVDS)* |
| AB28 | NC | - | | | PR87B | 3 | RDQ90 | C |
| - | - | - | | | VCCIO3 | 3 | | |
| AA26 | NC | - | | | PR87A | 3 | RDQ90 | T |
| AD33 | NC | - | | | PR86B | 3 | RDQ90 | C (LVDS)* |
| AD34 | NC | - | | | PR86A | 3 | RDQ90 | T (LVDS)* |
| AC29 | PR76B | 3 | RDQ73 | C | PR84B | 3 | RDQ81 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AA27 | PR76A | 3 | RDQ73 | T | PR84A | 3 | RDQ81 | T |
| AC32 | PR75B | 3 | RDQ73 | C (LVDS)* | PR83B | 3 | RDQ81 | C (LVDS)* |
| AC31 | PR75A | 3 | RDQ73 | T (LVDS)* | PR83A | 3 | RDQ81 | T (LVDS)* |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AA25 | PR74B | 3 | RDQ73 | C | PR82B | 3 | RDQ81 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AC24 | PR74A | 3 | RDQ73 | T | PR82A | 3 | RDQ81 | T |
| AC33 | PR73B | 3 | RDQ73 | C (LVDS)* | PR81B | 3 | RDQ81 | C (LVDS)* |
| AC34 | PR73A | 3 | RDQS73 | T (LVDS)* | PR81A | 3 | RDQS81 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AB24 | PR72B | 3 | RDQ73 | C | PR80B | 3 | RDQ81 | C |
| Y26 | PR72A | 3 | RDQ73 | T | PR80A | 3 | RDQ81 | T |
| AB33 | PR71B | 3 | RDQ73 | C (LVDS)* | PR79B | 3 | RDQ81 | C (LVDS)* |
| AB34 | PR71A | 3 | RDQ73 | T (LVDS)* | PR79A | 3 | RDQ81 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| Y27 | PR70B | 3 | RDQ73 | C | PR78B | 3 | RDQ81 | C |
| AB29 | PR70A | 3 | RDQ73 | T | PR78A | 3 | RDQ81 | T |
| AA34 | PR69B | 3 | RDQ73 | C (LVDS)* | PR77B | 3 | RDQ81 | C (LVDS)* |
| AA33 | PR69A | 3 | RDQ73 | T (LVDS)* | PR77A | 3 | RDQ81 | T (LVDS)* |
| AA31 | PR67B | 3 | RDQ64 | C | PR75B | 3 | RDQ72 | C |
| AA32 | PR67A | 3 | RDQ64 | T | PR75A | 3 | RDQ72 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AA28 | PR66B | 3 | RDQ64 | C (LVDS)* | PR74B | 3 | RDQ72 | C (LVDS)* |
| AA29 | PR66A | 3 | RDQ64 | T (LVDS)* | PR74A | 3 | RDQ72 | T (LVDS)* |
| AA30 | PR65B | 3 | RDQ64 | C | PR73B | 3 | RDQ72 | C |
| AB30 | PR65A | 3 | RDQ64 | T | PR73A | 3 | RDQ72 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| Y28 | PR64B | 3 | RDQ64 | C (LVDS)* | PR72B | 3 | RDQ72 | C (LVDS)* |
| Y29 | PR64A | 3 | RDQS64 | T (LVDS)* | PR72A | 3 | RDQS72 | T (LVDS)* |
| AA24 | PR63B | 3 | RDQ64 | C | PR71B | 3 | RDQ72 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| Y25 | PR63A | 3 | RDQ64 | T | PR71A | 3 | RDQ72 | T |
| Y31 | PR62B | 3 | RDQ64 | C (LVDS)* | PR70B | 3 | RDQ72 | C (LVDS)* |
| Y30 | PR62A | 3 | RDQ64 | T (LVDS)* | PR70A | 3 | RDQ72 | T (LVDS)* |
| Y24 | PR61B | 3 | RDQ64 | C | PR69B | 3 | RDQ72 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| W25 | PR61A | 3 | RDQ64 | T | PR69A | 3 | RDQ72 | T |
| Y33 | PR60B | 3 | RDQ64 | C (LVDS)* | PR68B | 3 | RDQ72 | C (LVDS)* |
| Y34 | PR60A | 3 | RDQ64 | T (LVDS)* | PR68A | 3 | RDQ72 | T (LVDS)* |
| W28 | PR58B | 3 | RLM3_SPLLC_FB_A/RDQ55 | C | PR66B | 3 | RLM4_SPLLC_FB_A/RDQ63 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| V26 | PR58A | 3 | RLM3_SPLLT_FB_A/RDQ55 | T | PR66A | 3 | RLM4_SPLLT_FB_A/RDQ63 | T |
| V28 | PR57B | 3 | RLM3_SPLLC_IN_A/RDQ55 | C (LVDS)* | PR65B | 3 | RLM4_SPLLC_IN_A/RDQ63 | C (LVDS)* |
| V27 | PR57A | 3 | RLM3_SPLLT_IN_A/RDQ55 | T (LVDS)* | PR65A | 3 | RLM4_SPLLT_IN_A/RDQ63 | T (LVDS)* |
| V25 | PR56B | 3 | RDQ55 | C | PR64B | 3 | RDQ63 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| W24 | PR56A | 3 | RDQ55 | T | PR64A | 3 | RDQ63 | T |
| W33 | PR55B | 3 | RDQ55 | C (LVDS)* | PR63B | 3 | RDQ63 | C (LVDS)* |
| W34 | PR55A | 3 | RDQS55 | T (LVDS)* | PR63A | 3 | RDQS63 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| V24 | PR54B | 3 | RDQ55 | C | PR62B | 3 | RDQ63 | C |
| U26 | PR54A | 3 | RDQ55 | T | PR62A | 3 | RDQ63 | T |
| W29 | PR53B | 3 | RDQ55 | C (LVDS)* | PR61B | 3 | RDQ63 | C (LVDS)* |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W30 | PR53A | 3 | RDQ55 | T (LVDS)* | PR61A | 3 | RDQ63 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U27 | PR52B | 3 | VREF2_3/RDQ55 | C | PR60B | 3 | VREF2_3/RDQ63 | C |
| V29 | PR52A | 3 | VREF1_3/RDQ55 | T | PR60A | 3 | VREF1_3/RDQ63 | T |
| V31 | PR51B | 3 | PCLKC3_0/RDQ55 | C (LVDS)* | PR59B | 3 | PCLKC3_0/RDQ63 | C (LVDS)* |
| V32 | PR51A | 3 | PCLKT3_0/RDQ55 | T (LVDS)* | PR59A | 3 | PCLKT3_0/RDQ63 | T (LVDS)* |
| V33 | PR49B | 2 | PCLKC2_0/RDQ46 | C | PR57B | 2 | PCLKC2_0/RDQ54 | C |
| V34 | PR49A | 2 | PCLKT2_0/RDQ46 | T | PR57A | 2 | PCLKT2_0/RDQ54 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| U24 | PR48B | 2 | RDQ46 | C (LVDS)* | PR56B | 2 | RDQ54 | C (LVDS)* |
| U25 | PR48A | 2 | RDQ46 | T (LVDS)* | PR56A | 2 | RDQ54 | T (LVDS)* |
| V30 | PR47B | 2 | RDQ46 | C | PR55B | 2 | RDQ54 | C |
| Y32 | PR47A | 2 | RDQ46 | T | PR55A | 2 | RDQ54 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| U28 | PR46B | 2 | RDQ46 | C (LVDS)* | PR54B | 2 | RDQ54 | C (LVDS)* |
| U29 | PR46A | 2 | RDQS46 | T (LVDS)* | PR54A | 2 | RDQS54 | T (LVDS)* |
| U33 | PR45B | 2 | RDQ46 | C | PR53B | 2 | RDQ54 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| U34 | PR45A | 2 | RDQ46 | T | PR53A | 2 | RDQ54 | T |
| T30 | PR44B | 2 | RDQ46 | C (LVDS)* | PR52B | 2 | RDQ54 | C (LVDS)* |
| U30 | PR44A | 2 | RDQ46 | T (LVDS)* | PR52A | 2 | RDQ54 | T (LVDS)* |
| T29 | PR43B | 2 | RUM3_SPLLC_FB_A/RDQ46 | C | PR51B | 2 | RUM3_SPLLC_FB_A/RDQ54 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| T28 | PR43A | 2 | RUM3_SPLLT_FB_A/RDQ46 | T | PR51A | 2 | RUM3_SPLLT_FB_A/RDQ54 | T |
| U31 | PR42B | 2 | RUM3_SPLLC_IN_A/RDQ46 | C (LVDS)* | PR50B | 2 | RUM3_SPLLC_IN_A/RDQ54 | C (LVDS)* |
| U32 | PR42A | 2 | RUM3_SPLLT_IN_A/RDQ46 | T (LVDS)* | PR50A | 2 | RUM3_SPLLT_IN_A/RDQ54 | T (LVDS)* |
| T33 | PR40B | 2 | RDQ37 | C | PR48B | 2 | RDQ45 | C |
| T34 | PR40A | 2 | RDQ37 | T | PR48A | 2 | RDQ45 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| R27 | PR39B | 2 | RDQ37 | C (LVDS)* | PR47B | 2 | RDQ45 | C (LVDS)* |
| R28 | PR39A | 2 | RDQ37 | T (LVDS)* | PR47A | 2 | RDQ45 | T (LVDS)* |
| R29 | PR38B | 2 | RDQ37 | C | PR46B | 2 | RDQ45 | C |
| R30 | PR38A | 2 | RDQ37 | T | PR46A | 2 | RDQ45 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| R33 | PR37B | 2 | RDQ37 | C (LVDS)* | PR45B | 2 | RDQ45 | C (LVDS)* |
| R34 | PR37A | 2 | RDQS37 | T (LVDS)* | PR45A | 2 | RDQS45 | T (LVDS)* |
| R32 | PR36B | 2 | RDQ37 | C | PR44B | 2 | RDQ45 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| R31 | PR36A | 2 | RDQ37 | T | PR44A | 2 | RDQ45 | T |
| P34 | PR35B | 2 | RDQ37 | C (LVDS)* | PR43B | 2 | RDQ45 | C (LVDS)* |
| P33 | PR35A | 2 | RDQ37 | T (LVDS)* | PR43A | 2 | RDQ45 | T (LVDS)* |
| R26 | PR34B | 2 | RDQ37 | C | PR42B | 2 | RDQ45 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| T25 | PR34A | 2 | RDQ37 | T | PR42A | 2 | RDQ45 | T |
| P28 | PR33B | 2 | RDQ37 | C (LVDS)* | PR41B | 2 | RDQ45 | C (LVDS)* |
| P27 | PR33A | 2 | RDQ37 | T (LVDS)* | PR41A | 2 | RDQ45 | T (LVDS)* |
| P30 | NC | - | | | PR40B | 2 | | C |
| - | - | - | | | GNDIO2 | - | | |
| P29 | NC | - | | | PR40A | 2 | | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| P31 | NC | - | | | PR39B | 2 | | C (LVDS)* |
| P32 | NC | - | | | PR39A | 2 | | T (LVDS)* |
| R25 | NC | - | | | PR38B | 2 | | C |
| - | - | - | | | VCCIO2 | 2 | | |
| T24 | NC | - | | | PR38A | 2 | | T |
| N34 | NC | - | | | PR37B | 2 | | C (LVDS)* |
| N33 | NC | - | | | PR37A | 2 | | T (LVDS)* |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| M34 | PR31B | 2 | RDQ28 | C | PR35B | 2 | RDQ32 | C |
| M33 | PR31A | 2 | RDQ28 | T | PR35A | 2 | RDQ32 | T |
| - | - | - | | | GNDIO2 | - | | |
| R24 | PR30B | 2 | RDQ28 | C (LVDS)* | PR34B | 2 | RDQ32 | C (LVDS)* |
| P24 | PR30A | 2 | RDQ28 | T (LVDS)* | PR34A | 2 | RDQ32 | T (LVDS)* |
| N30 | PR29B | 2 | RDQ28 | C | PR33B | 2 | RDQ32 | C |
| M29 | PR29A | 2 | RDQ28 | T | PR33A | 2 | RDQ32 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N28 | PR28B | 2 | RDQ28 | C (LVDS)* | PR32B | 2 | RDQ32 | C (LVDS)* |
| N29 | PR28A | 2 | RDQS28 | T (LVDS)* | PR32A | 2 | RDQS32 | T (LVDS)* |
| N24 | PR27B | 2 | RDQ28 | C | PR31B | 2 | RDQ32 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| N25 | PR27A | 2 | RDQ28 | T | PR31A | 2 | RDQ32 | T |
| M28 | PR26B | 2 | RDQ28 | C (LVDS)* | PR30B | 2 | RDQ32 | C (LVDS)* |
| M27 | PR26A | 2 | RDQ28 | T (LVDS)* | PR30A | 2 | RDQ32 | T (LVDS)* |
| L27 | PR25B | 2 | RDQ28 | C | PR29B | 2 | RDQ32 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M26 | PR25A | 2 | RDQ28 | T | PR29A | 2 | RDQ32 | T |
| M32 | PR24B | 2 | RDQ28 | C (LVDS)* | PR28B | 2 | RDQ32 | C (LVDS)* |
| M31 | PR24A | 2 | RDQ28 | T (LVDS)* | PR28A | 2 | RDQ32 | T (LVDS)* |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| - | - | - | | | VCCIO2 | 2 | | |
| L34 | PR22B | 2 | | C | PR22B | 2 | RDQ23 | C |
| L33 | PR22A | 2 | | T | PR22A | 2 | RDQ23 | T |
| L32 | PR21B | 2 | | C (LVDS)* | PR21B | 2 | RDQ23 | C (LVDS)* |
| L31 | PR21A | 2 | | T (LVDS)* | PR21A | 2 | RDQ23 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L28 | PR20B | 2 | | C | PR20B | 2 | RDQ23 | C |
| L29 | PR20A | 2 | | T | PR20A | 2 | RDQ23 | T |
| M30 | PR19B | 2 | | C (LVDS)* | PR19B | 2 | RDQ23 | C (LVDS)* |
| L30 | PR19A | 2 | | T (LVDS)* | PR19A | 2 | RDQ23 | T (LVDS)* |
| K34 | PR18B | 2 | RDQ15 | C | PR18B | 2 | RDQ15 | C |
| K33 | PR18A | 2 | RDQ15 | T | PR18A | 2 | RDQ15 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| K30 | PR17B | 2 | RDQ15 | C (LVDS)* | PR17B | 2 | RDQ15 | C (LVDS)* |
| K29 | PR17A | 2 | RDQ15 | T (LVDS)* | PR17A | 2 | RDQ15 | T (LVDS)* |
| J34 | PR16B | 2 | RDQ15 | C | PR16B | 2 | RDQ15 | C |
| J33 | PR16A | 2 | RDQ15 | T | PR16A | 2 | RDQ15 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J32 | PR15B | 2 | RDQ15 | C (LVDS)* | PR15B | 2 | RDQ15 | C (LVDS)* |
| J31 | PR15A | 2 | RDQS15 | T (LVDS)* | PR15A | 2 | RDQS15 | T (LVDS)* |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| H33 | PR14B | 2 | RDQ15 | C | PR14B | 2 | RDQ15 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| H34 | PR14A | 2 | RDQ15 | T | PR14A | 2 | RDQ15 | T |
| J30 | PR13B | 2 | RDQ15 | C (LVDS)* | PR13B | 2 | RDQ15 | C (LVDS)* |
| J29 | PR13A | 2 | RDQ15 | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J27 | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* |
| J28 | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| H31 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| H32 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H30 | XRES | 1 | | | XRES | 1 | | |
| B33 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| C33 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B34 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| C32 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| B32 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A33 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| C34 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| A32 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| B31 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| A31 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| D32 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A30 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| B30 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| C31 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| D31 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| C30 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| E29 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| E30 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D30 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| D29 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| C29 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| D27 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| C28 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| B29 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A29 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| E28 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| A28 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| B28 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| A27 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| D26 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A26 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| B27 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| C27 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B26 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| C26 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| D28 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E23 | PT82B | 1 | | C | PT100B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| F23 | PT82A | 1 | | T | PT100A | 1 | | T |
| F24 | NC | - | | | PT99B | 1 | | C |
| G23 | NC | - | | | PT99A | 1 | | T |
| D23 | PT80B | 1 | | C | PT98B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D22 | PT80A | 1 | | T | PT98A | 1 | | T |
| - | - | - | | | GNDIO1 | - | | |
| - | - | - | | | VCCIO1 | 1 | | |
| C21 | PT79B | 1 | | C | PT88B | 1 | | C |
| D21 | PT79A | 1 | | T | PT88A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| B21 | PT77B | 1 | | C | PT86B | 1 | | C |
| A21 | PT77A | 1 | | T | PT86A | 1 | | T |
| F22 | PT76B | 1 | | C | PT85B | 1 | | C |
| E22 | PT76A | 1 | | T | PT85A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| GNDIO | GNDIO1 | - | | | - | - | | |
| J22 | NC | - | | | PT84B | 1 | | C |
| G22 | NC | - | | | PT84A | 1 | | T |
| - | - | - | | | GNDIO1 | - | | |
| H22 | PT72B | 1 | | C | PT81B | 1 | | C |
| K22 | PT72A | 1 | | T | PT81A | 1 | | T |
| G21 | PT71B | 1 | | C | PT80B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J21 | PT71A | 1 | | T | PT80A | 1 | | T |
| H21 | NC | - | | | PT79B | 1 | | C |
| K21 | NC | - | | | PT79A | 1 | | T |
| D20 | PT69B | 1 | | C | PT78B | 1 | | C |
| F20 | PT69A | 1 | | T | PT78A | 1 | | T |
| C20 | PT68B | 1 | | C | PT77B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E20 | PT68A | 1 | | T | PT77A | 1 | | T |
| G20 | PT67B | 1 | | C | PT76B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J20 | PT67A | 1 | | T | PT76A | 1 | | T |
| A20 | PT66B | 1 | | C | PT75B | 1 | | C |
| B20 | PT66A | 1 | | T | PT75A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A19 | PT63B | 1 | | C | PT72B | 1 | | C |
| B19 | PT63A | 1 | | T | PT72A | 1 | | T |
| K20 | PT62B | 1 | | C | PT71B | 1 | | C |
| H20 | PT62A | 1 | | T | PT71A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| L19 | NC | - | | | PT70B | 1 | | C |
| L20 | NC | - | | | PT70A | 1 | | T |
| E19 | PT60B | 1 | | C | PT69B | 1 | | C |
| C18 | PT60A | 1 | | T | PT69A | 1 | | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| F19 | PT59B | 1 | | C | PT68B | 1 | | C |
| D18 | PT59A | 1 | | T | PT68A | 1 | | T |
| L18 | NC | - | | | PT67B | 1 | | C |
| K19 | NC | - | | | PT67A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A18 | PT57B | 1 | VREF2_1 | C | PT66B | 1 | VREF2_1 | C |
| B18 | PT57A | 1 | VREF1_1 | T | PT66A | 1 | VREF1_1 | T |
| G18 | PT56B | 1 | PCLKC1_0 | C | PT65B | 1 | PCLKC1_0 | C |
| E18 | PT56A | 1 | PCLKT1_0 | T | PT65A | 1 | PCLKT1_0 | T |
| F18 | PT55B | 0 | PCLKC0_0 | C | PT64B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| G19 | PT55A | 0 | PCLKT0_0 | T | PT64A | 0 | PCLKT0_0 | T |
| H18 | PT54B | 0 | VREF2_0 | C | PT63B | 0 | VREF2_0 | C |
| K18 | PT54A | 0 | VREF1_0 | T | PT63A | 0 | VREF1_0 | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J18 | PT53B | 0 | | C | PT60B | 0 | | C |
| L17 | PT53A | 0 | | T | PT60A | 0 | | T |
| G17 | PT52B | 0 | | C | PT59B | 0 | | C |
| - | - | - | | | GNDIO0 | - | | |
| J17 | PT52A | 0 | | T | PT59A | 0 | | T |
| H17 | PT51B | 0 | | C | PT58B | 0 | | C |
| - | - | - | | | VCCIO0 | 0 | | |
| K17 | PT51A | 0 | | T | PT58A | 0 | | T |
| B17 | PT50B | 0 | | C | PT57B | 0 | | C |
| GNDIO | GNDIO0 | - | | | - | - | | |
| A17 | PT50A | 0 | | T | PT57A | 0 | | T |
| D17 | PT49B | 0 | | C | PT56B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | - | - | | |
| F17 | PT49A | 0 | | T | PT56A | 0 | | T |
| B16 | PT48B | 0 | | C | PT55B | 0 | | C |
| A16 | PT48A | 0 | | T | PT55A | 0 | | T |
| - | - | - | | | GNDIO0 | - | | |
| - | - | - | | | VCCIO0 | 0 | | |
| E17 | PT47B | 0 | | C | PT52B | 0 | | C |
| C17 | PT47A | 0 | | T | PT52A | 0 | | T |
| K16 | PT46B | 0 | | C | PT51B | 0 | | C |
| J15 | PT46A | 0 | | T | PT51A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| G16 | PT45B | 0 | | C | PT50B | 0 | | C |
| H15 | PT45A | 0 | | T | PT50A | 0 | | T |
| A15 | PT44B | 0 | | C | PT49B | 0 | | C |
| B15 | PT44A | 0 | | T | PT49A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| L16 | PT43B | 0 | | C | PT48B | 0 | | C |
| K15 | PT43A | 0 | | T | PT48A | 0 | | T |
| F16 | PT42B | 0 | | C | PT47B | 0 | | C |
| E16 | PT42A | 0 | | T | PT47A | 0 | | T |
| E15 | PT41B | 0 | | C | PT46B | 0 | | C |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| G15 | PT41A | 0 | | T | PT46A | 0 | | T |
| J14 | NC | - | | | PT45B | 0 | | C |
| L15 | NC | - | | | PT45A | 0 | | T |
| H14 | NC | - | | | PT44B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K14 | NC | - | | | PT44A | 0 | | T |
| F15 | PT38B | 0 | | C | PT42B | 0 | | C |
| G14 | PT38A | 0 | | T | PT42A | 0 | | T |
| C15 | PT37B | 0 | | C | PT41B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| D14 | PT37A | 0 | | T | PT41A | 0 | | T |
| G13 | PT36B | 0 | | C | PT40B | 0 | | C |
| - | - | - | | | VCCIO0 | 0 | | |
| J13 | PT36A | 0 | | T | PT40A | 0 | | T |
| B14 | PT35B | 0 | | C | PT39B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | - | - | | |
| A14 | PT35A | 0 | | T | PT39A | 0 | | T |
| F13 | PT34B | 0 | | C | PT38B | 0 | | C |
| H13 | PT34A | 0 | | T | PT38A | 0 | | T |
| D13 | PT33B | 0 | | C | PT37B | 0 | | C |
| C14 | PT33A | 0 | | T | PT37A | 0 | | T |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| E13 | PT32B | 0 | | C | PT32B | 0 | | C |
| D12 | PT32A | 0 | | T | PT32A | 0 | | T |
| G12 | PT31B | 0 | | C | PT31B | 0 | | C |
| E12 | PT31A | 0 | | T | PT31A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F12 | NC | - | | | PT30B | 0 | | C |
| D11 | NC | - | | | PT30A | 0 | | T |
| F11 | NC | - | | | PT29B | 0 | | C |
| E11 | NC | - | | | PT29A | 0 | | T |
| D7 | ULC_SQ_VCCRX0 | 11 | | | ULC_SQ_VCCRX0 | 11 | | |
| C9 | ULC_SQ_HDINP0 | 11 | | T | ULC_SQ_HDINP0 | 11 | | T |
| B9 | ULC_SQ_VCCIB0 | 11 | | | ULC_SQ_VCCIB0 | 11 | | |
| C8 | ULC_SQ_HDINN0 | 11 | | C | ULC_SQ_HDINN0 | 11 | | C |
| B8 | ULC_SQ_VCCTX0 | 11 | | | ULC_SQ_VCCTX0 | 11 | | |
| A9 | ULC_SQ_HDOUTP0 | 11 | | T | ULC_SQ_HDOUTP0 | 11 | | T |
| D9 | ULC_SQ_VCCOB0 | 11 | | | ULC_SQ_VCCOB0 | 11 | | |
| A8 | ULC_SQ_HDOUTN0 | 11 | | C | ULC_SQ_HDOUTN0 | 11 | | C |
| B7 | ULC_SQ_VCCTX1 | 11 | | | ULC_SQ_VCCTX1 | 11 | | |
| A7 | ULC_SQ_HDOUTN1 | 11 | | C | ULC_SQ_HDOUTN1 | 11 | | C |
| E7 | ULC_SQ_VCCOB1 | 11 | | | ULC_SQ_VCCOB1 | 11 | | |
| A6 | ULC_SQ_HDOUTP1 | 11 | | T | ULC_SQ_HDOUTP1 | 11 | | T |
| B6 | ULC_SQ_VCCRX1 | 11 | | | ULC_SQ_VCCRX1 | 11 | | |
| C7 | ULC_SQ_HDINN1 | 11 | | C | ULC_SQ_HDINN1 | 11 | | C |
| D8 | ULC_SQ_VCCIB1 | 11 | | | ULC_SQ_VCCIB1 | 11 | | |
| C6 | ULC_SQ_HDINP1 | 11 | | T | ULC_SQ_HDINP1 | 11 | | T |
| E6 | ULC_SQ_VCCAUX33 | 11 | | | ULC_SQ_VCCAUX33 | 11 | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E5 | ULC_SQ_REFCLKN | 11 | | C | ULC_SQ_REFCLKN | 11 | | C |
| D5 | ULC_SQ_REFCLKP | 11 | | T | ULC_SQ_REFCLKP | 11 | | T |
| D6 | ULC_SQ_VCCP | 11 | | | ULC_SQ_VCCP | 11 | | |
| C5 | ULC_SQ_HDINP2 | 11 | | T | ULC_SQ_HDINP2 | 11 | | T |
| D4 | ULC_SQ_VCCIB2 | 11 | | | ULC_SQ_VCCIB2 | 11 | | |
| C4 | ULC_SQ_HDINN2 | 11 | | C | ULC_SQ_HDINN2 | 11 | | C |
| B5 | ULC_SQ_VCCRX2 | 11 | | | ULC_SQ_VCCRX2 | 11 | | |
| A5 | ULC_SQ_HDOUTP2 | 11 | | T | ULC_SQ_HDOUTP2 | 11 | | T |
| D3 | ULC_SQ_VCCOB2 | 11 | | | ULC_SQ_VCCOB2 | 11 | | |
| A4 | ULC_SQ_HDOUTN2 | 11 | | C | ULC_SQ_HDOUTN2 | 11 | | C |
| B4 | ULC_SQ_VCCTX2 | 11 | | | ULC_SQ_VCCTX2 | 11 | | |
| A3 | ULC_SQ_HDOUTN3 | 11 | | C | ULC_SQ_HDOUTN3 | 11 | | C |
| C1 | ULC_SQ_VCCOB3 | 11 | | | ULC_SQ_VCCOB3 | 11 | | |
| A2 | ULC_SQ_HDOUTP3 | 11 | | T | ULC_SQ_HDOUTP3 | 11 | | T |
| B3 | ULC_SQ_VCCTX3 | 11 | | | ULC_SQ_VCCTX3 | 11 | | |
| C3 | ULC_SQ_HDINN3 | 11 | | C | ULC_SQ_HDINN3 | 11 | | C |
| B1 | ULC_SQ_VCCIB3 | 11 | | | ULC_SQ_VCCIB3 | 11 | | |
| C2 | ULC_SQ_HDINP3 | 11 | | T | ULC_SQ_HDINP3 | 11 | | T |
| B2 | ULC_SQ_VCCRX3 | 11 | | | ULC_SQ_VCCRX3 | 11 | | |
| AA13 | VCC | - | | | VCC | - | | |
| AA14 | VCC | - | | | VCC | - | | |
| AA15 | VCC | - | | | VCC | - | | |
| AA16 | VCC | - | | | VCC | - | | |
| AA17 | VCC | - | | | VCC | - | | |
| AA18 | VCC | - | | | VCC | - | | |
| AA19 | VCC | - | | | VCC | - | | |
| AA20 | VCC | - | | | VCC | - | | |
| AA21 | VCC | - | | | VCC | - | | |
| AA22 | VCC | - | | | VCC | - | | |
| AB14 | VCC | - | | | VCC | - | | |
| AB15 | VCC | - | | | VCC | - | | |
| AB20 | VCC | - | | | VCC | - | | |
| AB21 | VCC | - | | | VCC | - | | |
| N14 | VCC | - | | | VCC | - | | |
| N15 | VCC | - | | | VCC | - | | |
| N20 | VCC | - | | | VCC | - | | |
| N21 | VCC | - | | | VCC | - | | |
| P13 | VCC | - | | | VCC | - | | |
| P14 | VCC | - | | | VCC | - | | |
| P15 | VCC | - | | | VCC | - | | |
| P16 | VCC | - | | | VCC | - | | |
| P17 | VCC | - | | | VCC | - | | |
| P18 | VCC | - | | | VCC | - | | |
| P19 | VCC | - | | | VCC | - | | |
| P20 | VCC | - | | | VCC | - | | |
| P21 | VCC | - | | | VCC | - | | |
| P22 | VCC | - | | | VCC | - | | |
| R13 | VCC | - | | | VCC | - | | |
| R14 | VCC | - | | | VCC | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| R21 | VCC | - | | | VCC | - | | |
| R22 | VCC | - | | | VCC | - | | |
| T14 | VCC | - | | | VCC | - | | |
| T21 | VCC | - | | | VCC | - | | |
| U14 | VCC | - | | | VCC | - | | |
| U21 | VCC | - | | | VCC | - | | |
| V14 | VCC | - | | | VCC | - | | |
| V21 | VCC | - | | | VCC | - | | |
| W14 | VCC | - | | | VCC | - | | |
| W21 | VCC | - | | | VCC | - | | |
| Y13 | VCC | - | | | VCC | - | | |
| Y14 | VCC | - | | | VCC | - | | |
| Y21 | VCC | - | | | VCC | - | | |
| Y22 | VCC | - | | | VCC | - | | |
| C12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C16 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E14 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H16 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| M14 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| M15 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C19 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| C23 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E21 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H19 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H23 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| M20 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| M21 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G32 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K28 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K32 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N27 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N32 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| P23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| R23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| T27 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| T32 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| AA23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AB27 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AB32 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AE28 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AE32 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AH32 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| W27 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| W32 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| Y23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AC20 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC21 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AG19 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AG23 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AK21 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AM19 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AM23 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC14 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC15 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG16 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AK14 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AM12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AM16 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA12 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AB3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AB8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AE3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AE7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AH3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y12 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| G3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| P12 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| R12 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AD28 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AG32 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AB12 | VCCAUX | - | | | VCCAUX | - | | |
| AB13 | VCCAUX | - | | | VCCAUX | - | | |
| AB22 | VCCAUX | - | | | VCCAUX | - | | |
| AB23 | VCCAUX | - | | | VCCAUX | - | | |
| AC13 | VCCAUX | - | | | VCCAUX | - | | |
| AC22 | VCCAUX | - | | | VCCAUX | - | | |
| M13 | VCCAUX | - | | | VCCAUX | - | | |
| M22 | VCCAUX | - | | | VCCAUX | - | | |
| N12 | VCCAUX | - | | | VCCAUX | - | | |
| N13 | VCCAUX | - | | | VCCAUX | - | | |
| N22 | VCCAUX | - | | | VCCAUX | - | | |
| N23 | VCCAUX | - | | | VCCAUX | - | | |
| A1 | GND | - | | | GND | - | | |
| A10 | GND | - | | | GND | - | | |
| A13 | GND | - | | | GND | - | | |
| A22 | GND | - | | | GND | - | | |
| A25 | GND | - | | | GND | - | | |
| A34 | GND | - | | | GND | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AB16 | GND | - | | | GND | - | | |
| AB17 | GND | - | | | GND | - | | |
| AB18 | GND | - | | | GND | - | | |
| AB19 | GND | - | | | GND | - | | |
| AB26 | GND | - | | | GND | - | | |
| AB31 | GND | - | | | GND | - | | |
| AB4 | GND | - | | | GND | - | | |
| AB9 | GND | - | | | GND | - | | |
| AC16 | GND | - | | | GND | - | | |
| AC17 | GND | - | | | GND | - | | |
| AC18 | GND | - | | | GND | - | | |
| AC19 | GND | - | | | GND | - | | |
| AD27 | GND | - | | | GND | - | | |
| AE27 | GND | - | | | GND | - | | |
| AE31 | GND | - | | | GND | - | | |
| AE4 | GND | - | | | GND | - | | |
| AE8 | GND | - | | | GND | - | | |
| AF12 | GND | - | | | GND | - | | |
| AF16 | GND | - | | | GND | - | | |
| AF19 | GND | - | | | GND | - | | |
| AF23 | GND | - | | | GND | - | | |
| AG31 | GND | - | | | GND | - | | |
| AH31 | GND | - | | | GND | - | | |
| AH4 | GND | - | | | GND | - | | |
| AJ14 | GND | - | | | GND | - | | |
| AJ21 | GND | - | | | GND | - | | |
| AK27 | GND | - | | | GND | - | | |
| AK8 | GND | - | | | GND | - | | |
| AL10 | GND | - | | | GND | - | | |
| AL16 | GND | - | | | GND | - | | |
| AL19 | GND | - | | | GND | - | | |
| AL2 | GND | - | | | GND | - | | |
| AL25 | GND | - | | | GND | - | | |
| AL33 | GND | - | | | GND | - | | |
| AP1 | GND | - | | | GND | - | | |
| AP10 | GND | - | | | GND | - | | |
| AP13 | GND | - | | | GND | - | | |
| AP22 | GND | - | | | GND | - | | |
| AP25 | GND | - | | | GND | - | | |
| AP34 | GND | - | | | GND | - | | |
| D10 | GND | - | | | GND | - | | |
| D16 | GND | - | | | GND | - | | |
| D19 | GND | - | | | GND | - | | |
| D2 | GND | - | | | GND | - | | |
| D25 | GND | - | | | GND | - | | |
| D33 | GND | - | | | GND | - | | |
| E27 | GND | - | | | GND | - | | |
| E8 | GND | - | | | GND | - | | |
| F14 | GND | - | | | GND | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F21 | GND | - | | | GND | - | | |
| G31 | GND | - | | | GND | - | | |
| G4 | GND | - | | | GND | - | | |
| J12 | GND | - | | | GND | - | | |
| J16 | GND | - | | | GND | - | | |
| J19 | GND | - | | | GND | - | | |
| J23 | GND | - | | | GND | - | | |
| K27 | GND | - | | | GND | - | | |
| K31 | GND | - | | | GND | - | | |
| K4 | GND | - | | | GND | - | | |
| K8 | GND | - | | | GND | - | | |
| M16 | GND | - | | | GND | - | | |
| M17 | GND | - | | | GND | - | | |
| M18 | GND | - | | | GND | - | | |
| M19 | GND | - | | | GND | - | | |
| N16 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| N18 | GND | - | | | GND | - | | |
| N19 | GND | - | | | GND | - | | |
| N26 | GND | - | | | GND | - | | |
| N31 | GND | - | | | GND | - | | |
| N4 | GND | - | | | GND | - | | |
| N9 | GND | - | | | GND | - | | |
| R16 | GND | - | | | GND | - | | |
| R17 | GND | - | | | GND | - | | |
| R18 | GND | - | | | GND | - | | |
| R19 | GND | - | | | GND | - | | |
| T12 | GND | - | | | GND | - | | |
| T13 | GND | - | | | GND | - | | |
| T15 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T18 | GND | - | | | GND | - | | |
| T19 | GND | - | | | GND | - | | |
| T20 | GND | - | | | GND | - | | |
| T22 | GND | - | | | GND | - | | |
| T23 | GND | - | | | GND | - | | |
| T26 | GND | - | | | GND | - | | |
| T31 | GND | - | | | GND | - | | |
| T4 | GND | - | | | GND | - | | |
| T9 | GND | - | | | GND | - | | |
| U12 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U15 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| U18 | GND | - | | | GND | - | | |
| U19 | GND | - | | | GND | - | | |
| U20 | GND | - | | | GND | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U22 | GND | - | | | GND | - | | |
| U23 | GND | - | | | GND | - | | |
| V12 | GND | - | | | GND | - | | |
| V13 | GND | - | | | GND | - | | |
| V15 | GND | - | | | GND | - | | |
| V16 | GND | - | | | GND | - | | |
| V17 | GND | - | | | GND | - | | |
| V18 | GND | - | | | GND | - | | |
| V19 | GND | - | | | GND | - | | |
| V20 | GND | - | | | GND | - | | |
| V22 | GND | - | | | GND | - | | |
| V23 | GND | - | | | GND | - | | |
| W12 | GND | - | | | GND | - | | |
| W13 | GND | - | | | GND | - | | |
| W15 | GND | - | | | GND | - | | |
| W16 | GND | - | | | GND | - | | |
| W17 | GND | - | | | GND | - | | |
| W18 | GND | - | | | GND | - | | |
| W19 | GND | - | | | GND | - | | |
| W20 | GND | - | | | GND | - | | |
| W22 | GND | - | | | GND | - | | |
| W23 | GND | - | | | GND | - | | |
| W26 | GND | - | | | GND | - | | |
| W31 | GND | - | | | GND | - | | |
| W4 | GND | - | | | GND | - | | |
| W9 | GND | - | | | GND | - | | |
| Y16 | GND | - | | | GND | - | | |
| Y17 | GND | - | | | GND | - | | |
| Y18 | GND | - | | | GND | - | | |
| Y19 | GND | - | | | GND | - | | |
| A11 | NC | - | | | NC | - | | |
| A12 | NC | - | | | NC | - | | |
| A23 | NC | - | | | NC | - | | |
| A24 | NC | - | | | NC | - | | |
| AA11 | NC | - | | | NC | - | | |
| AB11 | NC | - | | | NC | - | | |
| AC26 | NC | - | | | NC | - | | |
| AC30 | NC | - | | | NC | - | | |
| AD11 | NC | - | | | NC | - | | |
| AD12 | NC | - | | | NC | - | | |
| AD13 | NC | - | | | NC | - | | |
| AD14 | NC | - | | | NC | - | | |
| AD15 | NC | - | | | NC | - | | |
| AD19 | NC | - | | | NC | - | | |
| AD21 | NC | - | | | NC | - | | |
| AD22 | NC | - | | | NC | - | | |
| AD23 | NC | - | | | NC | - | | |
| AE10 | NC | - | | | NC | - | | |
| AE11 | NC | - | | | NC | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AE12 | NC | - | | | NC | - | | |
| AE13 | NC | - | | | NC | - | | |
| AE19 | NC | - | | | NC | - | | |
| AE21 | NC | - | | | NC | - | | |
| AE22 | NC | - | | | NC | - | | |
| AE23 | NC | - | | | NC | - | | |
| AF11 | NC | - | | | NC | - | | |
| AF21 | NC | - | | | NC | - | | |
| AF22 | NC | - | | | NC | - | | |
| AF24 | NC | - | | | NC | - | | |
| AF8 | NC | - | | | NC | - | | |
| AF9 | NC | - | | | NC | - | | |
| AG10 | NC | - | | | NC | - | | |
| AG11 | NC | - | | | NC | - | | |
| AG24 | NC | - | | | NC | - | | |
| AG25 | NC | - | | | NC | - | | |
| AG26 | NC | - | | | NC | - | | |
| AG3 | NC | - | | | NC | - | | |
| AG7 | NC | - | | | NC | - | | |
| AG8 | NC | - | | | NC | - | | |
| AG9 | NC | - | | | NC | - | | |
| AH10 | NC | - | | | NC | - | | |
| AH11 | NC | - | | | NC | - | | |
| AH13 | NC | - | | | NC | - | | |
| AH24 | NC | - | | | NC | - | | |
| AH25 | NC | - | | | NC | - | | |
| AH26 | NC | - | | | NC | - | | |
| AH27 | NC | - | | | NC | - | | |
| AH5 | NC | - | | | NC | - | | |
| AH6 | NC | - | | | NC | - | | |
| AH7 | NC | - | | | NC | - | | |
| AH8 | NC | - | | | NC | - | | |
| AH9 | NC | - | | | NC | - | | |
| AJ10 | NC | - | | | NC | - | | |
| AJ11 | NC | - | | | NC | - | | |
| AJ13 | NC | - | | | NC | - | | |
| AJ24 | NC | - | | | NC | - | | |
| AJ25 | NC | - | | | NC | - | | |
| AJ26 | NC | - | | | NC | - | | |
| AJ27 | NC | - | | | NC | - | | |
| AJ3 | NC | - | | | NC | - | | |
| AJ4 | NC | - | | | NC | - | | |
| AJ5 | NC | - | | | NC | - | | |
| AJ6 | NC | - | | | NC | - | | |
| AJ7 | NC | - | | | NC | - | | |
| AJ8 | NC | - | | | NC | - | | |
| AJ9 | NC | - | | | NC | - | | |
| AK10 | NC | - | | | NC | - | | |
| AK11 | NC | - | | | NC | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AK12 | NC | - | | | NC | - | | |
| AK24 | NC | - | | | NC | - | | |
| AK25 | NC | - | | | NC | - | | |
| AK26 | NC | - | | | NC | - | | |
| AK4 | NC | - | | | NC | - | | |
| AK9 | NC | - | | | NC | - | | |
| AL11 | NC | - | | | NC | - | | |
| AL12 | NC | - | | | NC | - | | |
| AL34 | NC | - | | | NC | - | | |
| AM10 | NC | - | | | NC | - | | |
| AM11 | NC | - | | | NC | - | | |
| AM13 | NC | - | | | NC | - | | |
| AM25 | NC | - | | | NC | - | | |
| AN10 | NC | - | | | NC | - | | |
| AN11 | NC | - | | | NC | - | | |
| AN12 | NC | - | | | NC | - | | |
| AN13 | NC | - | | | NC | - | | |
| AN24 | NC | - | | | NC | - | | |
| AN25 | NC | - | | | NC | - | | |
| AP11 | NC | - | | | NC | - | | |
| AP12 | NC | - | | | NC | - | | |
| AP24 | NC | - | | | NC | - | | |
| B10 | NC | - | | | NC | - | | |
| B11 | NC | - | | | NC | - | | |
| B12 | NC | - | | | NC | - | | |
| B13 | NC | - | | | NC | - | | |
| B22 | NC | - | | | NC | - | | |
| B23 | NC | - | | | NC | - | | |
| B24 | NC | - | | | NC | - | | |
| B25 | NC | - | | | NC | - | | |
| C10 | NC | - | | | NC | - | | |
| C11 | NC | - | | | NC | - | | |
| C13 | NC | - | | | NC | - | | |
| C22 | NC | - | | | NC | - | | |
| C24 | NC | - | | | NC | - | | |
| C25 | NC | - | | | NC | - | | |
| D1 | NC | - | | | NC | - | | |
| D15 | NC | - | | | NC | - | | |
| D24 | NC | - | | | NC | - | | |
| D34 | NC | - | | | NC | - | | |
| E10 | NC | - | | | NC | - | | |
| E24 | NC | - | | | NC | - | | |
| E25 | NC | - | | | NC | - | | |
| E26 | NC | - | | | NC | - | | |
| E3 | NC | - | | | NC | - | | |
| E31 | NC | - | | | NC | - | | |
| E32 | NC | - | | | NC | - | | |
| E33 | NC | - | | | NC | - | | |
| E34 | NC | - | | | NC | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E4 | NC | - | | | NC | - | | |
| E9 | NC | - | | | NC | - | | |
| F10 | NC | - | | | NC | - | | |
| F25 | NC | - | | | NC | - | | |
| F26 | NC | - | | | NC | - | | |
| F27 | NC | - | | | NC | - | | |
| F28 | NC | - | | | NC | - | | |
| F29 | NC | - | | | NC | - | | |
| F30 | NC | - | | | NC | - | | |
| F31 | NC | - | | | NC | - | | |
| F32 | NC | - | | | NC | - | | |
| F33 | NC | - | | | NC | - | | |
| F34 | NC | - | | | NC | - | | |
| F5 | NC | - | | | NC | - | | |
| F6 | NC | - | | | NC | - | | |
| F7 | NC | - | | | NC | - | | |
| F8 | NC | - | | | NC | - | | |
| F9 | NC | - | | | NC | - | | |
| G10 | NC | - | | | NC | - | | |
| G11 | NC | - | | | NC | - | | |
| G24 | NC | - | | | NC | - | | |
| G25 | NC | - | | | NC | - | | |
| G26 | NC | - | | | NC | - | | |
| G27 | NC | - | | | NC | - | | |
| G28 | NC | - | | | NC | - | | |
| G29 | NC | - | | | NC | - | | |
| G30 | NC | - | | | NC | - | | |
| G33 | NC | - | | | NC | - | | |
| G34 | NC | - | | | NC | - | | |
| G7 | NC | - | | | NC | - | | |
| G8 | NC | - | | | NC | - | | |
| G9 | NC | - | | | NC | - | | |
| H10 | NC | - | | | NC | - | | |
| H11 | NC | - | | | NC | - | | |
| H24 | NC | - | | | NC | - | | |
| H25 | NC | - | | | NC | - | | |
| H26 | NC | - | | | NC | - | | |
| H27 | NC | - | | | NC | - | | |
| H28 | NC | - | | | NC | - | | |
| H29 | NC | - | | | NC | - | | |
| H8 | NC | - | | | NC | - | | |
| H9 | NC | - | | | NC | - | | |
| J10 | NC | - | | | NC | - | | |
| J11 | NC | - | | | NC | - | | |
| J24 | NC | - | | | NC | - | | |
| J25 | NC | - | | | NC | - | | |
| J26 | NC | - | | | NC | - | | |
| J9 | NC | - | | | NC | - | | |
| K10 | NC | - | | | NC | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K11 | NC | - | | | NC | - | | |
| K12 | NC | - | | | NC | - | | |
| K13 | NC | - | | | NC | - | | |
| K23 | NC | - | | | NC | - | | |
| K24 | NC | - | | | NC | - | | |
| K25 | NC | - | | | NC | - | | |
| K26 | NC | - | | | NC | - | | |
| L11 | NC | - | | | NC | - | | |
| L12 | NC | - | | | NC | - | | |
| L13 | NC | - | | | NC | - | | |
| L14 | NC | - | | | NC | - | | |
| L21 | NC | - | | | NC | - | | |
| L22 | NC | - | | | NC | - | | |
| L23 | NC | - | | | NC | - | | |
| L24 | NC | - | | | NC | - | | |
| L25 | NC | - | | | NC | - | | |
| L26 | NC | - | | | NC | - | | |
| M11 | NC | - | | | NC | - | | |
| M24 | NC | - | | | NC | - | | |
| M25 | NC | - | | | NC | - | | |
| M6 | NC | - | | | NC | - | | |
| M8 | NC | - | | | NC | - | | |
| N10 | NC | - | | | NC | - | | |
| N11 | NC | - | | | NC | - | | |
| P10 | NC | - | | | NC | - | | |
| P25 | NC | - | | | NC | - | | |
| P26 | NC | - | | | NC | - | | |
| R9 | NC | - | | | NC | - | | |
| T11 | NC | - | | | NC | - | | |
| U11 | NC | - | | | NC | - | | |
| W11 | NC | - | | | NC | - | | |
| Y10 | NC | - | | | NC | - | | |
| Y11 | NC | - | | | NC | - | | |
| R15 | VCCPLL | - | | | VCCPLL | - | | |
| R20 | VCCPLL | - | | | VCCPLL | - | | |
| Y15 | VCCPLL | - | | | VCCPLL | - | | |
| Y20 | VCCPLL | - | | | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70, and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LatticeECP2/M Family Data Sheet Ordering Information

July 2012 Data Sheet DS1006

## LatticeECP2 Part Number Description

LFE2 – XX XE – X XXXXXX X

**Device Family**
ECP2 (LatticeECP2 FPGA)

**Logic Capacity**
6 = 6K LUTs
12 = 12K LUTs
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs

**Encryption**
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

**Supply Voltage**
E = 1.2V

**Grade**
C = Commercial
I = Industrial

**Package**
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FN256 = 256-ball Lead-Free fpBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN900 = 900-ball Lead-Free fpBGA

**Speed**
5 = Slowest
6
7 = Fastest

## Ordering Information

Note:þLatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

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## LatticeECP2 Standard Series Devices, Conventional Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5T144C | 90 | 1.2V | -5 | TQFP | 144 | COM | 6 |
| LFE2-6E-6T144C | 90 | 1.2V | -6 | TQFP | 144 | COM | 6 |
| LFE2-6E-7T144C | 90 | 1.2V | -7 | TQFP | 144 | COM | 6 |
| LFE2-6E-5F256C | 190 | 1.2V | -5 | fpBGA | 256 | COM | 6 |
| LFE2-6E-6F256C | 190 | 1.2V | -6 | fpBGA | 256 | COM | 6 |
| LFE2-6E-7F256C | 190 | 1.2V | -7 | fpBGA | 256 | COM | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5T144C | 93 | 1.2V | -5 | TQFP | 144 | COM | 12 |
| LFE2-12E-6T144C | 93 | 1.2V | -6 | TQFP | 144 | COM | 12 |
| LFE2-12E-7T144C | 93 | 1.2V | -7 | TQFP | 144 | COM | 12 |
| LFE2-12E-5Q208C | 131 | 1.2V | -5 | PQFP | 208 | COM | 12 |
| LFE2-12E-6Q208C | 131 | 1.2V | -6 | PQFP | 208 | COM | 12 |
| LFE2-12E-7Q208C | 131 | 1.2V | -7 | PQFP | 208 | COM | 12 |
| LFE2-12E-5F256C | 193 | 1.2V | -5 | fpBGA | 256 | COM | 12 |
| LFE2-12E-6F256C | 193 | 1.2V | -6 | fpBGA | 256 | COM | 12 |
| LFE2-12E-7F256C | 193 | 1.2V | -7 | fpBGA | 256 | COM | 12 |
| LFE2-12E-5F484C | 297 | 1.2V | -5 | fpBGA | 484 | COM | 12 |
| LFE2-12E-6F484C | 297 | 1.2V | -6 | fpBGA | 484 | COM | 12 |
| LFE2-12E-7F484C | 297 | 1.2V | -7 | fpBGA | 484 | COM | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5Q208C | 131 | 1.2V | -5 | PQFP | 208 | COM | 20 |
| LFE2-20E-6Q208C | 131 | 1.2V | -6 | PQFP | 208 | COM | 20 |
| LFE2-20E-7Q208C | 131 | 1.2V | -7 | PQFP | 208 | COM | 20 |
| LFE2-20E-5F256C | 193 | 1.2V | -5 | fpBGA | 256 | COM | 20 |
| LFE2-20E-6F256C | 193 | 1.2V | -6 | fpBGA | 256 | COM | 20 |
| LFE2-20E-7F256C | 193 | 1.2V | -7 | fpBGA | 256 | COM | 20 |
| LFE2-20E-5F484C | 331 | 1.2V | -5 | fpBGA | 484 | COM | 20 |
| LFE2-20E-6F484C | 331 | 1.2V | -6 | fpBGA | 484 | COM | 20 |
| LFE2-20E-7F484C | 331 | 1.2V | -7 | fpBGA | 484 | COM | 20 |
| LFE2-20E-5F672C | 402 | 1.2V | -5 | fpBGA | 672 | COM | 20 |
| LFE2-20E-6F672C | 402 | 1.2V | -6 | fpBGA | 672 | COM | 20 |
| LFE2-20E-7F672C | 402 | 1.2V | -7 | fpBGA | 672 | COM | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35E-5F484C | 331 | 1.2V | -5 | fpBGA | 484 | COM | 35 |
| LFE2-35E-6F484C | 331 | 1.2V | -6 | fpBGA | 484 | COM | 35 |
| LFE2-35E-7F484C | 331 | 1.2V | -7 | fpBGA | 484 | COM | 35 |
| LFE2-35E-5F672C | 450 | 1.2V | -5 | fpBGA | 672 | COM | 35 |
| LFE2-35E-6F672C | 450 | 1.2V | -6 | fpBGA | 672 | COM | 35 |
| LFE2-35E-7F672C | 450 | 1.2V | -7 | fpBGA | 672 | COM | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50E-5F484C | 339 | 1.2V | -5 | fpBGA | 484 | COM | 50 |
| LFE2-50E-6F484C | 339 | 1.2V | -6 | fpBGA | 484 | COM | 50 |
| LFE2-50E-7F484C | 339 | 1.2V | -7 | fpBGA | 484 | COM | 50 |
| LFE2-50E-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | COM | 50 |
| LFE2-50E-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | COM | 50 |
| LFE2-50E-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | COM | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70E-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | COM | 70 |
| LFE2-70E-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | COM | 70 |
| LFE2-70E-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | COM | 70 |
| LFE2-70E-5F900C | 583 | 1.2V | -5 | fpBGA | 900 | COM | 70 |
| LFE2-70E-6F900C | 583 | 1.2V | -6 | fpBGA | 900 | COM | 70 |
| LFE2-70E-7F900C | 583 | 1.2V | -7 | fpBGA | 900 | COM | 70 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5T144I | 90 | 1.2V | -5 | TQFP | 144 | IND | 6 |
| LFE2-6E-6T144I | 90 | 1.2V | -6 | TQFP | 144 | IND | 6 |
| LFE2-6E-5F256I | 190 | 1.2V | -5 | fpBGA | 256 | IND | 6 |
| LFE2-6E-6F256I | 190 | 1.2V | -6 | fpBGA | 256 | IND | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5T144I | 93 | 1.2V | -5 | TQFP | 144 | IND | 12 |
| LFE2-12E-6T144I | 93 | 1.2V | -6 | TQFP | 144 | IND | 12 |
| LFE2-12E-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | IND | 12 |
| LFE2-12E-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | IND | 12 |
| LFE2-12E-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | IND | 12 |
| LFE2-12E-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | IND | 12 |
| LFE2-12E-5F484I | 297 | 1.2V | -5 | fpBGA | 484 | IND | 12 |
| LFE2-12E-6F484I | 297 | 1.2V | -6 | fpBGA | 484 | IND | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | IND | 20 |
| LFE2-20E-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | IND | 20 |
| LFE2-20E-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | IND | 20 |
| LFE2-20E-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | IND | 20 |
| LFE2-20E-5F484I | 331 | 1.2V | -5 | fpBGA | 484 | IND | 20 |
| LFE2-20E-6F484I | 331 | 1.2V | -6 | fpBGA | 484 | IND | 20 |
| LFE2-20E-5F672I | 402 | 1.2V | -5 | fpBGA | 672 | IND | 20 |
| LFE2-20E-6F672I | 402 | 1.2V | -6 | fpBGA | 672 | IND | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35E-5F484I | 331 | 1.2V | -5 | fpBGA | 484 | IND | 35 |
| LFE2-35E-6F484I | 331 | 1.2V | -6 | fpBGA | 484 | IND | 35 |
| LFE2-35E-5F672I | 450 | 1.2V | -5 | fpBGA | 672 | IND | 35 |
| LFE2-35E-6F672I | 450 | 1.2V | -6 | fpBGA | 672 | IND | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50E-5F484I | 339 | 1.2V | -5 | fpBGA | 484 | IND | 50 |
| LFE2-50E-6F484I | 339 | 1.2V | -6 | fpBGA | 484 | IND | 50 |
| LFE2-50E-5F672I | 500 | 1.2V | -5 | fpBGA | 672 | IND | 50 |
| LFE2-50E-6F672I | 500 | 1.2V | -6 | fpBGA | 672 | IND | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70E-5F672I | 500 | 1.2V | -5 | fpBGA | 672 | IND | 70 |
| LFE2-70E-6F672I | 500 | 1.2V | -6 | fpBGA | 672 | IND | 70 |
| LFE2-70E-5F900I | 583 | 1.2V | -5 | fpBGA | 900 | IND | 70 |
| LFE2-70E-6F900I | 583 | 1.2V | -6 | fpBGA | 900 | IND | 70 |

## LatticeECP2 Standard Series Devices, Lead-Free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5TN144C | 90 | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-6TN144C | 90 | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-7TN144C | 90 | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-5FN256C | 190 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 6 |
| LFE2-6E-6FN256C | 190 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 6 |
| LFE2-6E-7FN256C | 190 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5TN144C | 93 | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-6TN144C | 93 | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-7TN144C | 93 | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-5FN484C | 297 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 12 |
| LFE2-12E-6FN484C | 297 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 12 |
| LFE2-12E-7FN484C | 297 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-5FN484C | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-6FN484C | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-7FN484C | 331 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-5FN672C | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 20 |
| LFE2-20E-6FN672C | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 20 |
| LFE2-20E-7FN672C | 402 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35E-5FN484C | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 35 |
| LFE2-35E-6FN484C | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 35 |
| LFE2-35E-7FN484C | 331 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 35 |
| LFE2-35E-5FN672C | 450 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 35 |
| LFE2-35E-6FN672C | 450 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 35 |
| LFE2-35E-7FN672C | 450 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50E-5FN484C | 339 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 50 |
| LFE2-50E-6FN484C | 339 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 50 |
| LFE2-50E-7FN484C | 339 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 50 |
| LFE2-50E-5FN672C | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 50 |
| LFE2-50E-6FN672C | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 50 |
| LFE2-50E-7FN672C | 500 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70E-5FN672C | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 70 |
| LFE2-70E-6FN672C | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 70 |
| LFE2-70E-7FN672C | 500 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 70 |
| LFE2-70E-5FN900C | 583 | 1.2V | -5 | Lead-Free fpBGA | 900 | COM | 70 |
| LFE2-70E-6FN900C | 583 | 1.2V | -6 | Lead-Free fpBGA | 900 | COM | 70 |
| LFE2-70E-7FN900C | 583 | 1.2V | -7 | Lead-Free fpBGA | 900 | COM | 70 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5TN144I | 90 | 1.2V | -5 | Lead-Free TQFP | 144 | IND | 6 |
| LFE2-6E-6TN144I | 90 | 1.2V | -6 | Lead-Free TQFP | 144 | IND | 6 |
| LFE2-6E-5FN256I | 190 | 1.2V | -5 | Lead-Free fpBGA | 256 | IND | 6 |
| LFE2-6E-6FN256I | 190 | 1.2V | -6 | Lead-Free fpBGA | 256 | IND | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5TN144I | 93 | 1.2V | -5 | Lead-Free TQFP | 144 | IND | 12 |
| LFE2-12E-6TN144I | 93 | 1.2V | -6 | Lead-Free TQFP | 144 | IND | 12 |
| LFE2-12E-5QN208I | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | IND | 12 |
| LFE2-12E-6QN208I | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | IND | 12 |
| LFE2-12E-5FN256I | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | IND | 12 |
| LFE2-12E-6FN256I | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | IND | 12 |
| LFE2-12E-5FN484I | 297 | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 12 |
| LFE2-12E-6FN484I | 297 | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5QN208I | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | IND | 20 |
| LFE2-20E-6QN208I | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | IND | 20 |
| LFE2-20E-5FN256I | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | IND | 20 |
| LFE2-20E-6FN256I | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | IND | 20 |
| LFE2-20E-5FN484I | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 20 |
| LFE2-20E-6FN484I | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 20 |
| LFE2-20E-5FN672I | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 20 |
| LFE2-20E-6FN672I | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35E-5FN484I | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 35 |
| LFE2-35E-6FN484I | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 35 |
| LFE2-35E-5FN672I | 450 | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 35 |
| LFE2-35E-6FN672I | 450 | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50E-5FN484I | 339 | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 50 |
| LFE2-50E-6FN484I | 339 | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 50 |
| LFE2-50E-5FN672I | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 50 |
| LFE2-50E-6FN672I | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70E-5FN672I | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 70 |
| LFE2-70E-6FN672I | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 70 |
| LFE2-70E-5FN900I | 583 | 1.2V | -5 | Lead-Free fpBGA | 900 | IND | 70 |
| LFE2-70E-6FN900I | 583 | 1.2V | -6 | Lead-Free fpBGA | 900 | IND | 70 |

## LatticeECP2 S-Series Devices, Conventional Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6SE-5T144C | 90 | 1.2V | -5 | TQFP | 144 | Com | 6 |
| LFE2-6SE-6T144C | 90 | 1.2V | -6 | TQFP | 144 | Com | 6 |
| LFE2-6SE-7T144C | 90 | 1.2V | -7 | TQFP | 144 | Com | 6 |
| LFE2-6SE-5F256C | 190 | 1.2V | -5 | fpBGA | 256 | Com | 6 |
| LFE2-6SE-6F256C | 190 | 1.2V | -6 | fpBGA | 256 | Com | 6 |
| LFE2-6SE-7F256C | 190 | 1.2V | -7 | fpBGA | 256 | Com | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12SE-5T144C | 93 | 1.2V | -5 | TQFP | 144 | Com | 12 |
| LFE2-12SE-6T144C | 93 | 1.2V | -6 | TQFP | 144 | Com | 12 |
| LFE2-12SE-7T144C | 93 | 1.2V | -7 | TQFP | 144 | Com | 12 |
| LFE2-12SE-5Q208C | 131 | 1.2V | -5 | PQFP | 208 | Com | 12 |
| LFE2-12SE-6Q208C | 131 | 1.2V | -6 | PQFP | 208 | Com | 12 |
| LFE2-12SE-7Q208C | 131 | 1.2V | -7 | PQFP | 208 | Com | 12 |
| LFE2-12SE-5F256C | 193 | 1.2V | -5 | fpBGA | 256 | Com | 12 |
| LFE2-12SE-6F256C | 193 | 1.2V | -6 | fpBGA | 256 | Com | 12 |
| LFE2-12SE-7F256C | 193 | 1.2V | -7 | fpBGA | 256 | Com | 12 |
| LFE2-12SE-5F484C | 297 | 1.2V | -5 | fpBGA | 484 | Com | 12 |
| LFE2-12SE-6F484C | 297 | 1.2V | -6 | fpBGA | 484 | Com | 12 |
| LFE2-12SE-7F484C | 297 | 1.2V | -7 | fpBGA | 484 | Com | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20SE-5Q208C | 131 | 1.2V | -5 | PQFP | 208 | Com | 20 |
| LFE2-20SE-6Q208C | 131 | 1.2V | -6 | PQFP | 208 | Com | 20 |
| LFE2-20SE-7Q208C | 131 | 1.2V | -7 | PQFP | 208 | Com | 20 |
| LFE2-20SE-5F256C | 193 | 1.2V | -5 | fpBGA | 256 | Com | 20 |
| LFE2-20SE-6F256C | 193 | 1.2V | -6 | fpBGA | 256 | Com | 20 |
| LFE2-20SE-7F256C | 193 | 1.2V | -7 | fpBGA | 256 | Com | 20 |
| LFE2-20SE-5F484C | 331 | 1.2V | -5 | fpBGA | 484 | Com | 20 |
| LFE2-20SE-6F484C | 331 | 1.2V | -6 | fpBGA | 484 | Com | 20 |
| LFE2-20SE-7F484C | 331 | 1.2V | -7 | fpBGA | 484 | Com | 20 |
| LFE2-20SE-5F672C | 402 | 1.2V | -5 | fpBGA | 672 | Com | 20 |
| LFE2-20SE-6F672C | 402 | 1.2V | -6 | fpBGA | 672 | Com | 20 |
| LFE2-20SE-7F672C | 402 | 1.2V | -7 | fpBGA | 672 | Com | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35SE-5F484C | 331 | 1.2V | -5 | fpBGA | 484 | Com | 35 |
| LFE2-35SE-6F484C | 331 | 1.2V | -6 | fpBGA | 484 | Com | 35 |
| LFE2-35SE-7F484C | 331 | 1.2V | -7 | fpBGA | 484 | Com | 35 |
| LFE2-35SE-5F672C | 450 | 1.2V | -5 | fpBGA | 672 | Com | 35 |
| LFE2-35SE-6F672C | 450 | 1.2V | -6 | fpBGA | 672 | Com | 35 |
| LFE2-35SE-7F672C | 450 | 1.2V | -7 | fpBGA | 672 | Com | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50SE-5F484C | 339 | 1.2V | -5 | fpBGA | 484 | Com | 50 |
| LFE2-50SE-6F484C | 339 | 1.2V | -6 | fpBGA | 484 | Com | 50 |
| LFE2-50SE-7F484C | 339 | 1.2V | -7 | fpBGA | 484 | Com | 50 |
| LFE2-50SE-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | Com | 50 |
| LFE2-50SE-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | Com | 50 |
| LFE2-50SE-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | Com | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70SE-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | Com | 70 |
| LFE2-70SE-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | Com | 70 |
| LFE2-70SE-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | Com | 70 |
| LFE2-70SE-5F900C | 583 | 1.2V | -5 | fpBGA | 900 | Com | 70 |
| LFE2-70SE-6F900C | 583 | 1.2V | -6 | fpBGA | 900 | Com | 70 |
| LFE2-70SE-7F900C | 583 | 1.2V | -7 | fpBGA | 900 | Com | 70 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6SE-5T144I | 90 | 1.2V | -5 | TQFP | 144 | Ind | 6 |
| LFE2-6SE-6T144I | 90 | 1.2V | -6 | TQFP | 144 | Ind | 6 |
| LFE2-6SE-5F256I | 190 | 1.2V | -5 | fpBGA | 256 | Ind | 6 |
| LFE2-6SE-6F256I | 190 | 1.2V | -6 | fpBGA | 256 | Ind | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12SE-5T144I | 93 | 1.2V | -5 | TQFP | 144 | Ind | 12 |
| LFE2-12SE-6T144I | 93 | 1.2V | -6 | TQFP | 144 | Ind | 12 |
| LFE2-12SE-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | Ind | 12 |
| LFE2-12SE-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | Ind | 12 |
| LFE2-12SE-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | Ind | 12 |
| LFE2-12SE-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | Ind | 12 |
| LFE2-12SE-5F484I | 297 | 1.2V | -5 | fpBGA | 484 | Ind | 12 |
| LFE2-12SE-6F484I | 297 | 1.2V | -6 | fpBGA | 484 | Ind | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20SE-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | Ind | 20 |
| LFE2-20SE-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | Ind | 20 |
| LFE2-20SE-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | Ind | 20 |
| LFE2-20SE-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | Ind | 20 |
| LFE2-20SE-5F484I | 331 | 1.2V | -5 | fpBGA | 484 | Ind | 20 |
| LFE2-20SE-6F484I | 331 | 1.2V | -6 | fpBGA | 484 | Ind | 20 |
| LFE2-20SE-5F672I | 402 | 1.2V | -5 | fpBGA | 672 | Ind | 20 |
| LFE2-20SE-6F672I | 402 | 1.2V | -6 | fpBGA | 672 | Ind | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35SE-5F484I | 331 | 1.2V | -5 | fpBGA | 484 | Ind | 35 |
| LFE2-35SE-6F484I | 331 | 1.2V | -6 | fpBGA | 484 | Ind | 35 |
| LFE2-35SE-5F672I | 450 | 1.2V | -5 | fpBGA | 672 | Ind | 35 |
| LFE2-35SE-6F672I | 450 | 1.2V | -6 | fpBGA | 672 | Ind | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50SE-5F484I | 339 | 1.2V | -5 | fpBGA | 484 | Ind | 50 |
| LFE2-50SE-6F484I | 339 | 1.2V | -6 | fpBGA | 484 | Ind | 50 |
| LFE2-50SE-5F672I | 500 | 1.2V | -5 | fpBGA | 672 | Ind | 50 |
| LFE2-50SE-6F672I | 500 | 1.2V | -6 | fpBGA | 672 | Ind | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70SE-5F672I | 500 | 1.2V | -5 | fpBGA | 672 | Ind | 70 |
| LFE2-70SE-6F672I | 500 | 1.2V | -6 | fpBGA | 672 | Ind | 70 |
| LFE2-70SE-5F900I | 583 | 1.2V | -5 | fpBGA | 900 | Ind | 70 |
| LFE2-70SE-6F900I | 583 | 1.2V | -6 | fpBGA | 900 | Ind | 70 |

## LatticeECP2 S-Series Devices, Lead-Free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6SE-5TN144C | 90 | 1.2V | -5 | Lead-Free TQFP | 144 | Com | 6 |
| LFE2-6SE-6TN144C | 90 | 1.2V | -6 | Lead-Free TQFP | 144 | Com | 6 |
| LFE2-6SE-7TN144C | 90 | 1.2V | -7 | Lead-Free TQFP | 144 | Com | 6 |
| LFE2-6SE-5FN256C | 190 | 1.2V | -5 | Lead-Free fpBGA | 256 | Com | 6 |
| LFE2-6SE-6FN256C | 190 | 1.2V | -6 | Lead-Free fpBGA | 256 | Com | 6 |
| LFE2-6SE-7FN256C | 190 | 1.2V | -7 | Lead-Free fpBGA | 256 | Com | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12SE-5TN144C | 93 | 1.2V | -5 | Lead-Free TQFP | 144 | Com | 12 |
| LFE2-12SE-6TN144C | 93 | 1.2V | -6 | Lead-Free TQFP | 144 | Com | 12 |
| LFE2-12SE-7TN144C | 93 | 1.2V | -7 | Lead-Free TQFP | 144 | Com | 12 |
| LFE2-12SE-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | Com | 12 |
| LFE2-12SE-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | Com | 12 |
| LFE2-12SE-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | Com | 12 |
| LFE2-12SE-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | Com | 12 |
| LFE2-12SE-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | Com | 12 |
| LFE2-12SE-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | Com | 12 |
| LFE2-12SE-5FN484C | 297 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 12 |
| LFE2-12SE-6FN484C | 297 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 12 |
| LFE2-12SE-7FN484C | 297 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20SE-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | Com | 20 |
| LFE2-20SE-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | Com | 20 |
| LFE2-20SE-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | Com | 20 |
| LFE2-20SE-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | Com | 20 |
| LFE2-20SE-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | Com | 20 |
| LFE2-20SE-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | Com | 20 |
| LFE2-20SE-5FN484C | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 20 |
| LFE2-20SE-6FN484C | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 20 |
| LFE2-20SE-7FN484C | 331 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 20 |
| LFE2-20SE-5FN672C | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | Com | 20 |
| LFE2-20SE-6FN672C | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | Com | 20 |
| LFE2-20SE-7FN672C | 402 | 1.2V | -7 | Lead-Free fpBGA | 672 | Com | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35SE-5FN484C | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 35 |
| LFE2-35SE-6FN484C | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 35 |
| LFE2-35SE-7FN484C | 331 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 35 |
| LFE2-35SE-5FN672C | 450 | 1.2V | -5 | Lead-Free fpBGA | 672 | Com | 35 |
| LFE2-35SE-6FN672C | 450 | 1.2V | -6 | Lead-Free fpBGA | 672 | Com | 35 |
| LFE2-35SE-7FN672C | 450 | 1.2V | -7 | Lead-Free fpBGA | 672 | Com | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50SE-5FN484C | 339 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 50 |
| LFE2-50SE-6FN484C | 339 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 50 |
| LFE2-50SE-7FN484C | 339 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 50 |
| LFE2-50SE-5FN672C | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | Com | 50 |
| LFE2-50SE-6FN672C | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | Com | 50 |
| LFE2-50SE-7FN672C | 500 | 1.2V | -7 | Lead-Free fpBGA | 672 | Com | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70SE-5FN672C | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | Com | 70 |
| LFE2-70SE-6FN672C | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | Com | 70 |
| LFE2-70SE-7FN672C | 500 | 1.2V | -7 | Lead-Free fpBGA | 672 | Com | 70 |
| LFE2-70SE-5FN900C | 583 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 70 |
| LFE2-70SE-6FN900C | 583 | 1.2V | -6 | Lead-Free fpBGA | 900 | Com | 70 |
| LFE2-70SE-7FN900C | 583 | 1.2V | -7 | Lead-Free fpBGA | 900 | Com | 70 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6SE-5TN144I | 90 | 1.2V | -5 | Lead-Free TQFP | 144 | Ind | 6 |
| LFE2-6SE-6TN144I | 90 | 1.2V | -6 | Lead-Free TQFP | 144 | Ind | 6 |
| LFE2-6SE-5FN256I | 190 | 1.2V | -5 | Lead-Free fpBGA | 256 | Ind | 6 |
| LFE2-6SE-6FN256I | 190 | 1.2V | -6 | Lead-Free fpBGA | 256 | Ind | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12SE-5TN144I | 93 | 1.2V | -5 | Lead-Free TQFP | 144 | Ind | 12 |
| LFE2-12SE-6TN144I | 93 | 1.2V | -6 | Lead-Free TQFP | 144 | Ind | 12 |
| LFE2-12SE-5QN208I | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | Ind | 12 |
| LFE2-12SE-6QN208I | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | Ind | 12 |
| LFE2-12SE-5FN256I | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | Ind | 12 |
| LFE2-12SE-6FN256I | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | Ind | 12 |
| LFE2-12SE-5FN484I | 297 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 12 |
| LFE2-12SE-6FN484I | 297 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20SE-5QN208I | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | Ind | 20 |
| LFE2-20SE-6QN208I | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | Ind | 20 |
| LFE2-20SE-5FN256I | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | Ind | 20 |
| LFE2-20SE-6FN256I | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | Ind | 20 |
| LFE2-20SE-5FN484I | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 20 |
| LFE2-20SE-6FN484I | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 20 |
| LFE2-20SE-5FN672I | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 20 |
| LFE2-20SE-6FN672I | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35SE-5FN484I | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 35 |
| LFE2-35SE-6FN484I | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 35 |
| LFE2-35SE-5FN672I | 450 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 35 |
| LFE2-35SE-6FN672I | 450 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50SE-5FN484I | 339 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 50 |
| LFE2-50SE-6FN484I | 339 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 50 |
| LFE2-50SE-5FN672I | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 50 |
| LFE2-50SE-6FN672I | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70SE-5FN672I | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 70 |
| LFE2-70SE-6FN672I | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 70 |
| LFE2-70SE-5FN900I | 583 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 70 |
| LFE2-70SE-6FN900I | 583 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 70 |

## LatticeECP2M Part Number Description

LFE2M XXX XE – X XXXXXX X

**Device Family**
ECP2M (LatticeECP2 FPGA + SERDES)

**Logic Capacity**
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs
100 = 100K LUTs

**Encryption**
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

**Supply Voltage**
E = 1.2V

**Grade**
C = Commercial
I = Industrial

**Package**
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
F1152 = 1152-ball fpBGA

FN256 = 256-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA
FN672 = 672-ball Lead-free fpBGA
FN900 = 900-ball Lead-free fpBGA
FN1152 = 1152-ball Lead-free fpBGA

**Speed**
5 = Slowest
6
7 = Fastest

## Ordering Information

Note:þLatticeECP2M devices are dual marked. For example, the commercial speed grade LFE2M50E-7F672C is also marked with industrial grade -6I (LFE2M50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial grade does not have industrial markings. The markings appear as follows:

## LatticeECP2M Standard Series Devices, Conventional Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20E-5F484C | 304 | 1.2V | -5 | fpBGA | 484 | COM | 20 |
| LFE2M20E-6F484C | 304 | 1.2V | -6 | fpBGA | 484 | COM | 20 |
| LFE2M20E-7F484C | 304 | 1.2V | -7 | fpBGA | 484 | COM | 20 |
| LFE2M20E-5F256C | 140 | 1.2V | -5 | fpBGA | 256 | COM | 20 |
| LFE2M20E-6F256C | 140 | 1.2V | -6 | fpBGA | 256 | COM | 20 |
| LFE2M20E-7F256C | 140 | 1.2V | -7 | fpBGA | 256 | COM | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35E-5F672C | 410 | 1.2V | -5 | fpBGA | 672 | COM | 35 |
| LFE2M35E-6F672C | 410 | 1.2V | -6 | fpBGA | 672 | COM | 35 |
| LFE2M35E-7F672C | 410 | 1.2V | -7 | fpBGA | 672 | COM | 35 |
| LFE2M35E-5F484C | 303 | 1.2V | -5 | fpBGA | 484 | COM | 35 |
| LFE2M35E-6F484C | 303 | 1.2V | -6 | fpBGA | 484 | COM | 35 |
| LFE2M35E-7F484C | 303 | 1.2V | -7 | fpBGA | 484 | COM | 35 |
| LFE2M35E-5F256C | 140 | 1.2V | -5 | fpBGA | 256 | COM | 35 |
| LFE2M35E-6F256C | 140 | 1.2V | -6 | fpBGA | 256 | COM | 35 |
| LFE2M35E-7F256C | 140 | 1.2V | -7 | fpBGA | 256 | COM | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50E-5F900C | 410 | 1.2V | -5 | fpBGA | 900 | COM | 50 |
| LFE2M50E-6F900C | 410 | 1.2V | -6 | fpBGA | 900 | COM | 50 |
| LFE2M50E-7F900C | 410 | 1.2V | -7 | fpBGA | 900 | COM | 50 |
| LFE2M50E-5F672C | 372 | 1.2V | -5 | fpBGA | 672 | COM | 50 |
| LFE2M50E-6F672C | 372 | 1.2V | -6 | fpBGA | 672 | COM | 50 |
| LFE2M50E-7F672C | 372 | 1.2V | -7 | fpBGA | 672 | COM | 50 |
| LFE2M50E-5F484C | 270 | 1.2V | -5 | fpBGA | 484 | COM | 50 |
| LFE2M50E-6F484C | 270 | 1.2V | -6 | fpBGA | 484 | COM | 50 |
| LFE2M50E-7F484C | 270 | 1.2V | -7 | fpBGA | 484 | COM | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70E-5F1152C | 436 | 1.2V | -5 | fpBGA | 1152 | COM | 70 |
| LFE2M70E-6F1152C | 436 | 1.2V | -6 | fpBGA | 1152 | COM | 70 |
| LFE2M70E-7F1152C | 436 | 1.2V | -7 | fpBGA | 1152 | COM | 70 |
| LFE2M70E-5F900C | 416 | 1.2V | -5 | fpBGA | 900 | COM | 70 |
| LFE2M70E-6F900C | 416 | 1.2V | -6 | fpBGA | 900 | COM | 70 |
| LFE2M70E-7F900C | 416 | 1.2V | -7 | fpBGA | 900 | COM | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100E-5F1152C | 520 | 1.2V | -5 | fpBGA | 1152 | COM | 100 |
| LFE2M100E-6F1152C | 520 | 1.2V | -6 | fpBGA | 1152 | COM | 100 |
| LFE2M100E-7F1152C | 520 | 1.2V | -7 | fpBGA | 1152 | COM | 100 |
| LFE2M100E-5F900C | 416 | 1.2V | -5 | fpBGA | 900 | COM | 100 |
| LFE2M100E-6F900C | 416 | 1.2V | -6 | fpBGA | 900 | COM | 100 |
| LFE2M100E-7F900C | 416 | 1.2V | -7 | fpBGA | 900 | COM | 100 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20E-5F484I | 304 | 1.2V | -5 | fpBGA | 484 | IND | 20 |
| LFE2M20E-6F484I | 304 | 1.2V | -6 | fpBGA | 484 | IND | 20 |
| LFE2M20E-5F256I | 140 | 1.2V | -5 | fpBGA | 256 | IND | 20 |
| LFE2M20E-6F256I | 140 | 1.2V | -6 | fpBGA | 256 | IND | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35E-5F672I | 410 | 1.2V | -5 | fpBGA | 672 | IND | 35 |
| LFE2M35E-6F672I | 410 | 1.2V | -6 | fpBGA | 672 | IND | 35 |
| LFE2M35E-5F484I | 303 | 1.2V | -5 | fpBGA | 484 | IND | 35 |
| LFE2M35E-6F484I | 303 | 1.2V | -6 | fpBGA | 484 | IND | 35 |
| LFE2M35E-5F256I | 140 | 1.2V | -5 | fpBGA | 256 | IND | 35 |
| LFE2M35E-6F256I | 140 | 1.2V | -6 | fpBGA | 256 | IND | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50E-5F900I | 410 | 1.2V | -5 | fpBGA | 900 | IND | 50 |
| LFE2M50E-6F900I | 410 | 1.2V | -6 | fpBGA | 900 | IND | 50 |
| LFE2M50E-5F672I | 372 | 1.2V | -5 | fpBGA | 672 | IND | 50 |
| LFE2M50E-6F672I | 372 | 1.2V | -6 | fpBGA | 672 | IND | 50 |
| LFE2M50E-5F484I | 270 | 1.2V | -5 | fpBGA | 484 | IND | 50 |
| LFE2M50E-6F484I | 270 | 1.2V | -6 | fpBGA | 484 | IND | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70E-5F1152I | 436 | 1.2V | -5 | fpBGA | 1152 | IND | 70 |
| LFE2M70E-6F1152I | 436 | 1.2V | -6 | fpBGA | 1152 | IND | 70 |
| LFE2M70E-5F900I | 416 | 1.2V | -5 | fpBGA | 900 | IND | 70 |
| LFE2M70E-6F900I | 416 | 1.2V | -6 | fpBGA | 900 | IND | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100E-5F1152I | 520 | 1.2V | -5 | fpBGA | 1152 | IND | 100 |
| LFE2M100E-6F1152I | 520 | 1.2V | -6 | fpBGA | 1152 | IND | 100 |
| LFE2M100E-5F900I | 416 | 1.2V | -5 | fpBGA | 900 | IND | 100 |
| LFE2M100E-6F900I | 416 | 1.2V | -6 | fpBGA | 900 | IND | 100 |

## LatticeECP2M Standard Series Devices, Lead-Free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20E-5FN484C | 304 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2M20E-6FN484C | 304 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2M20E-7FN484C | 304 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2M20E-5FN256C | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2M20E-6FN256C | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2M20E-7FN256C | 140 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35E-5FN672C | 410 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 35 |
| LFE2M35E-6FN672C | 410 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 35 |
| LFE2M35E-7FN672C | 410 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 35 |
| LFE2M35E-5FN484C | 303 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 35 |
| LFE2M35E-6FN484C | 303 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 35 |
| LFE2M35E-7FN484C | 303 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 35 |
| LFE2M35E-5FN256C | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 35 |
| LFE2M35E-6FN256C | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 35 |
| LFE2M35E-7FN256C | 140 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50E-5FN900C | 410 | 1.2V | -5 | Lead-Free fpBGA | 900 | COM | 50 |
| LFE2M50E-6FN900C | 410 | 1.2V | -6 | Lead-Free fpBGA | 900 | COM | 50 |
| LFE2M50E-7FN900C | 410 | 1.2V | -7 | Lead-Free fpBGA | 900 | COM | 50 |
| LFE2M50E-5FN672C | 372 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 50 |
| LFE2M50E-6FN672C | 372 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 50 |
| LFE2M50E-7FN672C | 372 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 50 |
| LFE2M50E-5FN484C | 270 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 50 |
| LFE2M50E-6FN484C | 270 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 50 |
| LFE2M50E-7FN484C | 270 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70E-5FN1152C | 436 | 1.2V | -5 | Lead-Free fpBGA | 1152 | COM | 70 |
| LFE2M70E-6FN1152C | 436 | 1.2V | -6 | Lead-Free fpBGA | 1152 | COM | 70 |
| LFE2M70E-7FN1152C | 436 | 1.2V | -7 | Lead-Free fpBGA | 1152 | COM | 70 |
| LFE2M70E-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | COM | 70 |
| LFE2M70E-6FN900C | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | COM | 70 |
| LFE2M70E-7FN900C | 416 | 1.2V | -7 | Lead-Free fpBGA | 900 | COM | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100E-5FN1152C | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | COM | 100 |
| LFE2M100E-6FN1152C | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | COM | 100 |
| LFE2M100E-7FN1152C | 520 | 1.2V | -7 | Lead-Free fpBGA | 1152 | COM | 100 |
| LFE2M100E-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | COM | 100 |
| LFE2M100E-6FN900C | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | COM | 100 |
| LFE2M100E-7FN900C | 416 | 1.2V | -7 | Lead-Free fpBGA | 900 | COM | 100 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20E-5FN484I | 304 | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 20 |
| LFE2M20E-6FN484I | 304 | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 20 |
| LFE2M20E-5FN256I | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | IND | 20 |
| LFE2M20E-6FN256I | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | IND | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35E-5FN672I | 410 | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 35 |
| LFE2M35E-6FN672I | 410 | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 35 |
| LFE2M35E-5FN484I | 303 | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 35 |
| LFE2M35E-6FN484I | 303 | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 35 |
| LFE2M35E-5FN256I | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | IND | 35 |
| LFE2M35E-6FN256I | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | IND | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50E-5FN900I | 410 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 50 |
| LFE2M50E-6FN900I | 410 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 50 |
| LFE2M50E-5FN672I | 372 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 50 |
| LFE2M50E-6FN672I | 372 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 50 |
| LFE2M50E-5FN484I | 270 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 50 |
| LFE2M50E-6FN484I | 270 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70E-5FN1152I | 436 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Ind | 70 |
| LFE2M70E-6FN1152I | 436 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Ind | 70 |
| LFE2M70E-5FN900I | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 70 |
| LFE2M70E-6FN900I | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100E-5FN1152I | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Ind | 100 |
| LFE2M100E-6FN1152I | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Ind | 100 |
| LFE2M100E-5FN900I | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 100 |
| LFE2M100E-6FN900I | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 100 |

## LatticeECP2M S-Series Devices, Conventional Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20SE-5F484C | 304 | 1.2V | -5 | fpBGA | 484 | Com | 20 |
| LFE2M20SE-6F484C | 304 | 1.2V | -6 | fpBGA | 484 | Com | 20 |
| LFE2M20SE-7F484C | 304 | 1.2V | -7 | fpBGA | 484 | Com | 20 |
| LFE2M20SE-5F256C | 140 | 1.2V | -5 | fpBGA | 256 | Com | 20 |
| LFE2M20SE-6F256C | 140 | 1.2V | -6 | fpBGA | 256 | Com | 20 |
| LFE2M20SE-7F256C | 140 | 1.2V | -7 | fpBGA | 256 | Com | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35SE-5F672C | 410 | 1.2V | -5 | fpBGA | 672 | Com | 35 |
| LFE2M35SE-6F672C | 410 | 1.2V | -6 | fpBGA | 672 | Com | 35 |
| LFE2M35SE-7F672C | 410 | 1.2V | -7 | fpBGA | 672 | Com | 35 |
| LFE2M35SE-5F484C | 303 | 1.2V | -5 | fpBGA | 484 | Com | 35 |
| LFE2M35SE-6F484C | 303 | 1.2V | -6 | fpBGA | 484 | Com | 35 |
| LFE2M35SE-7F484C | 303 | 1.2V | -7 | fpBGA | 484 | Com | 35 |
| LFE2M35SE-5F256C | 140 | 1.2V | -5 | fpBGA | 256 | Com | 35 |
| LFE2M35SE-6F256C | 140 | 1.2V | -6 | fpBGA | 256 | Com | 35 |
| LFE2M35SE-7F256C | 140 | 1.2V | -7 | fpBGA | 256 | Com | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50SE-5F900C | 410 | 1.2V | -5 | fpBGA | 900 | Com | 50 |
| LFE2M50SE-6F900C | 410 | 1.2V | -6 | fpBGA | 900 | Com | 50 |
| LFE2M50SE-7F900C | 410 | 1.2V | -7 | fpBGA | 900 | Com | 50 |
| LFE2M50SE-5F672C | 372 | 1.2V | -5 | fpBGA | 672 | Com | 50 |
| LFE2M50SE-6F672C | 372 | 1.2V | -6 | fpBGA | 672 | Com | 50 |
| LFE2M50SE-7F672C | 372 | 1.2V | -7 | fpBGA | 672 | Com | 50 |
| LFE2M50SE-5F484C | 270 | 1.2V | -5 | fpBGA | 484 | Com | 50 |
| LFE2M50SE-6F484C | 270 | 1.2V | -6 | fpBGA | 484 | Com | 50 |
| LFE2M50SE-7F484C | 270 | 1.2V | -7 | fpBGA | 484 | Com | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70SE-5F1152C | 436 | 1.2V | -5 | fpBGA | 1152 | Com | 70 |
| LFE2M70SE-6F1152C | 436 | 1.2V | -6 | fpBGA | 1152 | Com | 70 |
| LFE2M70SE-7F1152C | 436 | 1.2V | -7 | fpBGA | 1152 | Com | 70 |
| LFE2M70SE-5F900C | 416 | 1.2V | -5 | fpBGA | 900 | Com | 70 |
| LFE2M70SE-6F900C | 416 | 1.2V | -6 | fpBGA | 900 | Com | 70 |
| LFE2M70SE-7F900C | 416 | 1.2V | -7 | fpBGA | 900 | Com | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5F1152C | 520 | 1.2V | -5 | fpBGA | 1152 | Com | 100 |
| LFE2M100SE-6F1152C | 520 | 1.2V | -6 | fpBGA | 1152 | Com | 100 |
| LFE2M100SE-7F1152C | 520 | 1.2V | -7 | fpBGA | 1152 | Com | 100 |
| LFE2M100SE-5F900C | 416 | 1.2V | -5 | fpBGA | 900 | Com | 100 |
| LFE2M100SE-6F900C | 416 | 1.2V | -6 | fpBGA | 900 | Com | 100 |
| LFE2M100SE-7F900C | 416 | 1.2V | -7 | fpBGA | 900 | Com | 100 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20SE-5F484I | 304 | 1.2V | -5 | fpBGA | 484 | Ind | 20 |
| LFE2M20SE-6F484I | 304 | 1.2V | -6 | fpBGA | 484 | Ind | 20 |
| LFE2M20SE-5F256I | 140 | 1.2V | -5 | fpBGA | 256 | Ind | 20 |
| LFE2M20SE-6F256I | 140 | 1.2V | -6 | fpBGA | 256 | Ind | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35SE-5F672I | 410 | 1.2V | -5 | fpBGA | 672 | Ind | 35 |
| LFE2M35SE-6F672I | 410 | 1.2V | -6 | fpBGA | 672 | Ind | 35 |
| LFE2M35SE-5F484I | 303 | 1.2V | -5 | fpBGA | 484 | Ind | 35 |
| LFE2M35SE-6F484I | 303 | 1.2V | -6 | fpBGA | 484 | Ind | 35 |
| LFE2M35SE-5F256I | 140 | 1.2V | -5 | fpBGA | 256 | Ind | 35 |
| LFE2M35SE-6F256I | 140 | 1.2V | -6 | fpBGA | 256 | Ind | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50SE-5F900I | 410 | 1.2V | -5 | fpBGA | 900 | Ind | 50 |
| LFE2M50SE-6F900I | 410 | 1.2V | -6 | fpBGA | 900 | Ind | 50 |
| LFE2M50SE-5F672I | 372 | 1.2V | -5 | fpBGA | 672 | Ind | 50 |
| LFE2M50SE-6F672I | 372 | 1.2V | -6 | fpBGA | 672 | Ind | 50 |
| LFE2M50SE-5F484I | 270 | 1.2V | -5 | fpBGA | 484 | Ind | 50 |
| LFE2M50SE-6F484I | 270 | 1.2V | -6 | fpBGA | 484 | Ind | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70SE-5F1152I | 436 | 1.2V | -5 | fpBGA | 1152 | Ind | 70 |
| LFE2M70SE-6F1152I | 436 | 1.2V | -6 | fpBGA | 1152 | Ind | 70 |
| LFE2M70SE-5F900I | 416 | 1.2V | -5 | fpBGA | 900 | Ind | 70 |
| LFE2M70SE-6F900I | 416 | 1.2V | -6 | fpBGA | 900 | Ind | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5F1152I | 520 | 1.2V | -5 | fpBGA | 1152 | Ind | 100 |
| LFE2M100SE-6F1152I | 520 | 1.2V | -6 | fpBGA | 1152 | Ind | 100 |
| LFE2M100SE-5F900I | 416 | 1.2V | -5 | fpBGA | 900 | Ind | 100 |
| LFE2M100SE-6F900I | 416 | 1.2V | -6 | fpBGA | 900 | Ind | 100 |

## LatticeECP2M S-Series Devices, Lead-Free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20SE-5FN484C | 304 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 20 |
| LFE2M20SE-6FN484C | 304 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 20 |
| LFE2M20SE-7FN484C | 304 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 20 |
| LFE2M20SE-5FN256C | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | Com | 20 |
| LFE2M20SE-6FN256C | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | Com | 20 |
| LFE2M20SE-7FN256C | 140 | 1.2V | -7 | Lead-Free fpBGA | 256 | Com | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35SE-5FN672C | 410 | 1.2V | -5 | Lead-Free fpBGA | 672 | Com | 35 |
| LFE2M35SE-6FN672C | 410 | 1.2V | -6 | Lead-Free fpBGA | 672 | Com | 35 |
| LFE2M35SE-7FN672C | 410 | 1.2V | -7 | Lead-Free fpBGA | 672 | Com | 35 |
| LFE2M35SE-5FN484C | 303 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 35 |
| LFE2M35SE-6FN484C | 303 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 35 |
| LFE2M35SE-7FN484C | 303 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 35 |
| LFE2M35SE-5FN256C | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | Com | 35 |
| LFE2M35SE-6FN256C | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | Com | 35 |
| LFE2M35SE-7FN256C | 140 | 1.2V | -7 | Lead-Free fpBGA | 256 | Com | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50SE-5FN900C | 410 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 50 |
| LFE2M50SE-6FN900C | 410 | 1.2V | -6 | Lead-Free fpBGA | 900 | Com | 50 |
| LFE2M50SE-7FN900C | 410 | 1.2V | -7 | Lead-Free fpBGA | 900 | Com | 50 |
| LFE2M50SE-5FN672C | 372 | 1.2V | -5 | Lead-Free fpBGA | 672 | Com | 50 |
| LFE2M50SE-6FN672C | 372 | 1.2V | -6 | Lead-Free fpBGA | 672 | Com | 50 |
| LFE2M50SE-7FN672C | 372 | 1.2V | -7 | Lead-Free fpBGA | 672 | Com | 50 |
| LFE2M50SE-5FN484C | 270 | 1.2V | -5 | Lead-Free fpBGA | 484 | Com | 50 |
| LFE2M50SE-6FN484C | 270 | 1.2V | -6 | Lead-Free fpBGA | 484 | Com | 50 |
| LFE2M50SE-7FN484C | 270 | 1.2V | -7 | Lead-Free fpBGA | 484 | Com | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70SE-5FN1152C | 436 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Com | 70 |
| LFE2M70SE-6FN1152C | 436 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Com | 70 |
| LFE2M70SE-7FN1152C | 436 | 1.2V | -7 | Lead-Free fpBGA | 1152 | Com | 70 |
| LFE2M70SE-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 70 |
| LFE2M70SE-6FN900C | 416 | 416 | -6 | Lead-Free fpBGA | 900 | Com | 70 |
| LFE2M70SE-7FN900C | 416 | 416 | -7 | Lead-Free fpBGA | 900 | Com | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5FN1152C | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-6FN1152C | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-7FN1152C | 520 | 1.2V | -7 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-6FN900C | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-7FN900C | 416 | 1.2V | -7 | Lead-Free fpBGA | 900 | Com | 100 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M20SE-5FN484I | 304 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 20 |
| LFE2M20SE-6FN484I | 304 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 20 |
| LFE2M20SE-5FN256I | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | Ind | 20 |
| LFE2M20SE-6FN256I | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | Ind | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M35SE-5FN672I | 410 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 35 |
| LFE2M35SE-6FN672I | 410 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 35 |
| LFE2M35SE-5FN484I | 303 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 35 |
| LFE2M35SE-6FN484I | 303 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 35 |
| LFE2M35SE-5FN256I | 140 | 1.2V | -5 | Lead-Free fpBGA | 256 | Ind | 35 |
| LFE2M35SE-6FN256I | 140 | 1.2V | -6 | Lead-Free fpBGA | 256 | Ind | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M50SE-5FN900I | 410 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 50 |
| LFE2M50SE-6FN900I | 410 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 50 |
| LFE2M50SE-5FN672I | 372 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 50 |
| LFE2M50SE-6FN672I | 372 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 50 |
| LFE2M50SE-5FN484I | 270 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 50 |
| LFE2M50SE-6FN484I | 270 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M70SE-5FN1152I | 436 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Ind | 70 |
| LFE2M70SE-6FN1152I | 436 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Ind | 70 |
| LFE2M70SE-5FN900I | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 70 |
| LFE2M70SE-6FN900I | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 70 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5FN1152I | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Ind | 100 |
| LFE2M100SE-6FN1152I | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Ind | 100 |
| LFE2M100SE-5FN900I | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 100 |
| LFE2M100SE-6FN900I | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 100 |

# LatticeECP2/M Family Data Sheet Supplemental Information

**July 2012** **Data Sheet DS1006**

## For Further Information

A variety of technical notes for the LatticeECP2/M family are available on the Lattice web site at www.latticesemi.com.

- TN1102, LatticeECP2/M sysIO Usage Guide
- TN1103, LatticeECP2/M sysCLOCK PLL Design and Usage Guide
- TN1104, LatticeECP2/M Memory Usage Guide
- TN1105, LatticeECP2/M High-Speed I/O Interface
- TN1106, Power Estimation and Management for LatticeECP2/M Devices
- TN1107, LatticeECP2/M sysDSP Usage Guide
- TN1108, LatticeECP2/M sysCONFIG Usage Guide
- TN1109, LatticeECP2/M Configuration Encryption Usage Guide
- TN1113, LatticeECP2/M Soft Error Detection (SED) Usage Guide
- TN1124, LatticeECP2M SERDES/PCS Usage Guide
- TN1162, LatticeECP2/M Hardware Checklist

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

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# LatticeECP2/M Family Data Sheet Revision History

**September 2013** **Data Sheet DS1006**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2006 | 01.0 | — | Initial release. |
| August 2006 | 01.1 | Introduction | |
| | | | Updated Table 1-1 “LatticeECP2 Family Selection Guide”. |
| | | Architecture | Updated Figure 2-2 “PFU Diagram”. |
| | | | Updated Figure 2-13 “Secondary Clock Regions ECP2-50”. |
| | | | Updated Figure 2-25 “PIC Diagram”. |
| | | | Updated Figure 2-26 “Input Register Block for Left, Right and Bottom Edges”. |
| | | | Updated Figure 2-28 “Output Register Block for Left, Right and Bottom Edges”. |
| | | | Updated Figure 2-30 “DQS Input Routing for Left and Right Edges”. |
| | | | Updated Figure 2-32 “Edge Clock, DLL Calibration and DQS Local Bus Distribution”. |
| | | | Table 2-15 Selectable Master Clock (CCLK) Frequencies - Removed frequencies 15, 20, 21, 22, 23, 30, 34, 41, 45, 51, 55, 60. |
| | | | Replaced “CLKINDEL” with “CLKO”. |
| | | | Updated SED section. |
| | | | Qualified device migration capability when using DQS banks for DDR interfaces. |
| | | DC and Switching Characteristics | Added VCCPLL to the Recommended Operating Conditions table. |
| | | | Removed note 5 from “Hot Specifications” section. |
| | | | Added notes 7 and 8 to “Initialization Supply” Current table. |
| | | | Change note 6 - “...down to 95MHz” to “...down to 95MHz for DDR and 133MHz for DDR2” . |
| | | | New “Typical Building Block Function Performance” numbers. |
| | | | New External Switching Characteristics numbers. |
| | | | New Internal Switching Characteristics numbers. |
| | | | New Family Timing Adders numbers. |
| | | | Updated Timings for GPLLs, SPLLs and DLLs. |
| | | | Added sysCONFIG waveforms. |
| | | | Remove HSTL15D_II from sysIO Recommended Operating Conditions table. |
| | | | Updated Supply and Initialization Currents for ECP2-50. |
| | | Pinout Information | Added VCCPLL to the Signal Descriptions table. |
| | | | Updated Logic Signal Connections tables to include 484-fpBGA for the ECP2-50. |
| | | | Added Logic Signal Connections tables for ECP2-12 devices. |
| | | | Updated Pin Information Summary table to include ECP2-12. |
| | | | Updated Power Supply and NC Connections table to include ECP2-12. |
| | | | Added note 2 to DDR Strobe (DQS) Pin table. |
| | | | Added Information on: PCI, DDR & SPI4.2 Capabilities of the device-Package combination. |

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| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2006 (cont.) | 01.1 (cont.) | Pinout Information (cont.) | Added Information on: Available Device Resources per Packaged Device table. |
| | | Ordering Information | Updated ordering part number table to include ECP2-12. |
| | | | Updated topside mark drawing. |
| September 2006 | 02.0 | Multiple | Added information regarding LatticeECP2M support throughout. |
| September 2006 | 02.1 | DC and Switching Characteristics | Added Receiver Total Jitter Tolerance Specification table. |
| | | | Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table. |
| December 2006 | 02.2 | Introduction | LatticeECP2M Selection Guide table has been updated. |
| | | Architecture | Figure 2-16. Per Region Secondary Clock Selection has been updated. |
| | | | Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated. |
| | | DC and Switching | Footnotes have been added to Recommended Operating Conditions. |
| | | | DC Electrical Characteristics table has been updated. |
| | | | Supply Current (Standby) tables have been updated. |
| | | | Initialization Supply Current table have been updated. |
| | | | Updated timing numbers to include LFE2-12E (rev A 0.08). |
| | | Pinout Information | Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E. |
| | | Ordering Information | Updated to include the entire ECP2 and ECP2M device ordering information. |
| February 2007 | 02.3 | Architecture | Updated EBR Asynchronous Reset section. |
| March 2007 | 02.4 | DC and Switching Characteristics | Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz. |
| March 2007 | 02.5 | Introduction | Added “Security Series” to the LatticeECP2 and LatticeECP2M families. |
| | | Architecture | Enhanced Configuration Option section updated. |
| | | DC and Switching | Recommended Operating Conditions table - footnote 4 updated. |
| | | Ordering Information | “Security Series” ordering part numbers added. |
| April 2007 | 02.6 | Introduction | LatticeECP2M family table has been updated for user I/O counts. |
| | | Ordering Information | LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100. |
| July 2007 | 02.7 | Architecture | Updated text in Ripple Mode section. |
| | | DC and Switching | ECP2/M Supply Current information has been updated.<br>Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10).<br>SERDES timing information has been updated.<br>PCI Express timing information has been updated. |
| | | Pinout Information | Added LatticeECP2M20 pinout information. |
| August 2007 | 02.8 | Introduction | 1156-fpBGA package option has been removed from the LatticeECP2M family. |
| | | Architecture | Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated. |
| | | DC and Switching | Supply Current (Standby) table has been updated. |
| | | | DSP Function timing has been updated. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2007 (cont.) | 02.8 (cont.) | DC and Switching (cont.) | sysCLOCK GPLL timing has been updated. |
| | | Pinout Information | Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information. |
| | | Ordering Information | 1156-fpBGA package option has been removed from the LatticeECP2M family. |
| September 2007 | 02.9 | Pinout Information | Added Thermal Management text section. |
| February 2008 | 03.0 | Architecture | Added LVCMOS33D description. |
| | | DC and Switching | LatticeECP2M Supply Current has been updated. |
| | | | Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11). |
| | | | Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated. |
| | | | Table 3-8. Channel output Jitter (Max) has been updated. |
| | | Pinout Information | Signal description has been updated. |
| | | | Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100. |
| April 2008 | 03.1 | Pinout Information | Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated. |
| June 2008 | 03.2 | Introduction | Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device. |
| | | Architecture | Removed Read-Before-Write sysMEM EBR mode. |
| | | | Clarification of the operation of the secondary clock regions. |
| | | DC and Switching Characteristics | Removed Read-Before-Write sysMEM EBR mode. |
| August 2008 | 03.3 | Architecture | Clarification of the operation of the secondary clock regions. |
| | | Pinout Information | Added information for [LOC]DQ[num] to Signal Descriptions table. |
| January 2009 | 03.4 | DC and Switching Characteristics | Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode. |
| | | | Added Channel Output Jitter table for x20 mode. |
| November 2009 | 03.5 | DC and Switching Characteristics | Updated SPI/SPIm Configuration Waveforms diagram. |
| | | | Updated footnotes in LatticeECP2 Initialization Supply Current table. |
| | | | Updated footnotes in LatticeECP2M Initialization Supply Current table. |
| | | | Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table. |
| | | | Updated max. value for $t_{DINIT}$ parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Updated Figure 3-5 MLVDS |
| | | | Updated Table 3-7 Serial Output Timing and Levels |
| | | | Updated Table 3-15 Power Down/Power Up Specification |
| | | Pinout Information | Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| November 2009 (cont.) | 03.5 (cont.) | Pinout Information (cont.) | LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank. |
| | | | Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table. |
| | | | Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table. |
| | | | Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table. |
| | | | Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1). |
| | | Ordering Information | Updated LatticeECP2M Part Number Description diagram. |
| March 2010 | 03.6 | DC and Switching Characteristics | Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table. |
| | | Pinout Information | Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table. |
| July 2010 | 03.7 | Architecture | Updated the Typical sysIO Behavior During Power-up text section. |
| | | Pinout Information | Added reference to powerup information. |
| | | | Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP. |
| | | | Referenced footnote (***) for all D7/SPID0. |
| | | | Changed D7*** to D7/SPID0. |
| | | | Corrected *** footnote. |
| | | All Sections | Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified. |
| April 2011 | 03.8 | DC and Switching Characteristics | DC Electrical Characteristics table:<br>- Added footnote 3 to $I_{IH}$<br>- Added footnote 2 to $I_{IL}$, $I_{IH}$<br>- Updated C1 and C2 typ. and max. data. |
| | | | DLL Timing table – Removed line for $t_R$ and $t_F$. |
| | | | LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to $t_{DINIT}$. |
| | | | Figure 3-18 – Corrected label to be PRGM (not PRGMRJ). |
| | | Pinout Information | LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119. |
| January 2012 | 03.9 | Multiple | Removed references to ispLEVER design software. |
| | | Architecture | Corrected information regarding SED support. |
| | | DC and Switching Characteristics | Added reference to ESD information. |
| June 2013 | 04.0 | All | Updated document with new corporate logo. |
| | | Architecture | Architecture Overview – Added information on the state of the register on power up and after configuration. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| June 2013 (cont.) | 04.0 (cont.) | DC and Switching Characteristics | sysCLOCK SPLL Timing table – Corrected signal names for $t_{RST}$ parameter. |
| | | | LatticeECP2/M sysCONFIG Port Timing Specifications table – added $t_{SUMCDI}$ and $t_{HMCDI}$ parameters. |
| September 2013 | 04.1 | Architecture | Updated Selectable Master Clock (CCLK) Frequencies during Configuration table. |
| | | DC and Switching Characteristics | Added information on $f_{MAXSPI}$ parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table. |