

DUAL FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

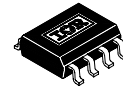
Description

The IPS022G are fully protected dual low side SMART POWER MOSFETs respectively. They feature over-current, over-temperature, ESD protection and drain to source active clamp. These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 5A. These devices restart once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

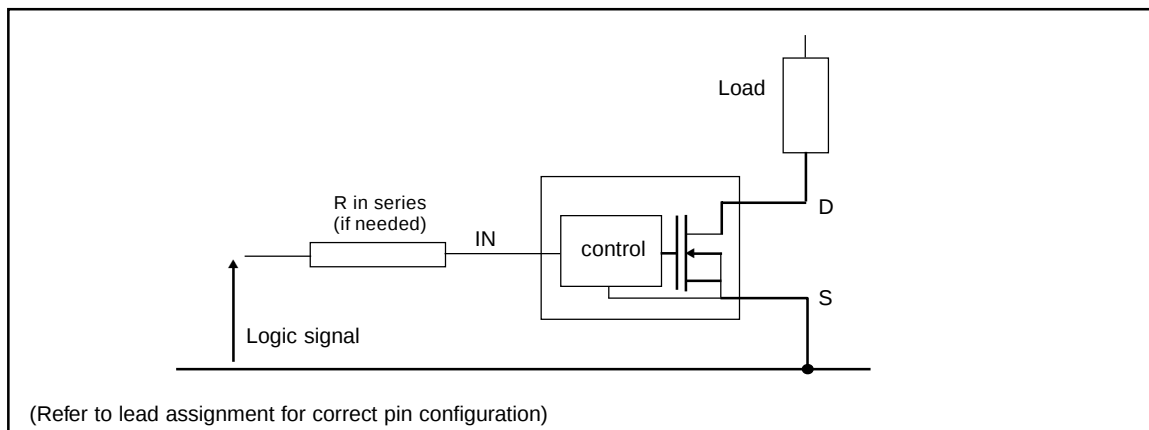
$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	5A
T_{on}/T_{off}	1.5μs

Package



8-Lead SOIC
IPS022G
(Dual)

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{\text{Ambient}} = 25^{\circ}\text{C}$ unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{\text{in, max}}$	Maximum IN current	-10	+10	mA	
$I_{\text{sd cont.}}$	Diode max. continuous current ⁽¹⁾ (ΣI_{sd} mosfets, $r_{\text{th}}=125^{\circ}\text{C/W}$)	—	1.4	A	
$I_{\text{sd pulsed}}$	Diode max. pulsed current ⁽¹⁾ (for ea. mosfet)	—	10		
P_{d}	Maximum power dissipation ⁽¹⁾ (ΣP_{d} mosfets, $r_{\text{th}}=125^{\circ}\text{C/W}$)	—	1	W	
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500 Ω ,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0 Ω , L=10 μH
$T_{\text{stor.}}$	Max. storage temperature	-55	150	$^{\circ}\text{C}$	
$T_{\text{J max.}}$	Max. junction temperature	-40	+150		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	100	—	$^{\circ}\text{C/W}$	
R_{th2} (1 mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	127	—		
R_{th3} (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	60	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V _{ds} (max)	Continuous drain to source voltage	—	35	V
V _{IH}	High level input voltage	4	6	
V _{IL}	Low level input voltage	0	0.5	
I _{ds}	Continuous drain current (T _{Ambient} = 85°C, I _N = 5V, r _{th} = 100°C/W, T _J = 85°C)	—	1	A
R _{in}	Recommended resistor in series with IN pin	0.5	5	kΩ
T _{r-in} (max)	Max recommended rise time for IN signal (see fig. 2)	—	1	μs
Fr-Isc ⁽²⁾	Max. frequency in short circuit condition (V _{cc} = 14V)	0	1	kHz

Static Electrical Characteristics

Standard footprint 70 μm copper thickness. (T_J = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R _{ds(on)}	ON state resistance T _J = 25°C T _J = 150°C	100 —	130 220	150 280	mΩ	V _{in} = 5V, I _{ds} = 1A
I _{dss 1}	Drain to source leakage current	0	0.01	25		V _{cc} = 14V, T _J = 25°C
I _{dss 2}	Drain to source leakage current	0	0.1	50	μA	V _{cc} = 40V, T _J = 25°C
V _{clamp 1}	Drain to source clamp voltage 1	48	54	56	V	I _d = 20mA (see Fig.3 & 4)
V _{clamp 2}	Drain to source clamp voltage 2	50	56	60		I _d =I _{shutdown} (see Fig.3 & 4)
V _{in clamp}	IN to source clamp voltage	7	8	9.5		I _{in} = 1 mA
V _{th}	IN threshold voltage	1	1.5	2		I _d = 50mA, V _{ds} = 14V
I _{in, -on}	ON state IN positive current	25	90	200	μA	V _{in} = 5V
I _{in, -off}	OFF state IN positive current	50	130	250		V _{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 10Ω, R_{input} = 50Ω, 100μs pulse, T_J = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T _{on}	Turn-on delay time	0.15	0.5	1	μs	See figure 2
T _r	Rise time	0.4	0.9	2		
T _{rf}	Time to 130% final R _{ds(on)}	2	6	12		
T _{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T _f	Fall time	0.5	1.3	2.5		
Q _{in}	Total gate charge	—	3.3	—	nC	V _{in} = 5V

(2) Operations at higher switching frequencies is possible. See Appl. notes.

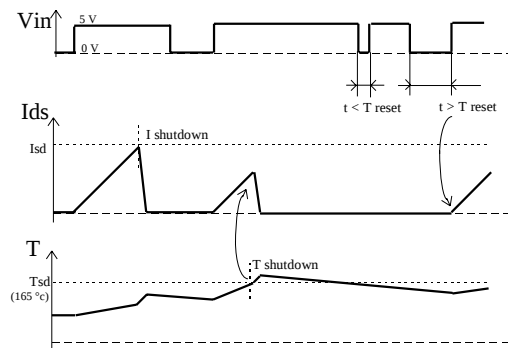


Figure 1 - Timing diagram

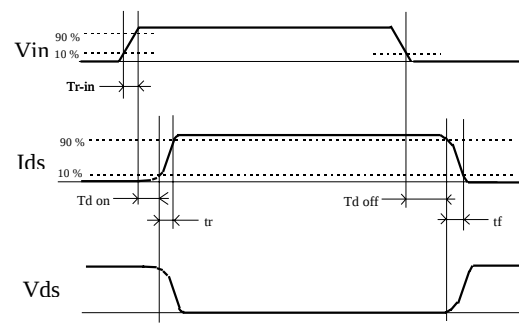


Figure 2 - IN rise time & switching time definitions

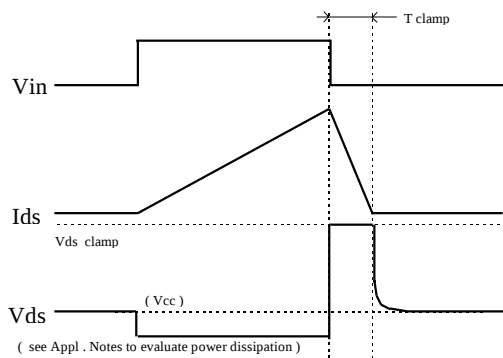


Figure 3 - Active clamp waveforms

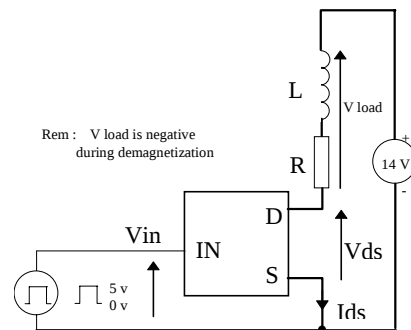


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

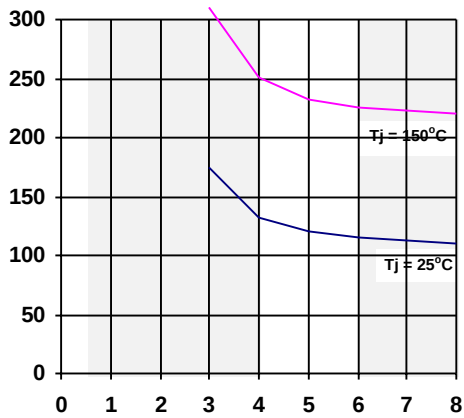


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

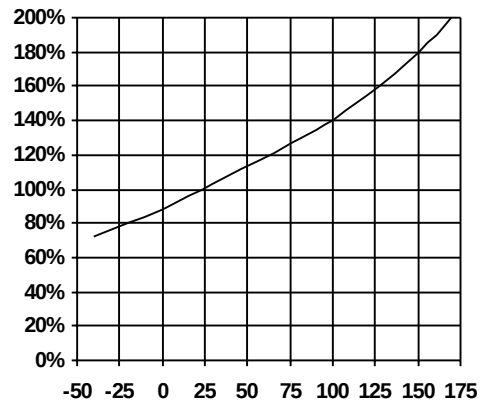


Figure 6 - Normalized Rds(on) (%) Vs Tj (°C)

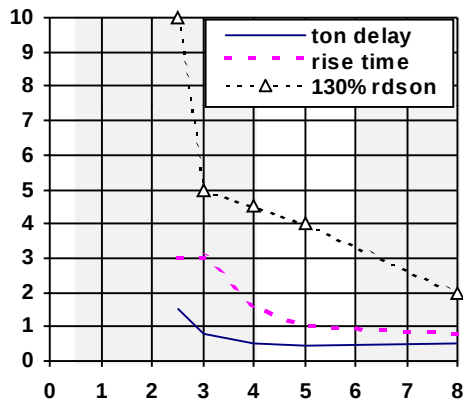


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs Input Voltage (V)

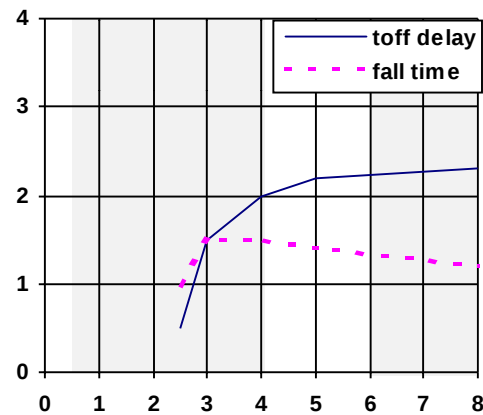


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

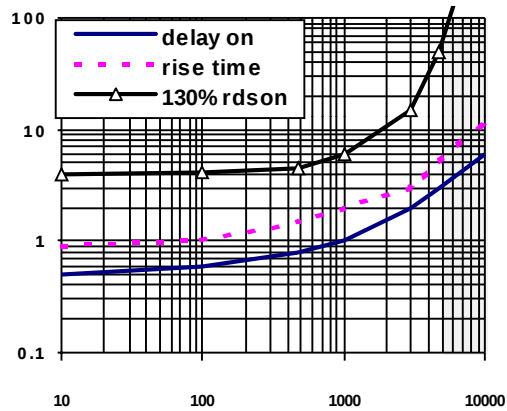


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{ds(on)}$ (us) Vs IN Resistor (Ω)

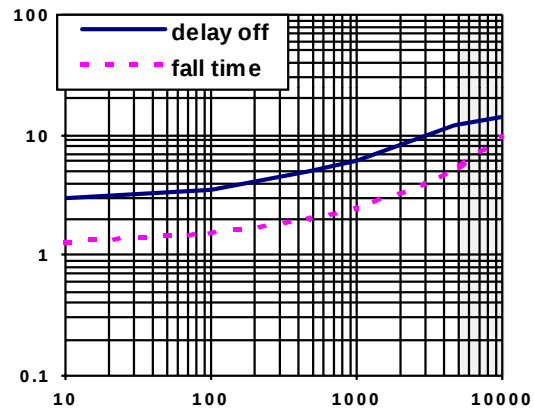


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

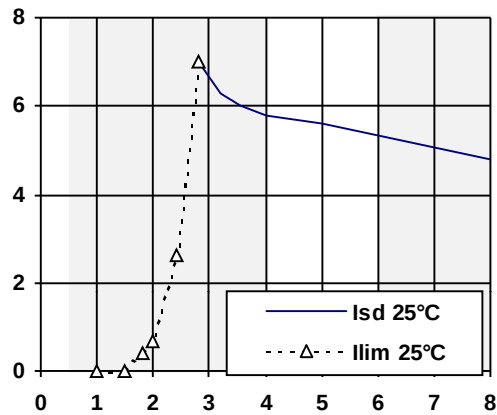


Figure 11 - Current lim. & I shutdown (A) Vs V_{in} (V)

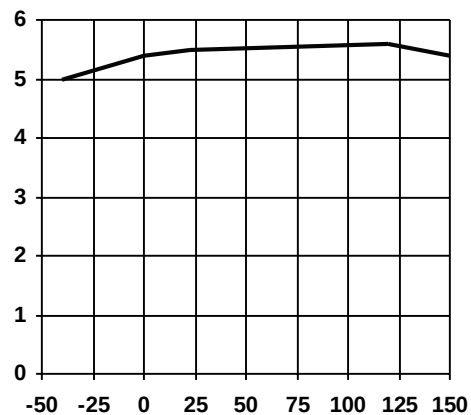


Figure 12 - I shutdown (A) Vs Temperature ($^{\circ}\text{C}$)

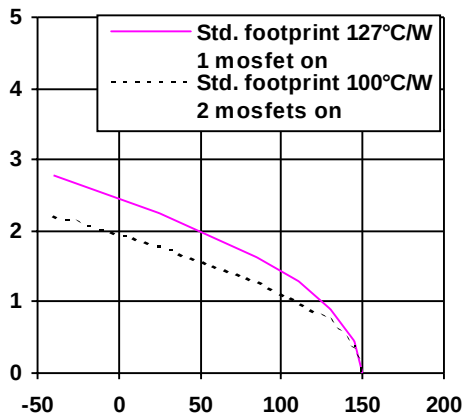


Figure 13 - Max.Cont. I_{ds} (A)
Vs Amb. Temperature ($^{\circ}\text{C}$)

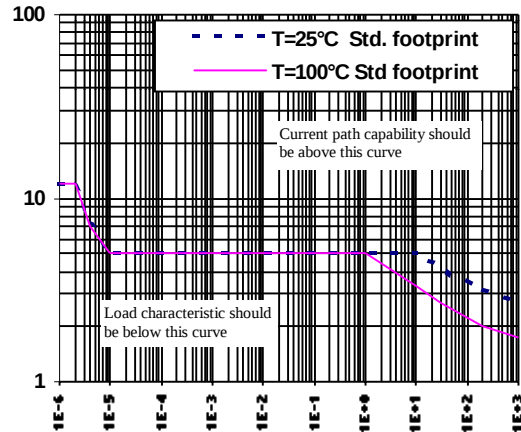


Figure 14 - I_{ds} (A) Vs Protection Resp. Time (s)

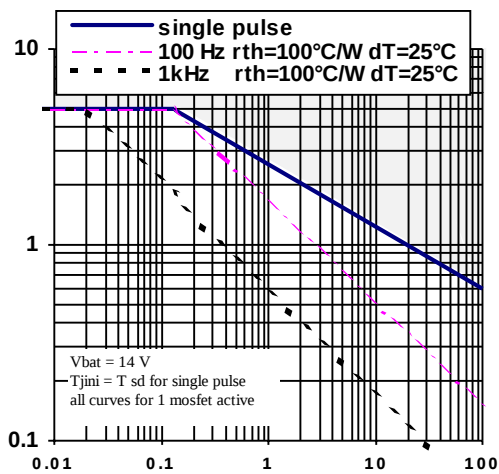


Figure 15 - I_{clamp} (A) Vs Inductive Load (mH)

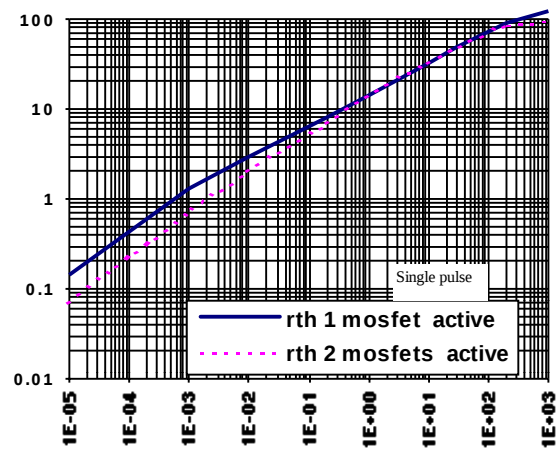


Figure 16 - Transient Thermal Imped. ($^{\circ}\text{C/W}$)
Vs Time (s)

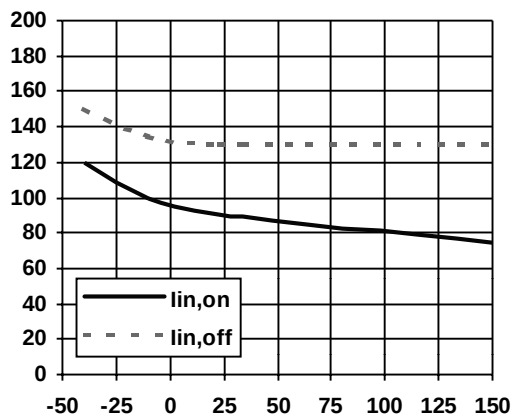


Figure 17 - Input Current (μA) Vs Junction Temperature ($^{\circ}\text{C}$)

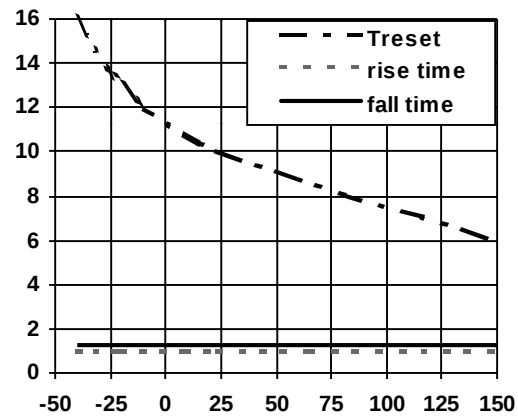


Figure 18 - Rise Time, Fall Time and Treset (μs) Vs T_j ($^{\circ}\text{C}$)

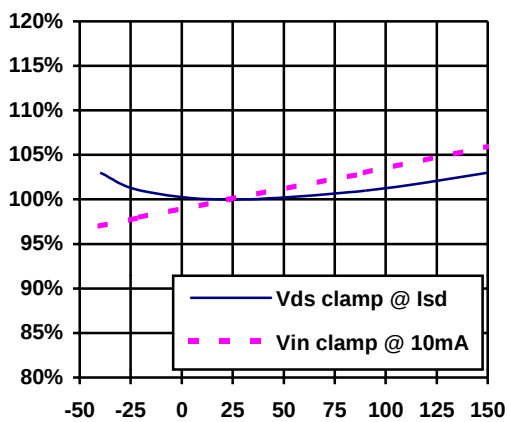
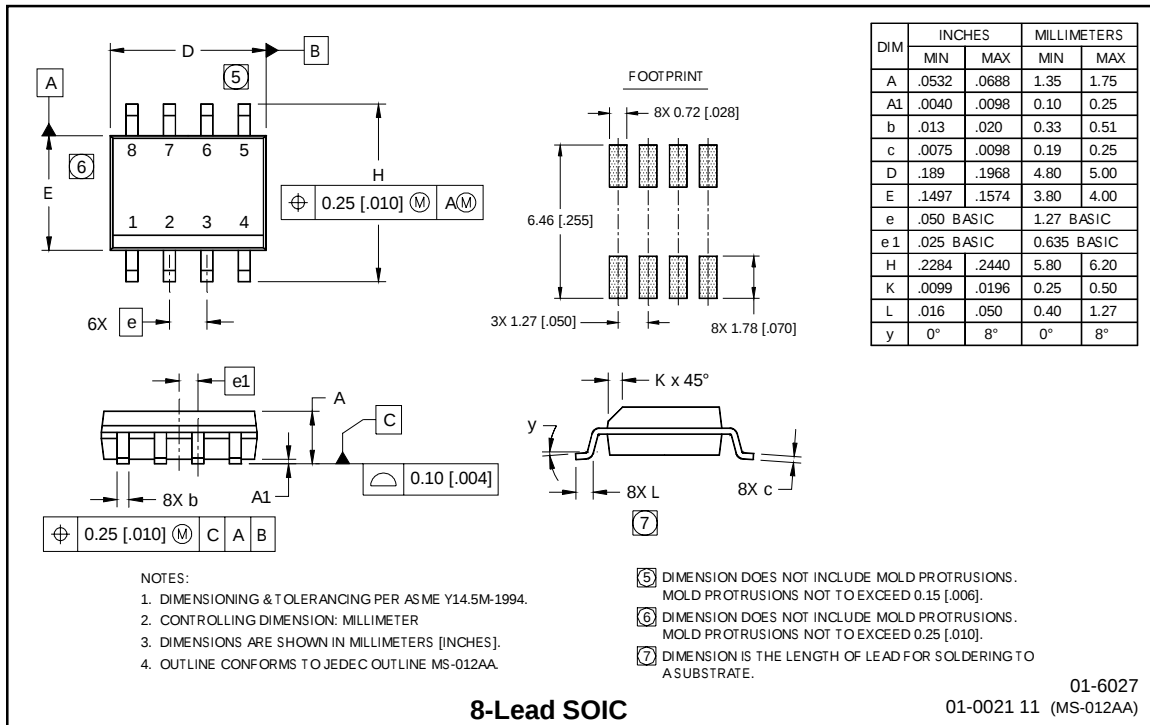


Figure 19 - Vin clamp and Vds clamp2 (%) Vs T_j ($^{\circ}\text{C}$)

Case Outline



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