◇PRODUCT　128 x 16 bit Electrically Erasable Programmable Rom

◇PART NUMBER　BR9020／F／FV／RFV／RFVM－W

◇DESCRIPTION

The BR9020-W series are serial EEPROMs that can be connected directly to a serial port and can be erased and written electrically. Writing and reading is perfomed in word units, using four types of operation commands. Communication occurs through $\overline{CS}$, $\overline{SK}$, DI, and DO pins, $\overline{WC}$ pin control is used to initiate a write disabled state, enabling these EEPROMs to be used as one-time ROMs. During writing, operation is checked via the internal status check.

◇APPLICATION　General Purpose

◇FEATURES

- 128words x 16 bit organization 2kbit serial EEPROM
- Single power supply
- Serial data I/O
- Self-timed programming cycle with auto-erase
- Low supply current
  - Active (5V); 2mA (max.)
  - Standby (5V); 3uA (max.) (CMOS INPUT)
- Noise filter on the $\overline{SK}$ pin
- Write protection when the supply is low
- Space Saving DIP8/SOP8/SSOP8/MSOP8pin Packages
- High reliability CMOS process
- 100,000 erase/write cycles endurance
- Provide 10 years of data retention
- Easy connection to serial port
- "FFFFh" stored in all address on shipped

◇ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Parameter	Symbol	Rating		Unit
Supply Voltage	VCC	−0.3～7.0		V
Power dissipation	Pd	DIP8	800(※1)	mW
		SOP8	450(※2)	
		SSOPB8	300(※3)	
		MSOP8	310(※4)	
Storage Temperature	Tstg	−65～125		℃
Operating Temperature	Topr	−40～85		℃
Terminal Voltage	−	−0.3～Vcc+0.3		V

※1 Degradation is done at 8.0mW/℃ for operation above Ta=25℃
※2 Degradation is done at 4.5mW/℃ for operation above Ta=25℃
※3 Degradation is done at 3.0mW/℃ for operation above Ta=25℃
※4 Degradation is done at 3.1mW/℃ for operation above Ta=25℃

◇RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	2.7～5.5(WRITE)	V
		2.7～5.5(READ)	
Input Voltage	Vin	0 ～ VCC	

◇ELECTRICAL CHARACTERISTICS

Unless otherwise specified(Ta=−40～85℃、VCC=2. 7～5. 5V)

Parameter	Symbol	Limit			Unit	Condition	Test Circuit
		Min.	Typ.	Max.			
Input Low Voltage 1	VIL1	—	—	0.3x VCC	V	DI Pin	
Input High Voltage 1	VIH1	0.7x VCC	—	—	V	DI Pin	
Input Low Voltage 2	VIL2	—	—	0.2x VCC	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin	
Input High Voltage 2	VIH2	0.8x VCC	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin	
Output Low Voltage	VOL	0	—	0.4	V	IOL=2.1mA	Fig.-4
Output High Voltage	VOH	VCC-0.4	—	VCC	V	IOH=-0.4mA	Fig.-5
Input Leakage Current	ILI	-1	—	1	μA	VIN=0V～VCC	Fig.-6
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0V～VCC,$\overline{CS}$ =VCC	Fig.-7
Operating Current	ICC1	—	—	2	mA	fSK=2MHz,tE/W=10ms (WRITE)	Fig.-8
	ICC2	—	—	1	mA	fSK=2MHz (READ)	Fig.-8
Standby Current	ISB	—	—	3	μA	$\overline{CS}$,$\overline{SK}$,DI,$\overline{WC}$=VCC DO,R/$\overline{B}$=OPEN	Fig.-9
Clock Frequency	fSK	—	—	2	MHz		

Unless otherwise specified (Ta=−40～85℃, VCC=2.7～3.3V)

Parameter	Symbol	Limit			Unit	Condition	Test Circuit
		Min.	Typ.	Max.			
Input Low Voltage 1	VIL1	—	—	0.3x VCC	V	DI Pin	
Input High Voltage 1	VIH1	0.7x VCC	—	—	V	DI Pin	
Input Low Voltage 2	VIL2	—	—	0.2x VCC	V	$\overline{CS}$, SK, $\overline{WC}$ Pin	
Input High Voltage 2	VIH2	0.8x VCC	—	—	V	$\overline{CS}$, SK, $\overline{WC}$ Pin	
Output Low Voltage	VOL	0	—	0.4	V	IOL=100uA	Fig.-4
Output High Voltage	VOH	VCC-0.4	—	VCC	V	IOH=-100uA	Fig.-5
Input Leakage Current	ILI	-1	—	1	μA	VIN=0～VCC	Fig.-6
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0～VCC,$\overline{CS}$=VCC	Fig.-7
Operating Current	ICC1	—	—	1.5	mA	fSK=2MHz,tE/W=10ms (WRITE)	Fig.-8
	ICC2	—	—	0.5	mA	fSK=2MHz (READ)	Fig.-8
Standby Current	ISB	—	—	2	μA	$\overline{CS}$,SK,DI,$\overline{WC}$=VCC DO,R/B=OPEN	Fig.-9
Clock Frequency	fSK	—	—	2	MHz		

○This product is not designed for protection against radioactive rays.

◇DIMENSION

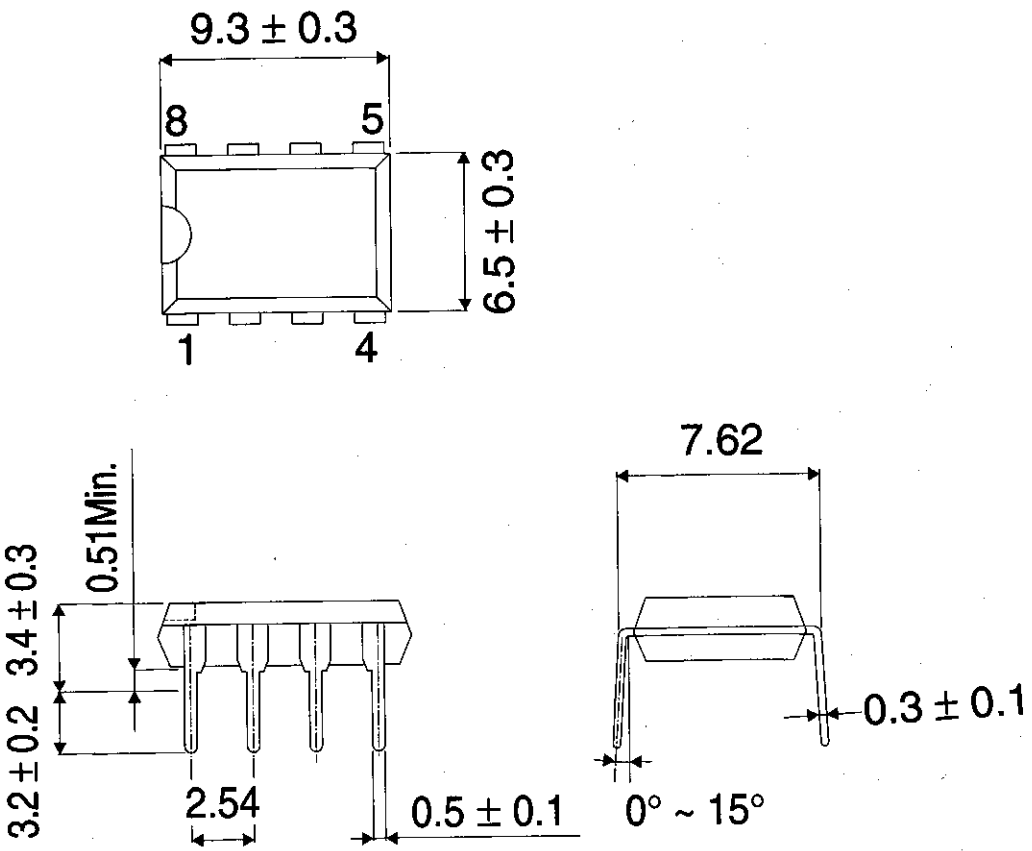


Fig.1-1 Outline Dimensions DIP8(BR9020-W)

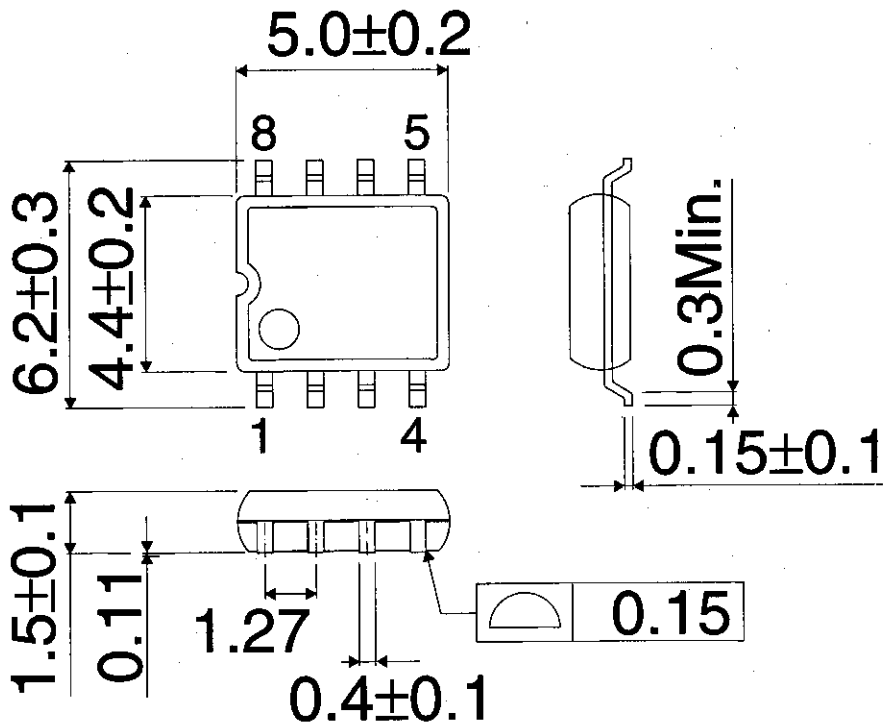


Fig.1-2 Outline Dimensions SOP8(BR9020F-W)

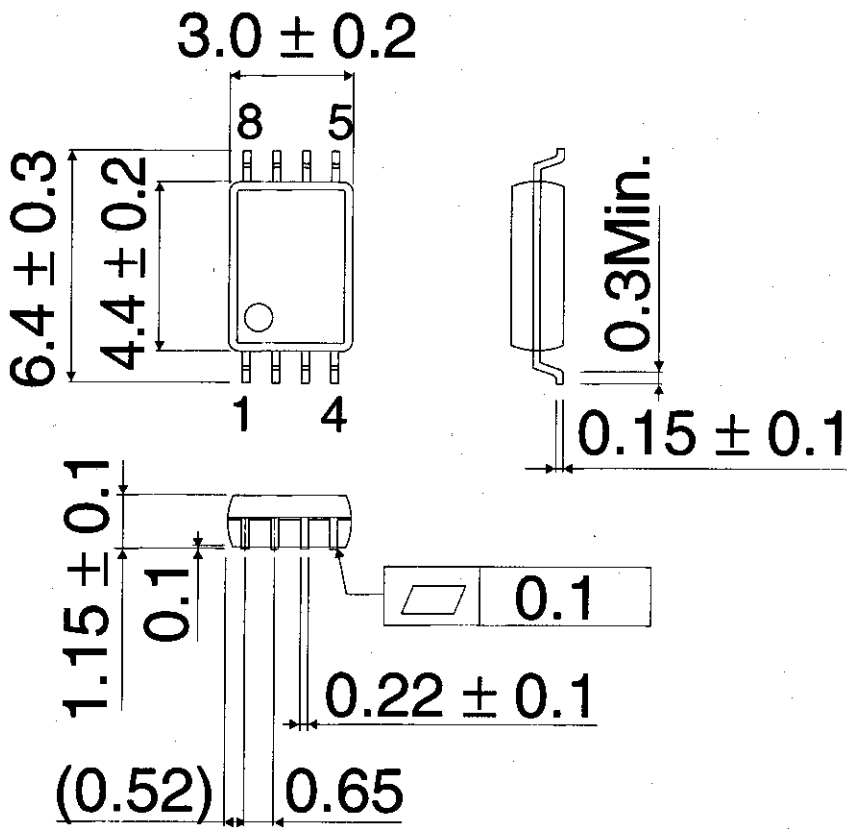


Fig.1-3 Outline Dimensions SSOPB8(BR9020RFV-W)

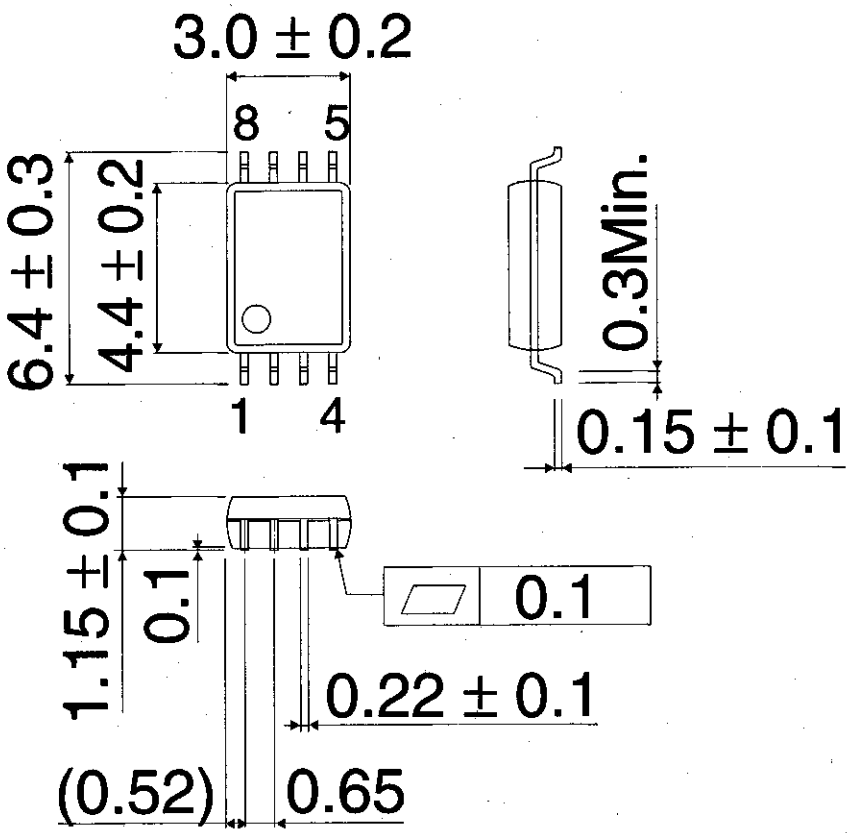


Fig.1-4 Outline Dimensions SSOPB8(BR9020FV-W)

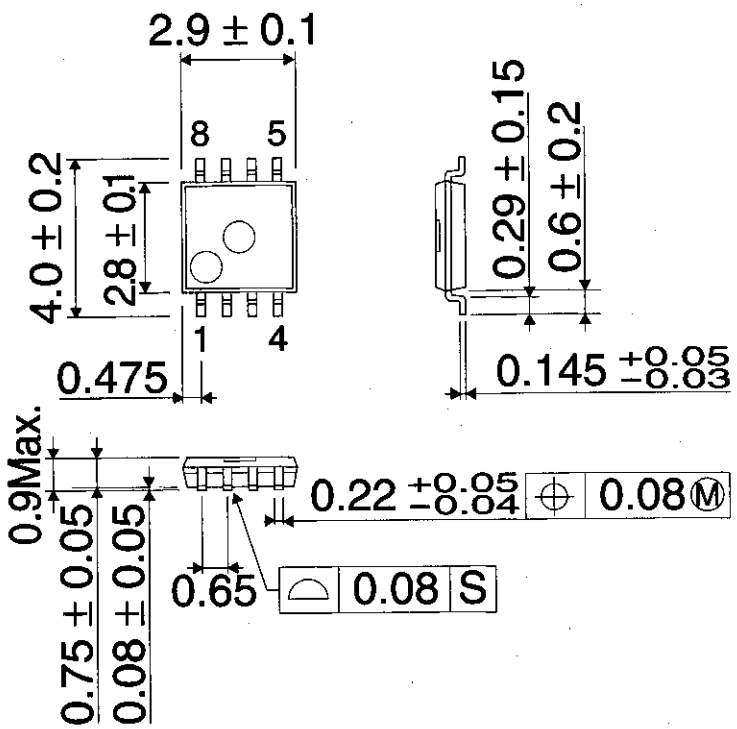


Fig.1-5 Outline Dimensions MSOP8(BR9020RFVM-W)

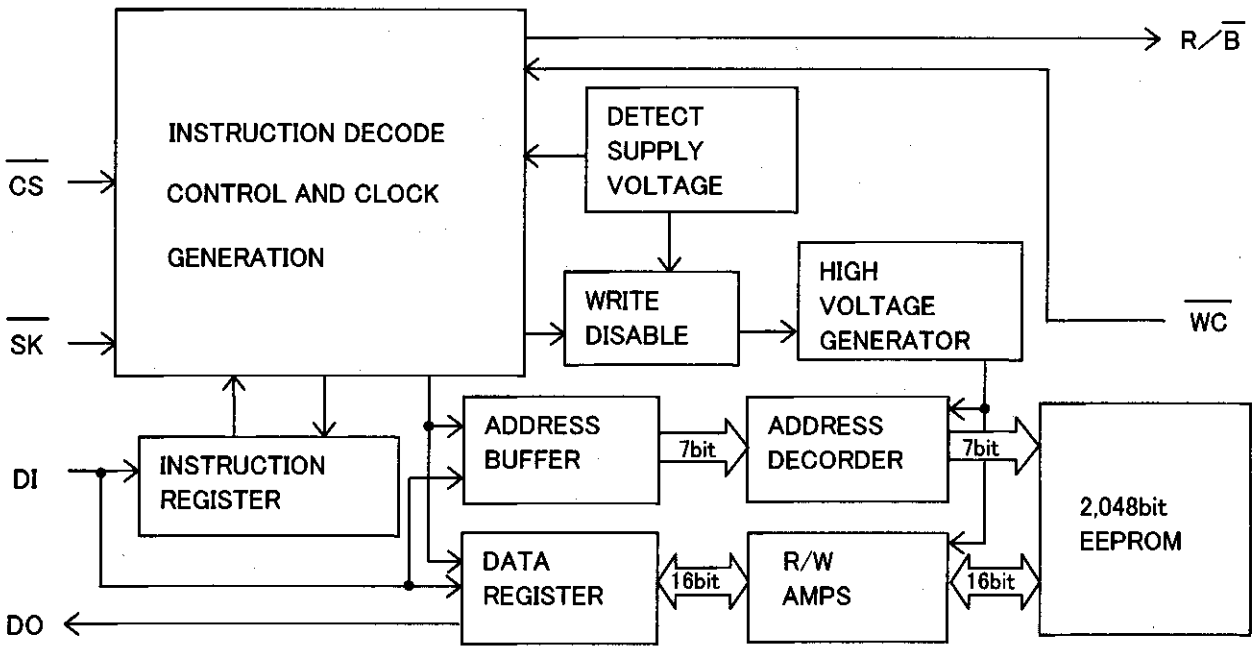
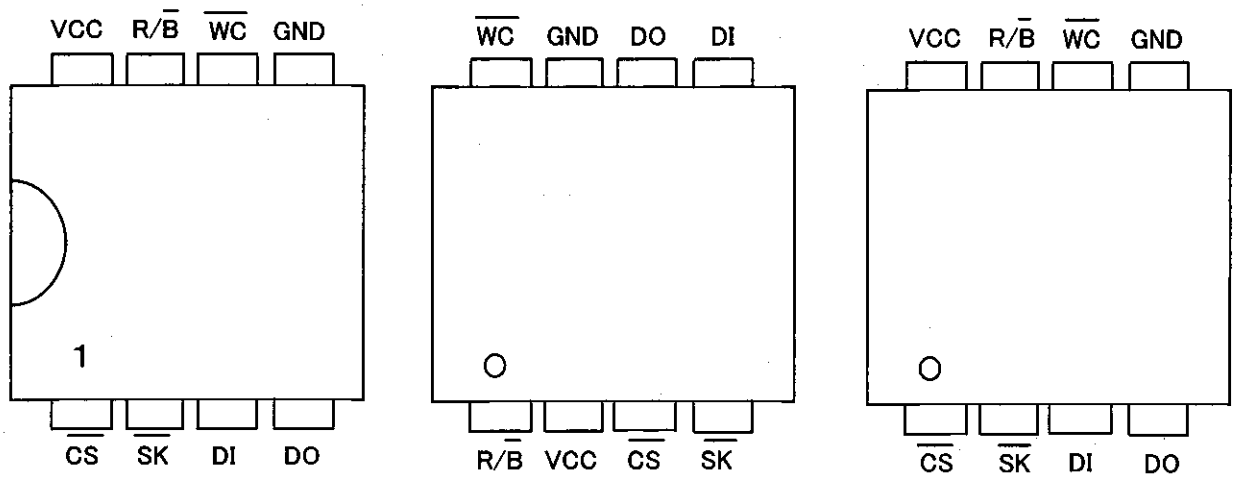


Fig.-2 Block Diagram

◇PIN CONFIGURATIONS



BR9020−W:DIP8

BR9020FV−W:SSOP8
BR9020F−W:SOP8

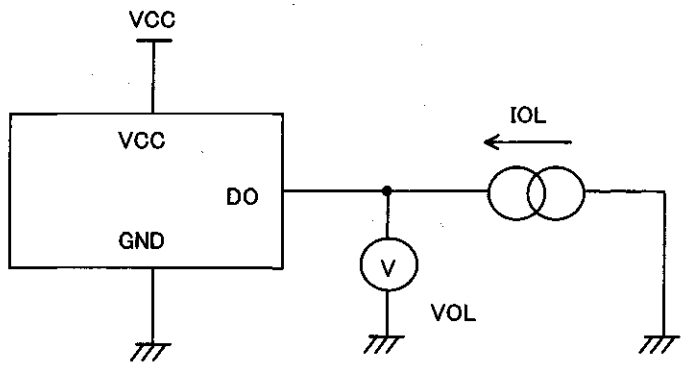
BR9020RFVM−W:MSOP8
BR9020RFV−W:SSOP8

Fig.-3 Pin Configurations

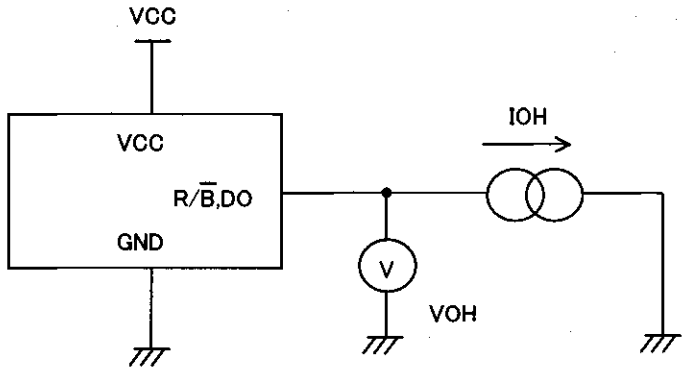
◇TERMINAL FUNCTION

Terminal	IN/OUT	Function
VCC	−	Power Supply
GND	−	Ground (0V)
$\overline{CS}$	INPUT	Chip Select Input
$\overline{SK}$	INPUT	Serial Data Clock Input
DI	INPUT	Serial Data Input (Op code, address)
DO	OUTPUT	Serial Data Output
$\overline{WC}$	INPUT	Write Control Input
R/$\overline{B}$	OUTPUT	READY/$\overline{BUSY}$ Status Output

◇TEST CIRCUIT



Set Output Pin to Low
Fig.-4 Output Low voltage test circuit



Set Output Pin to High
Fig.-5 Output High voltage test circuit

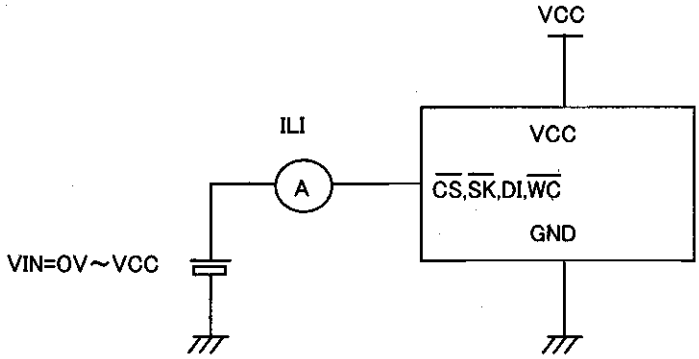


Fig.-6 Input leakage current test circuit

◇TEST CIRCUIT

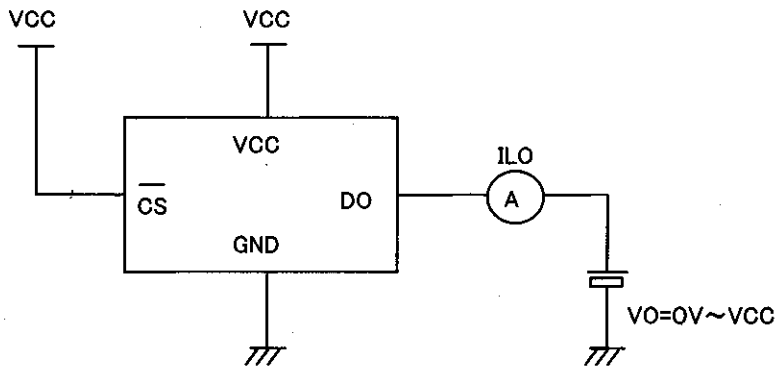


Fig.-7 Output leakage current test circuit

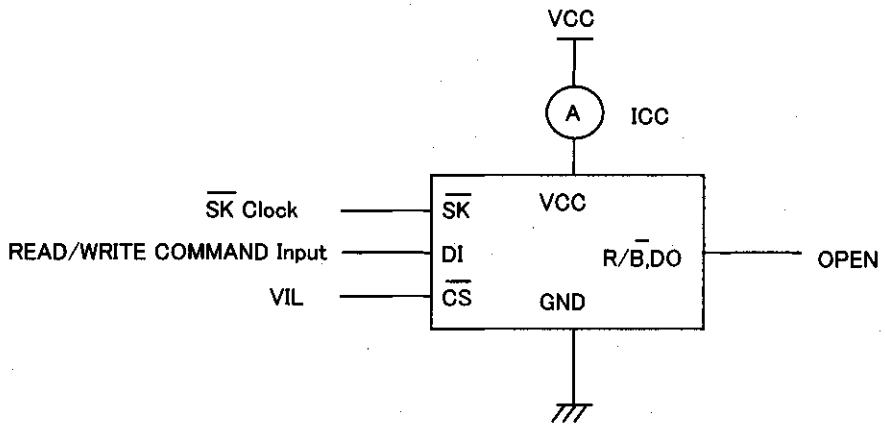


Fig.-8 Operating Current test circuit

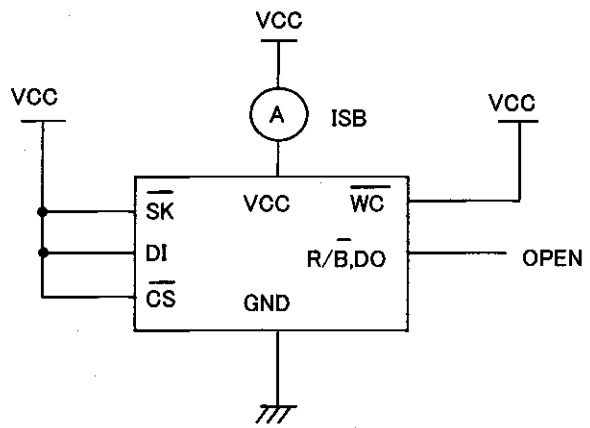


Fig.-9 Standby current test circuit

◇INSTRUCTION CODE

Instruction	Start Bit	Op Code	Address	Data
READ	1010	1000	A0 A1 A2 A3 A4 A5 A6 0	D0 D1 - D14 D15 (READ DATA)
WRITE	1010	0100	A0 A1 A2 A3 A4 A5 A6 0	D0 D1 - D14 D15 (WRITE DATA)
Write Enable(WEN)	1010	0011	* * * * * * * *	
Write Disable(WDS)	1010	0000	* * * * * * * *	

Address and data must be transferred from LSB.
"*" Means either VIH or VIL

◇SYNCHRONOUS DATA INPUT OUTPUT TIMING

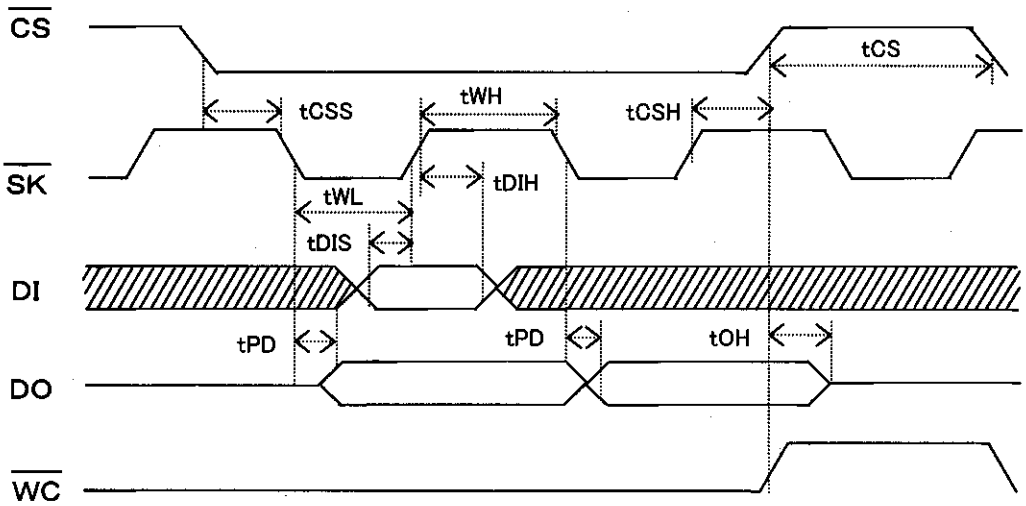


Fig.-10 Synchronous data input output timing

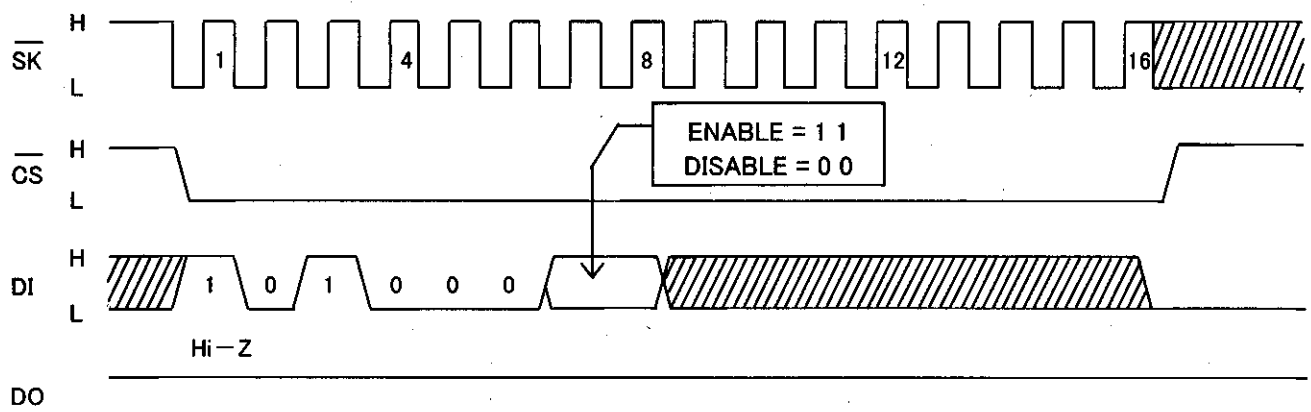
○Input Data is clocked into the DI pin on the rising edge of the clock $\overline{SK}$.
○Output data is clocked out on the falling edge of the $\overline{SK}$ clock.
○The $\overline{WC}$ pin does not have any affect on the READ, WEN and WDS operations.
○Between instructions, $\overline{CS}$ must be brought High for greater than the minimum of tCS.
If $\overline{CS}$ is maintained Low, the next instruction isn't detected.

◇AC OPERATION CHARACTERISTICS(Ta=−40~85℃、VCC=2. 7~5. 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Chip Select Setup Time	tCSS	100	—	—	ns
Chip Select Hold Time	tCSH	100	—	—	ns
Data In Setup Time	tDIS	100	—	—	ns
Data In Hold Time	tDIH	100	—	—	ns
Delay to Output High	tPD1	—	—	150	ns
Delay to Output Low	tPD0	—	—	150	ns
Self-Timed Program Cycle	tE/W	—	—	10	ms
Minimum Chip Select High Time	tCS	250	—	—	ns
Data Output Disable Time (From $\overline{CS}$)	tOH	0	—	150	ns
Clock High Time	tWH	230	—	—	ns
Clock Low Time	tWL	230	—	—	ns
Write Control Setup Time	tWCS	0	—	—	ns
Write Control Hold Time	tWCH	0	—	—	ns
Clock High to Output READY/$\overline{BUSY}$ Status	tSV	—	—	150	ns

◇TIMING CHART

1. WRITE Enable/Disable



R/$\overline{B}$ H

$\overline{WC}$ H or L

Fig.-11 WRITE Enable and Disable Cycle Timing

○When power is first applied, the device has been held in a reset status, with respect to the write enable, in the same way the write disable (WDS) instruction is executed. Before the write instruction is executed, the device must be received the write enable (WEN) instruction. Once the device is done, the device remains programmable until the write disable (WDS) instruction is executed or the supply is removed from the device.

○It is unnecessary to add the clock after 16th clock. If the device is recieved the clock, the device ignores the clock.

○As both of the enable and disable instructions don't depend on the status of the $\overline{WC}$ pin, the state of $\overline{WC}$ isn't cared during the instruction.

○The instruction is recognized after the rising edge of 8th clock for the address following 8clocks for the opcode, but the specified address isn't cared during the instructions.

2. READ INSTRUCTION

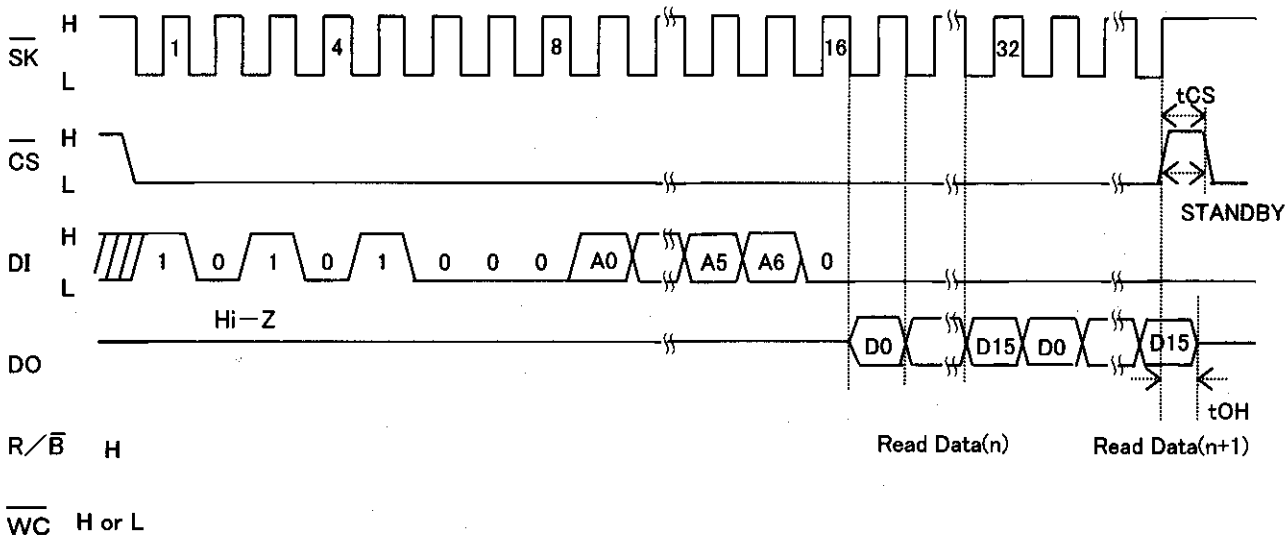


Fig.-12 READ Cycle Timing

○On the falling edge of 16th clock, the data stored in the specified address (n) is clocked out of the DO pin.
The output DO is toggled after the internal propagation tPD0 or tPD1 on the falling edge of SK. During tPD0 or tPD1, the data is the previous data or unstable, and to take in the data, tPD is needed.(Refer to Fig.-10 Synchronous data input output timing.)

○The data stored in the next address is clocked out of the device on the falling edge of 32nd clock. The data stored in the upper address every 16 clocks is output sequentially by the continual SK input. Also the read operation is reset by CS High.

3. WRITE INSTRUCTION

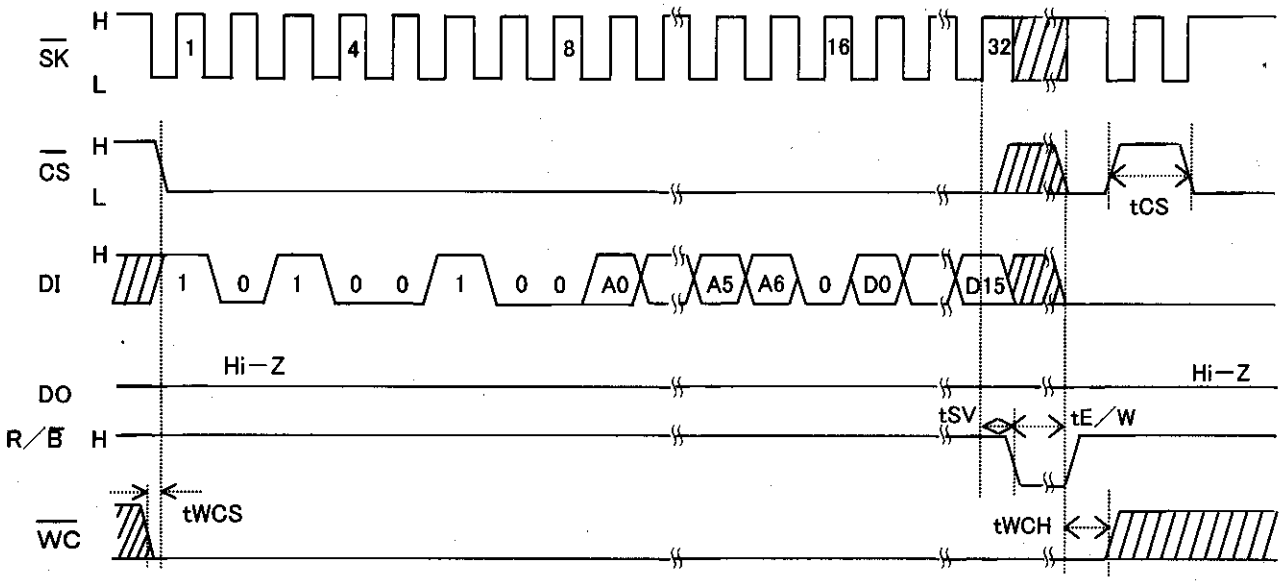


Fig.-13 WRITE Cycle Timing

- ○During the write instruction, $\overline{CS}$ must be brought Low. However once the write operation started, $\overline{CS}$ may be either High or Low. But in the case of connecting the $\overline{WC}$ pin to the $\overline{CS}$ pin, $\overline{CS}$ and $\overline{WC}$ must be brought Low during programming cycle. (If the $\overline{WC}$ pin is brought High during the write cycle, the write operation is halted. In that case, the data of the specified address is not guaranteed. It is necessary to rewrite it.)
- ○After the R/$\overline{B}$ pin changed Busy to Ready, once $\overline{CS}$ is brought High, then $\overline{CS}$ keep Low, which means the status of being able to accept an instruction. The device can take in the input from $\overline{SK}$ and DI, but in the case of keeping $\overline{CS}$ Low without being brought High once, the input is canceled until being $\overline{CS}$ High once.
- ○At the rising edge of 32nd clock, the R/$\overline{B}$ pin will be driven Low after the specified time delay(tSV).
- ○During programming, R/$\overline{B}$ is tied to Low by the device (On the rising edge of $\overline{SK}$ taken in the last data (D15), internal timer starts and automatically finished after the data of memory cell is written spending tE/W. $\overline{SK}$ could be either High or Low at the time.
- ○After input write instruction, also the DO pin will be able to show the status of R/$\overline{B}$, in the case that $\overline{CS}$ is falling from High to Low while $\overline{SK}$ is tied to Low. (Refer to READY/$\overline{BUSY}$ STATUS in the next page.)

◇READY/$\overline{\text{BUSY}}$ STATUS (on the R/$\overline{\text{B}}$ pin, the DO pin)

・The DO pin outputs the READY/$\overline{\text{BUSY}}$ status of the internal part, which shows whether the device is ready to receive the next instruction or not. (High or Low)
After the write instruction is completed, if $\overline{\text{CS}}$ is brought from high to low while $\overline{\text{SK}}$ is Low, the DO pin outputs the internal status.(The R/$\overline{\text{B}}$ pin may be no connection.)
When written to the memory cell, R/$\overline{\text{B}}$ status is output after tSV spent from the rising edge of 32th clock on $\overline{\text{SK}}$.

R/$\overline{\text{B}}$ =Low : under writing
After spending tE/W operating the internal timer, the device automatically finishes writing.
During tE/W, the memory array is accessed and any instruction is not received.

R/$\overline{\text{B}}$ =High : ready
Auto programming has been completed. The device is ready to receive the next Instruction.

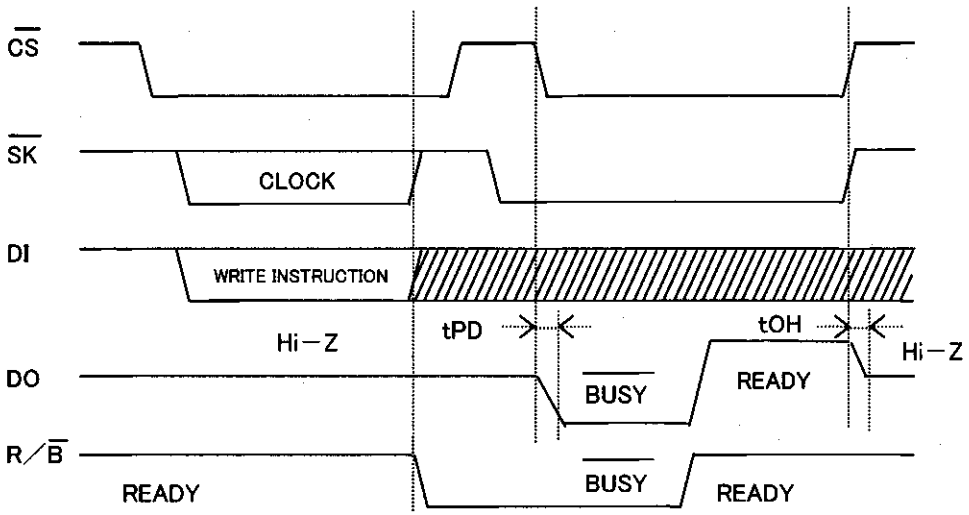


Fig.-14 READY/$\overline{\text{BUSY}}$ Status Output timing

◇About the direct connection between the DI and DO pins
The device can be used with the DI pin connected to the DO pin directly.
But when the READY/$\overline{\text{BUSY}}$ status is output, be careful about the bus conflict on the port of the controller.

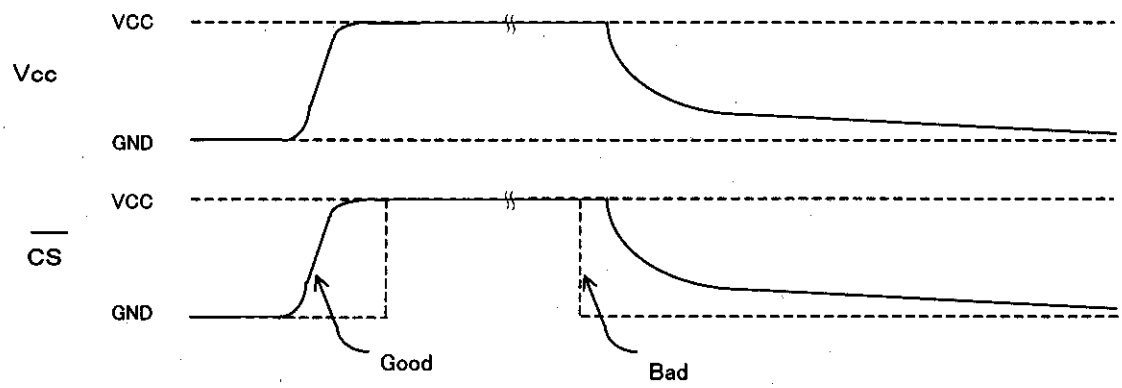
●ATTENTION TO USE

1. Power ON/OFF

- The $\overline{CS}$ is brought High during power-up and power-down.
- This device is in active state while $\overline{CS}$ is Low.
- The extraordinary function or data collapse may occur in that condition because of noise etc., if power-up and power-down is done with $\overline{CS}$ brought Low.
  In order to prevent above errors from happening, keep $\overline{CS}$ High during power-up and power-down.

(Good example) $\overline{CS}$ is brought High during power-up and power-down.
Please take more than 10ms between power-up and power-off, or the internal circuit is not always reset.

(Bad example) $\overline{CS}$ is brought Low during power-up and power-down.
The $\overline{CS}$ pin is always Low in this case, the noise may force the device to make malfunction or inadvertent write.
※ It sometimes occurs in the case that the $\overline{CS}$ pin is Hi-Z.



2. NOISE REJECTION

2-1 $\overline{SK}$ NOISE

If $\overline{SK}$ line has a lot of noise for rising time of $\overline{SK}$, the device may recognize the noise as a clock and then clock will be shifted.

2-2 $\overline{WC}$ NOISE

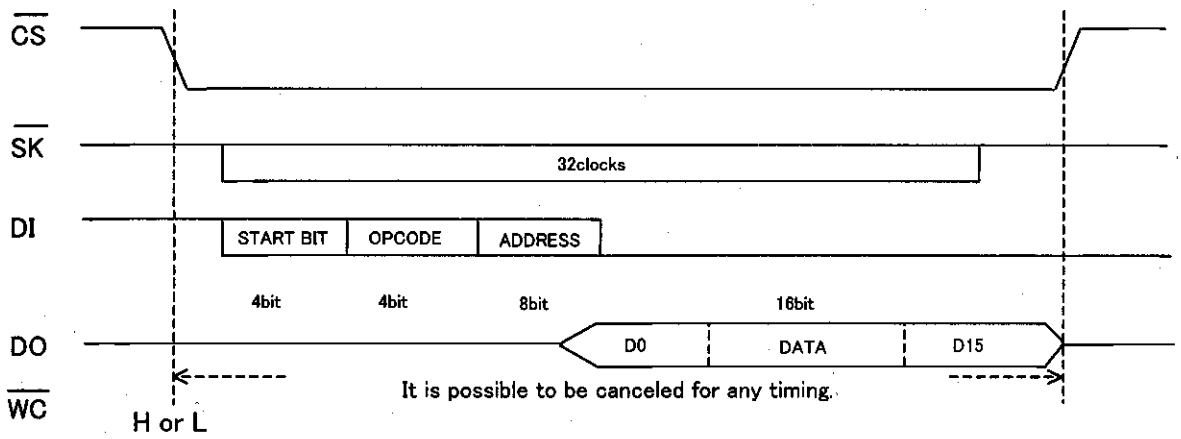
If $\overline{WC}$ line has noise during write cycle(tE/W), there may be a chance to deny the programming.

2-3 VCC NOISE

It recommended that capacitor is put between VCC and GND to prevent these case, since it is possible to occur malfunction by the effect of noise or surge on power line.

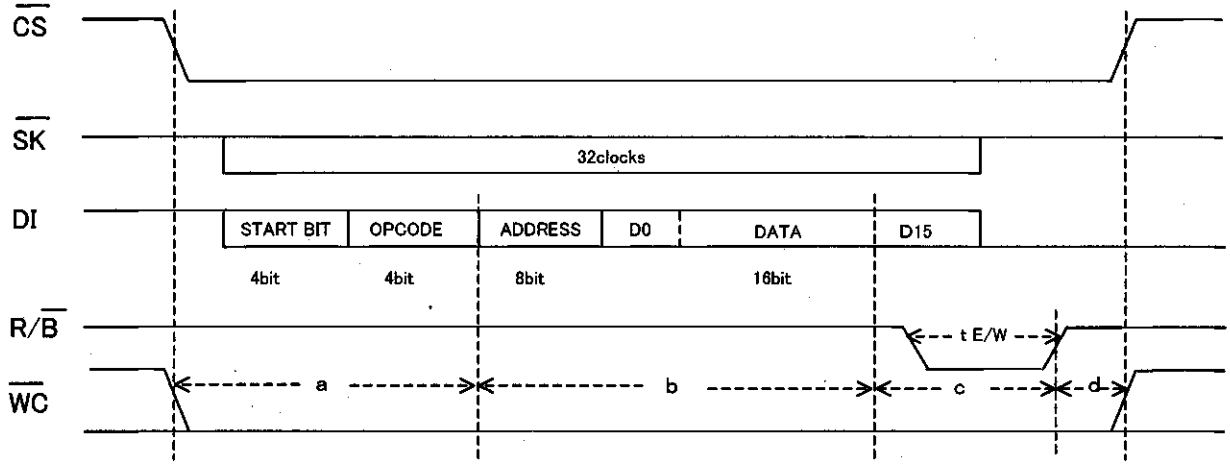
3. INSTRUCTION MODE CANCEL

3−1. READ instruction



How to cancel : $\overline{CS}$ is brought High.

3−2. Write instruction



How to cancel

a : $\overline{CS}$ is brought High to cancel the instruction, and $\overline{WC}$ may be either High or Low.

b : In case that $\overline{WC}$ is brought High for a moment, or $\overline{CS}$ is brought High, the write instruction is canceled, the data of the specified address is not changed.

c : When $\overline{WC}$ is brought High, or the device is powered down (But the latter way is not recommended), the instruction is canceled but the specified data is not guaranteed. Send the instruction again.

d : When $\overline{CS}$ is brought High during R/$\overline{B}$ High, the device is reset and ready to receive a next instruction.

NOTE : The document may be strategic technical data subject to COCOM regulations.