PRELIMINARY

CY62256V25

32K x 8 2.5V Static RAM

Features

- **Single 2.5V power supply**
- **Ideal for low-voltage and low-power cache memory applications**
- **70ns Access time**
- **Low active power**
- **81 mW**
- **Low CMOS standby power**
- **54 uW, f=fmax**
- **Low-power alpha immune 6T cell**
- **Plastic SOIC and TSOP packaging**

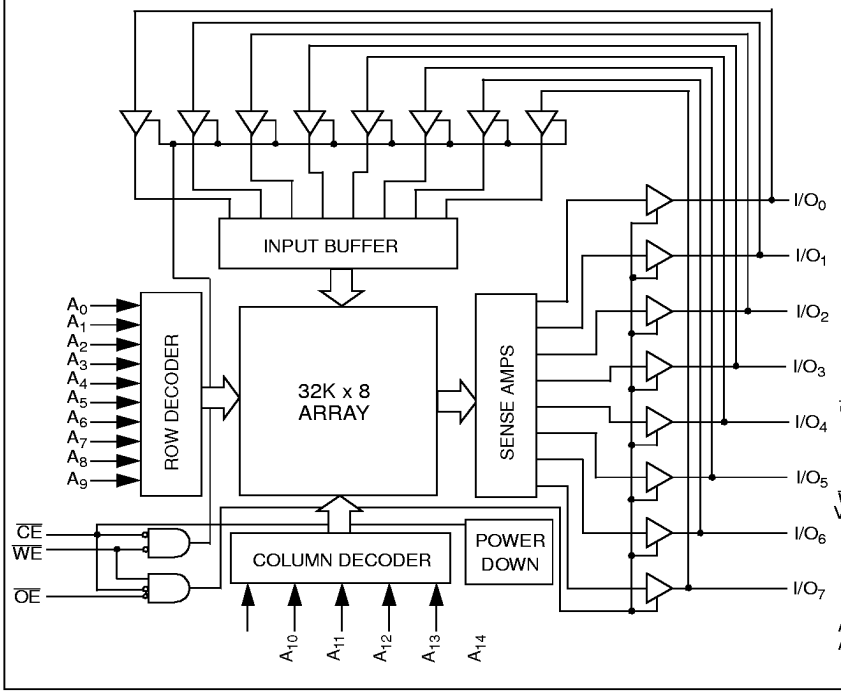
Functional Description

The CY62256V25 is a high-performance 2.5V CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 98% when deselected.

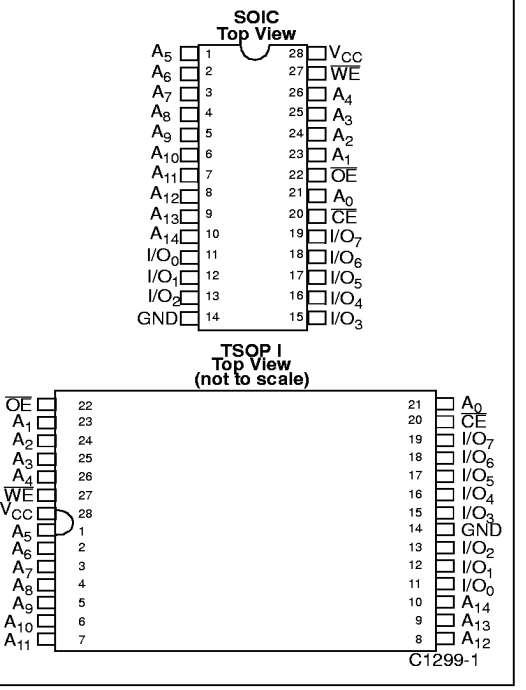
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. The CY62256V25 is available in standard 450-mil wide (300-mil body width) SOIC and 28 pin TSOP type I packages.

Logic Block Diagram



Pin Configurations



Selection Guide

		62256V25-70
Maximum Access Time (ns)		70
Maximum Operating Current (mA)		30
Maximum CMOS Standby Current (μA)		100
	L	20
	LL	5

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND.....–0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1].....–0.5 to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.5V ± 200mV

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62256V25-70 Min.	CY62256V25-70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA, $V_I = V_{IH}$ or V_{IL}		2.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 1.0 mA, $V_I = V_{IH}$ or V_{IL}			0.4	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH}$ (min)		1.7	V_{CC}+0.3V	V
V_{IL}	Input LOW Voltage			–0.3	0.7	V
I_{IX}	Input Load Current			–1	+1	µA
I_{OZ}	Output Leakage Current	GND < V_I < V_{CC}, Output Disabled		–5	+5	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			–300	mA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., I_{OUT} = 0mA, f = f_{MAX} = $1/t_{RC}$			30	mA
			L		30	mA
			LL		30	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$, or $V_{IN} \leq V_{IL}$, f = f_{MAX}			5	mA
			L		3	mA
			LL		1	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE} > V_{CC} – 0.2V$, $V_{IN} > V_{CC} – 0.2V$, or $V_{IN} < 0.2V$, $\overline{WE} > V_{CC} – 0.2V$ or $\overline{WE} < 0.2V$, f = f_{MAX}			100	µA
			L		20	µA
			LL		5	µA

Shaded area contains preliminary information.

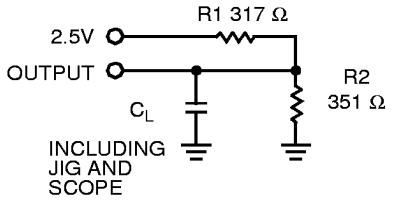
Capacitance[3]

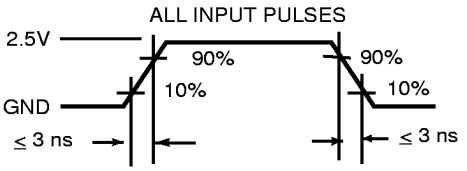
Parameter	Description	Test Conditions	Max	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25C, f = 1MHz, V_{CC} = 2.5V	5	pF
C_{IN}: Controls			6	pF
C_{OUT}	Output Capacitance		6	pF

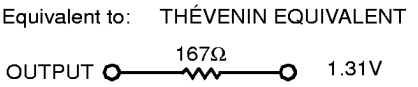
Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds..
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms







Switching Characteristics Over the Operating Range[4]

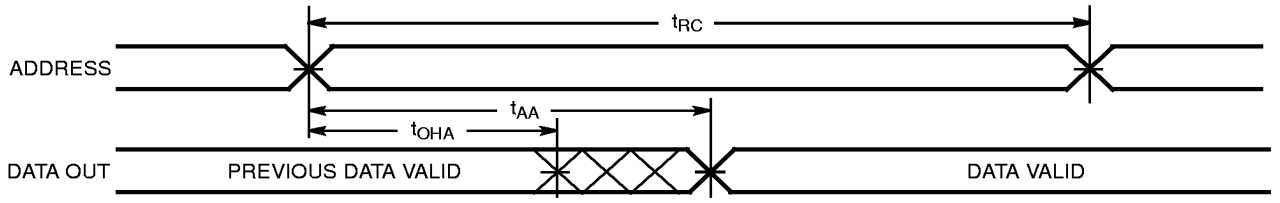
Parameter	Description	CY62256V25-70		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[5]	3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5,6]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[5]	3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5,6]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		70	ns
WRITE CYCLE[7,8]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5,6]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	3		ns

Notes:

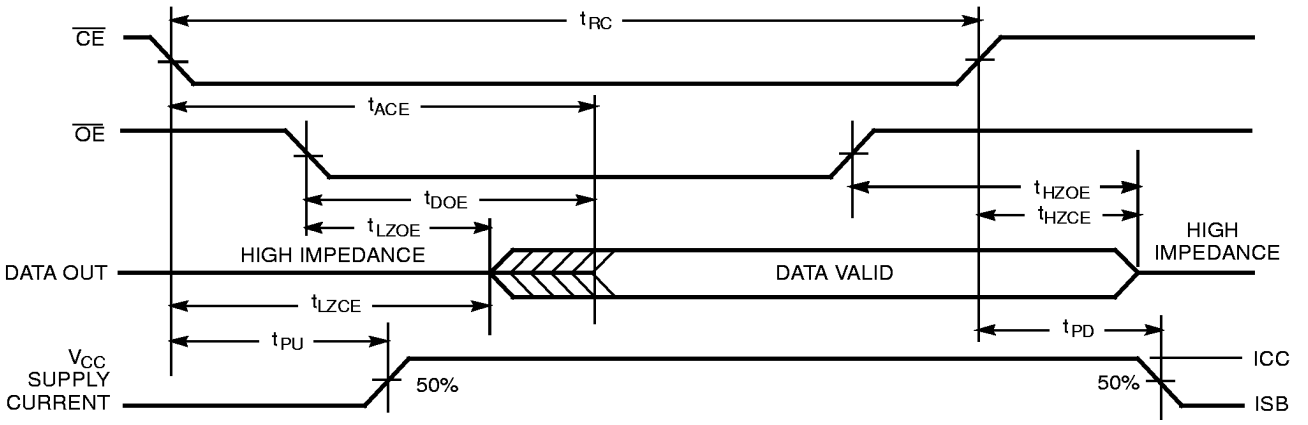
4. Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{SA}, t_{HZWE}, t_{SD} and t_{HD} and never less than t_{WC}

Switching Waveforms

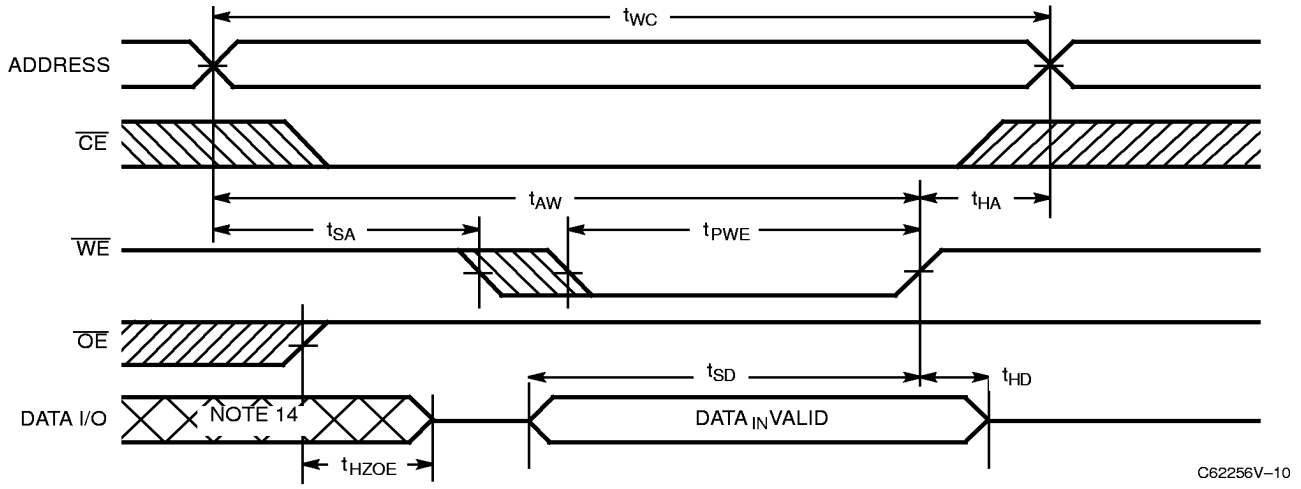
Read Cycle No.1 [9, 10]



Read Cycle No. 2 [10, 11]



Write Cycle No. 1 (WE Controlled) [7, 12, 13]

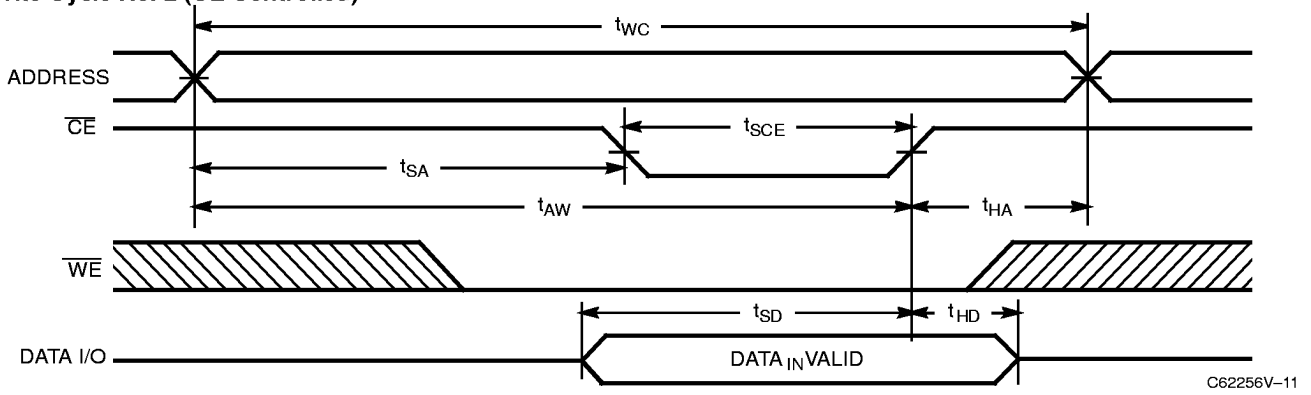


Notes:

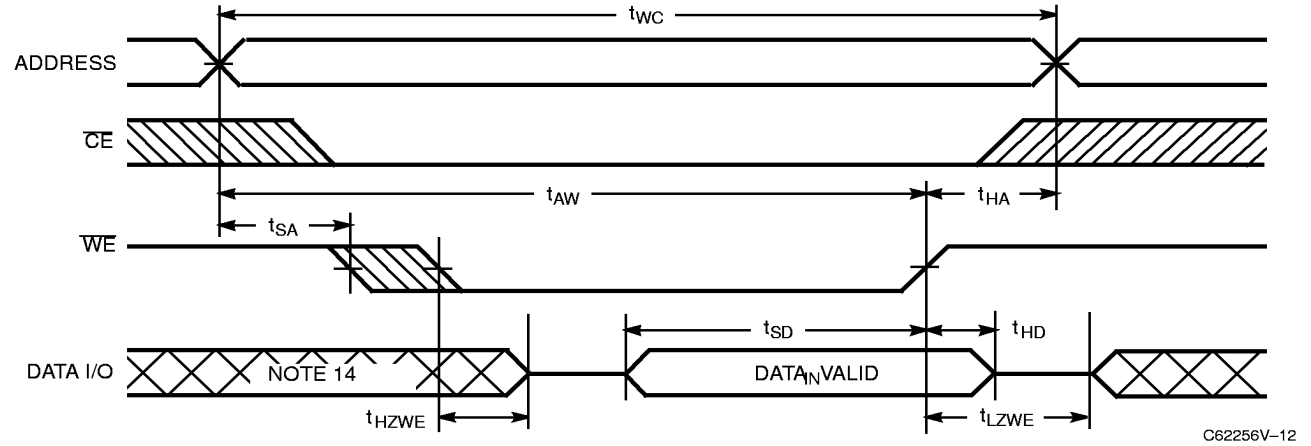
9. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
14. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [7, 12, 13]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [8, 13]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Read, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62256V25-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
70	CY62256V25L-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
70	CY62256V25LL-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
70	CY62256V25-70ZC	Z28	28-Lead Thin Small Outline Package	Commercial
70	CY62256V25L-70ZC	Z28	28-Lead Thin Small Outline Package	Commercial
70	CY62256V25LL-70ZC	Z28	28-Lead Thin Small Outline Package	Commercial

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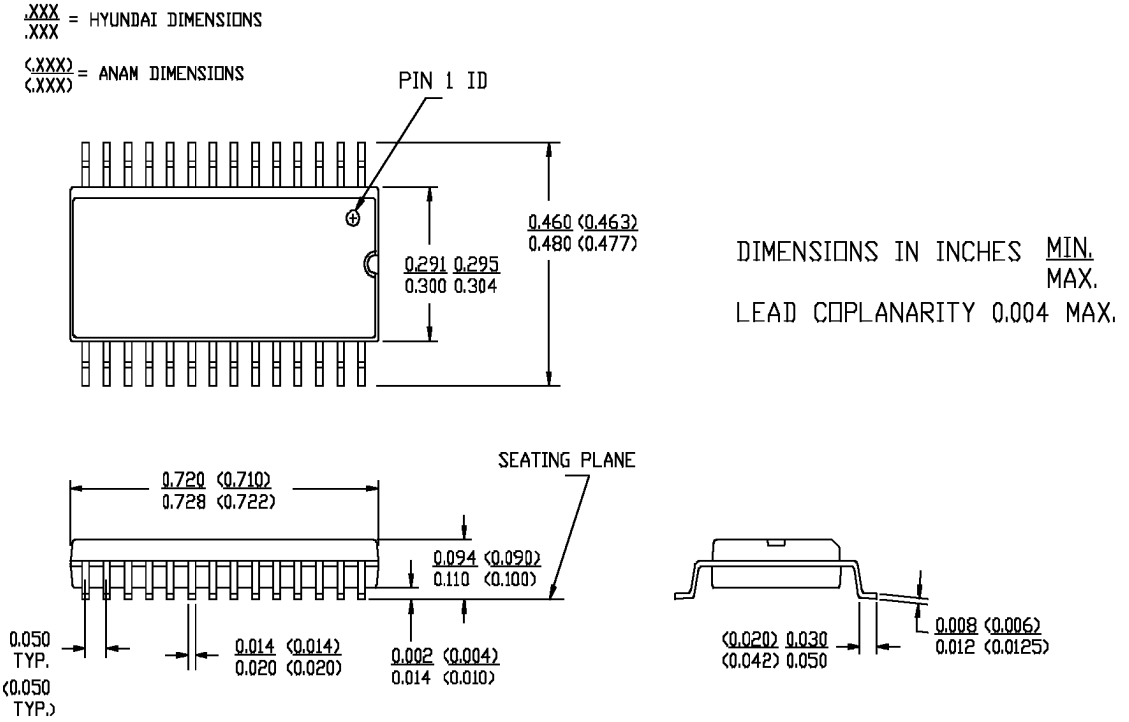
Package Diagrams

28-Lead 450-Mil (300-Mil Body Width) SOIC S22



Package Diagrams (continued)

28-Lead Thin Small Outline Package Z28