TDA7463AD

LOW VOLTAGE TONE CONTROL DIGITALLY CONTROLLED AUDIO PROCESSOR

1 FEATURES

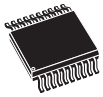
- 2 STEREO INPUT
- 1 STEREO OUTPUT
- TREBLE BOOST
- BASS CONTROL
- BASS AUTOMATIC LEVEL CONTROL
- VOLUME CONTROL IN 1dB STEPS
- MUTE
- STAND-BY FUNCTION SOFTWARE CONTROLLED
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS

2 DESCRIPTION

The TDA7463AD is a volume tone (bass and treble) processor for quality audio applications in Low voltage supply portable systems.

Bass ALC (Automatic Level Control) function can be adjusted by a dedicated pin.

Figure 1. Package



SSO20P

Table 1. Order Codes

Part Number	Package
TDA7463AD	SSO20P

The control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained

Figure 2. Block Diagram

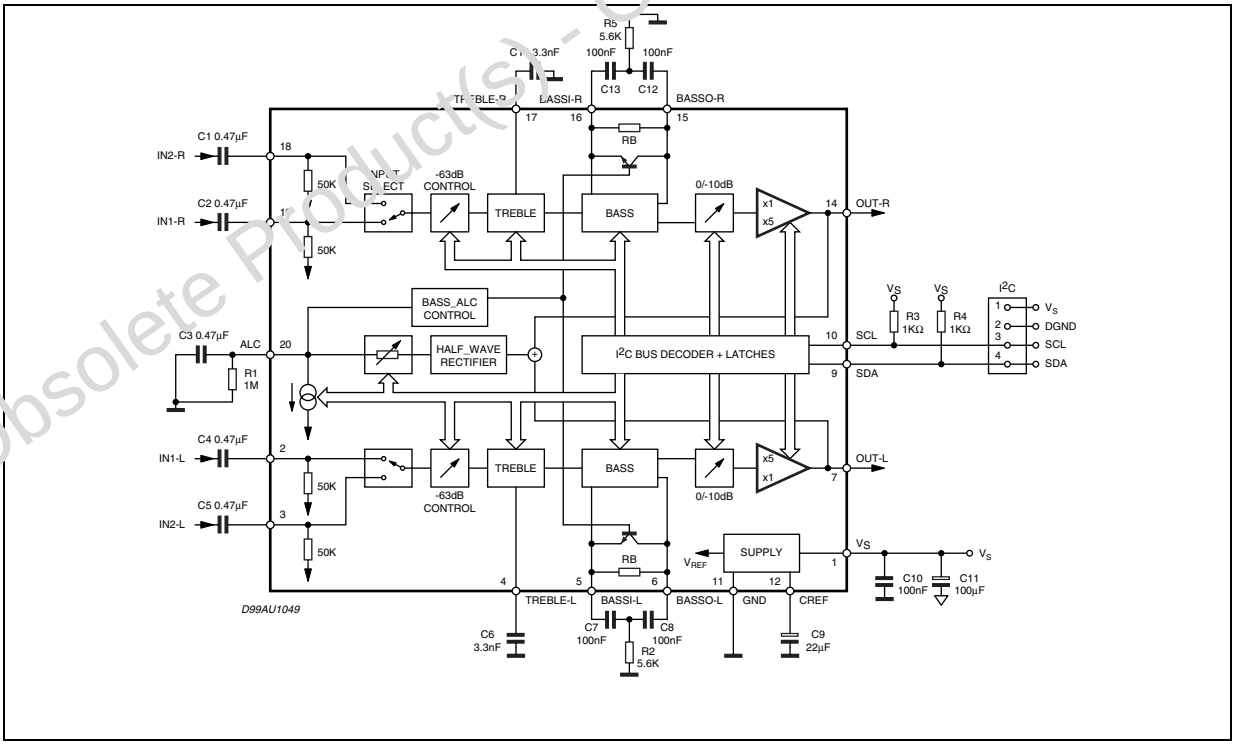


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	5	V
T_{amb}	Operating Ambient Temperature	-10 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Figure 3. Pin Connection (Top view)

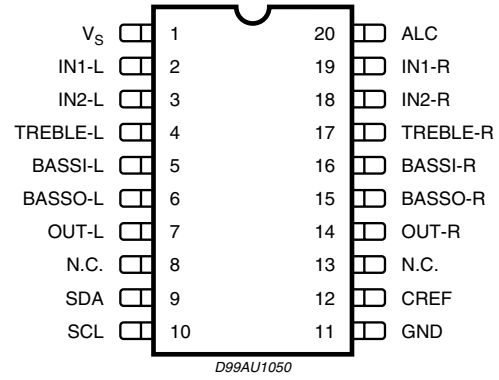


Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	85	°C/W

Table 4. Quick Reference Data

Symbol	Parameter	Min	Typ	Max	Unit
V_S	Supply Voltage	1.8	2.4	3	V
V_{CL}	Max. input signal handling	0.2			Vrms
THD	Total Harmonic Distortion V = 0.1Vrms; f = 1KHz			0.1	%
S/N	Signal to Noise Ratio V out = 0.1Vrms (mode = OFF)		80		dB
S_C	Channel Separationf = 1KHz		80		dB
	Volume Control (1dB step)	-63		0	dB
	-10dB damping	-10		0	dB
	14dB	0		14	dB
	Treble Control	0		8	dB
	Bass Control	0		14	dB
	Mute Attenuation		100		dB

Table 5. ELECTRICAL CHARACTERISTCS

(refer to the test circuit T_{amb} = 25°C, V_S =2.4V, R_L = 10KΩ, R_G = 600Ω, all controls flat, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		1.8	2.4	3	V
I_S	Supply Current			4		mA
I_{ST-BY}	Stand-By Current			50		µA
SVR	Ripple Rejection			70		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	K&
V_{CL}	Clipping Level	THD = 0.3%	0.2			Vrms
VOLUME CONTROL						
C_{RANGE}	Control Range			63		dB
$A_{V\ MIN}$	Min Attenuation		-1	0	1	dB
$A_{V\ MAX}$	Max. Attenuation		62	63	64	dB
A_{STEP}	Step Resolution			1		dB
A_{mute}	Mute Attenuation		80	100		dB
A-10dB	-10dB damping			10		dB
G14dB	14dB gain			14		dB
BASS CONTROL (1)						
Gb	Control Range	Max. Boost/on		14		dB
R_B	Internal Feedback Resistance		33.75	45	56.25	KΩ
TREBLE CONTROL (1)						
G_t	Control Range	Max. Boost on		8		dB
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	0.2			V_{RMS}
R_L	Output Load Resistance		10			K&
V_{DC}	DC Voltage Level			0.8		V
GENERAL						
E_{NO}	Output Noise	Outout Muted All gains = 0dB; BW = 20Hz to 20KHz flat		5 8		µV µV
E_t	Total Tracking Error			0	1	dB
S/N	Signal to Noise Ratio	All gains 0dB; V_O = 0.1V_{RMS} ;		80		dB
S_C	Channel Separation Left/Right			80		dB
d	Distortion	A_V = 0; V_I = 0.1V_{RMS} ;			0.1	%
BUS INPUT						
V_{IL}	Input Low Voltage				0.5	V
V_{IH}	Input High Voltage		1.9			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

Note: 1. BASS and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

3 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7463AD and vice versa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

3.1 Data Validity

As shown in fig. 4, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and Stop Conditions

As shown in fig.5 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

3.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 6). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 4. Data Validity on the I²CBUS

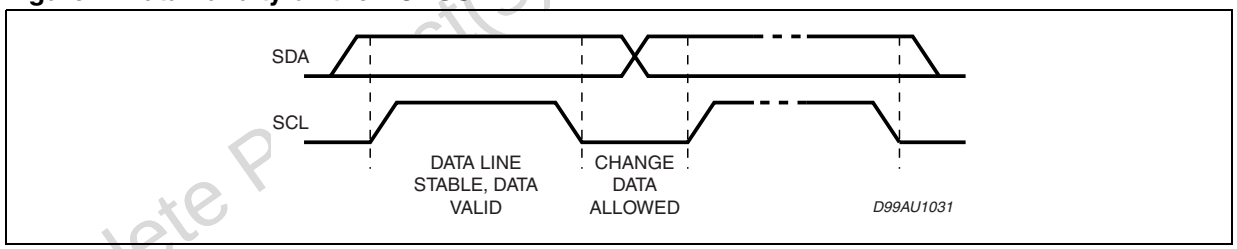


Figure 5. Timing Diagram of I²CBUS

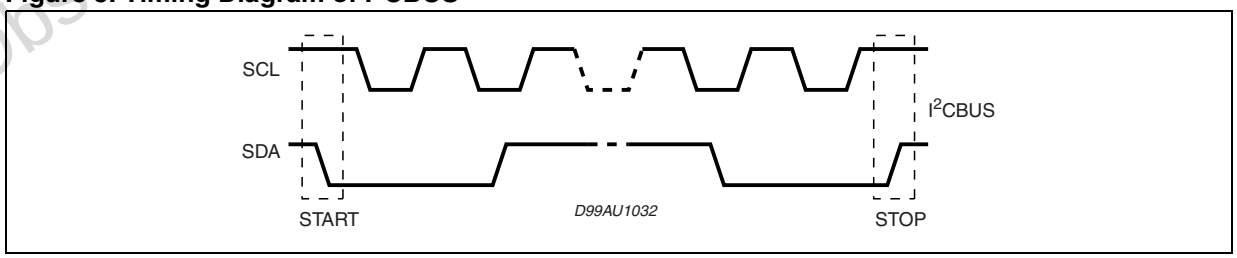
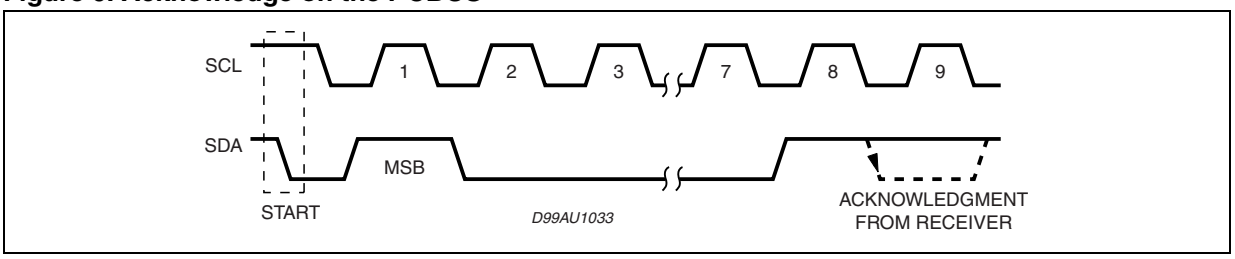


Figure 6. Acknowledge on the I²CBUS



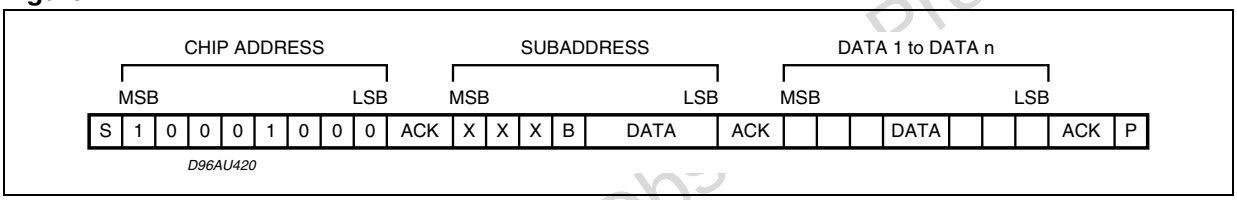
4 SOFTWARE SPECIFICATION

4.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7463AD address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

Figure 7.



ACK = Acknowledge
S = Start
P = Stop
A = Address
B = Auto Increment

5 DATA BYTES

Address = (HEX) 10001000

5.1 FUNCTION SELECTION:

The first byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
	X	X	B	0	0	0	0	STAND-BY & TREBLE & OTHERS
	X	X	B	0	0	0	1	BASS
	X	X	B	0	0	1	0	VOLUME

B = 1 incremental bus; active
B = 0 no incremental bus;
X = indifferent 0,1

5.1.1 STAND_BY & TREBLE & OTHERS

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	
								STAND-BY
							1	ALL CIRCUITS STOP
								TREBLE
						1		STAND-BY (Treble block stops)
					1	0		BOOST OFF
					0	0		BOOST ON
				1	0	0		High Boost (+8dB)
				0	0	0		Low Boost (+4dB)
								MUTE
			1					Input Mute ON
			0					Input Mute OFF
		1						Output Mute ON
		0						Output Mute OFF
								BASS
	1							Release Current Circuit ON
	0							Release Current Circuit OFF
								INPUT Select
1								INPUT 1
0								INPUT 2

5.1.2 BASS

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	
							1	STAND-BY (Bass block stops)
						1		BASS (boost OFF)
						0		BASS (boost ON)
					1	0		High boost (Ex. + 14dB)
					0	0		Low boost (Ex. + 6dB)
				1				ALC mode OFF (ALC block stops)
				0				ALC mode ON
		0	0					Attack time resistor (12.5K&)
								Release current (0.4 A)
		0	1					Attack time resistor (25K&)
								Release current (0.2 A)
		1	0					Attack time resistor (50K&)
								Release current (0.1 A)
		1	1					Attack time resistor (100K&)
								Release current (0.05 A)
0	0							Threshold1 (0.2Vrms)
0	1							Threshold2 (0.14Vrms)
1	0							Threshold3 (0.1Vrms)
1	1							Threshold4 (0.07Vrms)

5.1.3 VOLUME

MSB							LSB	VOLUME
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**1 dB STEPS**
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-3
					1	0	0	-4
					1	0	1	-5
					1	1	0	-6
					1	1	1	-7
								8 dB STEPS
		0	0	0				0
		0	0	1				-8
		0	1	0				-16
		0	1	1				-24
		1	0	0				-32
		1	0	1				-40
		1	1	0				-48
		1	1	1				-56
								OUTPUT GAIN
	1							0dB
	0							+14dB
								OUTPUT ATTENUATION
1								0dB
0								-10dB

VOLUME: 0 ~ -63dB

5.2 ALC IN general:

5.2.1 VOLUME setting with ALC

Target Volume [dB]	Volume [dB]	Output Gain 0/+14dB 0/+14dB	Output Attenuation 0/-10dB [dB]
0	-14	+14	0
-1	-15		
-2	-16		
-3	-17		
-4	-18		
-5	-19		
-6	-20		
-7	-21		
-8	-22		
-9	-23		
-10	-24		
-11	-25		
-12	-26		
-13	-27		
-14	-14	0	0
-15	-15		
-16	-16		
-17	-17		
-18	-18		
-19	-19		
-20	-20		
-21	-21		
-22	-22		
-23	-23		
-24	-14	0	-10
-25	-15		
-26	-16		
-27	-17		
:	:		
:	:		
-70	-60		
-71	-61		
-72	-62		
-73	-63		

Figure 8. PIN: IN-L, IN-R

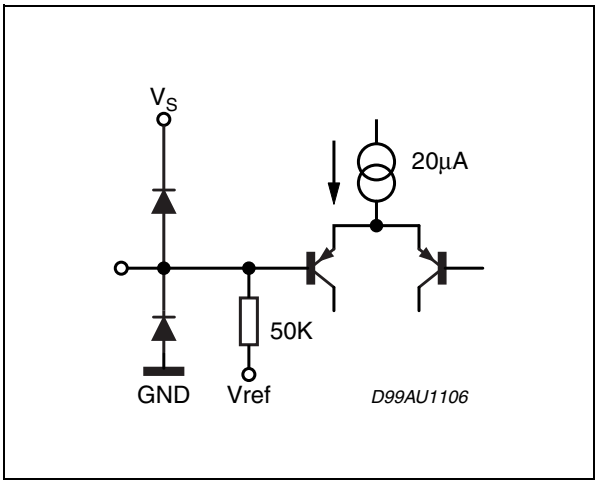


Figure 9. PIN: TREBLE-L, TREBLE-R

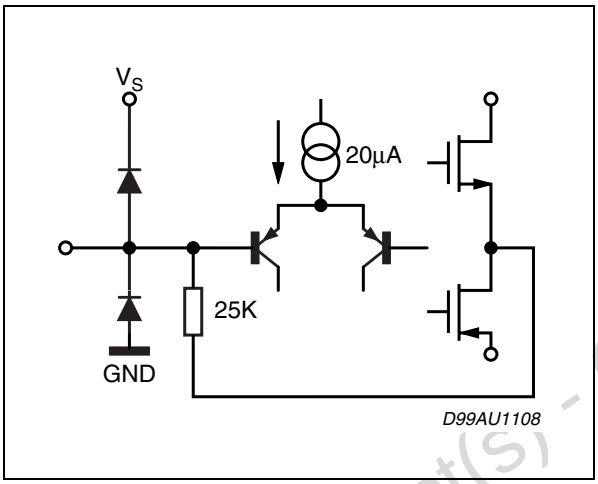


Figure 10. PIN: BASSI-L, BASSI-R

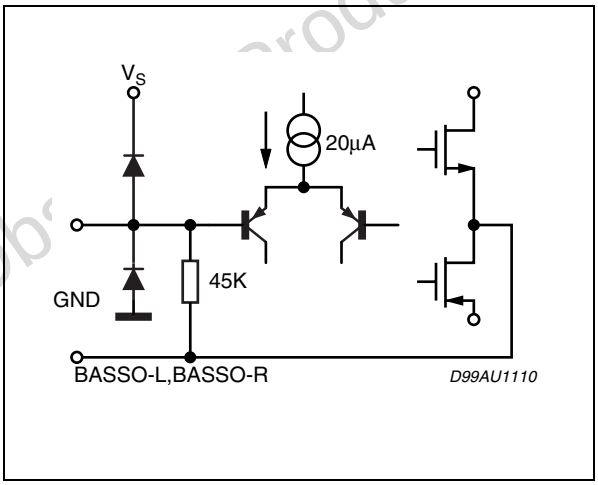


Figure 11. PIN: OUT-L, OUT-R

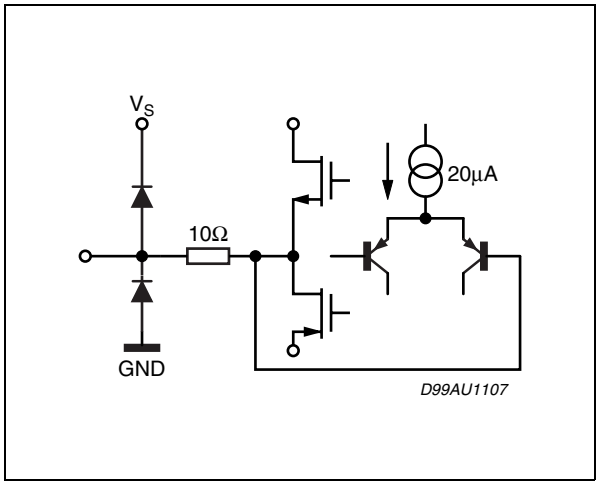


Figure 12. PIN: SCL, SDA

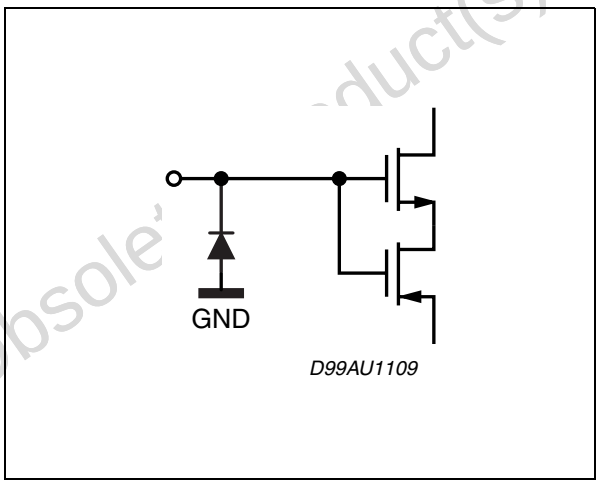


Figure 13. PIN: BASSO-L, BASSO-R

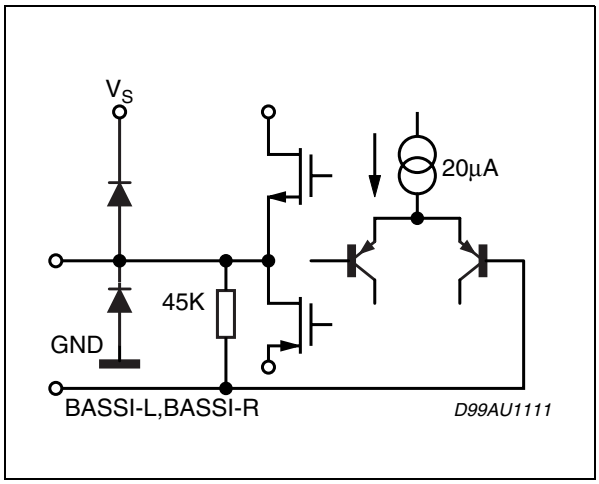


Figure 14. PIN: ALC

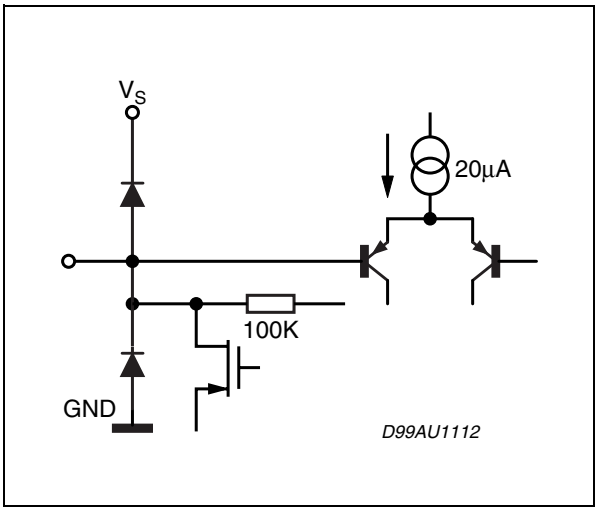


Figure 15. PIN: CREF

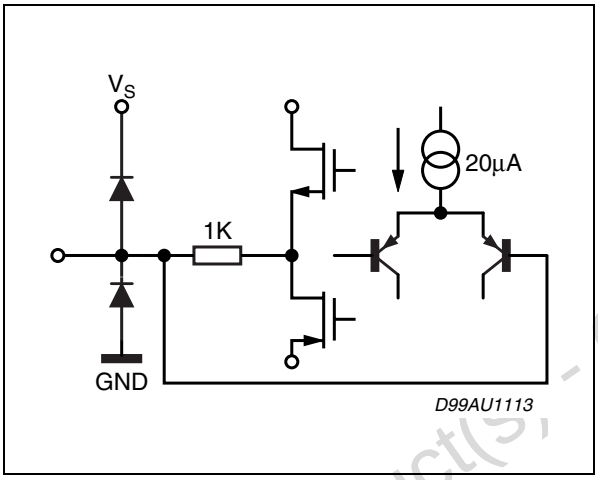


Figure 16. BASS ALC: Threshold Curve

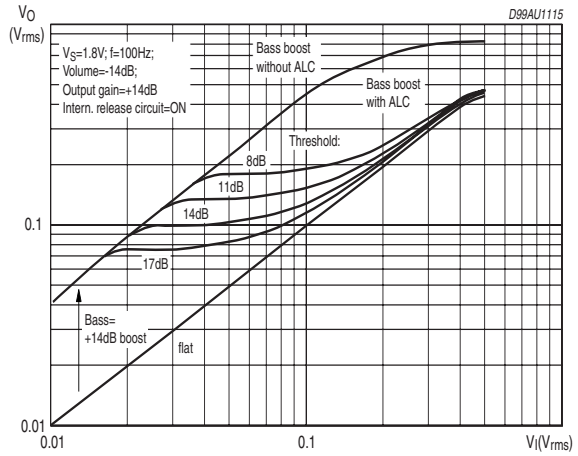


Figure 17. BAS ALC: THD

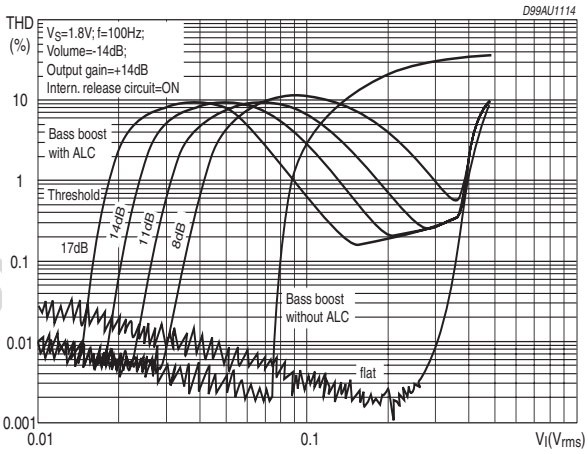
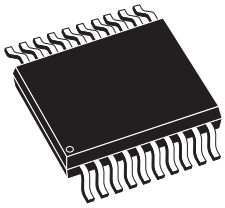


Figure 18. SSOP20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.000			0.079
A1	0.050			0.002		
A2	1.650	1.750	1.850	0.065	0.069	0.073
b	0.220		0.380	0.009		0.015
c	0.090		0.250	0.005		0.010
D (1)	6.900	7.200	7.500	0.272	0.283	0.295
E	7.400	7.800	8.200	0.291	0.307	0.323
E1 (1)	5.000	5.300	5.600	0.197	0.209	0.220
e (2)		0.650			0.026	
L	0.550	0.750	0.950	0.022	0.029	0.037
L1		1.250			0.049	
k	0° (min.), 4° (typ.), 8° (max.)					
ddd			0.100			0.004

Notes: 1. D and E1 does not include mold flash or protrusions, but do include mold mismatch and are measured at datum plane "H". Mold flash or potrusions shall not exceed 0.20mm (.008inch) both side.
2. "b" dimensions does not include dambar protusion/intrusion.

OUTLINE AND MECHANICAL DATA



SSOP20

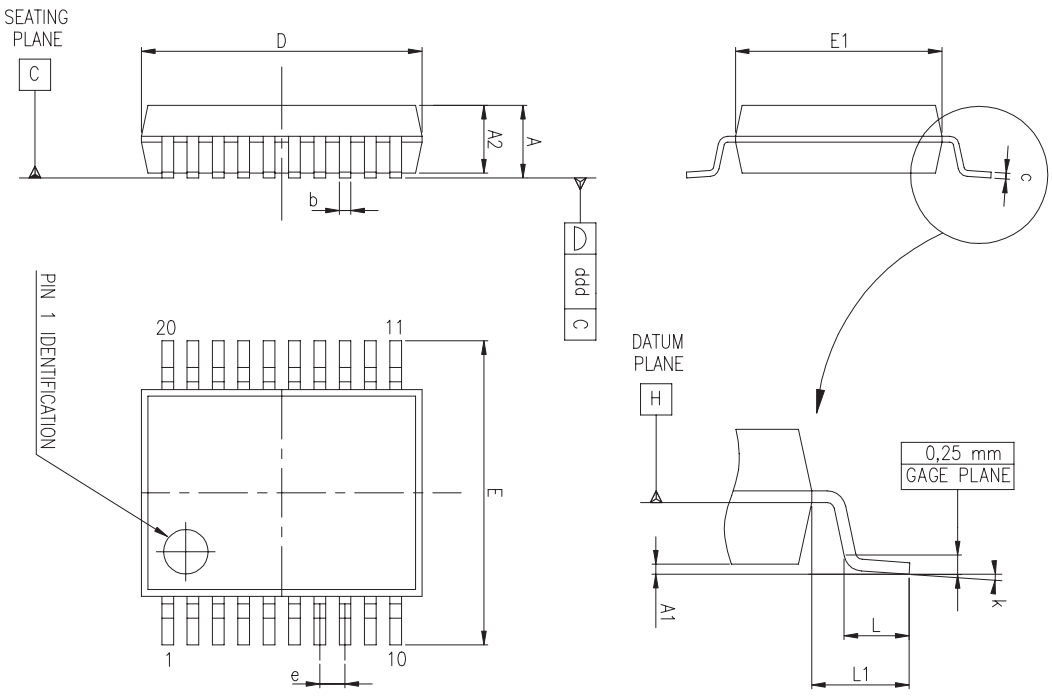


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Table 6. Revision History

Date	Revision	Description of Changes
January 2004	2	First Issue in EDOCS DMS
June 2004	3	Changed the Style-sheet in compliance to the new “Corporate Technical Pubblications Design Guide”
November 2005	4	Add section 3 and 4