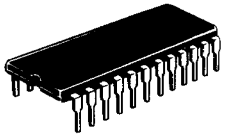
MOTOROLA

MC10183

MECL 10K SERIES

4 X 2 MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 623

4 X 2 MULTIPLIER

The MC10183 is a 4 x 2 bit multiplier that can multiply 2's complement numbers producing a 2's complement product without correction. The device can be used as a 4 x 2 bit multiplier cell to build larger iterative arrays.

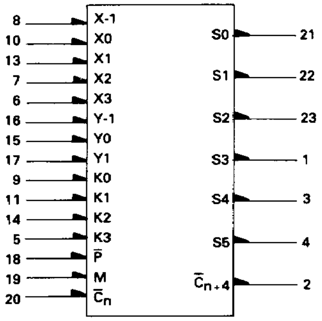
The part performs the function defined as F = XY + K, where K is an input field used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is a modified Booth's algorithm or multiplier coding technique. The device consists of a shift network and an adder/subtracter in which 0, 1 times X, or 2 times X is either added or subtracted to input constant K. The Y inputs control multiplication as shown in the Truth Table.

The most significant digit in a word carries a negative weight allowing 2's complement numbers of various lengths to be multiplied. An M-bit by N-bit multiplication produces an M + N bit product.

The $\overline{P}$ polarity input allows multiplication in either positive logic ($\overline{P}$ = high) or negative logic ($\overline{P}$ = low) representation. Also, mode control M inverts $\overline{C}_n$ when high and passes $\overline{C}_n$ directly when left low.

P_D = 760 mW typ/pkg (No Load)
t_{pd} = 50 ns typ (8 x 8 bit product)
t_r, t_f = 3.5 ns typ (20%–80%)

LOGIC DIAGRAM



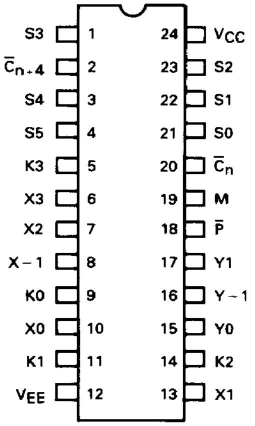
X-1, X0, X1, X2, X3	Multiplicand Inputs
Y-1, Y0, Y1	Multiplier Inputs
K0, K1, K2, K3	Constant Inputs
$\overline{C}_n$	Carry Input
$\overline{P}$	Polarity Control
M	Mode Control
S0, S1, S2, S3, S4, S5	Product Output
$\overline{C}_{n+4}$	Carry Output

V_{CC} = Pin 24
V_{EE} = Pin 12

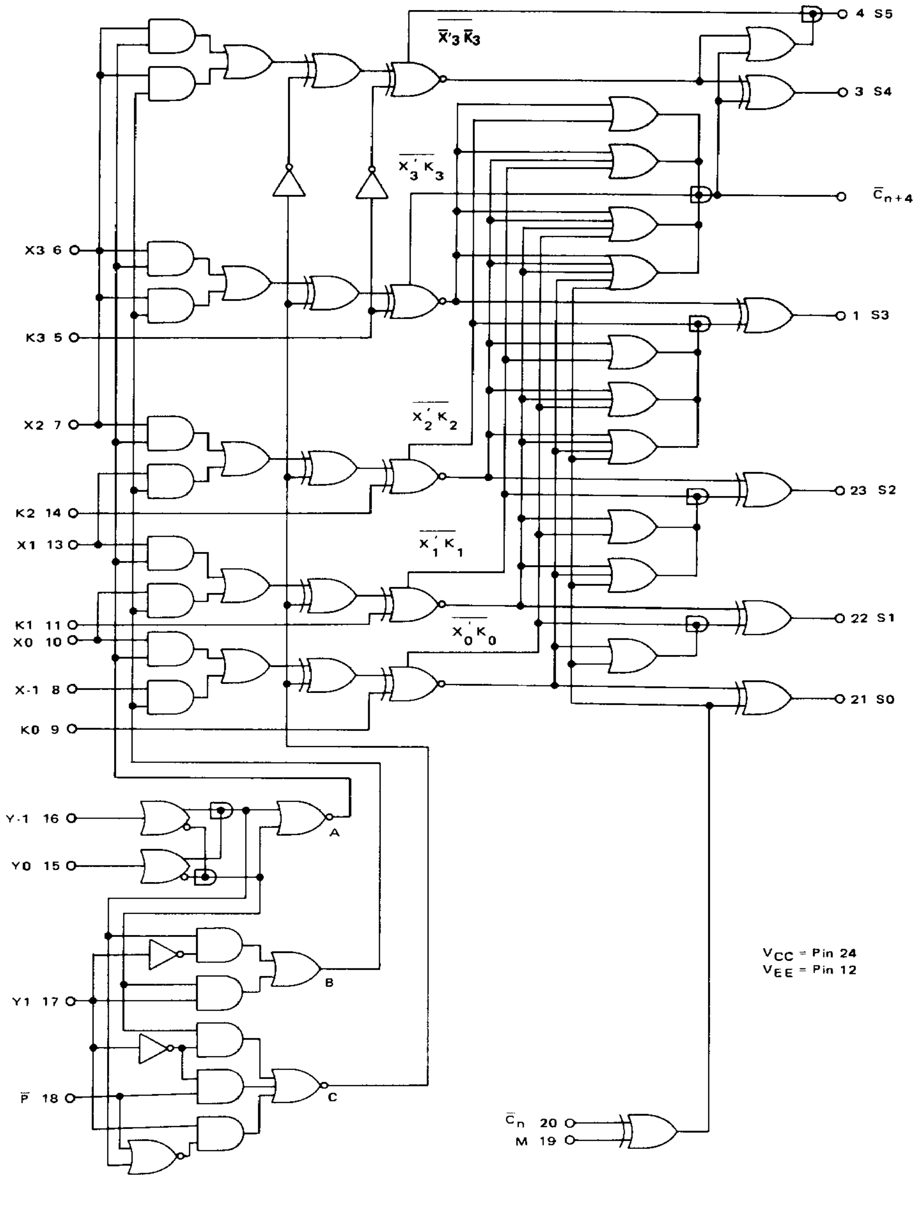
TRUTH TABLE

Y-2	Y0	Y1	$\overline{P}$	A	B	C	Operation	Complementor
L	L	L	L	L	L	L	Add Zero	Direct
H	L	L	L	H	L	L	Add 1X	Direct
L	H	L	L	H	L	L	Add 1X	Direct
H	H	L	L	L	H	L	Add 2X	Direct
L	L	H	L	L	H	H	Sub 2X	Invert
H	L	H	L	H	L	H	Sub 1X	Invert
L	H	H	L	H	L	H	Sub 1X	Invert
H	H	H	L	L	L	H	Sub Zero	Invert
L	L	L	H	L	L	L	Sub Zero	Direct
H	L	L	H	H	L	H	Sub 1X	Invert
L	H	L	H	H	L	H	Sub 1X	Invert
H	H	L	H	L	H	H	Sub 2X	Invert
L	L	H	H	L	H	L	Add 2X	Direct
H	L	H	H	H	L	L	Add 1X	Direct
L	H	H	H	H	L	L	Add 1X	Direct
H	H	H	H	L	L	H	Add Zero	Invert

PIN ASSIGNMENT



POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@Test Temperature	TEST VOLTAGE VALUES				
	Volts				
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10183 TEST LIMITS								VOLTAGE APPLIED TO PINS LISTED BELOW:					(V_{CC}) Gnd
			-30°C		+25°C			+85°C								
			Min	Max	Min	Typ	Max	Min	Max	Unit	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	12	–	201	–	146	183	–	201	mAdc	–	–	–	–	12	24
Input Current	I_{inH}	6	–	390	–	–	245	–	245	µAdc	6	–	–	–	12	24
		8	–	350	–	–	220	–	220	↓	8	–	–	–	↓	↓
		18	–	320	–	–	200	–	220	↓	18	–	–	–	↓	↓
	I_{inL}	8	0.5	–	0.5	–	–	0.3	–	µAdc	–	8	–	–	12	24
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	8,16,19	–	–	–	12	24
		21	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	8,16,19	–	–	–	12	24
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	17,18,19,20	–	–	–	12	24
		21	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	17,18,19,20	–	–	–	12	24
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	8,16,19	–	–	5	12	24
		21	-1.080	–	-0.980	–	–	-0.910	–	Vdc	8,16,19	–	–	15	12	24
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	8,16,19	–	5	–	12	24
		21	–	-1.655	–	–	-1.630	–	-1.595	Vdc	8,16,19	–	10	–	12	24
Switching Times (50 Ω Load)													Pulse In	Pulse Out	-3.2 Vdc	-2.0 Vdc
Propagation Delay	t_{20+2-}	2	1.0	5.3	1.0	4.5	5.0	1.0	5.5	ns	–	–	20	2	12	24
	t_{20+22+}	22	1.8	8.4	1.8	6.0	8.0	1.8	8.8	↓	–	–	20	22	↓	↓
	t_{20+3-}	3	1.8	8.4	1.8	8.0	8.0	1.8	8.8	↓	–	–	20	3	↓	↓
	t_{9+2-}	2	1.6	7.3	1.6	5.5	7.0	1.6	7.7	↓	–	–	9	2	↓	↓
	t_{9+1+}	1	2.5	11	2.5	8.0	10.5	2.5	11.5	↓	–	–	9	1	↓	↓
	t_{14+3-}	3	2.5	11	2.5	8.5	10.5	2.5	11.5	↓	–	–	14	3	↓	↓
	t_{10-2+}	2	1.8	8.4	1.8	6.0	8.0	1.8	8.8	↓	–	–	10	2	↓	↓
	t_{13+23+}	23	2.5	11	2.5	9.5	10.5	2.5	11.5	↓	–	–	13	23	↓	↓
	t_{14-3+}	3	2.5	11	2.5	10.0	10.5	2.5	11.5	↓	–	–	14	3	↓	↓
	t_{15-2-}	2	3.2	14.1	3.2	10.5	13.5	3.2	14.8	↓	–	–	15	2	↓	↓
	t_{15+23+}	23	↓	↓	↓	10.5	↓	↓	↓	↓	–	–	15	23	↓	↓
	t_{15-3+}	3	↓	↓	↓	11.5	↓	↓	↓	↓	–	–	15	3	↓	↓
Rise Time (20% to 80%)	t_{22+}	22	1.0	6.3	1.0	3.5	6.0	1.0	6.6	ns	–	–	9	22	12	24
Fall Time (20% to 80%)	t_{22-}	22	1.0	6.3	1.0	3.5	6.0	1.0	6.6	ns	–	–	9	22	12	24

MC10183 APPLICATIONS INFORMATION

The MC10183 is a 4 X 2 bit multiplier that uses a modified Booth's algorithm or multiplier coding technique. The device generates the function: S = X • Y + K

where

X = 4-bit multiplicand
Y = 2-bit multiplier
K = 4-bit constant

The addition of the constant allows the device to be used in an iterative array of parts for larger words. The algorithm for multiplication is:

y_{i-1}	y_i	y_{i+1}	Operation
0	0	0	add zero
1	0	0	add multiplicand
0	1	0	add multiplicand
1	1	0	add 2 times multiplicand
0	0	1	sub 2 times multiplicand
1	0	1	sub multiplicand
0	1	1	sub multiplicand
1	1	1	sub zero

DEVICE OPERATION

The device consists of three main sections; a decoder, a shifter, and a high speed look-ahead carry adder/subtractor.

1. The decoder uses the Y inputs to generate the control signals for the shifter and the adder/subtractor. Also, the polarity control $\overline{P}$ is used to allow operation in either positive or negative logic. Referring to the logic diagram, the control signals are:

$A = Y_{-1} \oplus Y_0$ (1 times multiplicand)

$B = Y_{-1}Y_0\overline{Y}_1 + \overline{Y}_{-1}\overline{Y}_0Y_1$
(2 times multiplicand)

$\overline{C} = \overline{P}\overline{Y}_1 + \overline{Y}_{-1}\overline{Y}_0\overline{Y}_1 + PY_1(\overline{Y}_{-1} + \overline{Y}_0)$
(add/subtract)

The $\overline{P}$ input is tied to a high logic level or ground for positive logic operation.

2. The shift network is a multiplexer that ripples through number X (1 times multiplicand), shifts number X by one bit (2 times multiplicand), or sets the output to zero. The network is controlled by decoder functions A and B which are generated in accordance with the multiply algorithm.

3. The adder/subtractor follows the shift network which performs the actual multiplication. The adder/subtractor produces the sum or difference of the newly formed partial product and the accumulated partial product (constant K). Subtraction is accomplished by inverting the shifted product and doing a two's complement addition. The carry in of the least significant bit must be a logic one during subtraction.

The two most significant bits of the product are used for sign detection and overflow for a two's complement multiply. These outputs are used only as the two most significant bits of the accumulated product at each addition level within a multiplier array.

Overflow can occur either as the result of 2 times the multiplicand, and/or of an addition or subtraction. To show all possible conditions (including overflow), the most significant bit (S5) must carry a negative binary weight. To show this for a 4 X 2 bit multiply plus constant, consider the following addition:

$$\begin{array}{rl} X'_4 \cdot X'_3\, X'_2\, X'_1\, X'_0 & \text{shifter outputs} \\ +\ K3 \cdot K3\, K2\, K1\, K0 & \text{constant} \\ \hline S5\ \ S4 \cdot S3\ S2\ S1\ S0 & \text{sum} \end{array}$$

The shift network produces 5 product bits (maximum value of 2 times multiplicand) and a 4-bit constant is added to the least signficant end of the product. The K3 bit is repeated to hold the proper binary weight. Because S5 has a negative weight all possible combinations are represented properly.

If no overflow occurs S4 = S5, and S4 can be used as a sign bit. Under overflow conditions S4 ≠ S5, and overflow can be detected by EXCLUSIVE-ORing S4 and S5.

USAGE RULES

The MC10183 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

1. For an M-bit by N-bit multiplier, an (M+N)-bit product is formed. The number of MC10183's equals (M * N)/8. As an example, an 8 X 8 bit (Figure 1) array requires (8X8)/8 = 8 packages.

2. The MC10183 can be used directly for both positive logic and negative logic representations. The $\overline{P}$ input can be tied to ground or to a high logic level for positive logic operation, or left at a low logic level for negative logic operation.

3. The M mode control input is used to invert $\overline{C}_n$ when placed at a high logic level or ground, or passes $\overline{C}_n$ directly when left as a low logic level. When $\overline{C}_n$ is driven from $\overline{C}_{n+4}$ of a preceding device, M control is left in a low logic state. When $\overline{C}_n$ is the least significant input carry bit for a level of addition within an array, $\overline{C}_n$ is tied to Y_1 of the same device, and the M input is placed at a high logic level. Y_1 controls when subtraction occurs, and carry in must be equal to a logic one during subtraction.

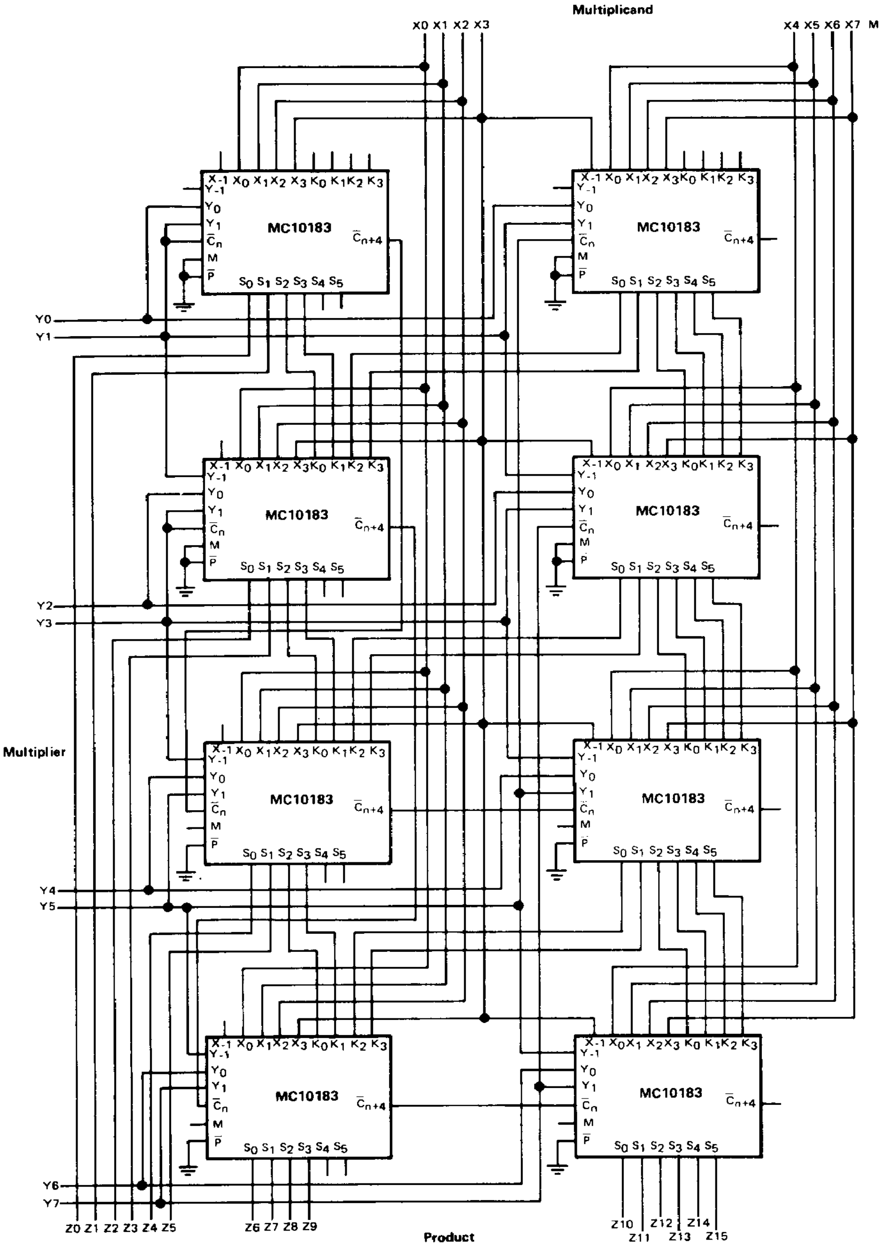


FIGURE 1 – 8-BIT × 8-BIT 2's COMPLEMENT MULTIPLIER

8 X 4 BIT EXAMPLE

Figure 2 shows 4 MC10183's in an 8 X 4 bit array. A 12-bit two's complement product is produced from a 4-bit multiplier and an 8-bit multiplicand. The array is used for positive logic representation, and all $\overline{P}$ inputs are tied to ground. At the first level of multiplication, the X_{-1} and Y_{-1} inputs are left open (logic "0") because the initial condition is treated as an add operation. The K inputs are used to add the accumulated partial product at each level of the array. If the initial partial product is zero, the least significant K inputs are left at a zero logic state (CONSTANT inputs in the figure). However, these inputs can also be used to add a constant to the least significant end of the product.

When the MC10183 is expanded to longer numbers, the carry out ($\overline{C}_{n+4}$) of a device must be rippled to the carry in ($\overline{C}_n$) of the next most significant device at the same level of multiplication. The least significant device must have the carry input equal to zero for an add and equal to one for a subtraction. In observing the multiplication algorithm y_{i+1} is always equal to 1 for a subtraction, and the carry input can be tied to Y_1. However, the M mode input must be tied to ground for this device to invert the carry input ($\overline{C}_n$) because the input requires a complemented signal.

The S4 and S5 outputs are used only at the most significant part of the array. These two sum outputs only have meaning as the two most significant bits of a two's complement number.

OTHER ARRAYS

The normal parallelogram structure consists of several stages, each multiplying two bits of multiplier times the multiplicand and adds the partial product. In larger arrays, faster configurations can be made by moving some multiplier blocks while maintaining the relative weight of each partial product. The typical times possible for various N-bit X N-bit arrays are:

Number of Bits	Total Multiply Time (ns)	Package Count
8	43	8
12	67	18
16	90	32

The times do not include wiring delays.

Because of the versatility of the MC10183, many other types of arrays can also be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can all be built.

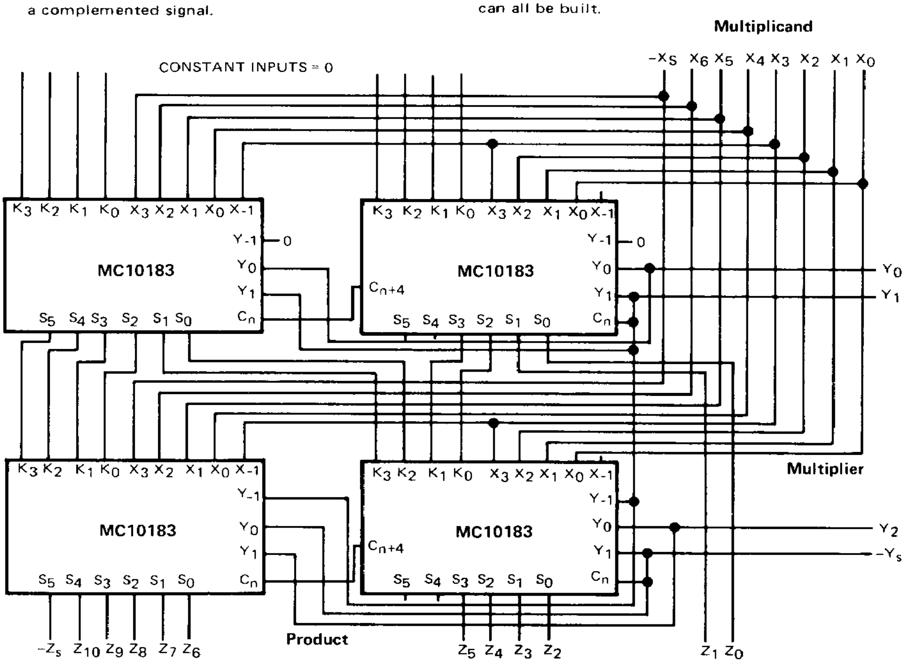


FIGURE 2 — 8-BIT BY 4-BIT 2's COMPLEMENT MULTIPLIER