CMOS 4-Bit Microcontroller

TMP47C662AN,TMP47C862AN

The TMP47C662A/862A are high speed and high performance 4-bit single chip micro computers, integrating the 8 bit AD converter, 12-bit programmable pulse generator and high-breakdown voltage outputs based on the TLCS-470 series.

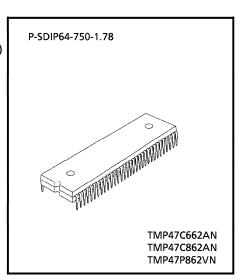
Part No.	ROM	RAM	Package	OTP
TMP47C662AN	6144 × 8-bit	384 × 4-bit	D CDIDCA 750 1 70	TMD47D0C3VAL
TMP47C862AN	8192 × 8-bit	512 × 4-bit	P-SDIP64-750-1.78	TMP47P862VN

Features

- ◆4-bit single chip microcomputer
- ullet Instruction execution time: 1.3 μ s (at 6 MHz), 244 μ s (at 32.8 kHz)
- ◆92 basic instructions
 - Table look-up instructions
 - 5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max
- ♦6 interrupt sources (External: 2, Internal: 4) All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (55 pins)
 - 5 pins Input 2 ports Output 3 pins 1 port 1/0 12 ports 47 pins
- ◆Interval Timer
- ◆Two 12-bit Timer / Counters

Timer, event counter, and pulse width measurement mode

- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
 - Simultaneous transmission and reception capability
 - 8/4-bit transfer, external / internal clock, and leading / trailing edge shift mode



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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◆Two 12-bit Programmable Pulse Generator

One-shot / continuous output, external / internal trigger, rising/falling edge trigger (external) mode

- ◆8-bit successive approximate type AD converter
 - With sample and hold
 - 8 analog inputs
 - Conversion time: 32 μ s (at 6 MHz)
- ◆Remote control pulse detector
- ◆High current outputs

LED direct drive capability (typ. 20 mA \times 4 bits)

♦ High breakdown voltage outputs

VFT direct drive capability (max 42V x 27 bits)

◆Dual-clock operation

High-speed/Low-power-consumption operating mode

◆ Hold function

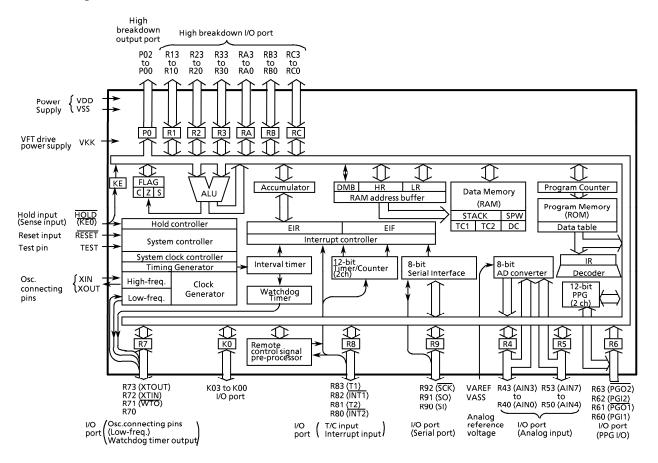
Battery/Capacitor back-up

♦ Real Time Emulator: BM47C862N0A

Pin Assignment (Top View)

P-SDIP64-750-1.78 64 ☐ ← VDD 63 ☐ ← R33 RA0 -VDD RA1 2 3 □ <> R32 RA2 62 □ <> R31 61 RB0 60 ☐ <> R30 RB1 59 ☐ <> R23 ☐ **←>** R22 RB2 ←> 58 ☐ <> R21 RB3 <> 8 57 E → R20 RC0 ←> 9 56 □ **←**➤ R13 55 RC1 10 E ←> R12 RC2 <> 54 11 53 ☐ <> R11 RC3 12 K00 13 K01 51 **→** P02 14 K02 50 15 K03 49 HOLD (KEO) 17 48 ☐ **←→** R83 (T1) XIN → □ 18
XOUT ← □ 19
RESET → □ 20
R70 ← □ 21
R71 (WTO) ← □ 22
R72 (XTIN) ← □ 22
R73 (XTOUT) ← □ 25
R91 (SO) ← □ 26
R92 (SCK) ← □ 27
R60 (PGI1) ← □ 28
R61 (PGO1) ← □ 29
R62 (PGI2) ← □ 30
R63 (PGO2) ← □ 31
VSS → □ 32 XIN -18 47 R82 (INT1) 46 R81 (T2)
R80 (INT2) 45 44 ☐ **→** R53 (AIN7) 43 R52 (AIN6) 42 R73 (XTOUT) ←> 41 ☐ **→** R51 (AIN5) R50 (AIN4) 39 □ <>> R43 (AIN3) 38 R42 (AIN2) □ <> R41 (AIN1) 37

Block Diagram



36 ☐ ←→ R40 (AIN0) 35 ☐ **←**VAREF

<---VASS —TEST

34 | 33 |

Pin Function

Pin Name	Input / Output	Functions				
K03 to K00	Input	4-bit input port				
R53 (AIN7) to R40 (AIN0)	I/O (Input)		AD converter analog input			
R63 (PGO2)	I/O (Output)	4-bit I/O port with latch.	PPG2 output			
R62 (PGI2)	I/O (Input)	When using as input port, watchdog timer output, analog input, PPG (programmable	PPG2 input			
R61 (PGO1)	I/O (Output)	pulse generator) output, or PPG trigger input, the latch must be set to "1".	PPG1 output			
R60 (PGI1)	I/O (Input)	Set to Dual-clock operating mode, when	PPG1 input			
R73 (XTOUT)	I/O (Output)	R73, R72 pin use as clock generator.	Resonator connecting pin (Low-freq.).			
R72 (XTIN)	I/O (Input)	Can be set, cleared, and tested for each bit	For inputting external clock, XTIN is used and XTOUT is opened.			
R71 (WTO)	I/O (Output)	as specified by L register indirect addressing bit manipulation instructions.	Watchdog timer output			
R70	I/O		•			
R83 (T1)		4-bit I/O port with latch.	Timer / Counter 1 external input			
R82 (INT1)	1/O (Innut)	When using as input port, external	External interrupt 1 input			
R81 (T2)	I/O (Input)	interrupt input pin, or timer/counter external input pin, the latch must be set to	Timer / Counter 2 external input			
R80 (INT2)		"1".	External interrupt 2 or REMO-CON input			
R92 (SCK)	I/O (I/O)	3-bit I/O port with latch.	Serial clock I/O			
R91 (SO)	I/O (Output)	When using as input port or serial port, the	Serial data output			
R90 (SI)	I/O (Input)	latch must be set to "1".	Serial data input			
P02 to P00	Output	3-bit high breakdown voltage output port wi	th latch			
R13 to R10	1/0	4-bit high breakdown voltage I/O port with I				
R23 to R20	I/O	8-bit data are output by the 5-bit to 8-bit data When using as input port, the latch must be o				
R33 to R30						
RA3 to RA0	I/O	4-bit high breadown voltage I/O port with lat	ch.			
RB3 to RB0	1/0	When using as input port, the latch must be o	cleared to "0".			
RC3 to RC0						
XIN, XOUT	Input, Output	Resonator connecting pin (High-frequency) . For inputting external clock, XIN is used and	XOUT is opened.			
RESET	Input	Reset signal input				
HOLD (KEO)	Input (Input)	Hold request/release signal input Sence input				
TEST	Input	Test pin for out-going test. Be opened or fixe	ed to low level.			
VDD, VSS		+5 V, 0 V (GND)				
VAREF, VASS	Power supply	AD converter analog reference voltage				
VKK		VFT drive power supply				

Operational Description

Concerning the TMP47C662A/862A the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the TMP47C660/860, the technical data sheets for the TMP47C660/860 shall also be referred to.

1. System Configuration

♦ Internal CPU Function

They are the same as those of the TMP47C660/860.

- Peripheral Hardware Function
 - ① I/O Port
 - 2 Interval Timer
 - 3 Timer / Counters (TC1, TC2)
 - 4 Watchdog Timer
 - 5 Remote control pulse detector
 - 6 AD converter
 - 7 Programmable Pulse Generator
 - 8 Serial Interface

The description has been provide with priority on functions (① and ⑦) added to and changed from the TMP47C660/860.

2. Peripheral Hardware Function

2.1 I/O Ports

TMP47C662A/862A have 15 I/O ports (55pins) each as follows:

① K0 ; 4-bit input ② P0 ; 3-bit output

3 R1, R2 ; 4-bit input / output

R4, R5 ; 4-bit input / output (shared with AD converter analog inputs)

R6 ; 4-bit input / output (shared with programmable pulse generator I/O)
 R7 ; 4-bit input / output (shared with the low-frequency resonator)

connecting pins and the watchdog timer output)

timer / counter input)

8 R9 ; 3-bit input / output (shared with serial port)

This section describes ports of ②, ③, ⑤ and ⑨ which are changed from the TMP47C660/860.

Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Ports P0 (P02 to P00)

Ports P0 is 3-bit high breakdown voltage output ports with latch. The latch is initialized to "0" during reset.

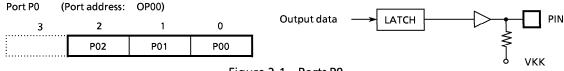


Figure 2-1. Ports P0

(2) Ports R1 (R13 to R10), R2 (R23 to R20)

The 4-bit high breakdown voltage I/O ports with latch, which can directly Vacume Fuolrescent Tubes (VFT) . The latch should be cleared to "0" when used as an inuput port. The latch is initialized to "0" during reset.

Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		- 0.3 to V _{DD} + 0.3	V
	V _{OUT1}	R4, R5, R7	- 0.3 to V _{DD} + 0.3	
Output Voltage	V _{OUT2}	R6, R8, R9	- 0.3 to 10	V
	V _{OUT3}	Source open drain pin	- 35 to V _{DD} + 0.3	
	I _{OUT1}	R6	30	
Output Compant (nor 1 min)	I _{OUT2}	R4, R5, R7 to R9	3.2	^
Output Current (per 1 pin)	I _{OUT3}	P0, R1, R2	- 10	mA
	I _{OUT4}	R3, RA, RB, RC	– 25	
Output Company (Tatal)	Σ l _{OUT1}	R6	60	A
Output Currnent (Total)	Σ I _{OUT2}	R3, RA, RB, RC	- 100	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
			In the Normal mode	4.5		
Supply Voltage	V_{DD}		In the SLOW mode	2.7	6.0	V
			In the HOLD mode	2.0		
	V _{IH1}	Except Hysteresis Input	\/ > A E\/	$V_{DD} \times 0.7$		
Input High Voltage	V_{IH2}	Hysteresis Input	V _{DD} ≧ 4.5V	$V_{DD} \times 0.75$	V_{DD}	٧
	V _{IH3}		$V_{DD} < 4.5V$ $V_{DD} \times 0.9$			
	V_{IL1}	XIN, XOUT	\/ > A E\/		$V_{DD} \times 0.3$	
Input Low Voltage	V_{IL2}	XTIN, XTOUT	V _{DD} ≧ 4.5V	0	$V_{DD} \times 0.25$	V
	V_{IL3}		V _{DD} < 4.5V		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	6.0	MHz
	fs			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage V_{IH3} , V_{IL3} : In the SLOW or HOLD mode.

DC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit	
Hysteresis Voltage	V_{HS}	Hysteresis Input		_	0.7	_	٧	
	I _{IN1}	KO, TEST, RESET, HOLD	V _{DD} = 5.5 V,				_	
Input Current	I _{IN2}	R ports (open drain)	en drain) V _{IN} = 5.5 V / 0 V		_	±2	μ A	
Lawyt Davistanaa	R _{IN1}	K0 port with pull-up/pull-down		30	70	150		
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ	
Pull-down resistance	R _K	source open drain	$V_{DD} = 5.5 \text{ V}, V_{KK} = -30 \text{ V}$	_	80	_		
I _{LO1}		sink open drain	V _{DD} = 5.5 V, V _{IN} = 5.5 V	_	_	2	_	
Output Leakage Current	I _{LO2}	source open drain	$V_{DD} = 5.5 \text{ V}, V_{OUT} = -32 \text{ V}$	_	_	- 2	μ A	
Output Level High Voltage	V _{OH}	P0, R1, R2	$V_{DD} = 4.5 \text{ V}, I_{OH} = -5 \text{ mA}$	2.4	_	_	V	
Output Level Low Voltage	V _{OL}	R4, R5, R7-R9	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	_	0.4	V	
Output Level High Voltage	I _{OH}	R3, RA, RB, RC	$V_{DD} = 4.5 \text{ V}, V_{OH} = 2.4 \text{ V}$	_	- 15	_	mA	
Output Level Low Voltage	l _{OL}	R6	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	_	20	_	mA	
Supply Current (in the Normal mode)	I _{DD}		V _{DD} = 5.5 V, fc = 4 MHz	_	3	6	mA	
Supply Current (in the SLOW mode)	I _{DD\$}		V _{DD} = 3.0 V, fs = 32.768 kHz	_	30	_	μΑ	
Supply Current (in the HOLD mode)	I _{DDH}		V _{DD} = 5.5 V	_	0.5	10	μΑ	

Note 1: Typ. values show those at Topr = 25° C, $V_{DD} = 5 V$.

Note 2: Input Current I_{IN1}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Supply Current I_{DD} , I_{DDH} ; $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$

The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

Supply Current I_{DDS} ; $V_{IN} = 2.8 \text{ V} / 0.2 \text{ V}$

Low frequency clock is only osillated (connecting XTIN, XTOUT).

AD Conversion Characteristics

 $(Topr = -40 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Analan Bafarran Walter	V _{AREF}		V _{DD} _ 1.5	_	V _{DD}	
Analog Reference Voltage	V _{ASS}		V _{SS}	_	1.5	\ \
Analog Reference Voltage Range	$_{\Delta}V_{AREF}$	V _{AREF} -V _{ASS}	2.5	_	_	V
Analog Input Voltage	V _{AIN}		V _{ASS}	_	V _{AREF}	V
Analog Supply Current	I _{REF}		_	0.5	1.0	mA
Nonlinearity Error			_	_	± 1	
Zero Point Error		$V_{DD} = 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1	
Full Scale Error		V _{AREF} = 5.000 V	-	_	± 1	LSB
Total Error		V _{ASS} = 0.000 V	_	_	± 2	

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AC Characteristics

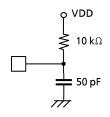
 $(V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70^{\circ}\text{C})$

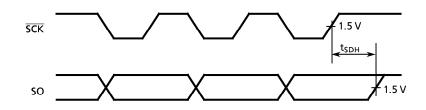
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Instruction Cycle Time	tcy	In the Normal mode	1.3	_	20	ns
		In the SLOW mode	235	_	267	
High level Clock pulse Width	t _{WCH}	E tourist de la contra				
Low level Clock pulse Width	t _{WCL}	External clock mode	80	_	_	ns
AD Sampling Time	t _{AIN}	fc = 4 MHz	_	4	_	μS
Shift Data Hold Time	t _{SDH}		0.5 tcy – 0.3	_	_	μS

Note: Shift Data Hold Time

External circuit for SCK pin and SO pin

Serial port (completion of transmission)





Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, T_{opr} = -40 \text{ to } 70^{\circ}\text{C})$

(1) 6 MHz

Ceramic Resonator

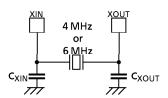
CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30 \text{ pF}$

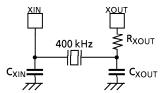
(2) 4 MHz

Ceramic Resonator

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT} = 20 \text{ pF}$



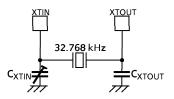


(3) 400 kHz

Ceramic Resonator

CSB400B (MURATA) $C_{XIN} = C_{XOUT} = 220 \text{ pF}, R_{XOUT} = 6.8 \text{ k}\Omega$ KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT} = 100 \text{ pF}, R_{XOUT} = 10 \text{ k}\Omega$

(4) 32.768 kHz $(V_{SS} = 0V, V_{DD} = 2.7 \text{ to } 6.0 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$ Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33 pF



Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

Typical Characteristics

