N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.025 @ V_{GS} = 10 V	9.3
	0.028 @ V_{GS} = 6.0 V	8.8

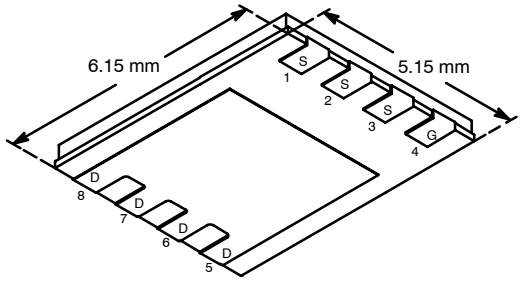
FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100% R_g Tested

APPLICATIONS

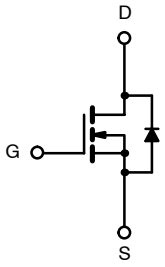
- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V, Full-/Half-Bridge DC/DC
- Industrial and 42-V Automotive

PowerPAK SO-8



Bottom View

Ordering Information: Si7456DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	9.3	5.7	A
	T_A = 85°C		6.7	4.1	
Pulsed Drain Current		I_{DM}	40		
Avalanche Current	L = 0.1 mH	I_{AS}	30		
Single Avalanche Energy (Duty Cycle ≤ 1%)		E_{AS}	45		mJ
Continuous Source Current (Diode Conduction)[a]		I_S	4.3	1.6	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	5.2	1.9	W
	T_A = 85°C		2.7	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	19	24	°C/W
	Steady State		52	65	
Maximum Junction-to-Case	Steady State	R_{thJC}	1.5	1.8	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

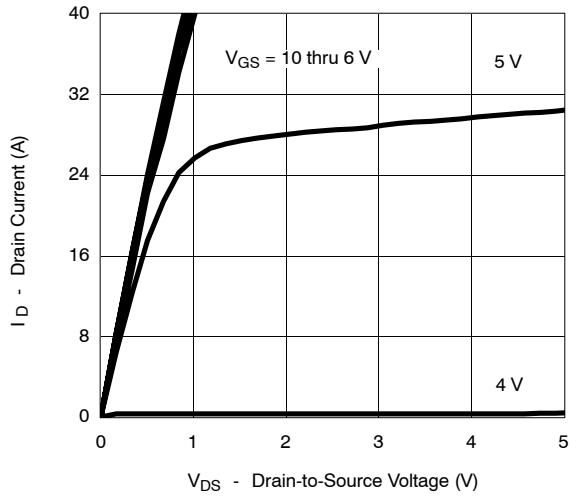
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 85°C			20	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 9.3 A		0.021	0.025	Ω
		V_{GS} = 6.0 V, I_D = 8.8 A		0.023	0.028	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 9.3 A		35		S
Diode Forward Voltage[a]	V_{SD}	I_S = 4.3 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 9.3 A		36	44	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			8.6		
Gate Resistance	R_g		0.5	1.27	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 50 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		20	40	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			46	90	
Fall Time	t_f			26	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 4.3 A, di/dt = 100 A/μs		50	80	

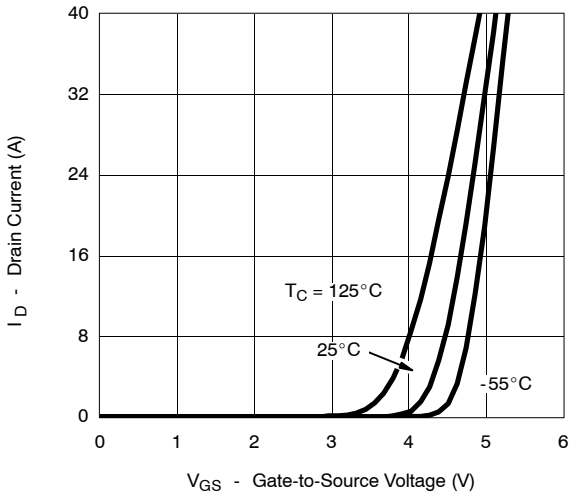
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

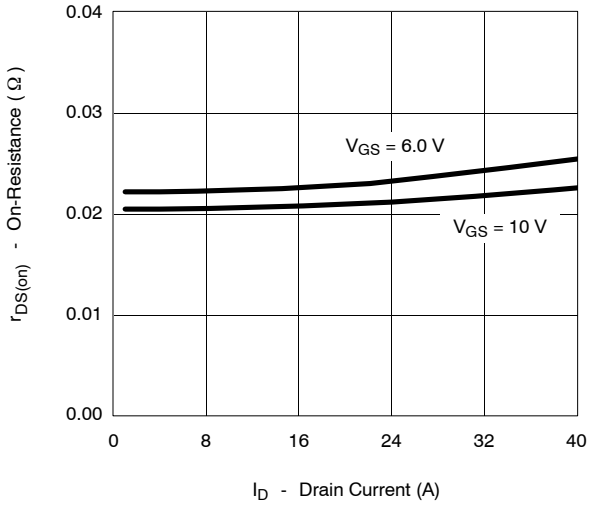


Transfer Characteristics

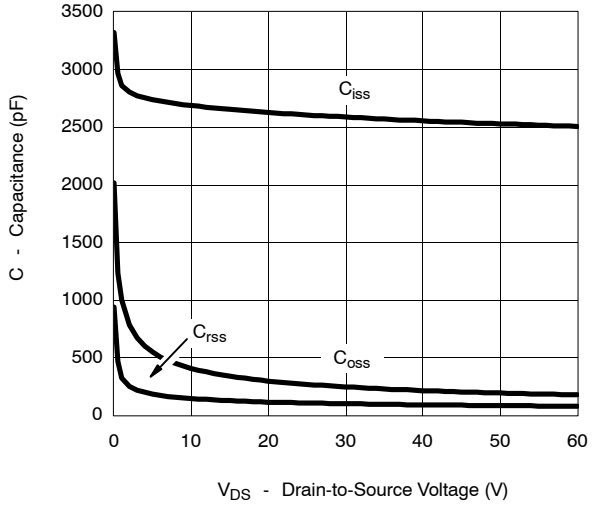


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

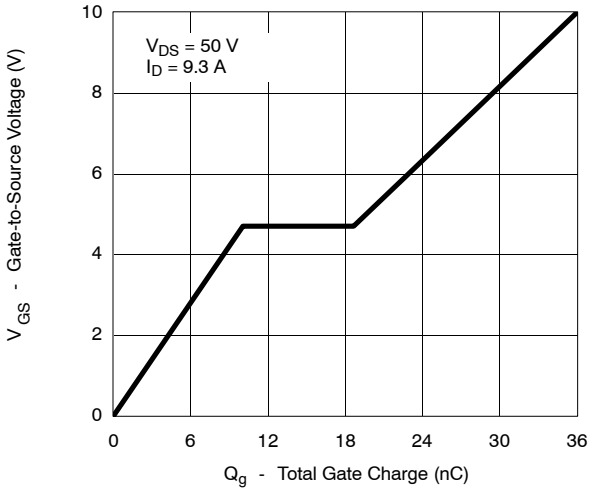
On-Resistance vs. Drain Current



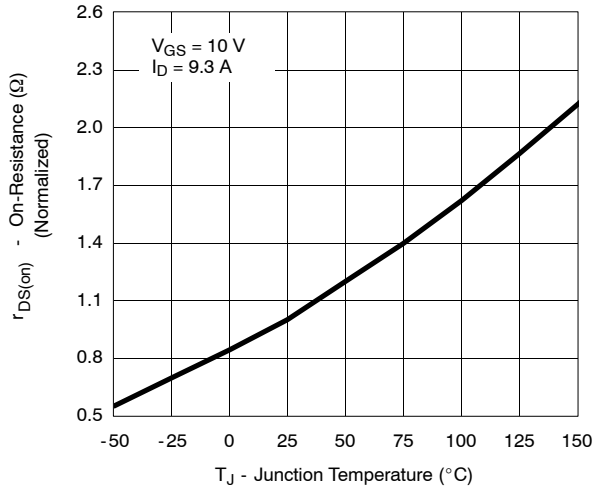
Capacitance



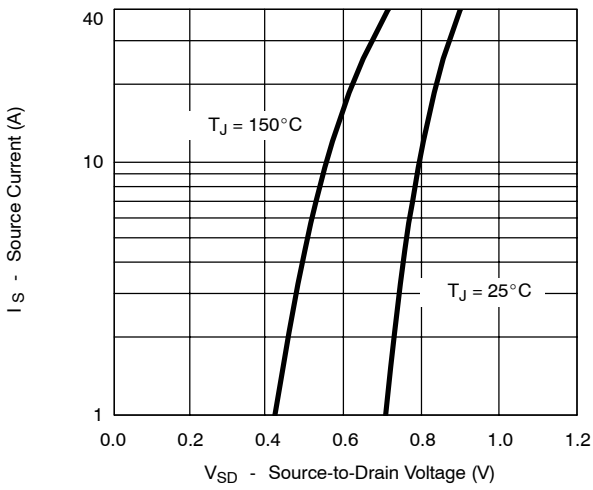
Gate Charge



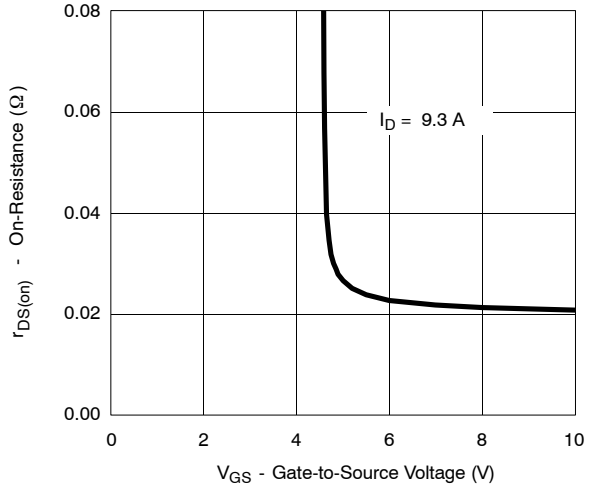
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

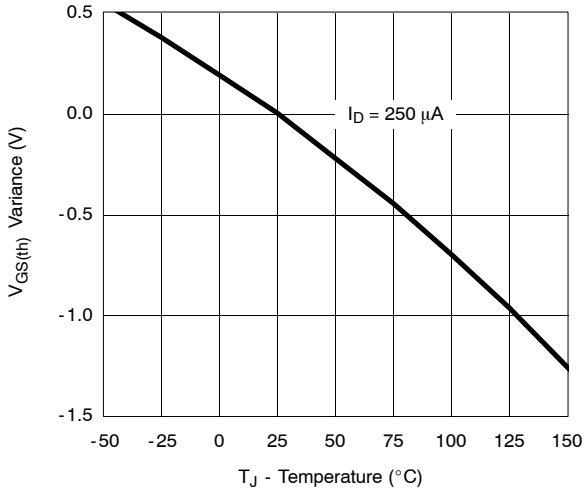


On-Resistance vs. Gate-to-Source Voltage

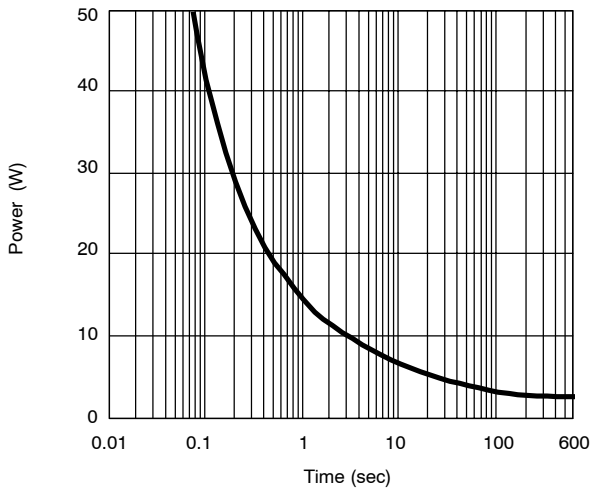


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

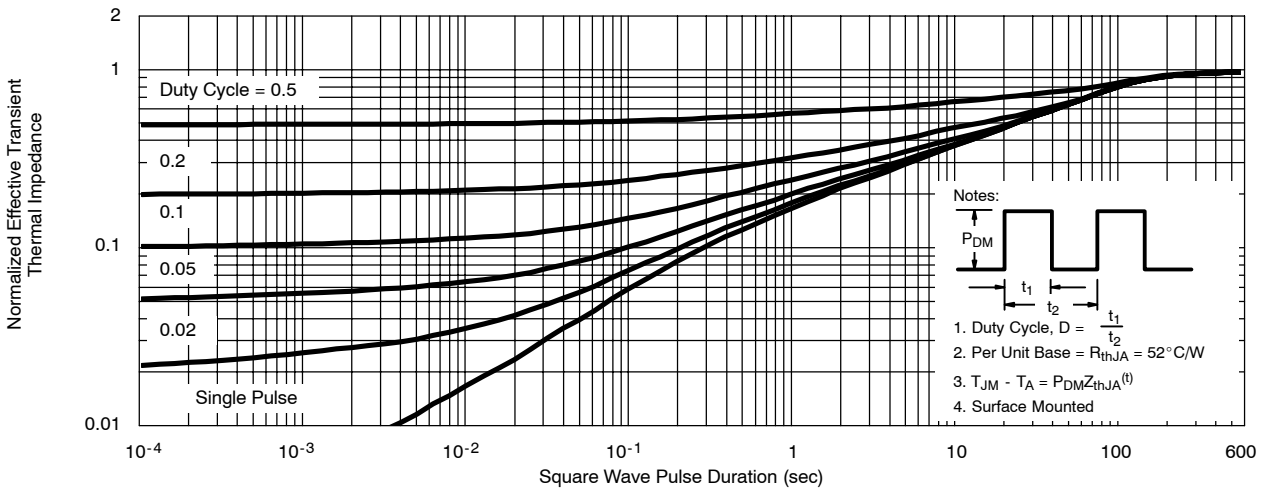
Threshold Voltage



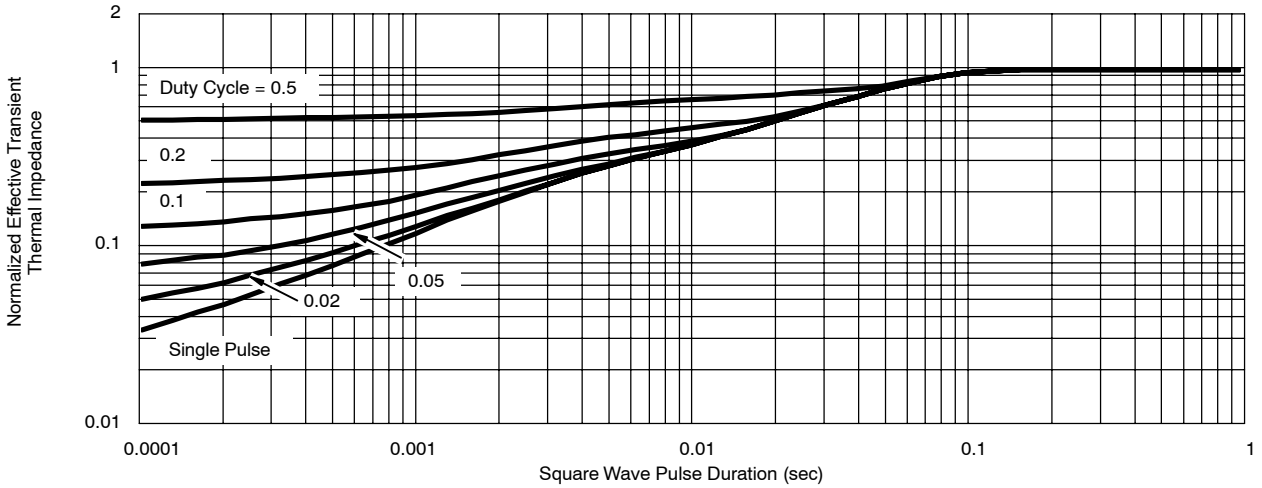
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



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