

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ P6

600V CoolMOS™ P6 Power Transistor
IPL60R360P6S

Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

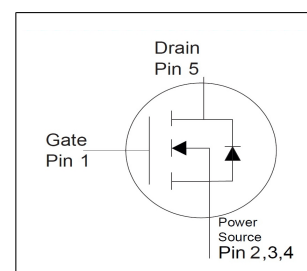
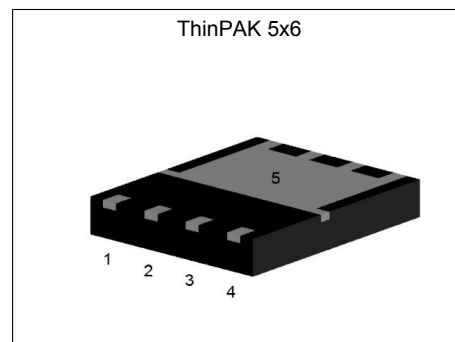


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.36	Ω
$Q_{g,typ}$	22	nC
$I_{D,pulse}$	30	A
$E_{oss@400V}$	3	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPL60R360P6S	ThinPAK 5x6 SMD	60P6360	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	11.3 7.1	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	30	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	247	mJ	$I_D = 2.1\text{A}$; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.37	mJ	$I_D = 2.1\text{A}$; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	2.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS} = 0 \dots 480\text{V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation (non FullPAK)	P_{tot}	-	-	89.3	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	9.8	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	29.7	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed ³⁾	di/dt	-	-	500	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$

3 Thermal characteristics

Table 3 Thermal characteristics (non FullPAK)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.4	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	35	62	$^\circ\text{C/W}$	Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm ² (one layer 70 μm thick) copper area for drain connection and cooling. PCB is vertical without blown air.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	reflow MSL1

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DCLink}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.50	4	4.50	V	$V_{DS}=V_{GS}$, $I_D=0.37mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=600V$, $V_{GS}=0V$, $T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.32	0.36	Ω	$V_{GS}=10V$, $I_D=4.5A$, $T_j=25^\circ C$ $V_{GS}=10V$, $I_D=4.5A$, $T_j=150^\circ C$
Gate resistance	R_G	-	6.7	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1010	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Output capacitance	C_{oss}	-	47	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	38	-	pF	$V_{GS}=0V$, $V_{DS}=0...480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	155	-	pF	$I_D=constant$, $V_{GS}=0V$, $V_{DS}=0...480V$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.6A$, $R_G=3.4\Omega$
Rise time	t_r	-	7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.6A$, $R_G=3.4\Omega$
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.6A$, $R_G=3.4\Omega$
Fall time	t_f	-	7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=5.6A$, $R_G=3.4\Omega$

Table 6 Gate charge characteristics

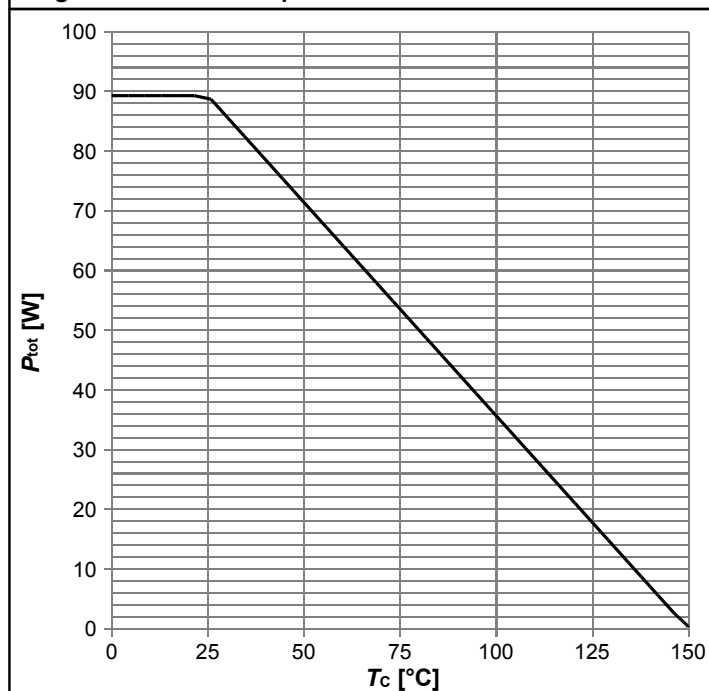
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6	-	nC	$V_{DD}=480V$, $I_D=5.6A$, $V_{GS}=0\text{ to }10V$
Gate to drain charge	Q_{gd}	-	8	-	nC	$V_{DD}=480V$, $I_D=5.6A$, $V_{GS}=0\text{ to }10V$
Gate charge total	Q_g	-	22	-	nC	$V_{DD}=480V$, $I_D=5.6A$, $V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	$V_{DD}=480V$, $I_D=5.6A$, $V_{GS}=0\text{ to }10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

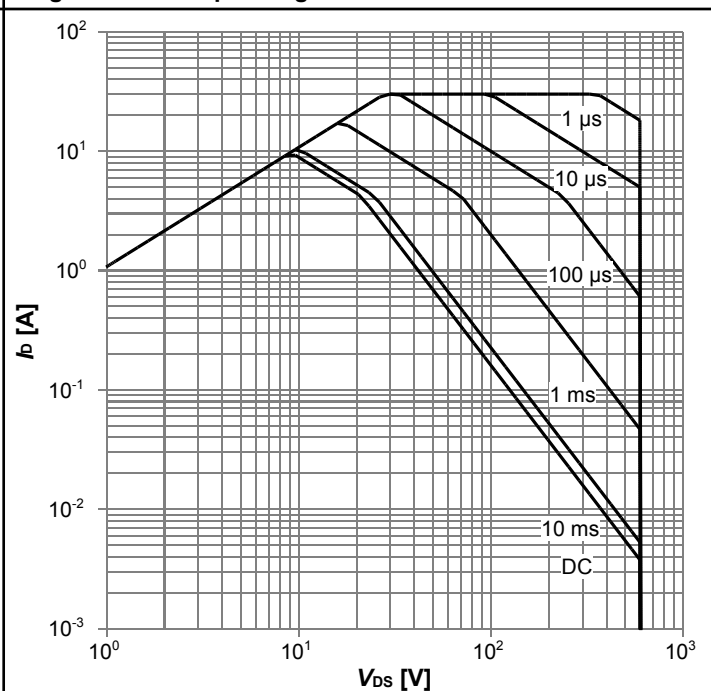
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=5.6A$, $T_i=25^{\circ}C$
Reverse recovery time	t_{rr}	-	257	-	ns	$V_R=400V$, $I_F=5.6A$, $di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	3	-	μC	$V_R=400V$, $I_F=5.6A$, $di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	18	-	A	$V_R=400V$, $I_F=5.6A$, $di_F/dt=100A/\mu s$

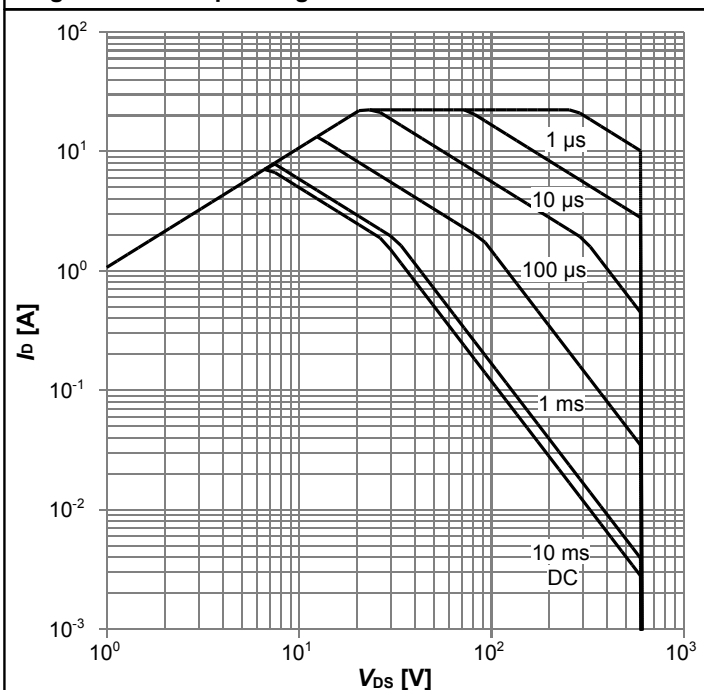
5 Electrical characteristics diagrams

Diagram 1: Power dissipation


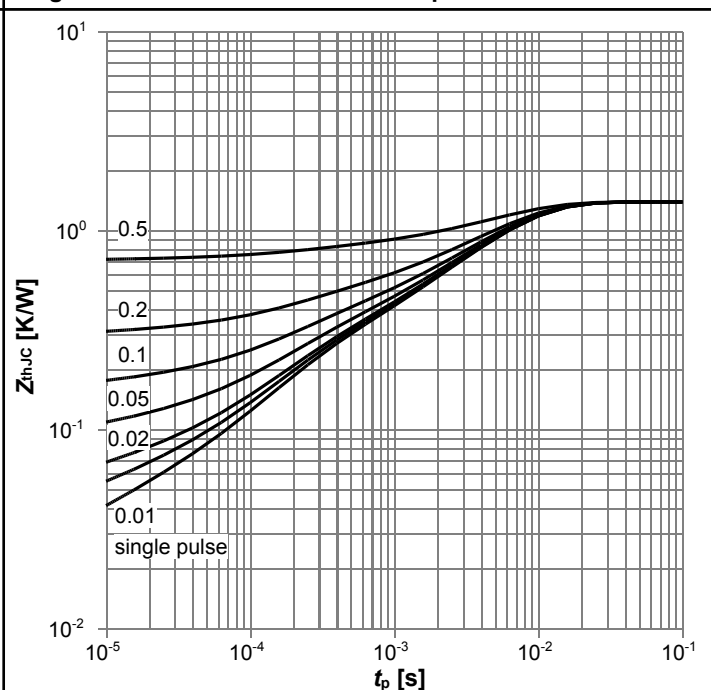
$$P_{tot}=f(T_c)$$

Diagram 2: Safe operating area


$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 3: Safe operating area


$$I_D=f(V_{DS}); T_c=80\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance


$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics

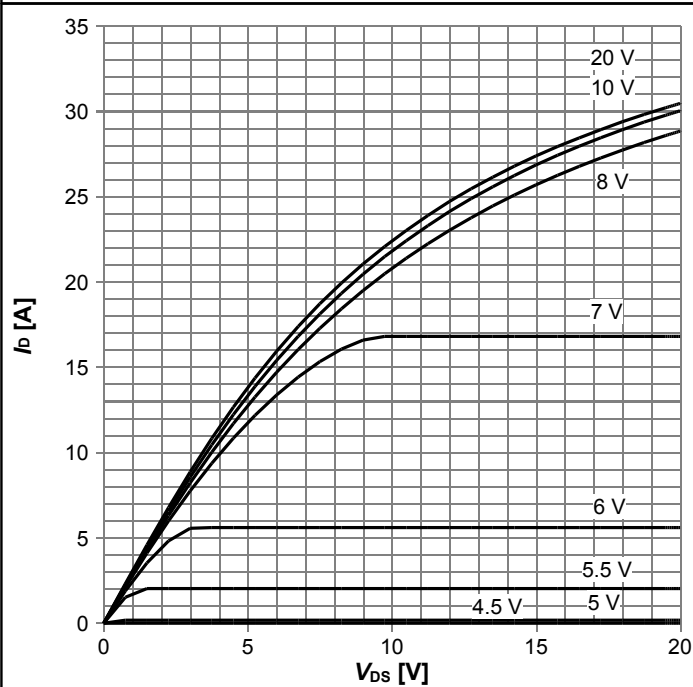

 $I_D = f(V_{DS})$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics

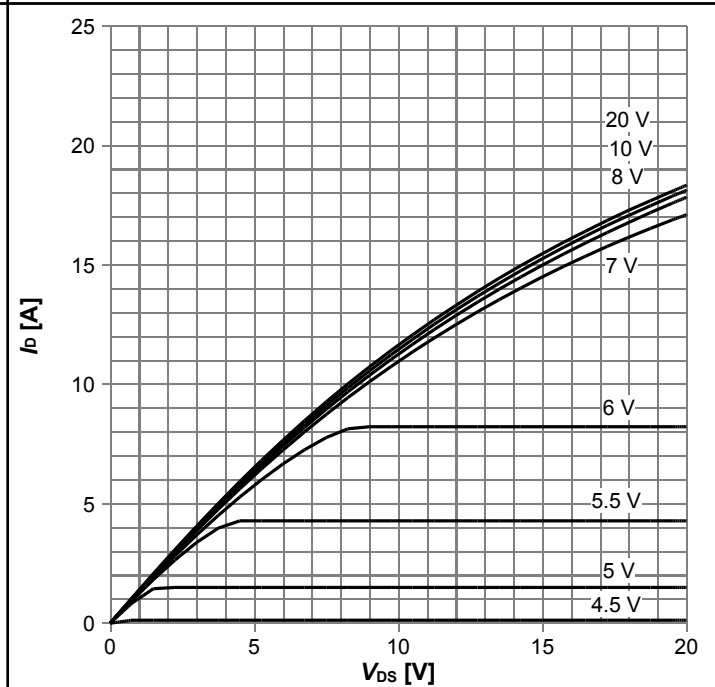

 $I_D = f(V_{DS})$; $T_J = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance

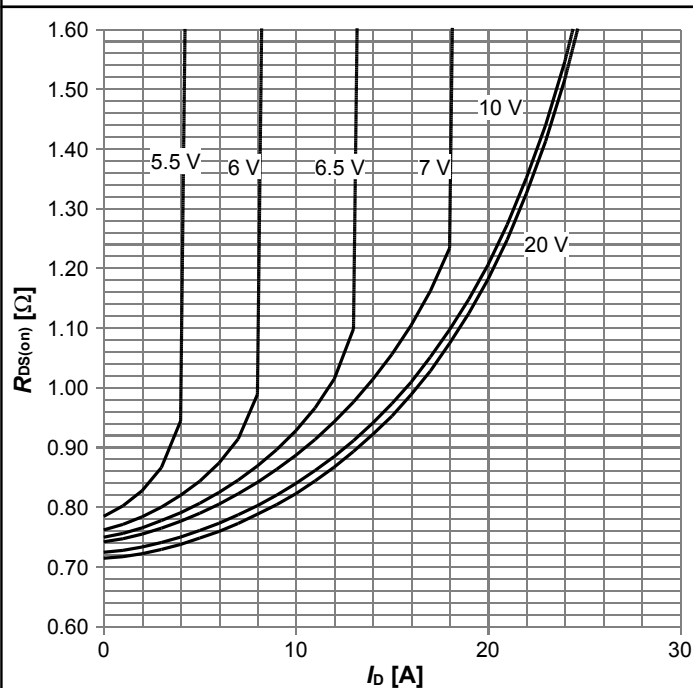

 $R_{DS(on)} = f(I_D)$; $T_J = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance

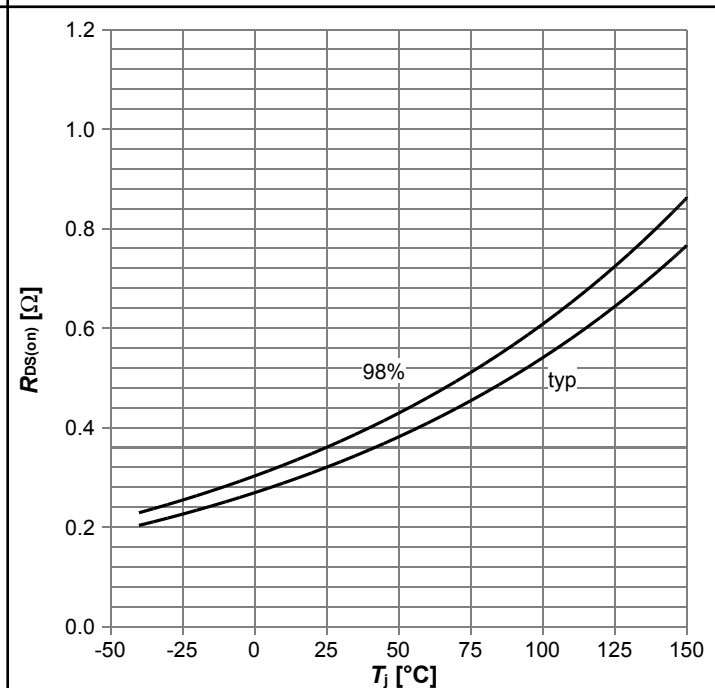

 $R_{DS(on)} = f(T_J)$; $I_D = 5.6\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics

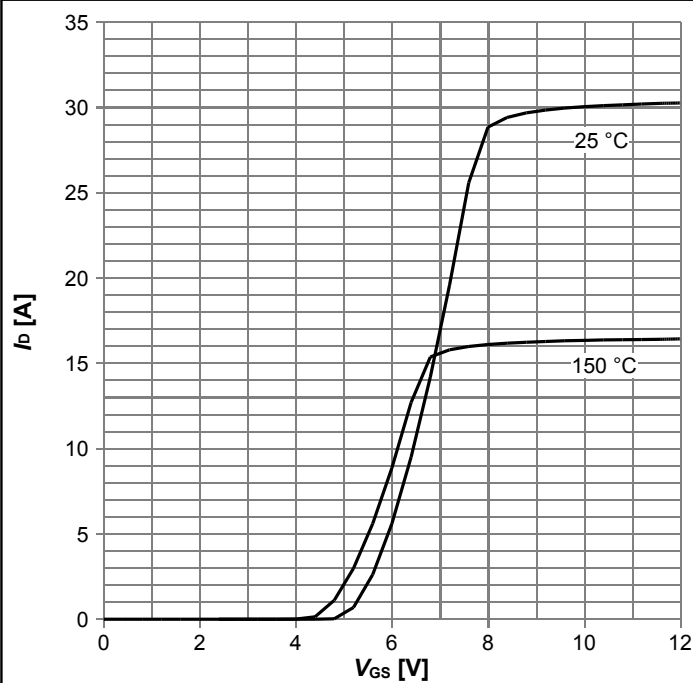

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

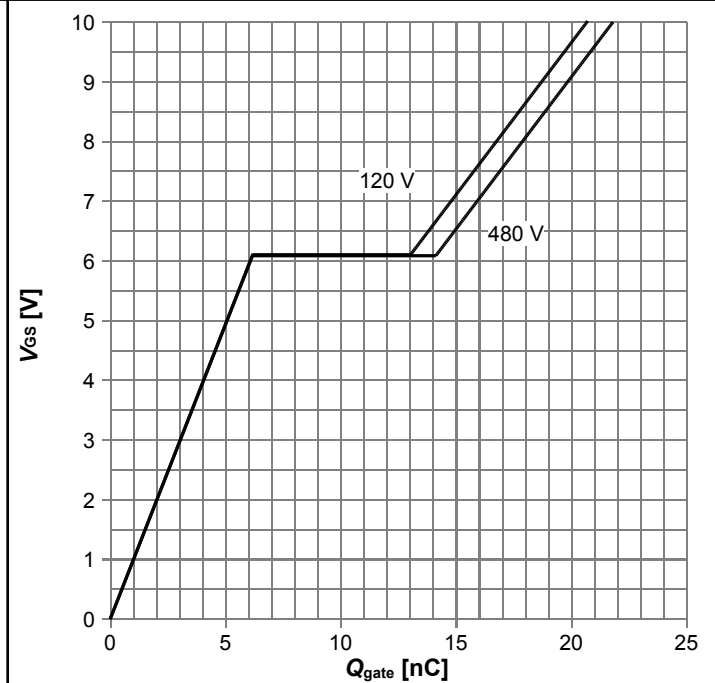

 $V_{GS} = f(Q_{gate}); I_D = 5.6 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode

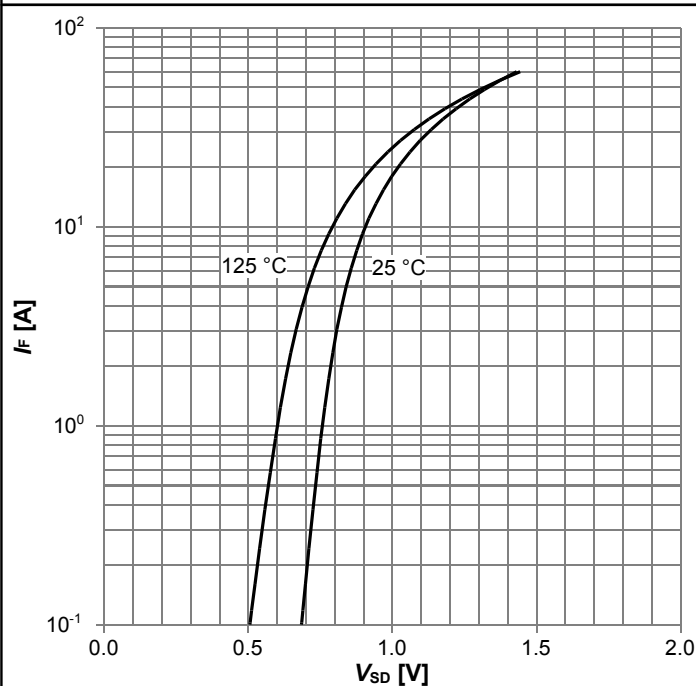

 $I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

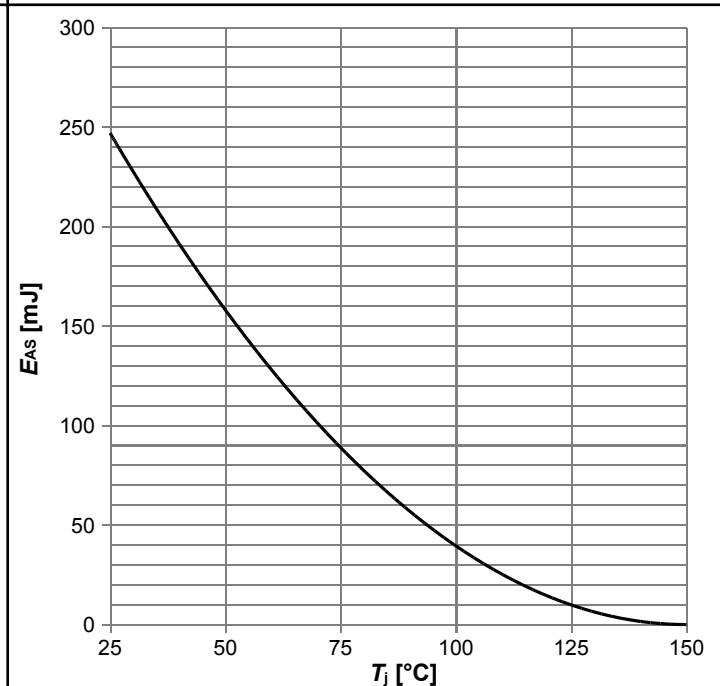
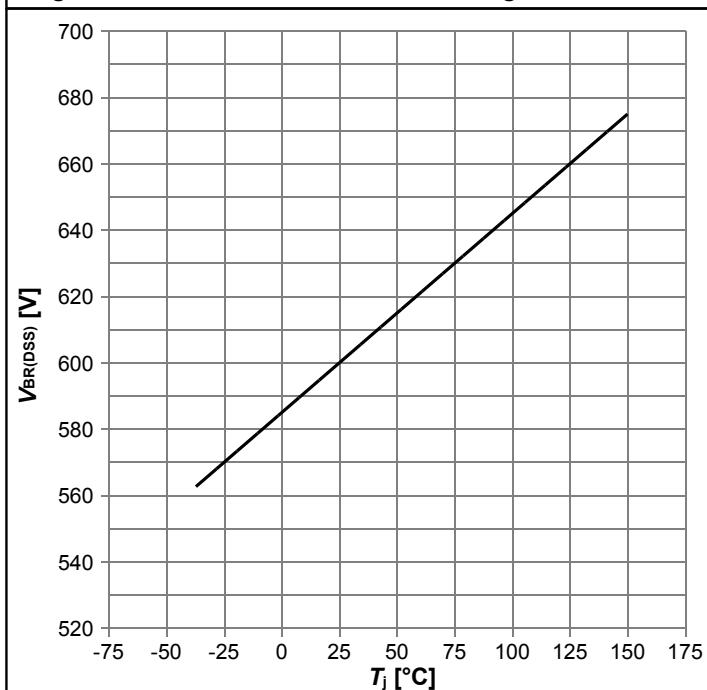
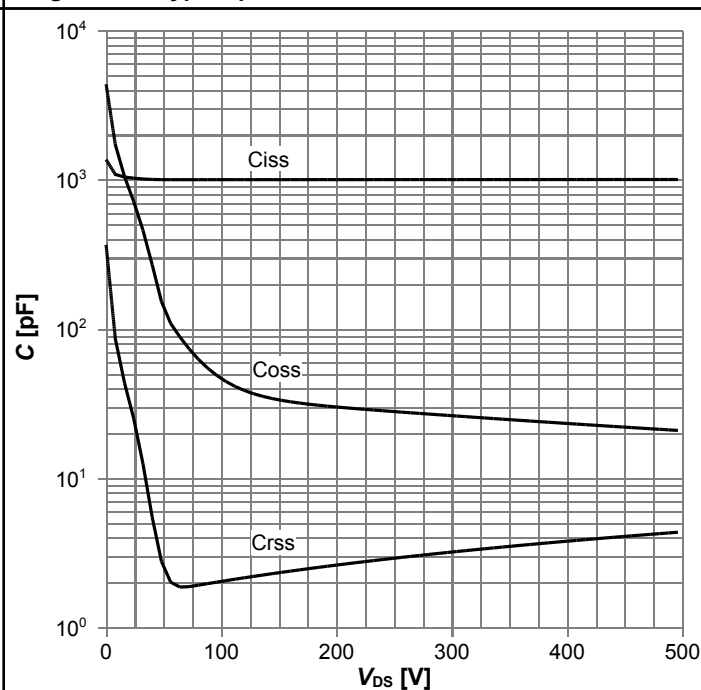

 $E_{AS} = f(T_j); I_D = 2.1 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



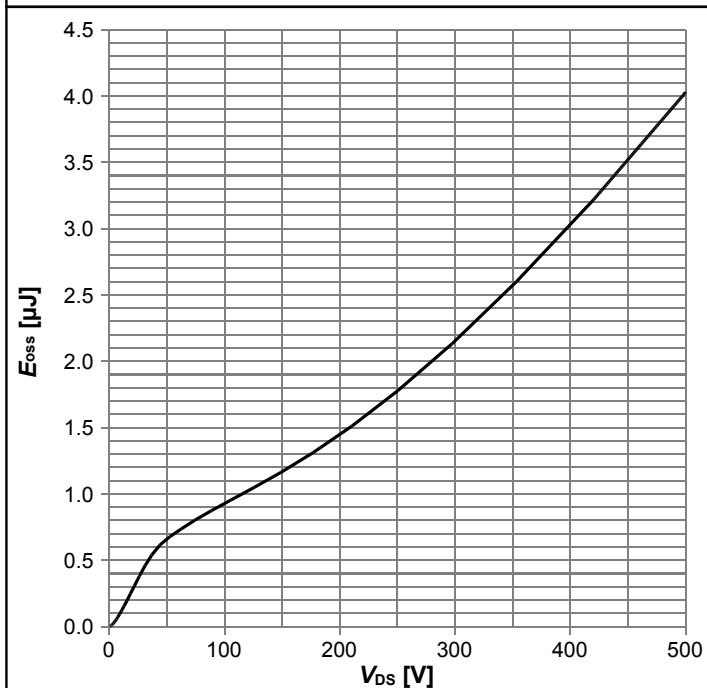
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$
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Table 9 Switching times

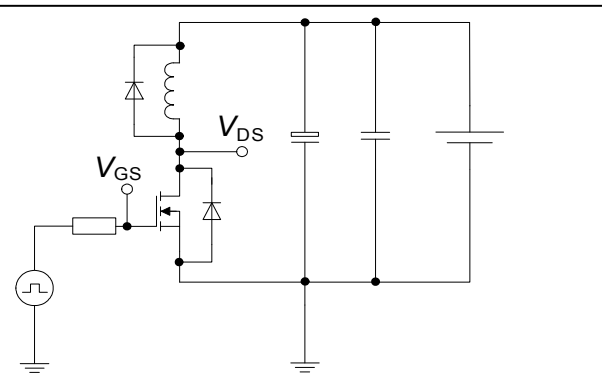
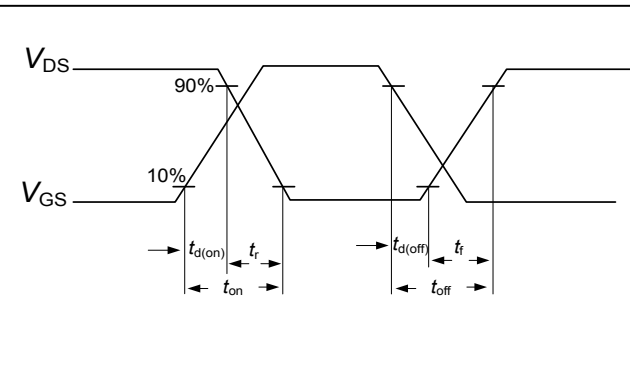
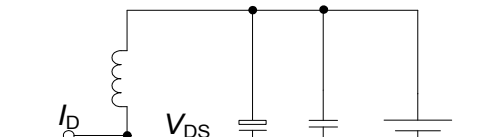
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a MOSFET switching an inductive load. A pulse generator is connected to the gate of the MOSFET through a resistor, with the gate voltage labeled V_{GS}. The MOSFET's drain is connected to a series combination of an inductor and a diode (for freewheeling). The load is connected to a DC voltage source. The drain-source voltage V_{DS} is measured across the inductor and diode. The MOSFET is shown with its internal body diode.	 The timing diagram shows the relationship between the drain-source voltage V_{DS} and the gate-source voltage V_{GS} during switching transitions. The V_{GS} signal is a square wave that transitions between a high level and a low level. The V_{DS} signal shows the voltage across the load during these transitions. Key points on the V_{DS} waveform are marked at 90% and 10% of the supply voltage. The switching times are defined as follows: $t_{d(on)}$: Delay time from the 10% V_{GS} threshold to the 90% V_{DS} threshold during turn-on. t_r: Rise time from the 90% V_{DS} threshold to the steady-state high level during turn-on. t_{on}: Total turn-on time from the 10% V_{GS} threshold to the steady-state high level. $t_{d(off)}$: Delay time from the 90% V_{DS} threshold to the 10% V_{GS} threshold during turn-off. t_f: Fall time from the 90% V_{DS} threshold to the steady-state low level during turn-off. t_{off}: Total turn-off time from the 90% V_{DS} threshold to the steady-state low level.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

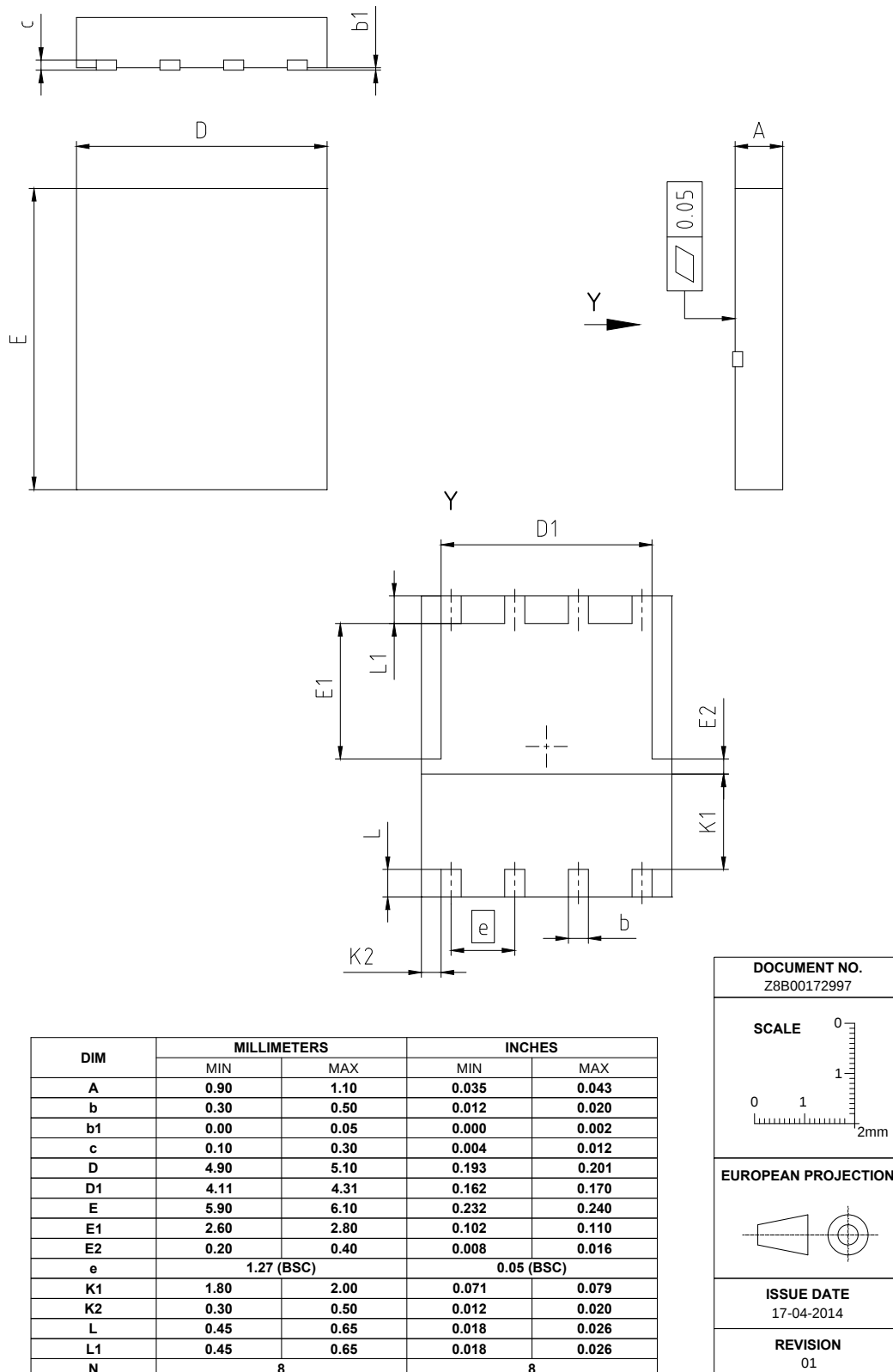


Figure 1 Outline ThinPAK 5x6 SMD, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPL60R360P6S

Revision: 2014-07-08, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-07-08	Release of final version

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