

Single Event Radiation Hardened High Speed, Current Mode PWM

IS-1845ASRH, IS-1845ASEH



The IS-1845ASRH, IS-1845ASEH are designed to be used in switching power supplies operating in current-mode. The rising edge of the on-chip oscillator turns on the output. Turn-off

is controlled by the current sense comparator and occurs when the sensed current reaches a peak controlled by the error amplifier.

Constructed with Intersil's Rad Hard Silicon Gate (RSG) dielectrically isolated BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide a high level of immunity to single event transients. All specified parameters are guaranteed and tested for 300krad(Si) total dose performance at a high dose rate and 50krad(Si) total dose at a low dose rate.

Detailed Electrical Specifications for these devices are contained in the SMD [5962-01509](#). A "hot-link" is also provided on our website for downloading the SMD.

Features

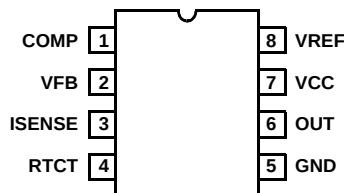
- Electrically Screened to DSCC SMD # [5962-01509](#)
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
 - High Dose Rate. 300 krad(Si) (Max)
 - Low Dose Rate 50 krad(Si) (Max)
 - SEL Immune Dielectrically Isolated
 - SEU Immune. 35MeV/mg/cm²
 - SEU Cross-Section at 89MeV/mg/cm². 5 x 10⁻⁶cm²
- Low Start-up Current 100µA (Typ)
- Fast Propagation Delay 80ns (Typ)
- Supply Voltage Range 12V to 20V
- High Output Drive. 1A (Peak, Typ)
- Undervoltage Lockout 8.8V Start (Typ), 8.2V Stop (Typ)

Applications

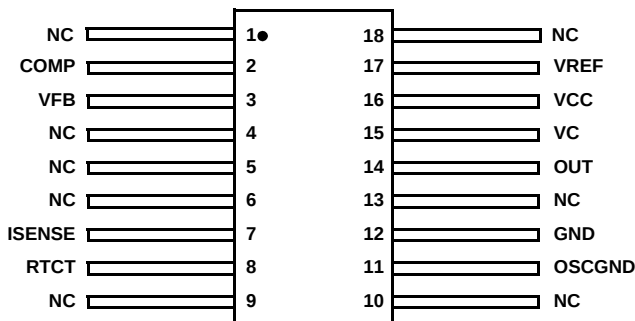
- Current-Mode Switching Power Supplies
- Control of High Current FET Drivers
- Motor Speed and Direction Control

Pin Configurations

IS7-1845ASRH, IS7-1845ASEH
(8 LD CDIP2-T8 SBDIP)
TOP VIEW



IS9-1845ASRH, IS9-1845ASEH
(18 LD FLATPACK)
TOP VIEW



NOTES:

1. Grounding the COMP pin does not inhibit the output. The output may be inhibited by applying >1.2V to the ISENSE pin.
2. This part should be operated with C_t = 3.3nF and R_t = 10k timing components only.

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962F0150901V9A	IS0-1845ASRH-Q	-50 to +125		
5962F0150902V9A	IS0-1845ASEH-Q	-50 to +125		
IS0-1845ASRH/Sample	IS0-1845ASRH/Sample	-50 to +125		
5962F0150901VPC	IS7-1845ASRH-Q	-50 to +125	8 Ld SBDIP	D8.3
5962F0150902VPC	IS7-1845ASEH-Q	-50 to +125	8 Ld SBDIP	D8.3
5962F0150901VPC	IS7-1845ASRH-QS9000	-50 to +125	8 Ld SBDIP	D8.3
5962F0150901QPC	IS7-1845ASRH-8	-50 to +125	8 Ld SBDIP	D8.3
5962F0150901QPC	IS7-1845ASRH-8S9000	-50 to +125	8 Ld SBDIP	D8.3
5962F0150901VXC	IS9-1845ASRH-Q	-50 to +125	18 Ld Flatpack	K18.B
5962F0150902VXC	IS9-1845ASEH-Q	-50 to +125	18 Ld Flatpack	K18.B
5962F0150901VXC	IS9-1845ASRH-QS9000	-50 to +125	18 Ld Flatpack	K18.B
5962F0150901QXC	IS9-1845ASRH-8	-50 to +125	18 Ld Flatpack	K18.B
IS7-1845ASRH/Proto	IS7-1845ASRH/Proto	-50 to +125	8 Ld SBDIP	D8.3
IS9-1845ASRH/Proto	IS9-1845ASRH/Proto	-50 to +125	18 Ld Flatpack	K18.3

Typical Performance Curves

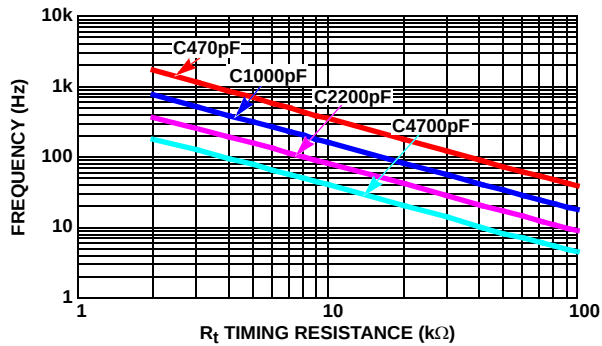


FIGURE 1. OSCILLATOR FREQUENCY vs R_t and C_t

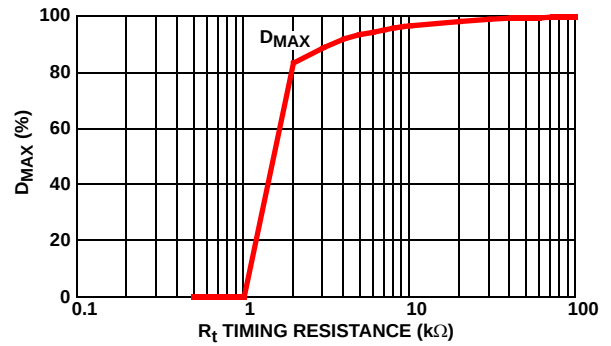


FIGURE 2. MAXIMUM DUTY CYCLE vs R_t

IS-1845ASRH, IS-1845ASEH

Die Characteristics

DIE DIMENSIONS

3090 μ m x 4080 μ m (121.6 mils x 159.0 mils)
Thickness: 483 μ m $\pm$ 25.4 μ m (19 mils $\pm$ 1 mil)

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kÅ $\pm$ 1.0kÅ

Top Metallization

Type: AlSiCu
Thickness: 16.0kÅ $\pm$ 2kÅ

Substrate

Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

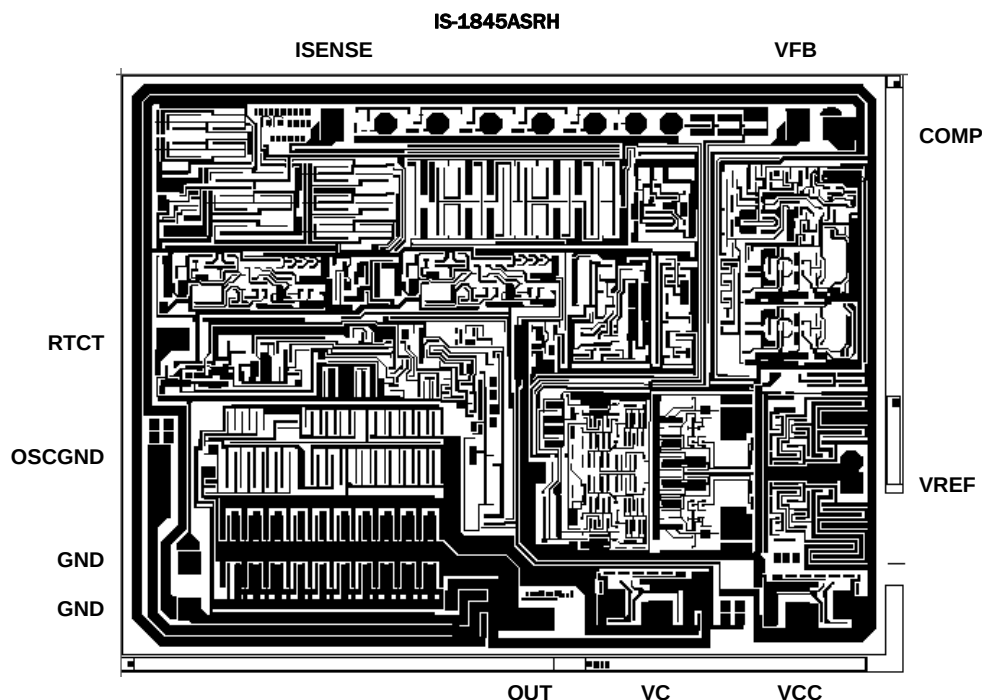
Worst Case Current Density

$<2.0 \times 10^5$ A/cm²

Transistor Count

582

Metallization Mask Layout



NOTES:

- Both the GND pads must be bonded to ground.
- The OUT double-sized bond pad must be double bonded for current sharing purposes.
- The OSCGND double-sized bond pad must be double bonded to ground for current sharing purposes.

For additional products, see www.intersil.com/product_tree

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