Freescale Semiconductor
Data Sheet: Product Preview

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MPC5553 Microcontroller Data Sheet

by: Microcontroller Division

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5553 microcontroller device. For functional characteristics, refer to the MPC5553/MPC5554 *Microcontroller Reference Manual*.

1 Overview

The MPC5553 microcontroller (MCU) is a member of the MPC5500 family of microcontrollers based on the PowerPC™ Book E architecture. This family of parts contains many new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement over the MPC500 family.

The host processor core of this device is compatible with the PowerPC Book E architecture. It is 100% user mode compatible (with floating point library) with the classic PowerPC instruction set. The Book E architecture has enhancements that improve the PowerPC architecture's fit in embedded applications. This core also has additional instructions, including digital signal processing (DSP) instructions, beyond the classic

Contents

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PowerPC instruction set. This family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The MPC5553 of the MPC5500 family has two levels of memory hierarchy. The fastest accesses are to the 8-kilobyte unified cache. The next level in the hierarchy contains the 64-kilobyte on-chip internal SRAM and 1.5 Mbyte internal Flash memory. Both the internal SRAM and the Flash memory can hold instructions and data. The external bus interface has been designed to support most of the standard memories used with the MPC5xx family.

The complex I/O timer functions of the MPC5500 family are performed by an enhanced time processor unit engine (eTPU). The eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing 24-bit timers, double action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU can be programmed using a high-level programming language.

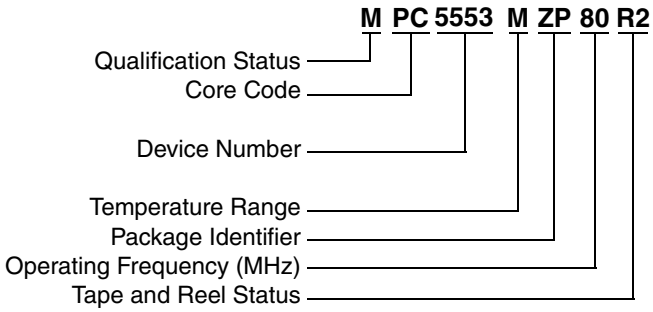
The less complex timer functions of the MPC5500 family are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single action, double action, pulse width modulation (PWM), and modulus counter operation. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPI), and enhanced serial communications interfaces (eSCIs). The DSPIs support pin reduction through hardware serialization and deserialization of timer channels and general-purpose input/output (GPIO) signals.

The MCU of the MPC5553 has an on-chip 40-channel enhanced queued dual analog-to-digital converter (eQADC).

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also found in the SIU. The internal multiplexer submodule (SIU_DISR) provides multiplexing of eQADC trigger sources, daisy chaining the DSPIs and external interrupt signal multiplexing.

2 Ordering Information



Temperature Range
M = -40° C to 125° C
A = -55° C to 125° C

Package Identifier
ZP = 416PBGA SnPb
VR = 416PBGA Pb-free
VF = 208MAPBGA SnPb
VM = 208MAPBGA Pb-free
ZQ = 324PBGA SnPb
VZ = 324PBGA Pb-free

Operating Frequency
80 = 80MHz
112 = 112MHz
132 = 132MHz

Tape and Reel Status
R2 = Tape and Reel
(blank) = Trays

Qualification Status
P = Pre Qualification
M = Full Spec Qualified

Note: Not all options are available on all devices. Refer to Table 1.

Figure 1. MPC5500 Family Part Number Example

Table 1. Orderable Part Numbers

Freescale Part Number	Description	Speed (MHz)	Max Speed[1] (MHz) (f_{MAX})	Temperature
MPC5553MVR132	MPC5553 Lead free 416 package	132	132	-40° C to 125° C
MPC5553MZP132	MPC5553 Lead 416 package	132	132	-40° C to 125° C
MPC5553MVZ132	MPC5553 Lead free 324 package	132	132	-40° C to 125° C
MPC5553MZQ132	MPC5553 Lead 324 package	132	132	-40° C to 125° C
MPC5553MVF132	MPC5553 Lead 208 package	132	132	-40° C to 125° C
MPC5553MVM132	MPC5553 Lead free 208 package	132	132	-40° C to 125° C
MPC5553MVR112	MPC5553 Lead free 416 package	112	114	-40° C to 125° C
MPC5553MZP112	MPC5553 Lead 416 package	112	114	-40° C to 125° C
MPC5553MVZ112	MPC5553 Lead free 324 package	112	114	-40° C to 125° C
MPC5553MZQ112	MPC5553 Lead 324 package	112	114	-40° C to 125° C
MPC5553MVF112	MPC5553 Lead 208 package	112	114	-40° C to 125° C
MPC5553MVM112	MPC5553 Lead free 208 package	112	114	-40° C to 125° C
MPC5553MVR80	MPC5553 Lead free 416 package	80	82	-40° C to 125° C
MPC5553MZP80	MPC5553 Lead 416 package	80	82	-40° C to 125° C
MPC5553MVZ80	MPC5553 Lead free 324 package	80	82	-40° C to 125° C
MPC5553MZQ80	MPC5553 Lead 324 package	80	82	-40° C to 125° C

Table 1. Orderable Part Numbers (continued)

MPC5553MVF80	MPC5553 Lead 208 package	80	82	-40° C to 125° C
MPC5553MVM80	MPC5553 Lead free 208 package	80	82	-40° C to 125° C

[1] Speed is the nominal maximum frequency. Max Speed is the maximum speed allowed including any frequency modulation. 80-MHz parts allow for 80 MHz + 2% modulation. However, 132-MHz allows only 128 MHz + 2% FM.

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	1.5V Core Supply Voltage [3]	V_{DD}	– 0.3	1.7	V
2	Flash Program/Erase Voltage	V_{PP}	– 0.3	6.5	V
3	Flash Core Voltage	V_{DDF}	– 0.3	1.7	V
4	Flash Read Voltage	V_{FLASH}	– 0.3	4.6	V
5	SRAM Standby Voltage	V_{STBY}	– 0.3	1.7	V
6	Clock Synthesizer Voltage	V_{DDSYN}	– 0.3	4.6	V
7	3.3V I/O Buffer Voltage	V_{DD33}	–0.3	4.6	V
8	Voltage Regulator Control Input Voltage	V_{RC33}	–0.3	4.6	V
9	Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	– 0.3	5.5	V
10	I/O Supply Voltage (Fast I/O Pads) [4]	V_{DDE}	– 0.3	4.6	V
11	I/O Supply Voltage (Slow/Medium I/O Pads) [4]	V_{DDEH}	– 0.3	6.5	V
12	DC Input Voltage[5] VDDEH powered I/O Pads, except eTPUB15 and SINB (DSPI_B_SIN) VDDEH powered I/O Pads (eTPUB15 and SINB) VDDE powered I/O Pads	V_{IN}	 –1.0[6] –0.3[7] –1.0[6]	 6.5[8] 6.5[8] 4.6[9]	V
13	Analog Reference High Voltage (reference to VRL)	V_{RH}	– 0.3	5.5	V
14	VSS Differential Voltage	$V_{SS} – V_{SSA}$	– 0.1	0.1	V
15	VDD Differential Voltage	$V_{DD} – V_{DDA}$	$– V_{DDA}$	V_{DD}	V
16	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	– 0.3	5.5	V
17	V_{RH} to VDDA Differential Voltage	$V_{RH} – V_{DDA}$	– 5.5	5.5	V
18	V_{RL} to VSSA Differential Voltage	$V_{RL} – V_{SSA}$	– 0.3	0.3	V
19	V_{DDEH} to V_{DDA} Differential Voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} Differential Voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	This spec has been moved to Table 9, spec 43a.				
22	VSSSYN to VSS Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V

Table 2. Absolute Maximum Ratings[1] (continued)

Num	Characteristic	Symbol	Min	Max[2]	Unit
23	V_{RCVSS} to V_{SS} Differential Voltage	$V_{RCVSS} - V_{SS}$	–0.1	0.1	V
24	Maximum DC Digital Input Current [10] (per pin, applies to all digital pins)[5]	I_{MAXD}	–2	2	mA
25	Maximum DC Analog Input Current [11] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum Operating Temperature Range [12] — Die Junction Temperature	T_J	– 40.0	150.0	°C
27	Storage Temperature Range	T_{STG}	– 55.0	150.0	°C
28	Maximum Solder Temperature [13]	T_{SDR}	—	260.0	°C
29	Moisture Sensitivity Level [14]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 1.5V +/– 10% for proper operation. This parameter is specified at a maximum junction temperature of 150C.

4 All functional non-supply I/O pins are clamped to VSS and VDDE or VDDEH.

5 AC signal over and undershoot of the input voltages of up to +/– 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

6 Internal structures will hold the voltage above –1.0 volt if the injection current limit of 1 mA is met.

7 Internal structures will not clamp to a safe voltage. External protection must be used to ensure that voltage on the pin stays above –0.3 volts.

8 Internal structures hold the input voltage below this maximum voltage on all pads powered by VDDEH supplies, if the maximum injection current specification is met (1 mA for all pins) and VDDEH is within Operating Voltage specifications.

9 Internal structures hold the input voltage below this maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met (1 mA for all pins) and VDDE is within Operating Voltage specifications.

10 Total injection current for all pins (including both digital and analog) must not exceed 25mA.

11 Total injection current for all analog input pins must not exceed 15mA.

12 Lifetime operation at these specification limits is not guaranteed.

13 Solder profile per CDF-AEC-Q100.

14 Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

Table 3. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	324 PBGA	416 PBGA
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	41	30	29
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	25	21	21

Table 3. Thermal Characteristics (continued)

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	324 PBGA	416 PBGA
3	Junction to Ambient [1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	33	24	23
4	Junction to Ambient [1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	22	17	18
5	Junction to Board [4] (Four layer board 2s2p)	$R_{\theta JB}$	°C/W	15	12	13
6	Junction to Case [5]	$R_{\theta JC}$	°C/W	7	8	9
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	°C/W	2	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal

performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted

to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- 1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- 2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
- 3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5553 is available in packaged form. Package options are listed in Section 2, “Ordering Information.”

Refer to Section 4, “Mechanicals,” for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications[1]

Num	Characteristic	Min. Value	Typ. Value	Max. Value	Unit
1	Scan Range	0.15	—	1000	MHz
2	Operating Frequency	—	—	132	MHz
3	V_{DD} Operating Voltages	—	1.5	—	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} Operating Voltages	—	3.3	—	V
5	VPP, VDDEH, VDDA Operating Voltages	—	5.0	—	V
6	Maximum Amplitude	—	—	14[2] 32[3]	dBuV
7	Operating Temperature	—	—	25	°C

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing is performed on the MPC5554 and applied to MPC5500 family as generic EMI performance data.

2 As measured with “single-chip” EMI program.

3 As measured with “expanded” EMI program.

3.5 ESD Characteristics

Table 5. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

3.6 VRC/POR Electrical Specifications

Table 6. VRC/POR Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Units
1	1.5V (VDD) POR Negated (Ramp Up) 1.5V (VDD) POR Asserted (Ramp Down)	V_POR15	1.1 1.1	1.35 1.35	V
2	3.3V (VDDSYN) POR Negated (Ramp Up) 3.3V (VDDSYN) POR Asserted (Ramp Down)	V_POR33	2.0 2.0	2.85 2.85	V
3	RESET Pin Supply (VDDEH6) POR Negated (Ramp Up) RESET Pin Supply (VDDEH6) POR Asserted (Ramp Down)	V_POR5	2.0 2.0	2.85 2.85	V
4	VRC33 voltage before regulator controller allows the pass transistor to start turning on	V_TRANS_START	1.0	2.0	V
5	VRC33 voltage when regulator controller allows the pass transistor to completely turn on[1, 2]	V_TRANS_ON	2.0	2.85	V
6	VRC33 voltage above which the regulator controller will keep the 1.5V supply in regulation[3, 4]	V_VRC33REG	3.0	—	V
7	Current which can be sourced by VRCCTL	I_VRCCTL[5]			mA
	– 40C		11.0	—	mA
	25C		9.0	—	mA
	150C (Tj)		7.5	—	mA
8	Voltage differential during power up that VDD33 can lag VDDSYN or $\overline{\text{VDDEH6}}$ before VDDSYN and $\overline{\text{VDDEH6}}$ reach V_POR33 and V_POR5 minimums respectively	VDD33_LAG	—	1.0	V
9	Absolute value of Slew Rate on power supply pins		—	50	V/ms
10	Required Gain: Idd / I_VRCCTL (@vdd = 1.35v, f_{sys} = 132MHz)[4, 6]	BETA[7]			
	– 40C		55.0[8]	—	—
	25C		58.0[8]	—	—
	150C (Tj)		70.0[8]	500	—

1 User must be able to supply full operating current for the 1.5V supply when the 3.3V supply reaches this range.

2 Current limit may be reached during ramp up and should not be treated as short circuit current.

3 At peak current for device.

4 Assumes that the Freescale recommended board requirements and transistor recommendations are met. Board signal traces/routing from the VRCCTL package signal to the base of the external pass transistor and between the emitter of the pass transistor to the VDD package signals should have a maximum of 100 nH inductance and minimal resistance (<1 ohm). VRCCTL should have a nominal 1μF phase compensation capacitor to ground. VDD should have a 20 μF (nominal) bulk capacitor (> 4 μF over all conditions, including lifetime). High frequency bypass capacitors consisting of eight 0.01 μF, two 0.1 μF, and one 1 μF capacitors should be place around the package on the VDD supply signals.

5 I_VRCCTL measured at the following conditions: VDD=1.35V, VRC33=3.1V, V_VRCCTL=2.2V.

6 Values are based on IDD from high use applications as explained in the IDD Electrical Specification.

7 BETA is measured on a per part basis and is calculated as IDD / I_VRCCTL and represents the worst case external transistor BETA.

8 Preliminary value. Final specification pending characterization.

3.7 Power Up/Down Sequencing

Power sequencing between the 1.5-V power supply and VDDSYN or the RESET power supplies is required if the user provides an external 1.5-V power supply and ties VRC33 to ground. To avoid this power sequencing requirement, power up VRC33 within the specified operating range, even if not using the on-chip voltage regulator controller. Refer to Section 3.7.1, "Power Up Sequence (If VRC33 Grounded)" and Section 3.7.2, "Power Down Sequence (If VRC33 Grounded)."

Another power sequencing requirement is that VDD33 must be of sufficient voltage before POR negates, so that the values on certain pins are treated as 1s when POR does negate. Refer to Section 3.7.3, "Input Value of Pins During POR Dependent on VDD33."

Although there is no power sequencing required between VRC33 and VDDSYN during power up, for the VRC stage turn-on to operate within specification, VRC33 must not lead VDDSYN by more than 600 mV or lag by more than 100 mV. Higher spikes in the emitter current of the pass transistor will occur if VRC33 leads or lags VDDSYN by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock will start to toggle, adding another large increase of the current consumption from VRC33. If VRC33 lags VDDSYN by more than 100 mV, this increased current consumption can drop VDD low enough to assert the 1.5-V POR again. Oscillations are even possible because when the 1.5-V POR asserts, the system clock stops, causing the voltage on VDD to rise until the 1.5-V POR negates again. Any oscillations stop when VRC33 is powered sufficiently.

When powering down, VRC33 and VDDSYN do not have a delta requirement to each other, because the bypass capacitors internal and external to the device are already charged.

When not powering up or down, VRC33 and VDDSYN do not have a delta requirement to each other for the VRC to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type), and Table 8 for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 7. Power Sequence Pin States (Fast Pads)

V_{DDE}	V_{DD33}	V_{DD}	pad_fc (Fast) Output Driver State	Comment
LOW	X	X	Low	Functional I/O pins are clamped to VSS and VDDE
VDDE	LOW	X	High	
VDDE	VDD33	LOW	High Impedance	POR asserted.
VDDE	VDD33	VDD	Functional	No POR asserted

Table 8. Power Sequence Pin States (Medium and Slow Pads)

V_{DDEH}	V_{DD}	pad_mh/pad_sh (Medium and Slow) Output Driver	Comment
LOW	X	Low	Functional I/O pins are clamped to VSS and VDDEH
VDDEH	LOW	High Impedance	POR asserted
VDDEH	VDD	Functional	No POR asserted

3.7.1 Power Up Sequence (If VRC33 Grounded)

In this case, the 1.5-V VDD supply must rise to 1.35-V before the 3.3-V VDDSYN and the RESET power supplies rises above 2.0 V. This ensures that digital logic in the PLL on the 1.5-V supply will not begin to operate below the specified operation range lower limit of 1.35 V. Since the internal 1.5-V POR is disabled, the internal 3.3-V POR or the RESET power POR must be depended on to hold the device in reset. Since they may negate as low as 2.0 V, it is necessary for VDD to be within spec before the 3.3-V POR and the RESET POR negate.

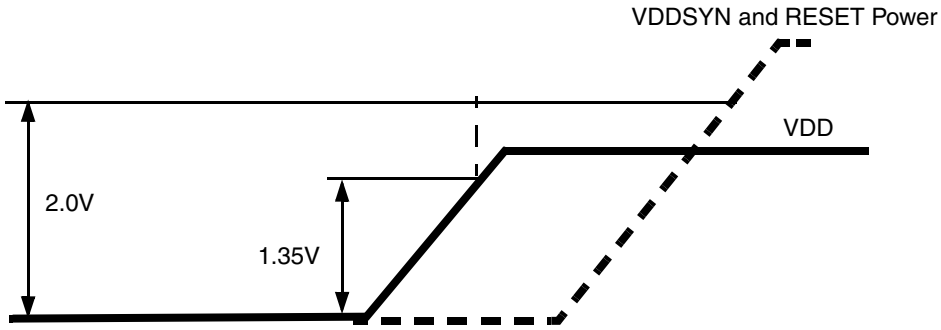


Figure 2. Power Up Sequence if VRC33 Grounded

3.7.2 Power Down Sequence (If VRC33 Grounded)

In this case, the only requirement is that if VDD falls below its operating range, VDDSYN or the RESET power must fall below 2.0 V before VDD is allowed to rise back into its operating range. This ensures that digital 1.5-V logic that is only reset by ORed_POR, which may have been affected by the 1.5V supply falling below spec, is reset properly.

3.7.3 Input Value of Pins During POR Dependent on VDD33

In order to avoid accidentally selecting the bypass clock because PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not treated as 1s when POR negates, VDD33 must not lag VDDSYN and the RESET pin power (VDDEH6) when powering the device by more than the VDD33 lag specification in Table 6. VDD33 individually can lag either VDDSYN or the RESET pin power (VDDEH6) by more than the VDD33 lag specification. VDD33 can lag one of the VDDSYN or VDDEH6 supplies, but cannot lag both by more than the VDD33 lag specification. This VDD33 lag specification only applies during power up. VDD33 has no lead or lag requirements when powering down.

3.8 DC Electrical Specifications

Table 9. DC Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage (average DC RMS voltage)	V_{DD}	1.35	1.65	V
2	I/O Supply Voltage (Fast I/O)	V_{DDE}	1.62	3.6	V
3	I/O Supply Voltage (Slow/Medium I/O)	V_{DDEH}	3.0	5.25	V
4	3.3V I/O Buffer Voltage	V_{DD33}	3.0	3.6	V
5	Voltage Regulator Control Input Voltage	V_{RC33}	3.0	3.6	V
6	Analog Supply Voltage[1]	V_{DDA}	4.5	5.25	V
8	Flash Programming Voltage[2]	VPP	4.5	5.25	V
9	Flash Read Voltage	VFLASH	3.0	3.6	V
10	SRAM Standby Voltage[3]	VSTBY	0.8	1.2	V
11	Clock Synthesizer Operating Voltage	VDDSYN	3.0	3.6	V
12	Fast I/O Input High Voltage	V_{IH_F}	0.65 * V_{DDE}	V_{DDE} + 0.3	V
13	Fast I/O Input Low Voltage	V_{IL_F}	V_{SS} – 0.3	0.35 * V_{DDE}	V
14	Medium/Slow I/O Input High Voltage	V_{IH_S}	0.65 * V_{DDEH}	V_{DDEH} + 0.3	V
15	Medium/Slow I/O Input Low Voltage	V_{IL_S}	V_{SS} – 0.3	0.35 * V_{DDEH}	V
16	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 * V_{DDE}		V
17	Medium/Slow I/O Input Hysteresis	V_{HYS_S}	0.1 * V_{DDEH}		V
18	Analog Input Voltage	V_{INDC}	VSSA – 0.3	VDDA + 0.3	V
19	Fast I/O Output High Voltage (I_{OH_F} = –2.0mA)	V_{OH_F}	0.8 * VDDE	—	V
20	Slow/Medium I/O Output High Voltage (I_{OH_S} = –2.0mA)	V_{OH_S}	0.8 * VDDEH	—	V
21	Fast I/O Output Low Voltage (I_{OL_F} = 2.0mA)	V_{OL_F}	—	0.2 * VDDE	V
22	Slow/Medium I/O Output Low Voltage (I_{OL_S} = 2.0mA)	V_{OL_S}	—	0.2 * VDDEH	V
23	Load Capacitance (Fast I/O)[4] DSC(SIU_PCR[8:9]) = 0b00 DSC(SIU_PCR[8:9]) = 0b01 DSC(SIU_PCR[8:9]) = 0b10 DSC(SIU_PCR[8:9]) = 0b11	C_L	 — — —	 10 20 30 50	 pF pF pF pF
24	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
25	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF

Table 9. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
26	Input Capacitance (Shared digital and analog pins AN12_MA0_SDS, AN12_MA1_SDO, AN14_MA2_SDI, and AN15_FCK)	C_{IN_M}	—	12	pF
27a	Operating Current[5] 1.5V Supplies @ 132MHz:				
	VDD (including VDDF max current)[6, 7] @1.65V Typical Use	IDD	—	550[9]	mA
	VDD (including VDDF max current)[6, 7] @1.35V Typical Use	IDD	—	450[9]	mA
	VDD (including VDDF max current) [7, 8] @1.65V High Use	IDD	—	600[9]	mA
	VDD (including VDDF max current)[7, 8]@1.35V High Use	IDD	—	490[9]	mA
27b	Operating Current [5]1.5V Supplies @ 114MHz:				
	VDD (including VDDF max current)[6, 7]@1.65V Typical Use	IDD	—	460[9]	mA
	VDD (including VDDF max current)[6, 7]@1.35V Typical Use	IDD	—	380[9]	mA
	VDD (including VDDF max current)[7, 8] @1.65V High Use	IDD	—	520[9]	mA
	VDD (including VDDF max current)[7, 8] @1.35V High Use	IDD	—	420[9]	mA
27c	Operating Current[5] 1.5V Supplies @ 82MHz:				
	VDD (including VDDF max current)[6, 7] @1.65V Typical Use	IDD	—	350[9]	mA
	VDD (including VDDF max current)[6, 7] @1.35V Typical Use	IDD	—	290[9]	mA
	VDD (including VDDF max current)[7, 8] @1.65V High Use	IDD	—	400[9]	mA
	VDD (including VDDF max current)[7, 8] @1.35V High Use	IDD	—	330[9]	mA
27d	IDD_{STBY} @ 25C				
	VSTBY @ 0.8V	IDD_{STBY}	—	20	µA
	VSTBY @ 1.0V	IDD_{STBY}	—	30	µA
	VSTBY @ 1.2V	IDD_{STBY}	—	50	µA
	IDD_{STBY} @ 60C				
	VSTBY @ 0.8V	IDD_{STBY}	—	70	µA
	VSTBY @ 1.0V	IDD_{STBY}	—	100	µA
	VSTBY @ 1.2V	IDD_{STBY}	—	200	µA
	IDD_{STBY} @ 150C (Tj)				
	VSTBY @ 0.8V	IDD_{STBY}	—	1200	µA
	VSTBY @ 1.0V	IDD_{STBY}	—	1500	µA
	VSTBY @ 1.2V	IDD_{STBY}	—	2000	µA
28	Operating Current 3.3V Supplies @ 132MHz:				
	VDD33[10]	IDD_{33}	—	2 + values derived from procedure of Footnote [10]	mA
	VFLASH	I_{VFLASH}	—	10	mA
	VDDSYN	I_{DDSYN}	—	15	mA

Table 9. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
29	Operating Current 5.0V Supplies @ 132MHz (12MHz ADCLK): VDDA (VDDA0 + VDDA1) Analog Reference Supply Current (VRH, VRL) VPP	 IDD_A I_{REF} I_{PP}	— — — —	 20.0 1.0 25	 mA mA mA
30	Operating Current VDDE[11] Supplies: VDDEH1 VDDE2 VDDE3 VDDEH4 VDDE5 VDDEH6 VDDE7 VDDEH8 VDDEH9	 IDD1 IDD2 IDD3 IDD4 IDD5 IDD6 IDD7 IDD8 IDD9	 — — — — — — — — —	 See Footnote [11] 	 mA mA mA mA mA mA mA mA mA
31	Fast I/O Weak Pull Up Current[12] 1.62V – 1.98V 2.25V – 2.75V 3.0V – 3.6V	I_{ACT_F}	 10 20 20	 110 130 170	 µA µA µA
	Fast I/O Weak Pull Down Current[12] 1.62V – 1.98V 2.25V – 2.75V 3.0V – 3.6V		 10 20 20	 100 130 170	 µA µA µA
32	Slow/Medium I/O Weak Pull Up/Down Current[13] 3.0V – 3.6V 4.5V – 5.5V	I_{ACT_S}	 10 20	 150 170	 µA µA
33	I/O Input Leakage Current[14]	I_{INACT_D}	– 2.5	2.5	µA
34	DC Injection Current (per pin)	I_{IC}	– 2.0	2.0	mA
35	Analog Input Current, Channel Off[15]	I_{INACT_A}	–150	150	nA
35a	Analog Input Current, Shared Analog/Digital pins (AN12, AN13, AN14, AN15)	I_{INACT_AD}	– 2.5	2.5	µA
36	VSS Differential Voltage[16]	VSS – VSSA	– 100	100	mV
37	Analog Reference Low Voltage	VRL	VSSA – 0.1	VSSA + 0.1	V
38	VRL Differential Voltage	VRL – VSSA	–100	100	mV
39	Analog Reference High Voltage	VRH	VDDA – 0.1	VDDA + 0.1	V
40	V_{REF} Differential Voltage	VRH – VRL	4.5	5.25	V
41	VSSSYN to VSS Differential Voltage	VSSSYN – VSS	–50	50	mV
42	VRCVSS to VSS Differential Voltage	VRCVSS – VSS	–50	50	mV
43	VDDF to VDD Differential Voltage[2]	VDDF – VDD	–100	100	mV

Table 9. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
43a	VRC33 to VDDSYN Differential Voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1[17]	V
44	Analog Input Differential Signal Range (with common mode 2.5V)	V_{IDIFF}	– 2.5	2.5	V
45	Operating Temperature Range — Ambient (Packaged)	T_A (T_L to T_H)	– 40.0	125.0	°C
46	Slew rate on power supply pins	—	—	50	V/ms

1 | VDDA0–VDDA1 | must be < 0.1V

2 VPP can drop to 3.0 volts during read operations.

3 During standby operation. If standby operation is not required, VSTBY can be connected to ground.

4 Applies to CLKOUT, external bus pins, and Nexus pins.

5 Maximum average RMS DC current.

6 Average current measured on Automotive benchmark.

7 Peak currents may be higher on specialized code.

8 High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents could be seen if an “idle” loop that crosses cache lines is run from cache. Code should be written to avoid this condition.

9 Preliminary. Final specification pending characterization.

10 Power requirements for the VDD33 supply are dependent on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See Table 11 for values to calculate power dissipation for specific operation.

11 Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

12 Absolute value of current, measured at V_{IL} and V_{IH}.

13 Absolute value of current, measured at V_{IL} and V_{IH}.

14 Weak pull up/down inactive. Measured at VDDE = 3.6 V and VDDEH = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

15 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types: pad_a and pad_ae.

16 VSSA refers to both VSSA0 and VSSA1. | VSSA0–VSSA1 | must be < 0.1V

17 Up to 0.6 volts during power up and power down.

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current[1]

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimated from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

3.8.2 I/O Pad VDD33 Current Specifications

The power consumption of the VDD33 supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin VDD33 currents for all I/O segments. The output pin VDD33 current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin VDD33 current can be calculated from Table 11 based on the voltage,

frequency, and load on all pad_sh and pad_sh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. VDD33 Pad Average DC Current[1]

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.7
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins only for the fast pads and to input pins only for the slow and medium pads.

2 All loads are lumped.

3.9 Oscillator & FMPLL Electrical Characteristics

Table 12. HiP7 FMPLL Electrical Specifications

(V_{DDSYN} = 3.0V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range: Crystal reference External reference Dual Controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys}/2$	MHz
2	System Frequency [1]	f_{sys}	$f_{ico(min)} \div 2^{RFD}$	f_{MAX} [2]	MHz
3	System Clock Period	t_{CYC}	—	1 / f_{sys}	ns
4	Loss of Reference Frequency [3]	f_{LOR}	100	1000	kHz
5	Self Clocked Mode (SCM) Frequency [4]	f_{SCM}	7.4	17.5	MHz
6	EXTAL Input High Voltage Crystal Mode [5] All other modes (Dual Controller (1:1), Bypass, External Reference)	 V_{IHEXT} V_{IHEXT}	 Vxtal + 0.4v ((VDDE5/2) + 0.4v)	 — —	 V V
7	EXTAL Input Low Voltage Crystal Mode [6] All other modes (Dual Controller (1:1), Bypass, External Reference)	 V_{ILEXT} V_{ILEXT}	 — —	 Vxtal – 0.4v ((VDDE5/2) – 0.4v)	 V V
8	XTAL Current [7]	I_{XTAL}	0.8	3	mA
9	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
12	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [8]	pF
13	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [8]	pF
14	PLL Lock Time[9]	t_{lpll}	—	750	µs
15	Dual Controller (1:1) Clock Skew (between CLKOUT and EXTAL) [10, 11]	t_{skew}	–2	2	ns
16	Duty Cycle of reference	t_{dc}	40	60	%
17	Frequency un-LOCK Range	f_{UL}	– 4.0	4.0	% f_{sys}
18	Frequency LOCK Range	f_{LCK}	– 2.0	2.0	% f_{sys}
19	CLKOUT Period Jitter,[12, 13] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5.0 .01	% f_{clkout}

Table 12. HiP7 FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
20	Frequency Modulation Range Limit [14] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.4	%f_{sys}
21	ICO Frequency. f_{ico}=[f_{ref}*(MFD+4)]/(PREDIV+1)[15]	f_{ico}	48	f_{sys}	MHz
22	Predivider Output Frequency (to PLL)	f_{PREDIV}	4	f_{MAX}	MHz

1 All internal registers retain data at 0 Hz.

2 Up to the maximum frequency rating of the device (see Table 1).

3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

4 Self clocked mode (SCM) frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured on the CLKOUT pin with the divider set to divide-by-2 of the system clock. NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

5 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, $V_{extal} - V_{xtal}$ >= 400mV criteria has to be met for oscillator's comparator to produce output clock.

6 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, $V_{xtal} - V_{extal}$ >= 400mV criteria has to be met for oscillator's comparator to produce output clock.

7 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

8 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively

9 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time will also include the crystal startup time.

10 PLL is operating in 1:1 PLL mode.

11 VDDE = 3.0 to 3.6V

12 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider set to divide-by-2.

13 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of jitter + Cmod.

14 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

15 $f_{sys} = f_{ico} / (2^{RFD})$

3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications (Operating)

Num	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency[1]	F_{ADCLK}	1	12	MHz
2	Conversion Cycles Differential Single Ended	CC	 13+2 (or 15) 14+2 (or 16)	 13+128 (or 141) 14+128 (or 142)	ADCLK cycles
3	Stop Mode Recovery Time[2]	T_{SR}	10	—	µs
4	Resolution[3]	—	1.25	—	mV
5	INL: 6 MHz ADC Clock	INL6	–4	4	Counts[3]
6	INL: 12 MHz ADC Clock	INL12	–8	8	Counts

Table 13. eQADC Conversion Specifications (Operating) (continued)

Num	Characteristic	Symbol	Min	Max	Unit
7	DNL: 6 MHz ADC Clock	DNL6	–3 [4]	3 [4]	Counts
8	DNL: 12 MHz ADC Clock	DNL12	–6 [4]	6 [4]	Counts
9	Offset Error with Calibration	OFFWC	–4 [5]	4 [5]	Counts
10	Full Scale Gain Error with Calibration	GAINWC	–8 [6]	8 [6]	Counts
11	Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
12	Incremental Error due to injection current. All channels have same 10kΩ < Rs <100kΩ Channel under test has Rs=10kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}	E_{INJ}	–4	4	Counts
13	Total Unadjusted Error for single ended conversions with calibration [11, 12, 13, 14, 15]	TUE	–4	4	Counts

1 Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800KS/s and the minimum value is based on 20MHz oscillator clock frequency divided by a maximum 16 factor.

2 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.

3 At VRH – VRL = 5.12 V, one lsb = 1.25 mV = one count

4 Guaranteed 10-bit monotonicity

5 The absolute value of the offset error without calibration ≤ 100 counts.

6 The absolute value of the full scale gain error without calibration ≤ 120 counts.

7 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5V$ and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.

10 Condition applies to two adjacent pads on the internal pad.

11 The TUE specification will always be better than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

12 TUE does not apply to differential conversions.

13 Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: –16 counts < TUE < 16 counts.

14 TUE includes all internal device error such as internal reference variation (75% Ref, 25% Ref)

15 Depending on the customer input impedance, the Analog Input Leakage current (DC Electrical specification 35a) may affect the actual TUE measured on analog channels AN12, AN13, AN14, AN15.

3.11 H7Fa Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications[1]

Num	Characteristic	Symbol	Min	Typ	Initial Max[2]	Max[3]	Unit
3	Double Word (64 bits) Program Time[4]	$T_{dwprogram}$	—	10	—	500	µs
4	Page Program Time[4]	$T_{pprogram}$	—	22	44[5]	500	µs
7	16 Kbyte Block Pre-program and Erase Time	$T_{16kpperase}$	—	265	400	5000	ms
9	48 Kbyte Block Pre-program and Erase Time	$T_{48kpperase}$	—	340	400	5000	ms

Table 14. Flash Program and Erase Specifications[1] (continued)

Num	Characteristic	Symbol	Min	Typ	Initial Max[2]	Max[3]	Unit
10	64 Kbyte Block Pre-program and Erase Time	$T_{64kpperase}$	—	400	500	5000	ms
8	128 Kbyte Block Pre-program and Erase Time	$T_{128kpperase}$	—	500	1250	15,000	ms
11	Minimum operating frequency for program and erase operations[6]	—	25	—	—	—	MHz

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Page size is 256 bits (8 words).

6 Read frequency of the flash can be up to the maximum operating frequency of the device. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life (Full Temperature Range)

Num	Characteristic	Symbol	Min	Typical[1]	Unit
1a	Number of Program/Erase cycles per block for 16 Kbyte, 48 Kbyte, and 64 Kbyte blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
1b	Number of Program/Erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	P/E	10,000	100,000	cycles
2	Data retention Blocks with 0 – 1,000 P/E cycles Blocks with 1,001 – 100,000 P/E cycles	Retention	 20 5	—	years

1 Typical endurance is evaluated at 25C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619 “Typical Endurance for Nonvolatile Memory.”

Table 16 shows the FLASH_BIU settings versus frequency of operation. Refer to the device Reference Manual for definitions of these bit-fields.

Table 16. FLASH_BIU Settings vs. Frequency of Operation

Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN	IPFEN	PFLIM	BFEN
up to and including 82 MHz[1]	0b001	0b001	0b01	0b00, 0b01, or 0b11[2]	0b00, 0b01, or 0b11[2]	0b000-0b110[3]	0b0, 0b1[4]
up to and including 102 MHz[5]	0b001	0b010	0b01	0b00, 0b01, or 0b11[2]	0b00, 0b01, or 0b11[2]	0b000-0b110[3]	0b0, 0b1[4]
up to and including132 MHz[6]	0b010	0b011	0b01	0b00, 0b01, or 0b11[2]	0b00, 0b01, or 0b11[2]	0b000-0b110[3]	0b0, 0b1[4]
Default Setting after Reset	0b111	0b111	0b11	0b00	0b00	0b000	0b0

1 This setting allows for 80 MHz system clock with 2% frequency modulation.

2 For maximum flash performance, this should be set to 0b11.
3 For maximum flash performance, this should be set to 0b110.
4 For maximum flash performance, this should be set to 0b1.
5 This setting allows for 100 MHz system clock with 2% frequency modulation.
6 This setting allows for 128 MHz system clock with 2% frequency modulation.

3.12 AC Specifications

3.12.1 Pad AC Specifications

Table 17. Pad AC Specifications (VDDEH = 5.0V, VDDE = 1.8V)[1]

Num	Pad	SRC/DSC	Out Delay[2, 3, 4] (ns)	Rise/Fall[4, 5] (ns)	Load Drive (pF)
1	Slow High Voltage (SH)	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200
2	Medium High Voltage (MH)	11	16	8	50
			43	30	200
		01	34	15	50
			61	35	200
		00	192	100	50
			239	125	200
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDE = 1.62V to 1.98V, VDDEH = 4.5V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH.
2 This parameter is supplied for reference and is not guaranteed by design and not tested.
3 Out delay is shown in Figure 3. Add a maximum of one system clock to the output delay for delay with respect to system clock.
4 Delay and rise/fall are measured to 20% or 80% of the respective signal.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.

Table 18. De-rated Pad AC Specifications (VDDEH = 3.3V, VDDE = 3.3V)[1]

Num	Pad	SRC/DSC	Out Delay[2, 3, 4] (ns)	Rise/Fall[3, 5] (ns)	Load Drive (pF)
1	Slow High Voltage (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium High Voltage (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9500	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDE = 3.0V to 3.6V, VDDEH = 3.0V to 3.6V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 Out delay is shown in Figure 3. Add a maximum of one system clock to the output delay for delay with respect to system clock.

5 This parameter is guaranteed by characterization before qualification rather than 100% tested.

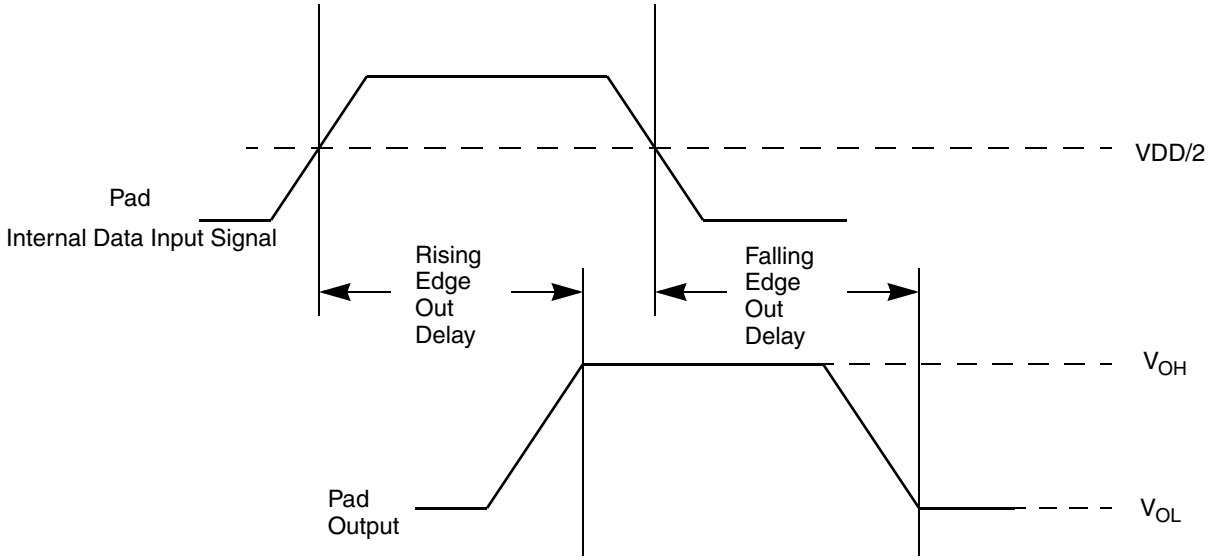


Figure 3. Pad Output Delay

3.13 AC Timing

3.13.1 Reset and Configuration Pin Timing

Table 19. Reset and Configuration Pin Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{CYC}
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{CYC}
3	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ Hold Time from $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{CYC}

[1] Reset timing specified at F_{SYS} = 132MHz, VDDEH = 3.0V to 5.25V, VDD = 1.35V to 1.65V, T_A = TL to TH.

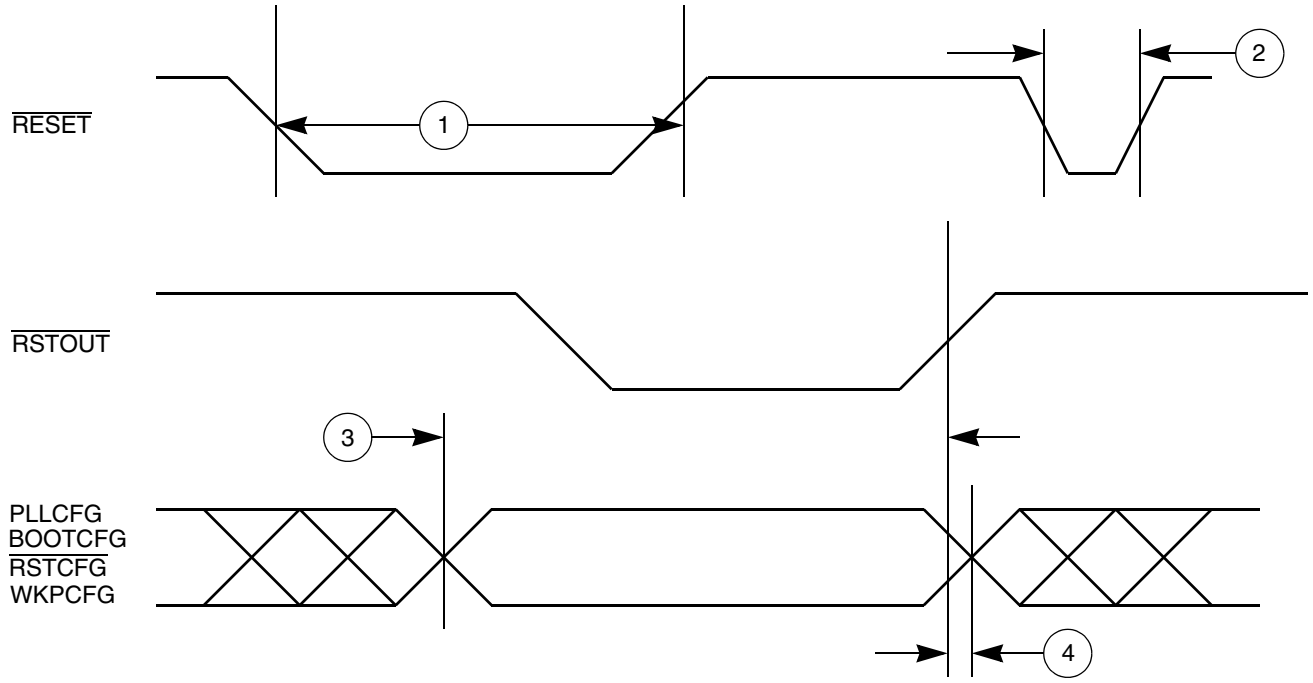


Figure 4. Reset and Configuration Pin Timing

3.13.2 IEEE 1149.1 Interface Timing

Table 20. JTAG Pin AC Electrical Characteristics[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at VDDE/2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	20	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at VDD = 1.35V to 1.65V, VDDE = 3.0V to 3.6V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 30pF with DSC = 0b10, SRC = 0b11. See Table 21 for functional specifications.

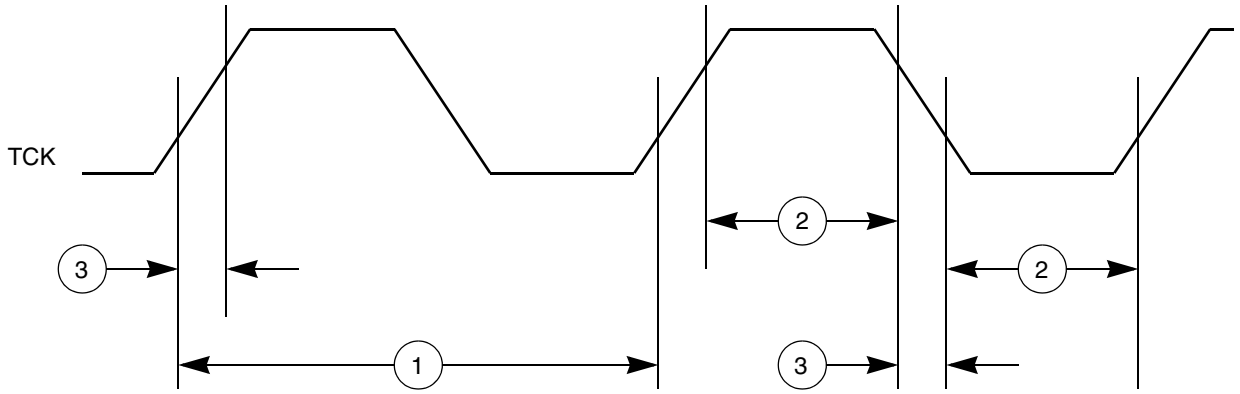


Figure 5. JTAG Test Clock Input Timing

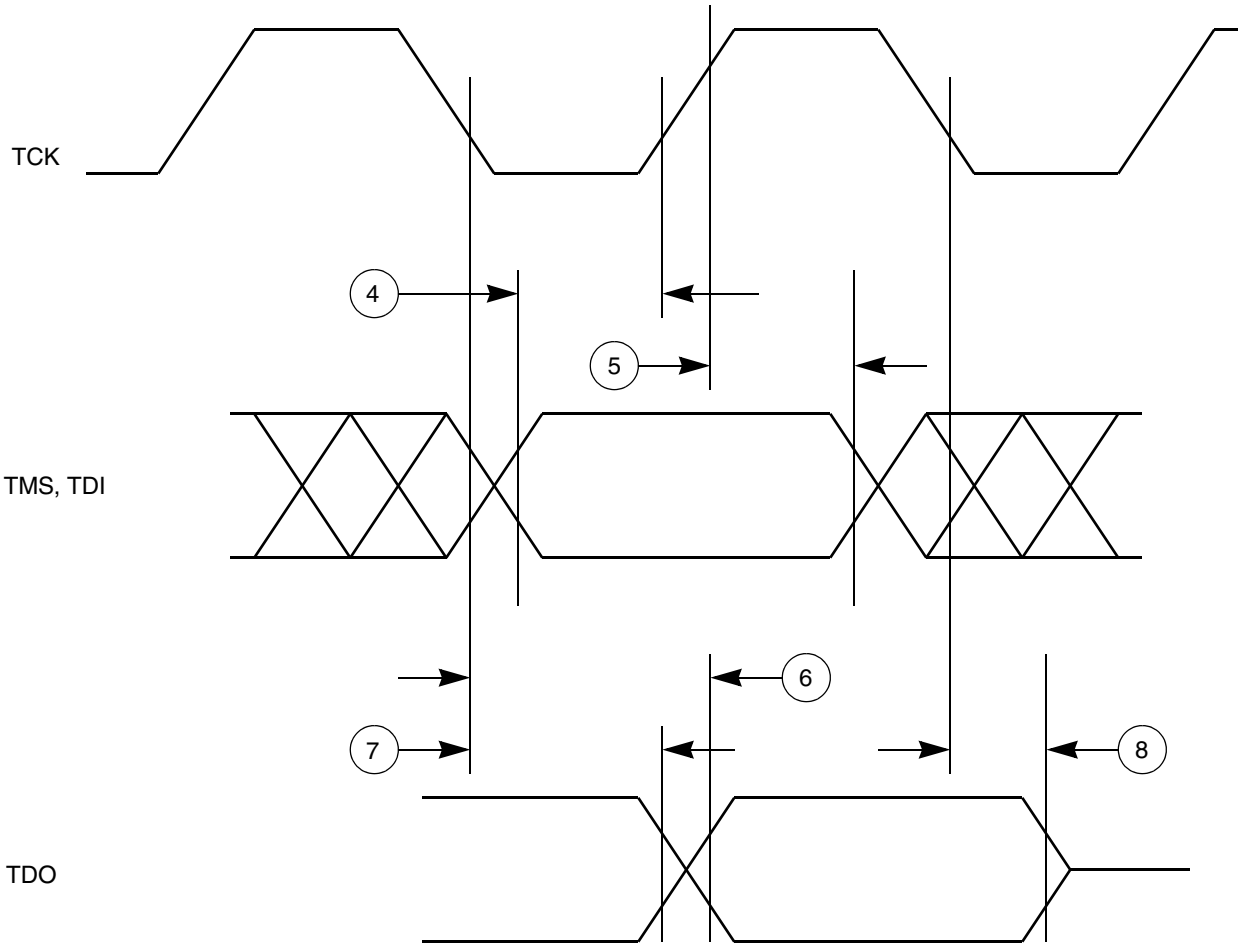


Figure 6. JTAG Test Access Port Timing

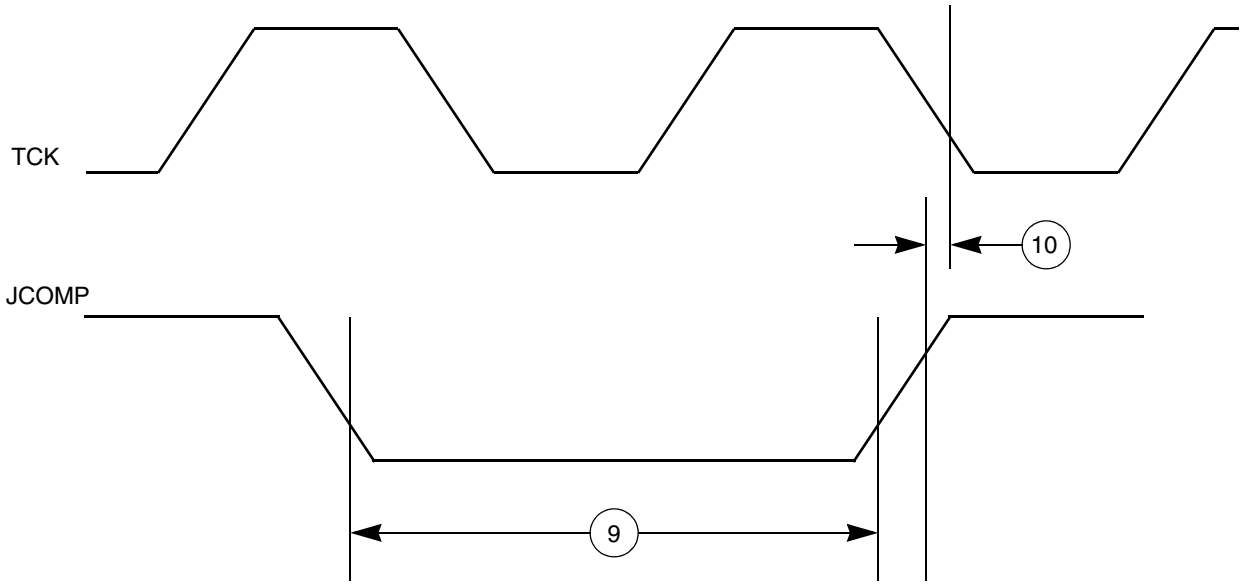


Figure 7. JTAG JCOMP Timing

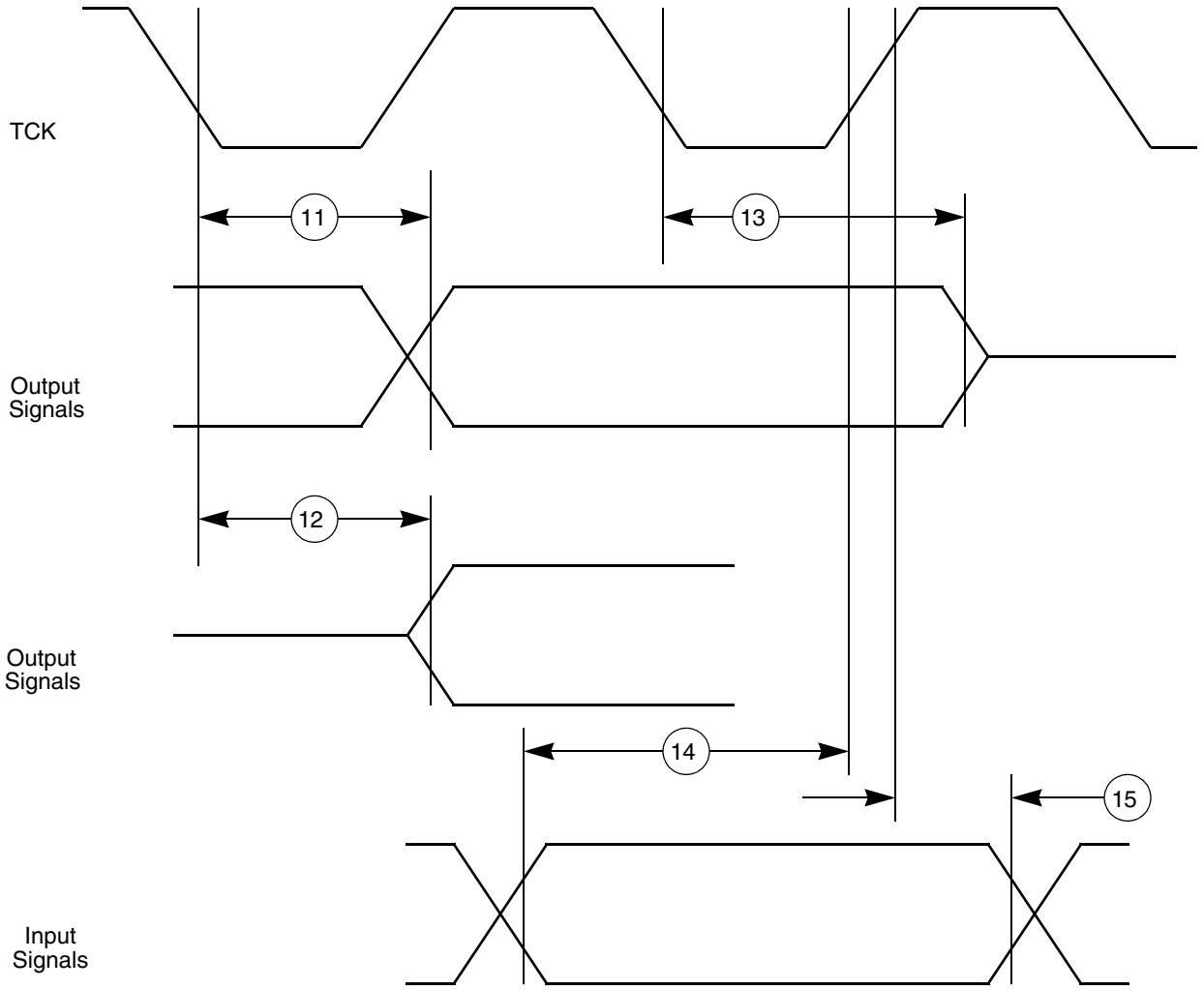


Figure 8. JTAG Boundary Scan Timing

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	1[2]	8	t_{CYC}
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4[4]	—	t_{CYC}
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{JOV}			
	VDDE = 2.25 to 3.0 volts		0	12	ns
	VDDE = 3.0 to 3.6 volts		0	9	ns
13	$\overline{\text{RDY}}$ Valid to MCKO[5]	—	—	—	—

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at VDD = 1.35V to 1.65V, VDDE = 2.25V to 3.6V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 30pF with DSC = 0b10.

2 The Nexus AUX port can only run up to 82MHz. The NPC_PCR[MCKO_DIV] must be set to divide by 2 if the system frequency is above 82MHz

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

4 The maximum frequency must be limited to approximately 16 MHz (VDDE= 2.25 to 3.0 volts) or 22 MHz (VDDE= 3.0 to 3.6 volts) to meet the timing specification for t_{JOV} of 0.2 x t_{JCYC} as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

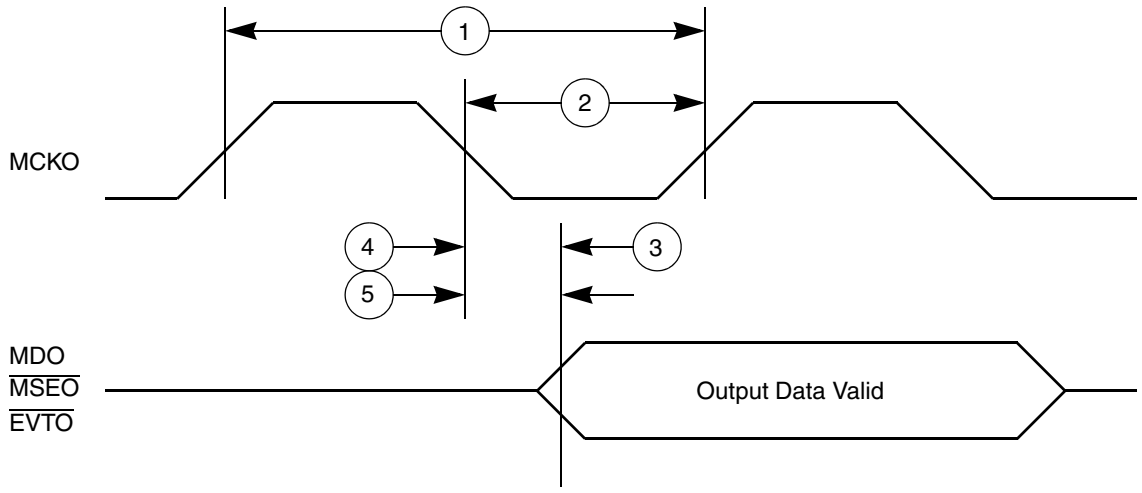


Figure 9. Nexus Output Timing

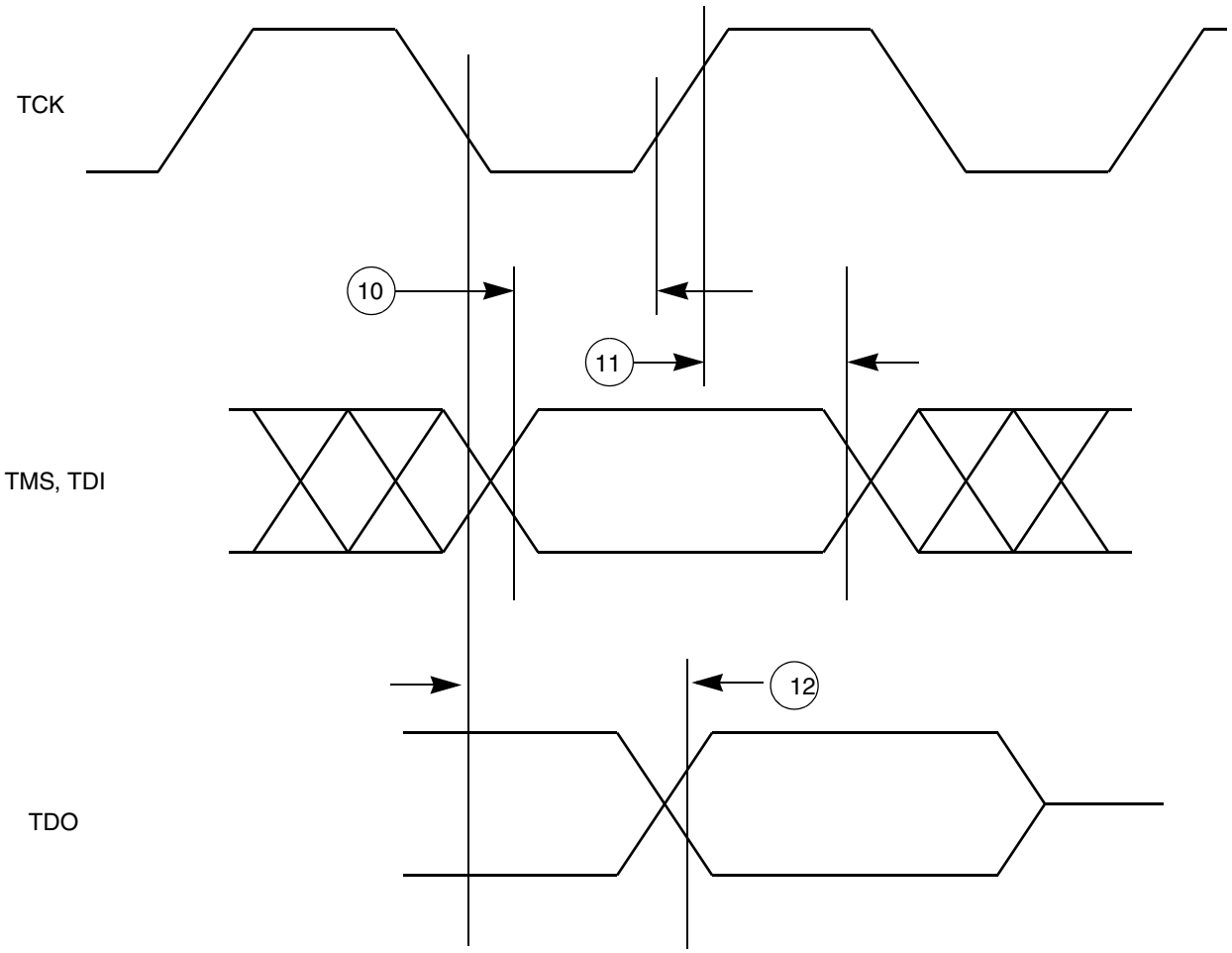


Figure 10. Nexus TDI, TMS, TDO Timing

3.13.4 External Bus Interface (EBI) Timing

Table 22. Bus Operation Timing[1]

#	Characteristic/Description	Symbol	40 MHz (ext. bus)[2]		56 MHz (ext. bus)[2]		66 MHz (ext. bus)[2]		Unit	Notes
			Min	Max	Min	Max	Min	Max		
1	CLKOUT Period	T_C	25.0	—	17.9	—	15.2	—	ns	Signals are measured at 50% VDDE.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	—	—[3]	—	—[3]	—	—[3]	ns	
4	CLKOUT fall time	t_{CFT}	—	—[3]	—	—[3]	—	—[3]	ns	
5	CLKOUT Positive Edge to Output Signal Invalid or High Z (Hold Time) ADDR[8:31] BDIP BG[4] BR[5] CS[0:3] DATA[0:31] OE RD_WR TA TEA TS TSIZ[0:1] $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	t_{COH}	1.0[6]/ 1.5	—	1.0[6]/ 1.5	—	1.0[6]/ 1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS=0/EBTS=1
6	CLKOUT Posedge to Output Signal Valid (Output Delay) ADDR[8:31] BDIP BG[4] BR[5] CS[0:3] DATA[0:31] OE RD_$\overline{WR}$ TA TEA TS TSIZ[0:1] $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	t_{COV}	—	10.0[6]/ 11.0	—	7.5[6]/ 8.5	—	6.0[6]/ 7.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS=0/EBTS=1

Table 22. Bus Operation Timing[1] (continued)

#	Characteristic/Description	Symbol	40 MHz (ext. bus)[2]		56 MHz (ext. bus)[2]		66 MHz (ext. bus)[2]		Unit	Notes
			Min	Max	Min	Max	Min	Max		
7	Input Signal Valid to CLKOUT Posedge (Setup Time) ADDR[8:31] BB BG[5] BR[5] DATA[0:31] RD_$\overline{WR}$ TA TEA TS TSIZ[0:1]	t_{CIS}	10.0	—	7.0	—	5.0	—	ns	
8	CLKOUT Posedge to Input Signal Invalid (Hold Time) ADDR[8:31] BB BG[5] BR[5] DATA[0:31] RD_$\overline{WR}$ TA TEA TS TSIZ[0:1]	t_{CIH}	1.0	—	1.0	—	1.0	—	ns	

1 EBI timing specified at VDD = 1.35V to 1.65V, VDDE = 1.6V to 3.6V (unless stated otherwise), VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 30pF with DSC = 0b10.

2 The external bus is limited to half the speed of the internal bus.

3 Refer to Fast Pad timing in Table 17 and Table 18 (different values for 1.8V vs 3.3V).

4 Internal Arbitration

5 External Arbitration

6 The EBTS=0 timings are only valid/ tested at VDDE=2.25-3.6V, whereas EBTS=1 timings are valid/tested at 1.6–3.6V.

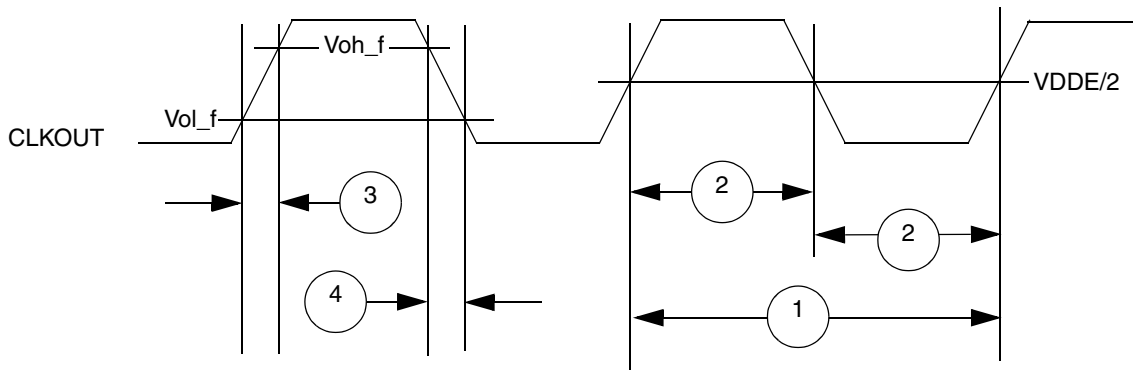


Figure 11. CLKOUT Timing

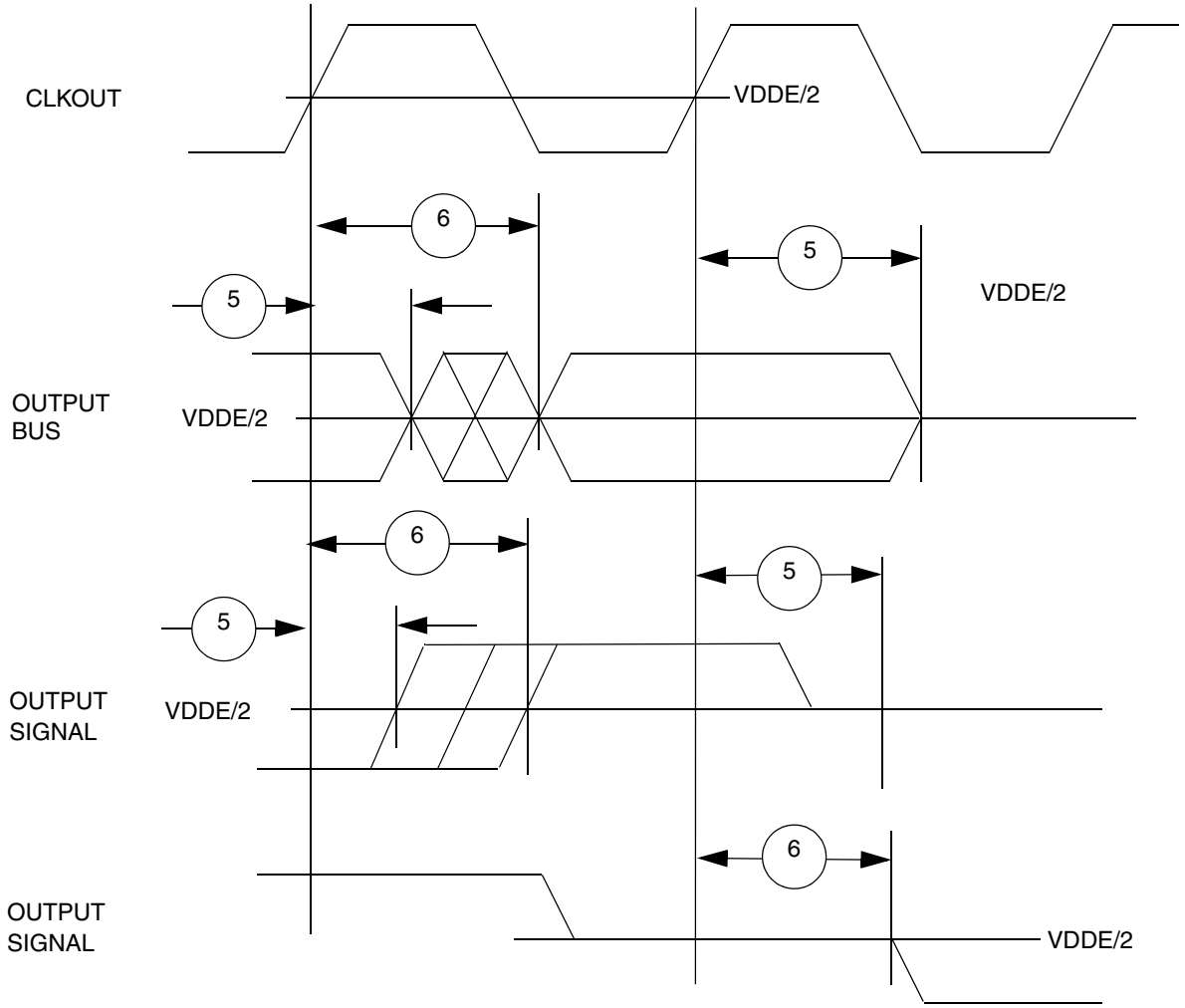


Figure 12. Synchronous Output Timing

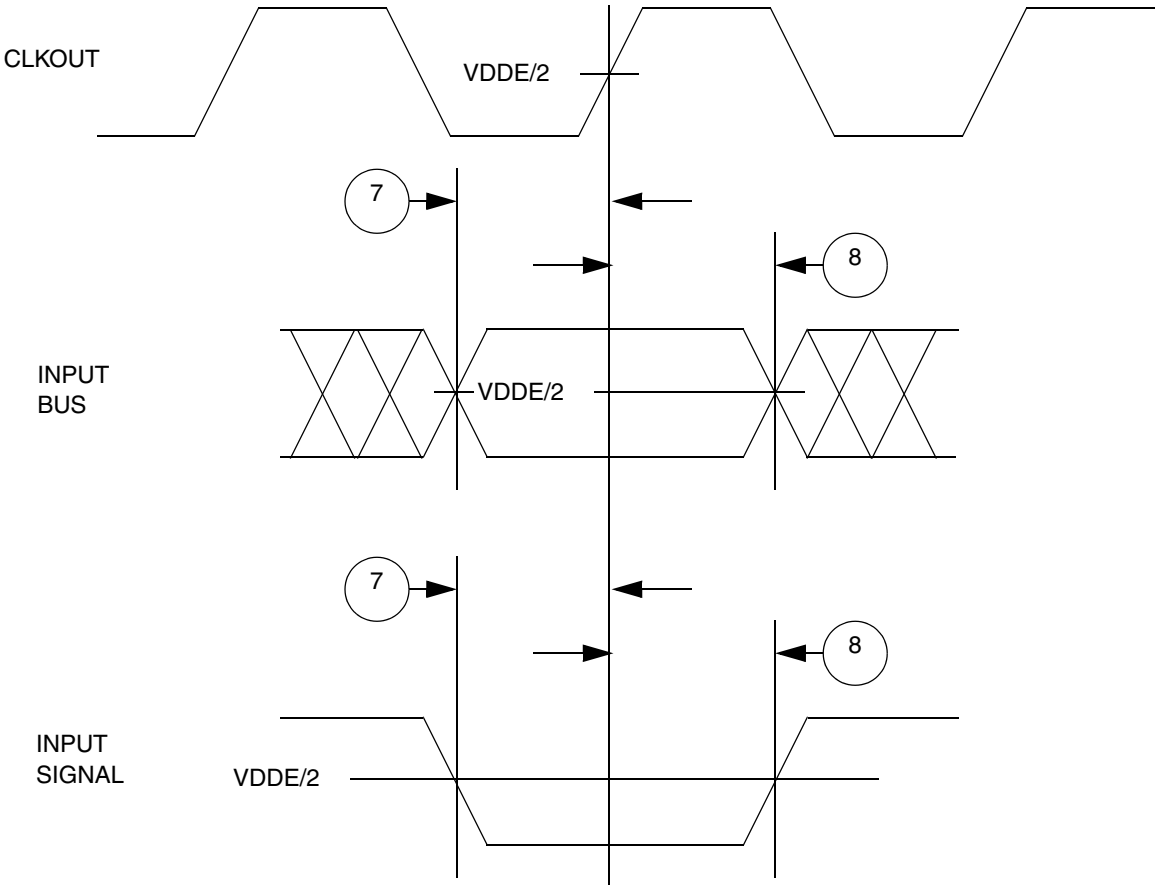


Figure 13. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Pin)

Table 23. External Interrupt Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{CYC}
2	IRQ Pulse Width High	T_{IPWH}	3	—	t_{CYC}
3	IRQ Edge to Edge Time[2]	t_{ICYC}	6	—	t_{CYC}

1 IRQ timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 200pF with SRC = 0b11.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

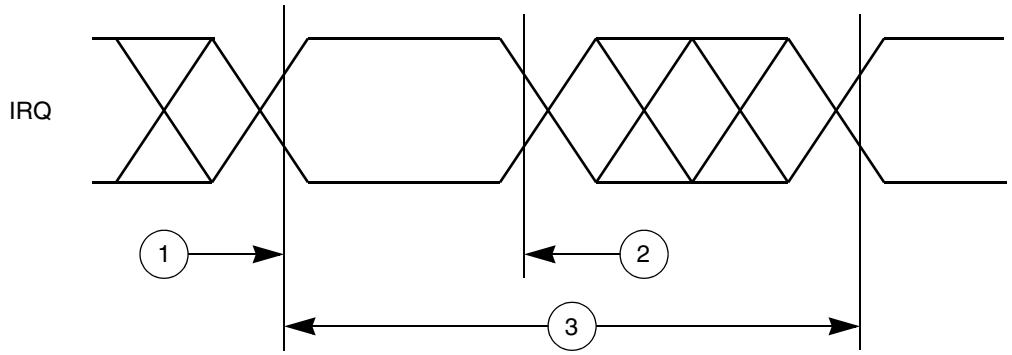


Figure 14. External Interrupt Timing

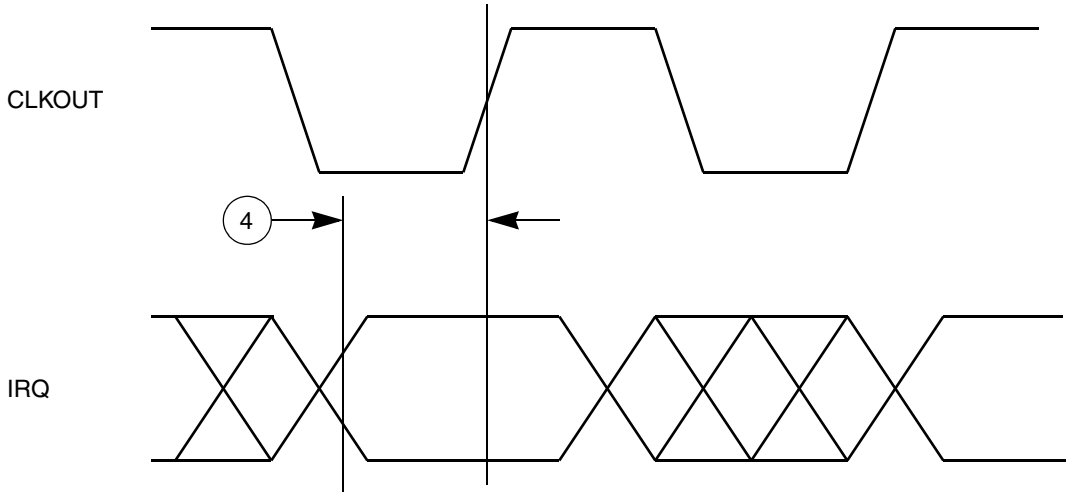


Figure 15. External Interrupt Setup Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{CYC}
2	eTPU Output Channel Pulse Width	t_{OCPW}	2	—	t_{CYC}

[1] eTPU timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 200pF with SRC = 0b11.

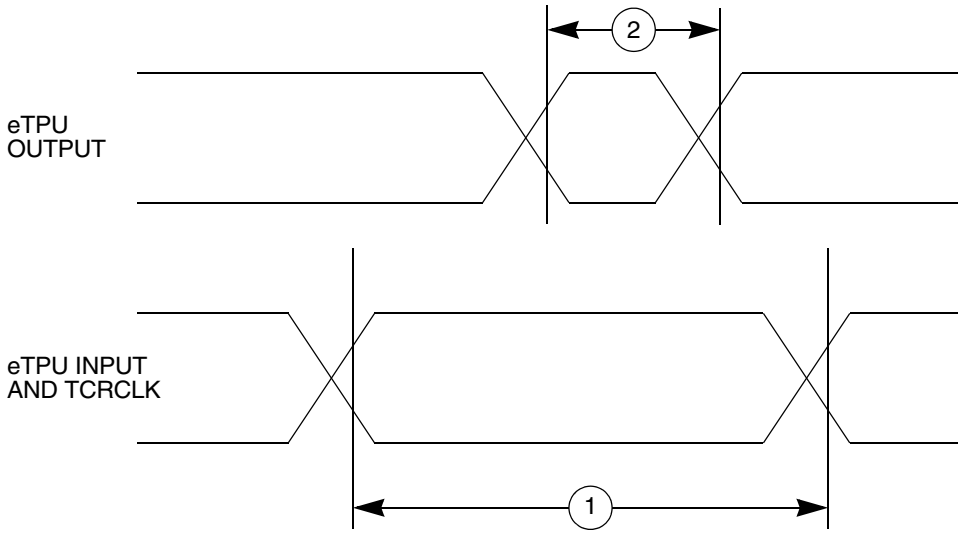


Figure 16. eTPU Timing

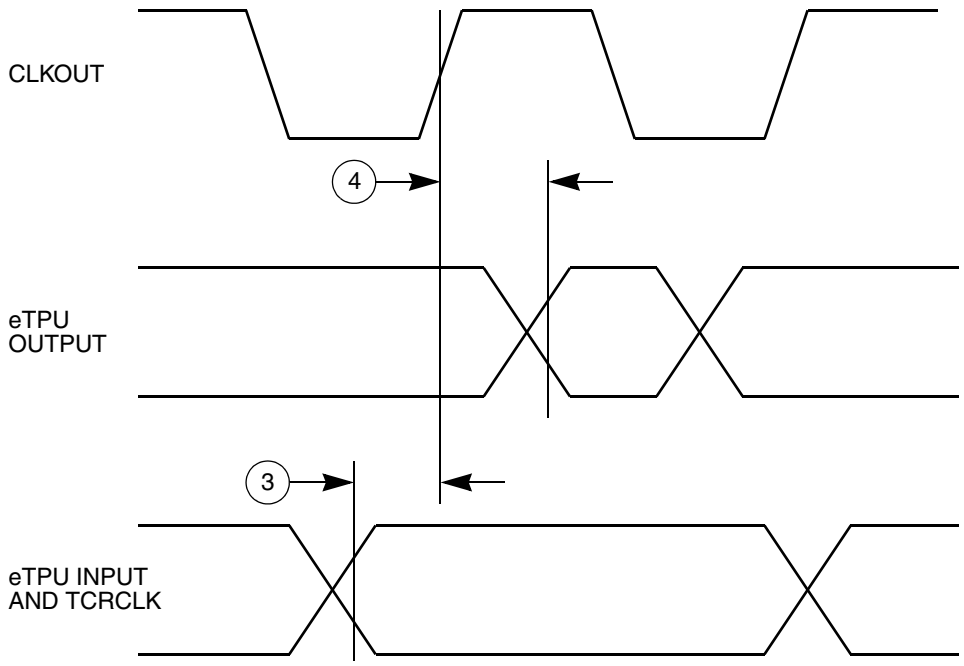


Figure 17. eTPU Input/Output Timing

3.13.7 eMIOS (MTS) Timing

Table 25. MTS Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	eMIOS (MTS) Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS (MTS) Output Pulse Width	t_{MOPW}	1	—	t_{CYC}

1 MTS timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

3.13.8 DSPI Timing

Table 26. DSPI Timing[1]

Num	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	SCK Cycle TIme[2,3]	t_{SCK}	25ns	2.9ms	17.9ns	2.0ms	15.2ns	1.7ms	—
2	PCS to SCK Delay[4]	t_{CSC}	23	—	15	—	13	—	ns
3	After SCK Delay[5]	t_{ASC}	22	—	14	—	12	—	ns
4	SCK Duty Cycle	t_{SDC}	$t_{SCK}/2$ –2ns	$t_{SCK}/2$ + 2ns	—	—	—	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT driven)	t_A	—	25	—	25	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	—	25	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	4	—	4	—	4	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	5	—	5	—	5	—	ns
9	Data Setup Time for Inputs	t_{SUI}							
	Master (MTFE = 0)		20	—	20	—	20	—	ns
	Slave		2	—	2	—	2	—	ns
	Master (MTFE = 1, CPHA = 0)[6]		–4	—	3	—	6	—	ns
	Master (MTFE = 1, CPHA = 1)		20	—	20	—	20	—	ns
10	Data Hold Time for Inputs	t_{HI}							
	Master (MTFE = 0)		–4	—	–4	—	–4	—	ns
	Slave		7	—	7	—	7	—	ns
	Master (MTFE = 1, CPHA = 0)[6]		21	—	14	—	12	—	ns
	Master (MTFE = 1, CPHA = 1)		–4	—	–4	—	–4	—	ns

Table 26. DSPI Timing[1] (continued)

Num	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min	Max	Min	Max	Min	Max	
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA=0) Master (MTFE = 1, CPHA=1)	t_{SUO}	 — — — —	 5 25 18 5	 — — — —	 5 25 14 5	 — — — —	 5 25 13 5	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –5 5.5 8 –5	 — — — —	 –5 5.5 4 –5	 — — — —	 –5 5.5 3 –5	 — — — —	 ns ns ns ns

1 DSPI timing specified at VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

2 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

3 The actual minimum SCK Cycle Time is limited by pad performance.

4 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]

5 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]

6 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

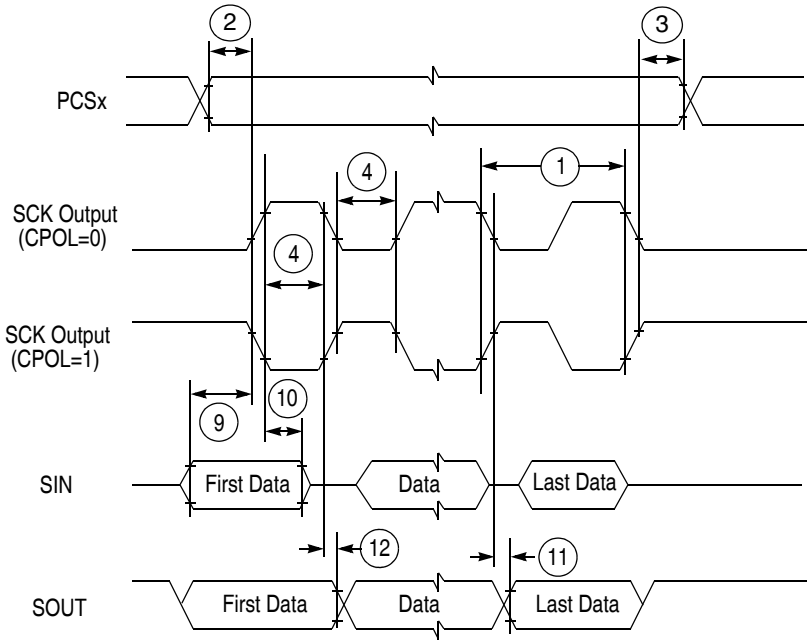


Figure 18. DSPI Classic SPI Timing — Master, CPHA = 0

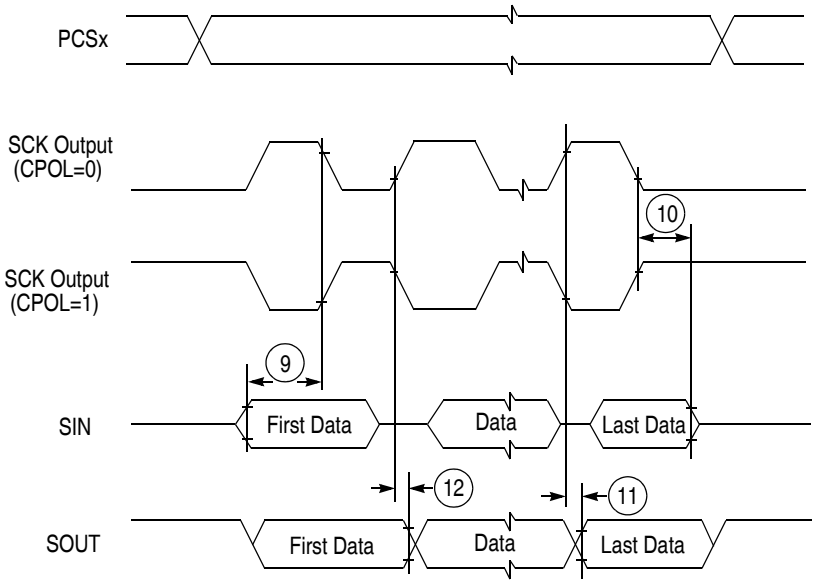


Figure 19. DSPI Classic SPI Timing — Master, CPHA = 1

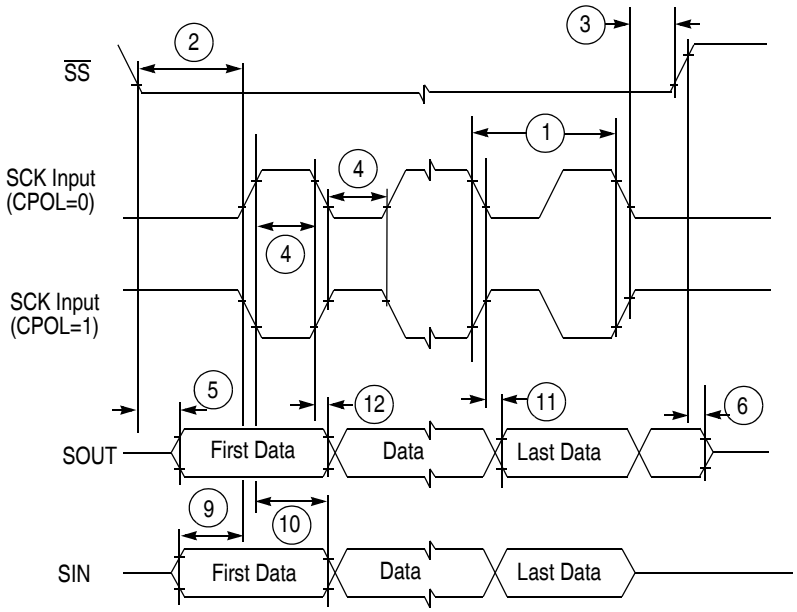


Figure 20. DSPI Classic SPI Timing — Slave, CPHA = 0

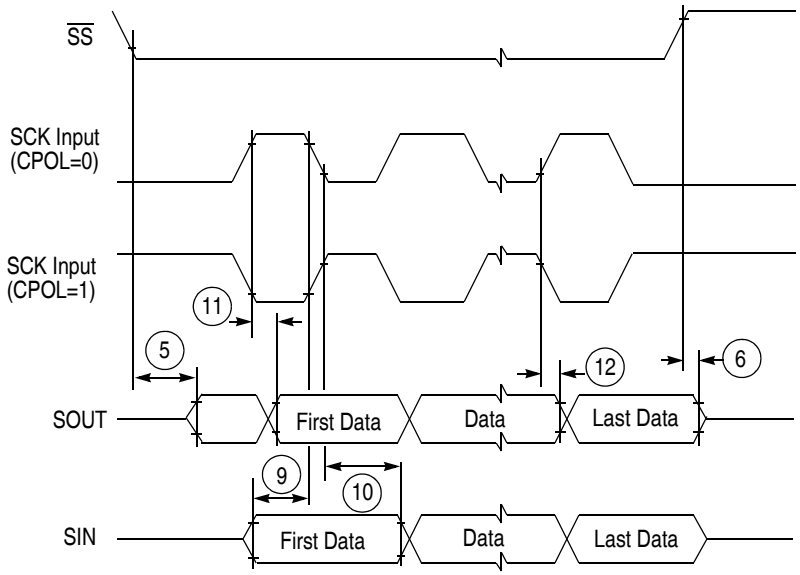


Figure 21. DSPI Classic SPI Timing — Slave, CPHA = 1

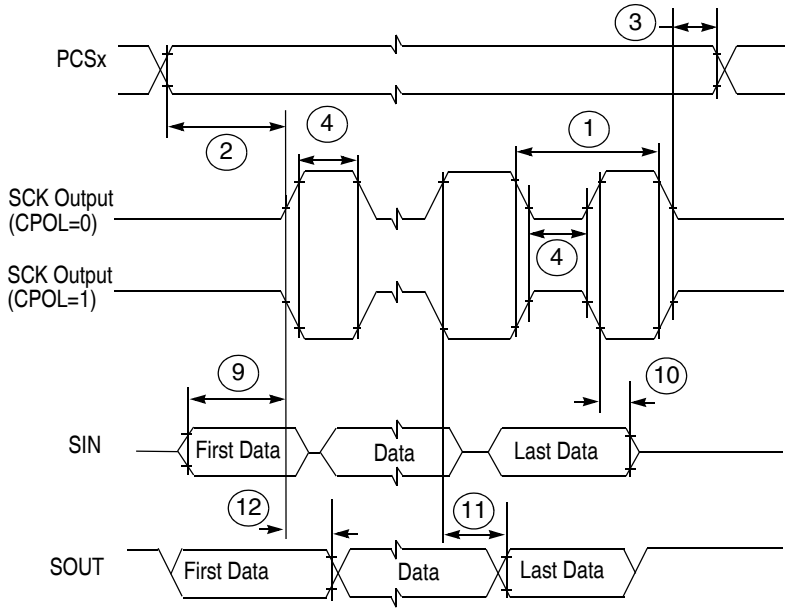


Figure 22. DSPI Modified Transfer Format Timing — Master, CPHA = 0

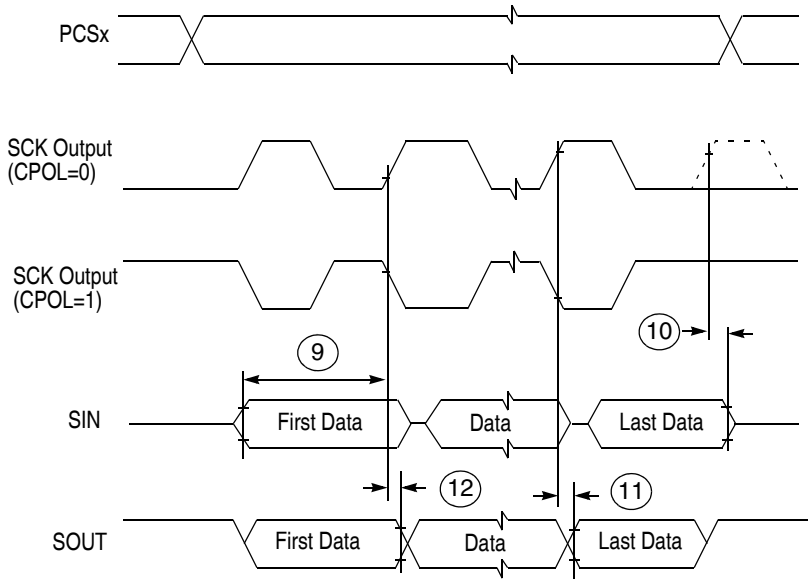


Figure 23. DSPI Modified Transfer Format Timing — Master, CPHA = 1

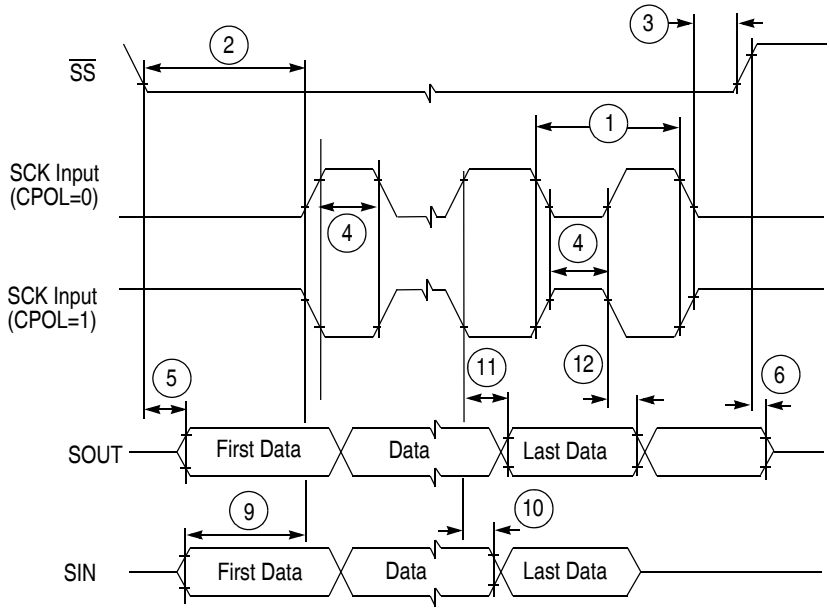


Figure 24. DSPI Modified Transfer Format Timing — Slave, CPHA =0

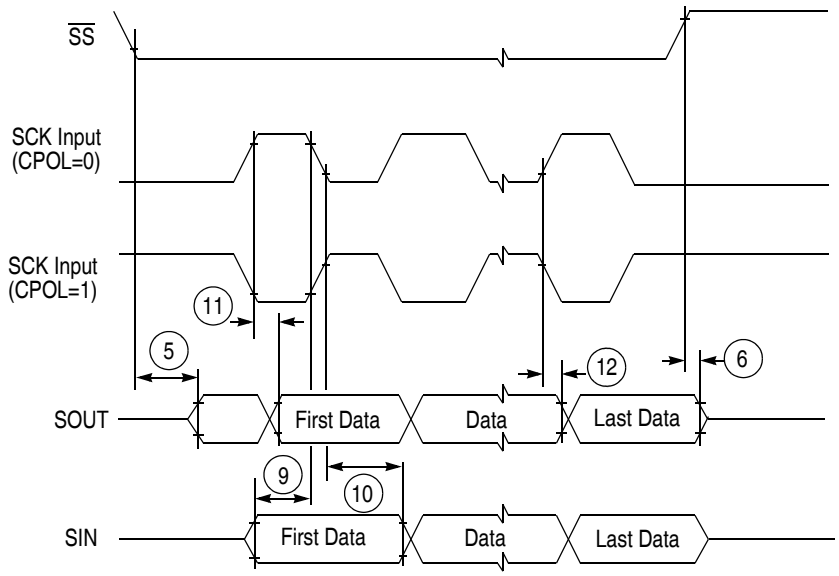


Figure 25. DSPI Modified Transfer Format Timing — Slave, CPHA =1

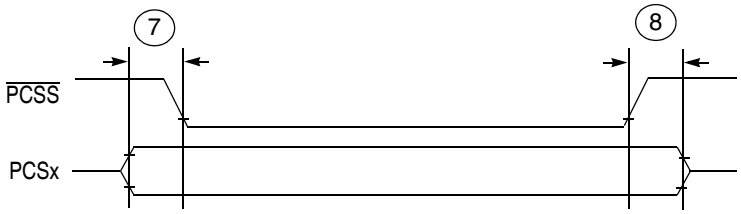


Figure 26. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

3.13.9 eQADC SSI Timing

Table 27. EQADC SSI Timing Characteristics (pads at 3.3V or at 5.0V) [1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	FCK Frequency [2, 3]	f_{FCK}	1/17	—	1/2	f_{SYS_CLK}
2	FCK Period (t_{FCK} = 1/ f_{FCK})	t_{FCK}	2	—	17	t_{SYS_CLK}
3	Clock (FCK) High Time	t_{FCKHT}	t_{SYS_CLK} − 6.5	—	9* t_{SYS_CLK} + 6.5	ns
4	Clock (FCK) Low Time	t_{FCKLT}	t_{SYS_CLK} − 6.5	—	8* t_{SYS_CLK} + 6.5	ns
5	SDS Lead/Lag Time	t_{SDS_LL}	–7.5	—	+7.5	ns
6	SDO Lead/Lag Time	t_{SDO_LL}	–7.5	—	+7.5	ns
7	EQADC Data Setup Time (Inputs)	t_{EQ_SU}	22	—	—	ns
8	EQADC Data Hold Time (Inputs)	t_{EQ_HO}	1	—	—	ns

1 SS timing specified at F_{SYS} = 132MHz, VDD = 1.35V to 1.65V, VDDEH = 3.0V to 5.5V, VDD33 and VDDSYN = 3.0V to 3.6V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

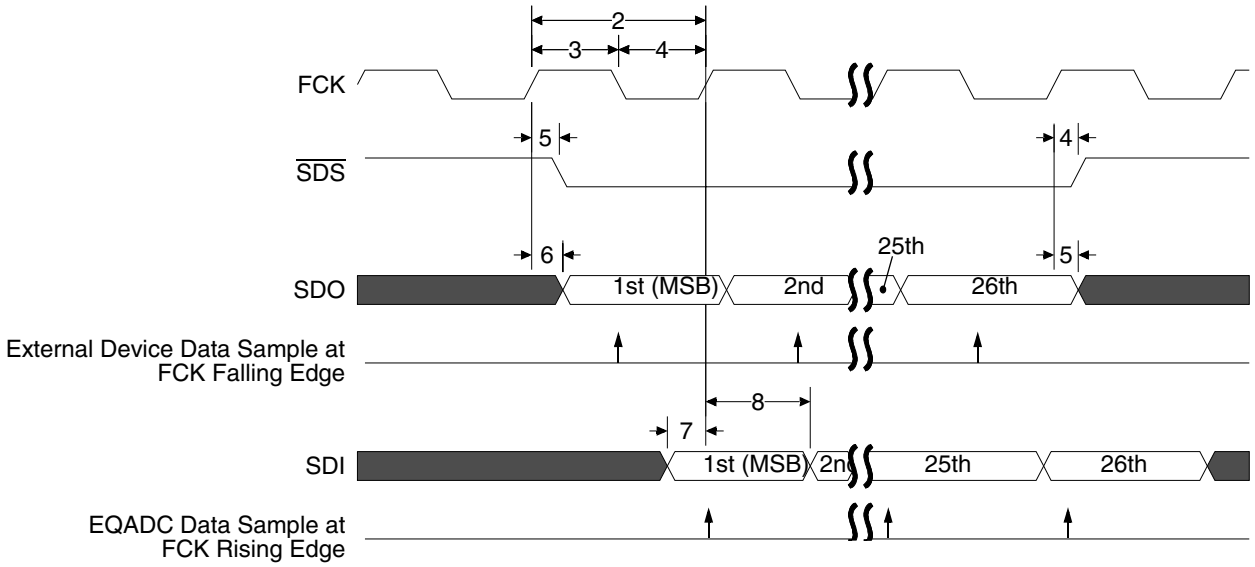


Figure 27. EQADC SSI Timing

3.14 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 3.3 V. Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation).

3.14.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed 4× the RX_CLK frequency.

Table 28 lists MII receive channel timings.

Table 28. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
3	RX_CLK pulse width high	35%	65%	RX_CLK period
4	RX_CLK pulse width low	35%	65%	RX_CLK period

Figure 28 shows MII receive signal timings listed in Table 28.

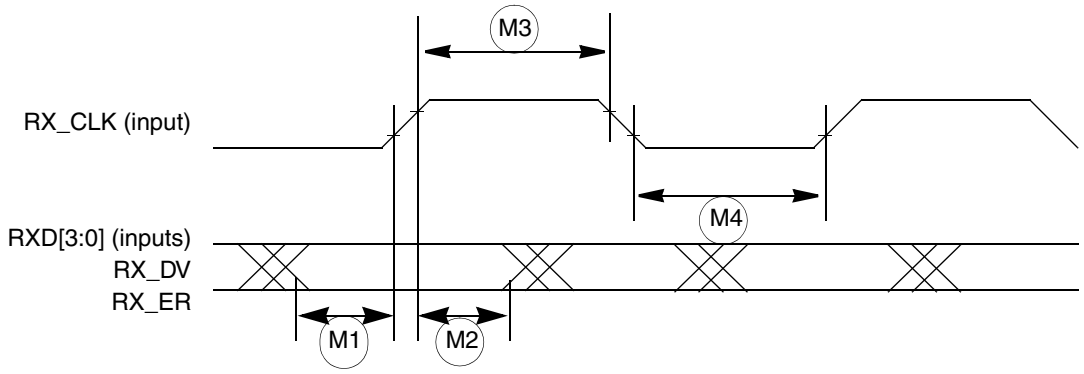


Figure 28. MII Receive Signal Timing Diagram

3.14.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the ethernet chapter of the device Reference Manual for details of this option and how to enable it.

Table 29 lists MII transmit channel timings.

Table 29. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
7	TX_CLK pulse width high	35%	65%	TX_CLK period
8	TX_CLK pulse width low	35%	65%	TX_CLK period

Figure 29 shows MII transmit signal timings listed in Table 29.

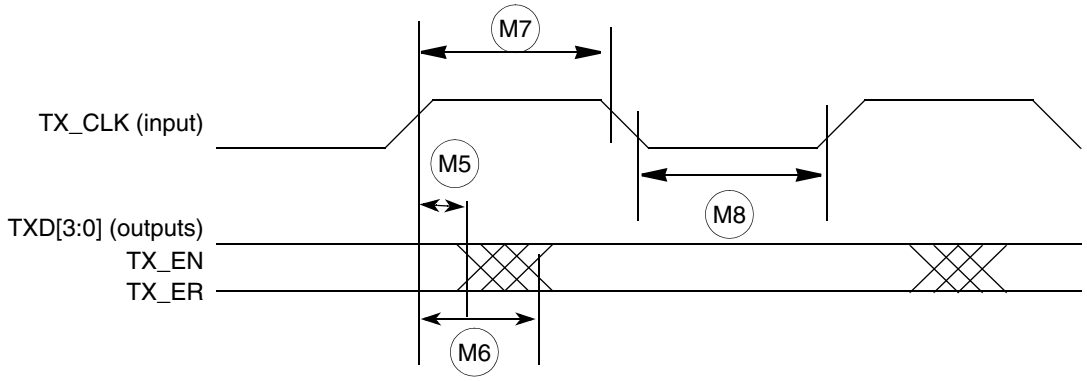


Figure 29. MII Transmit Signal Timing Diagram

3.14.3 MII Async Inputs Signal Timing (CRS and COL)

Table 30 lists MII asynchronous inputs signal timing.

Table 30. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 30 shows MII asynchronous input timings listed in Table 30.

Figure 30. MII Async Inputs Timing Diagram

3.14.4 MII Serial Management Channel Timing (MDIO and MDC)

Table 31 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 31. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
12	MDIO (input) to MDC rising edge setup	10	—	ns
13	MDIO (input) to MDC rising edge hold	0	—	ns
14	MDC pulse width high	40%	60%	MDC period
15	MDC pulse width low	40%	60%	MDC period

Figure 31 shows MII serial management channel timings listed in Table 31.

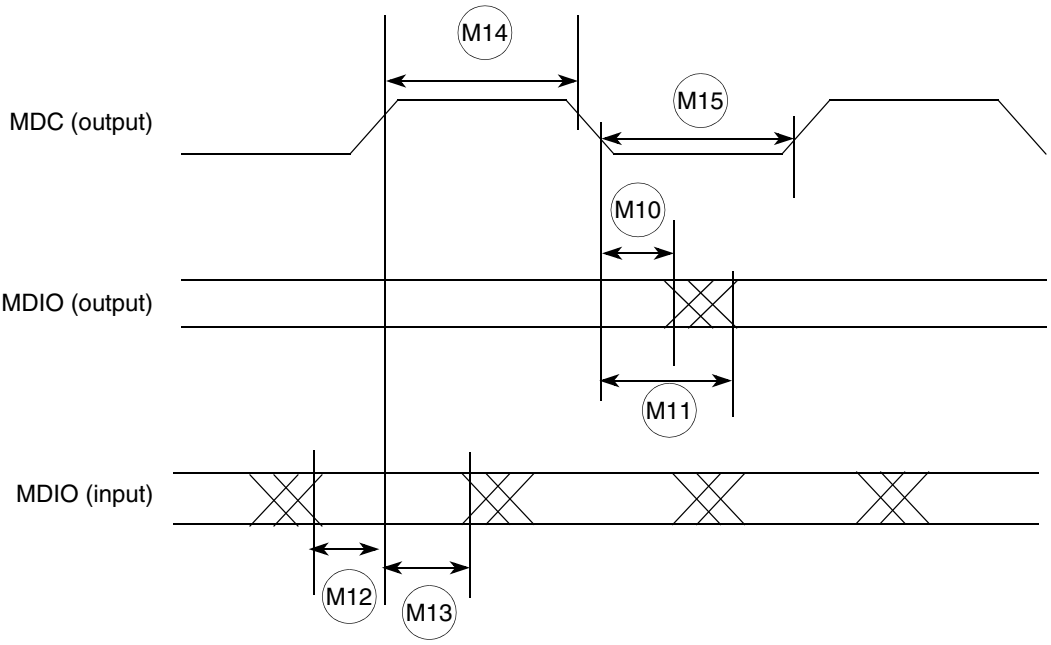


Figure 31. MII Serial Management Channel Timing Diagram

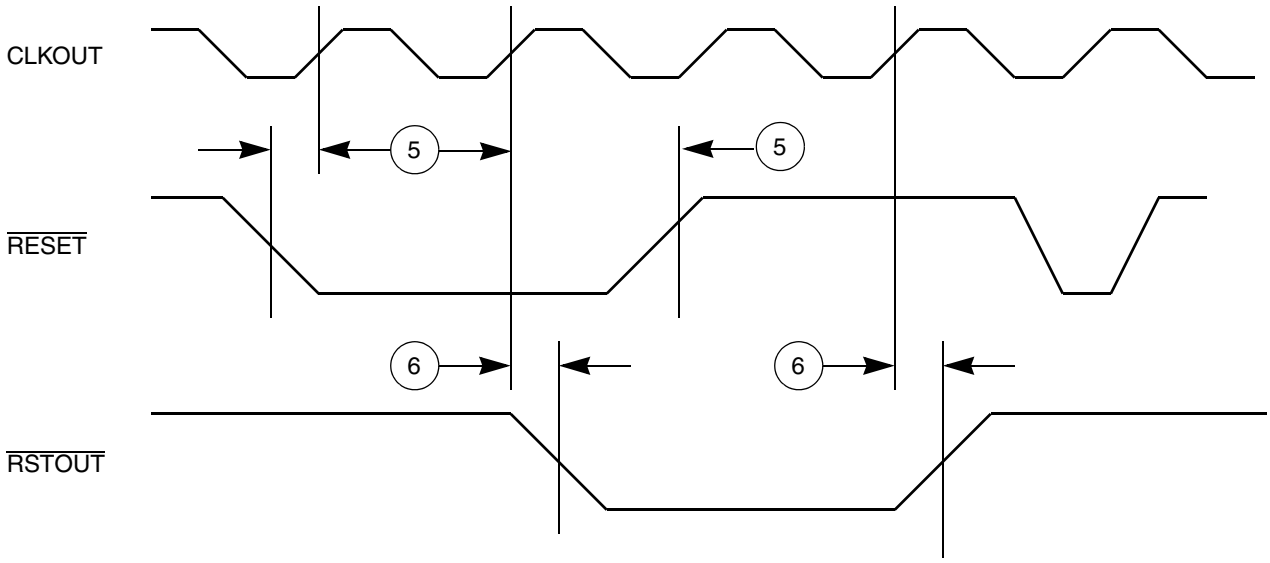


Figure 32. Reset and Configuration Pin Timing

4 Mechanicals

4.1 Pinouts

4.1.1 MPC5553 416 PBGA Pinout

Figure 33, Figure 34, and Figure 35 show the pinout for the MPC5553 416 PBGA package. While the MPC5553 and the MPC5554/MPC5565/MPC5566 are pin-compatible, the MPC5553 ball map is shown here to highlight the balls that are not connected to any signal on the MCP5553 (the eTPUB[0:31] and TSIZ[0:1]). The alternate Ethernet signals that are multiplexed with the data bus are not shown for the MPC5553.

NOTE

Some pins have names that include functions that are not available on all family members. For example, ball R25 of the 416 BGA package is named 'SINA,' but the MPC5553 does not have a DSPI_A module. In this case, the SINA pin can only be used for its alternate functions of GPIO94 or PCSC2. See the specific device reference manual for functions available on each device in the family.

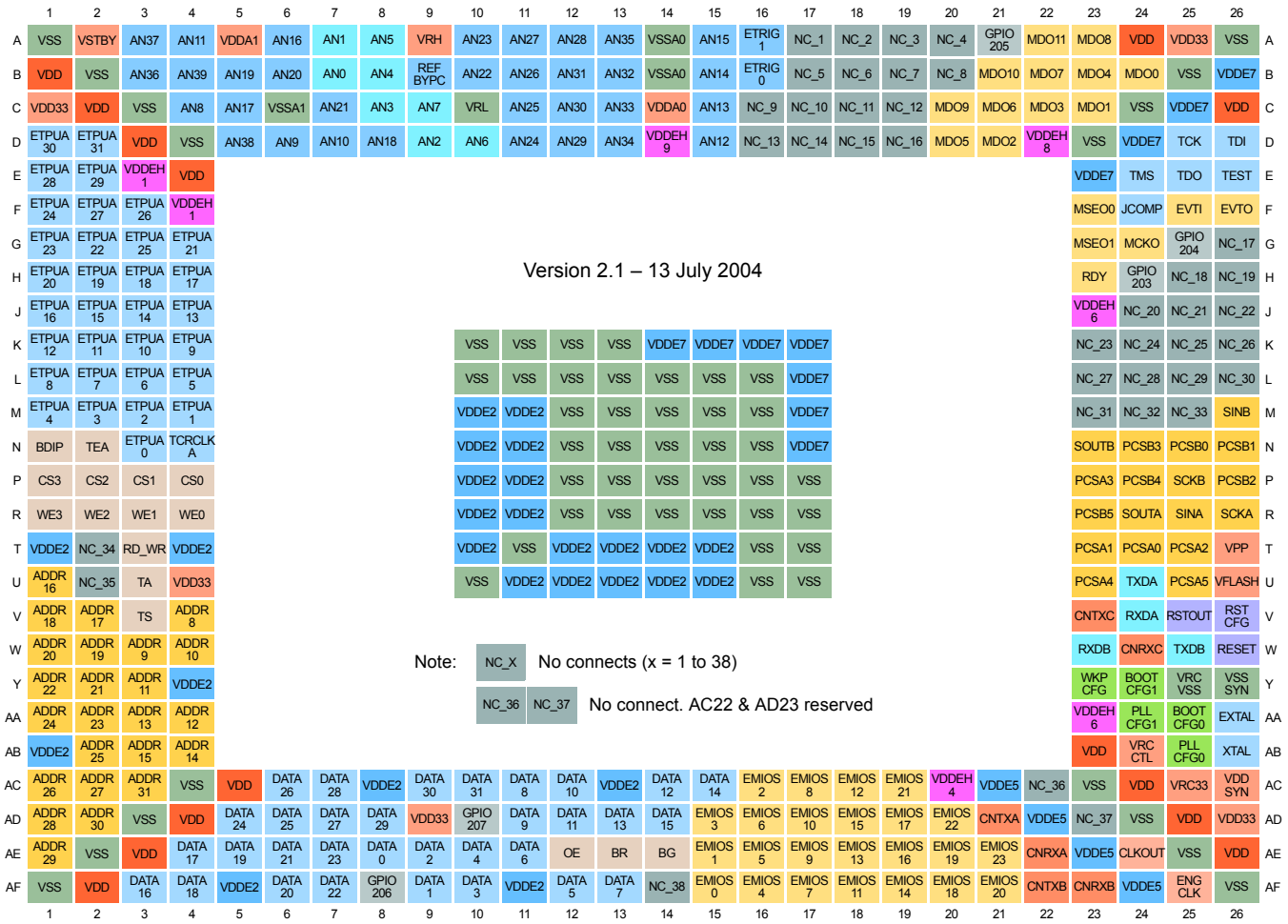


Figure 33. MPC5553 416 Package

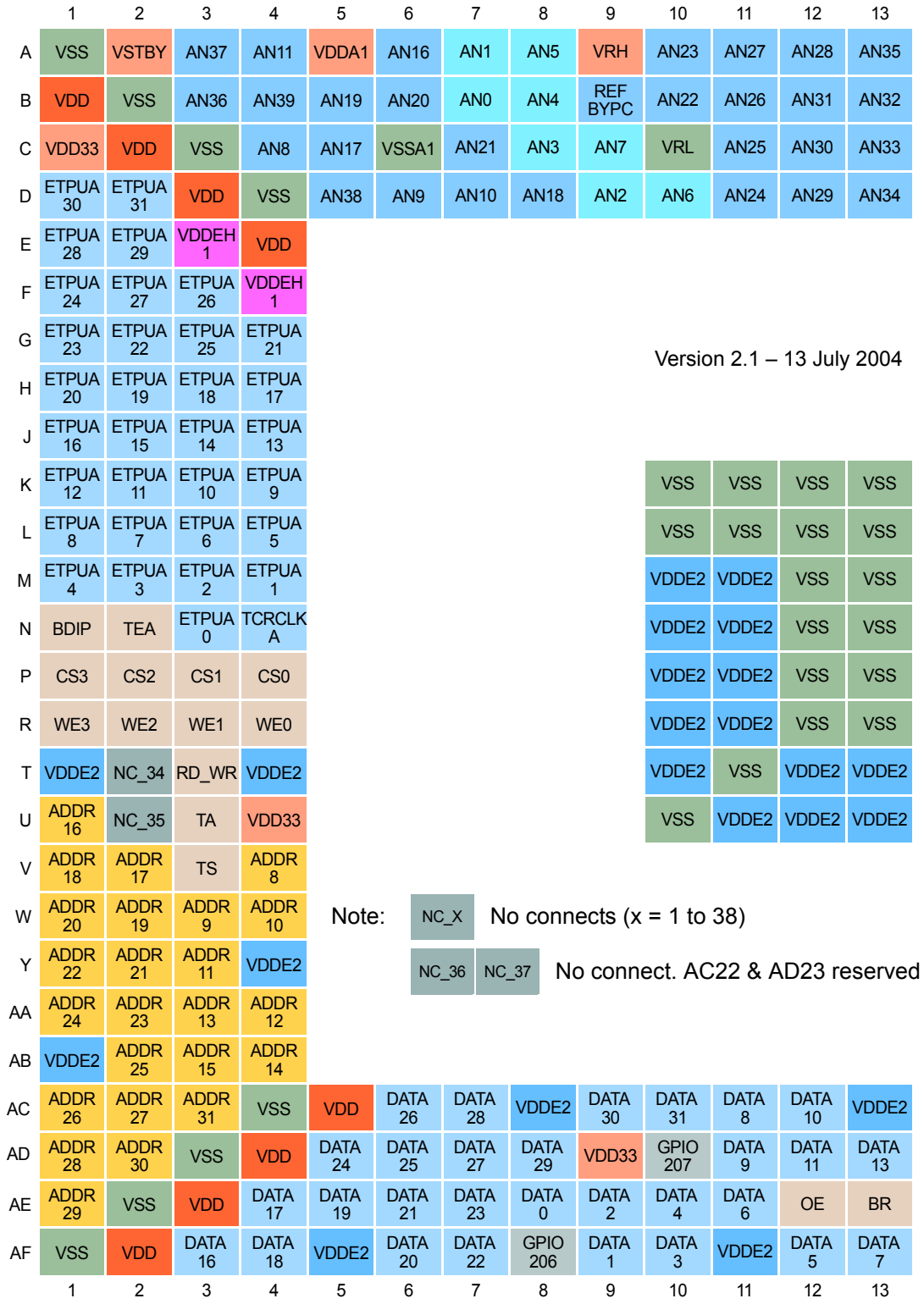
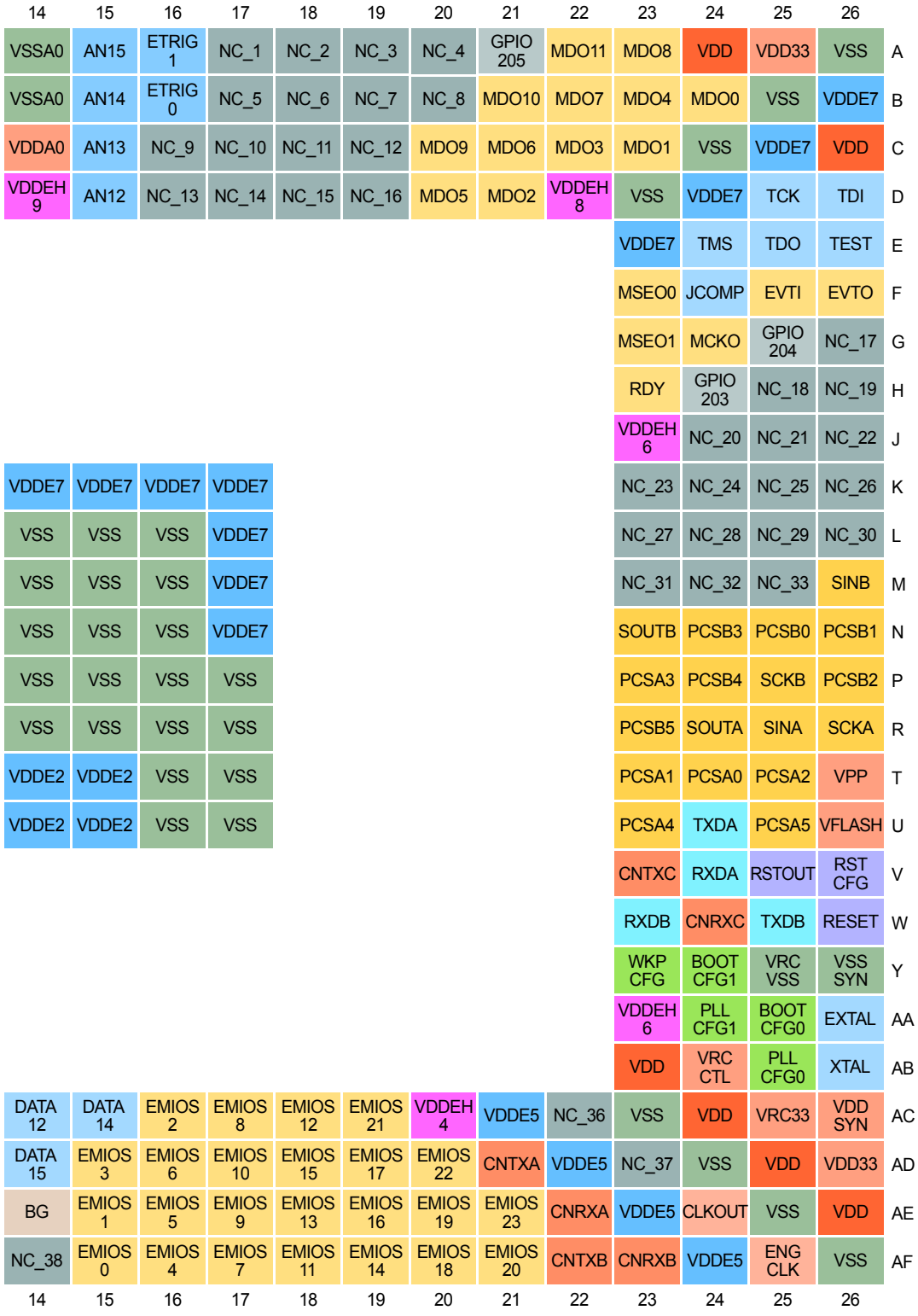


Figure 34. MPC5553 416 Package, Left Side



14	15	16	17	18	19	20	21	22	23	24	25	26	
VSSA0	AN15	ETRIG 1	NC_1	NC_2	NC_3	NC_4	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS	A
VSSA0	AN14	ETRIG 0	NC_5	NC_6	NC_7	NC_8	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7	B
VDDA0	AN13	NC_9	NC_10	NC_11	NC_12	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD	C
VDDEH 9	AN12	NC_13	NC_14	NC_15	NC_16	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI	D
									VDDE7	TMS	TDO	TEST	E
									MSEO0	JCOMP	EVTI	EVTO	F
									MSEO1	MCKO	GPIO 204	NC_17	G
									RDY	GPIO 203	NC_18	NC_19	H
									VDDEH 6	NC_20	NC_21	NC_22	J
VDDE7	VDDE7	VDDE7	VDDE7						NC_23	NC_24	NC_25	NC_26	K
VSS	VSS	VSS	VDDE7						NC_27	NC_28	NC_29	NC_30	L
VSS	VSS	VSS	VDDE7						NC_31	NC_32	NC_33	SINB	M
VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1	N
VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2	P
VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA	R
VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP	T
VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH	U
									CNTXC	RXDA	RSTOUT	RST CFG	V
									RXDB	CNRXC	TXDB	RESET	W
									WKP CFG	BOOT CFG1	VRC VSS	VSS SYN	Y
									VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	AA
									VDD	VRC CTL	PLL CFG0	XTAL	AB
DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC_36	VSS	VDD	VRC33	VDD SYN	AC
DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC_37	VSS	VDD	VDD33	AD
BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AE
NC_38	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 35. MPC5553 416 Package, Right Side

4.1.2 MPC5553 324 PBGA Pinout

Figure 36 is a pinout for the MPC5553 324 PBGA package.

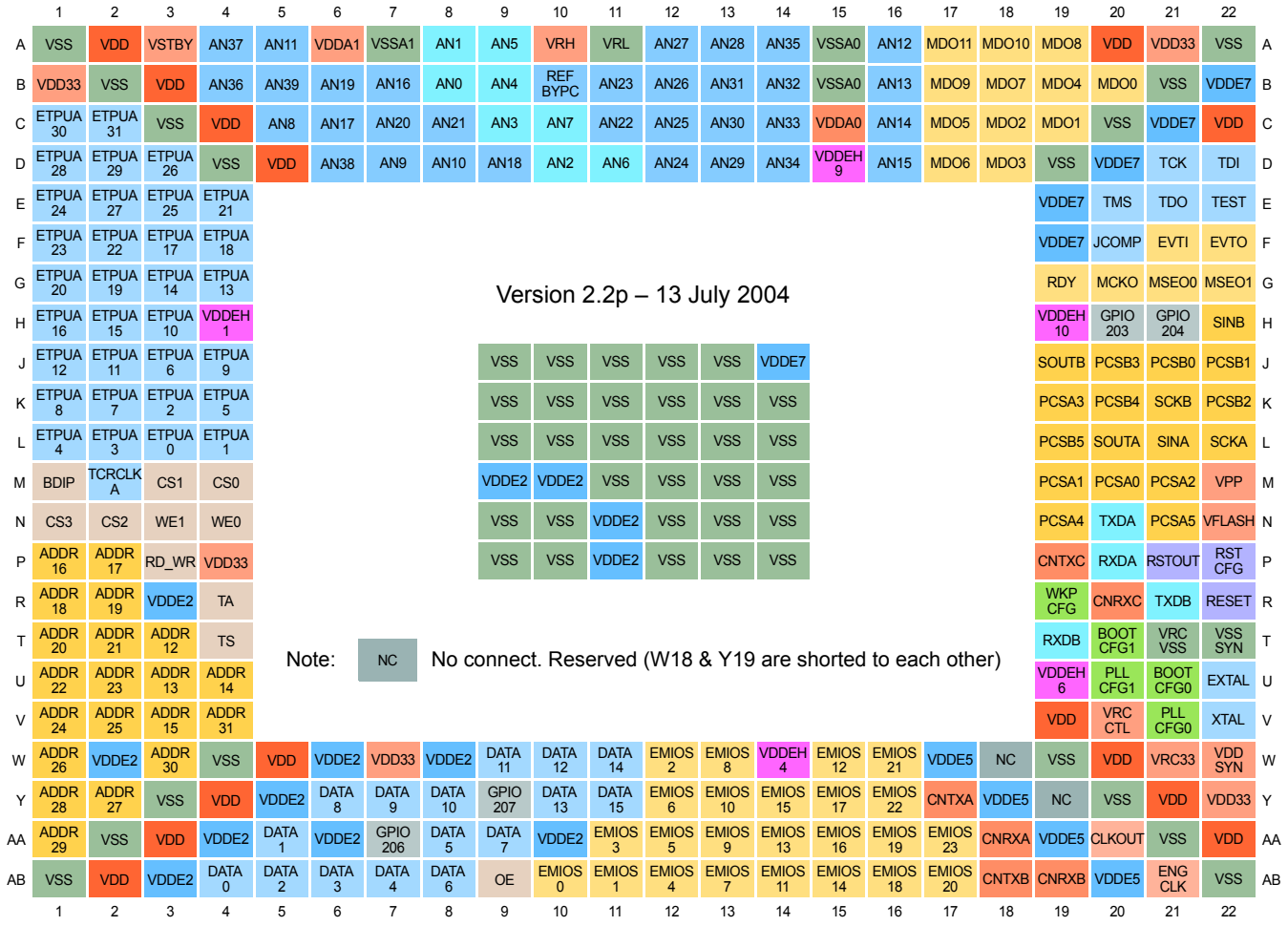


Figure 36. MPC5553 324 Package

4.1.3 MPC5553 208 MAP BGA Pinout

Figure 37 is a pinout for the MPC5553 208 MAP BGA package.

NOTE

VDDEH10 and VDDEH6 are connected internally on the 208-ball package and are listed as VDDEH6.

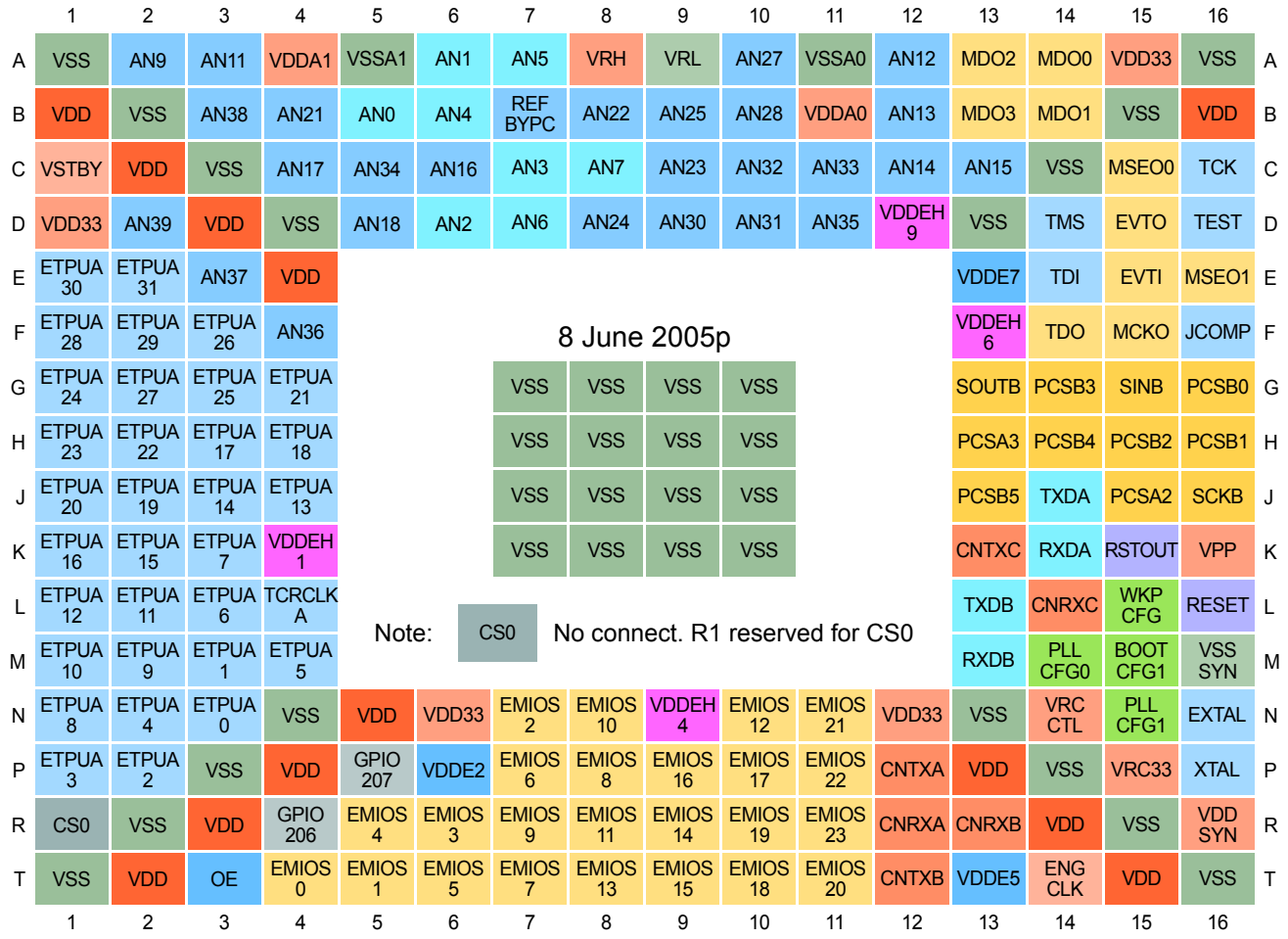


Figure 37. MPC5553 208 Package

4.2 Package Dimensions

4.2.1 MPC5553 416-Pin Package

Figure 38 is a package drawing of the MPC5553 416 pin TEPBGA package.

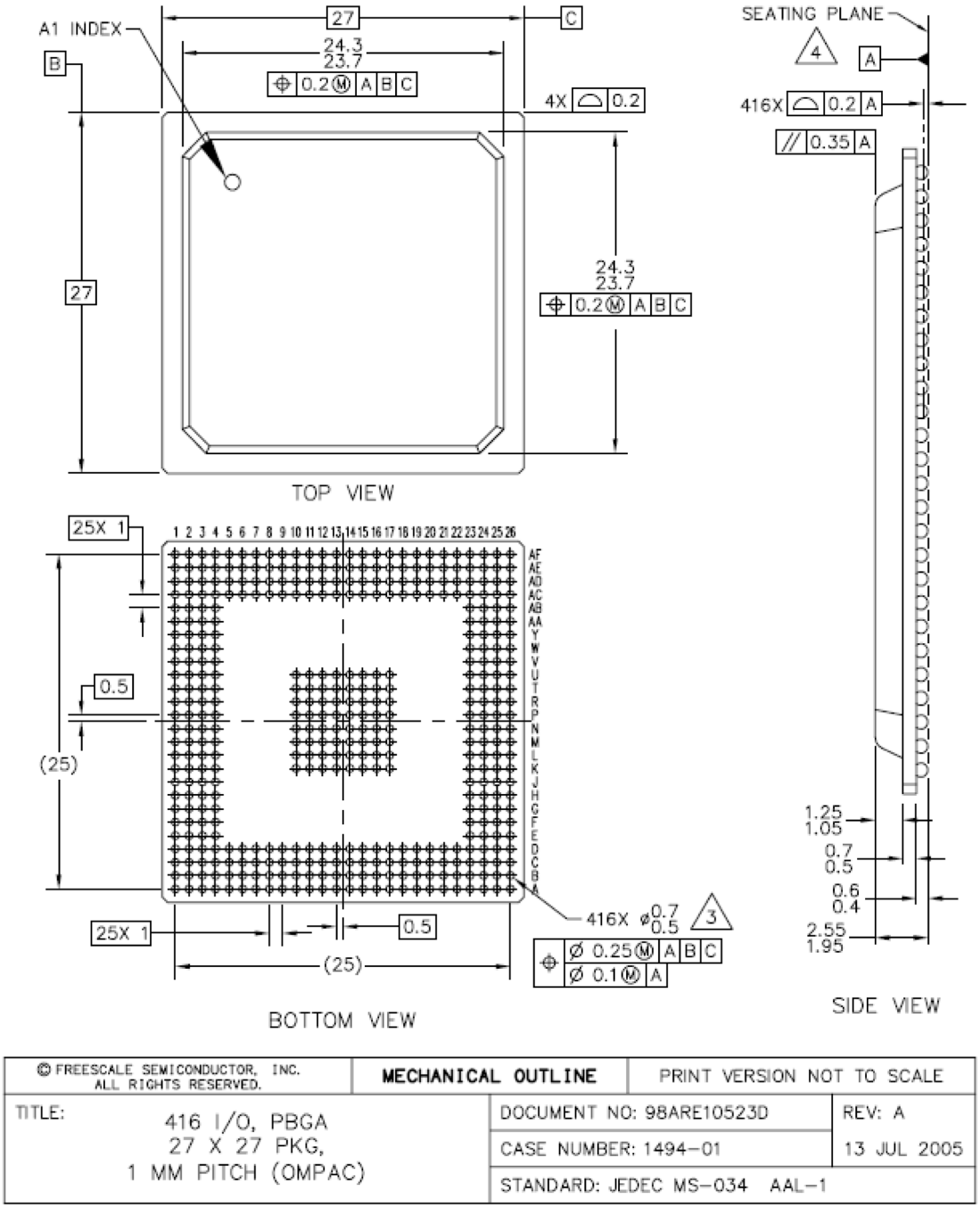


Figure 38. MPC5553 416 TEPBGA Package

4.2.2 MPC5553 324-Pin Package

Figure 39 is a package drawing of the MPC5553 324-pin TEPBGA package.

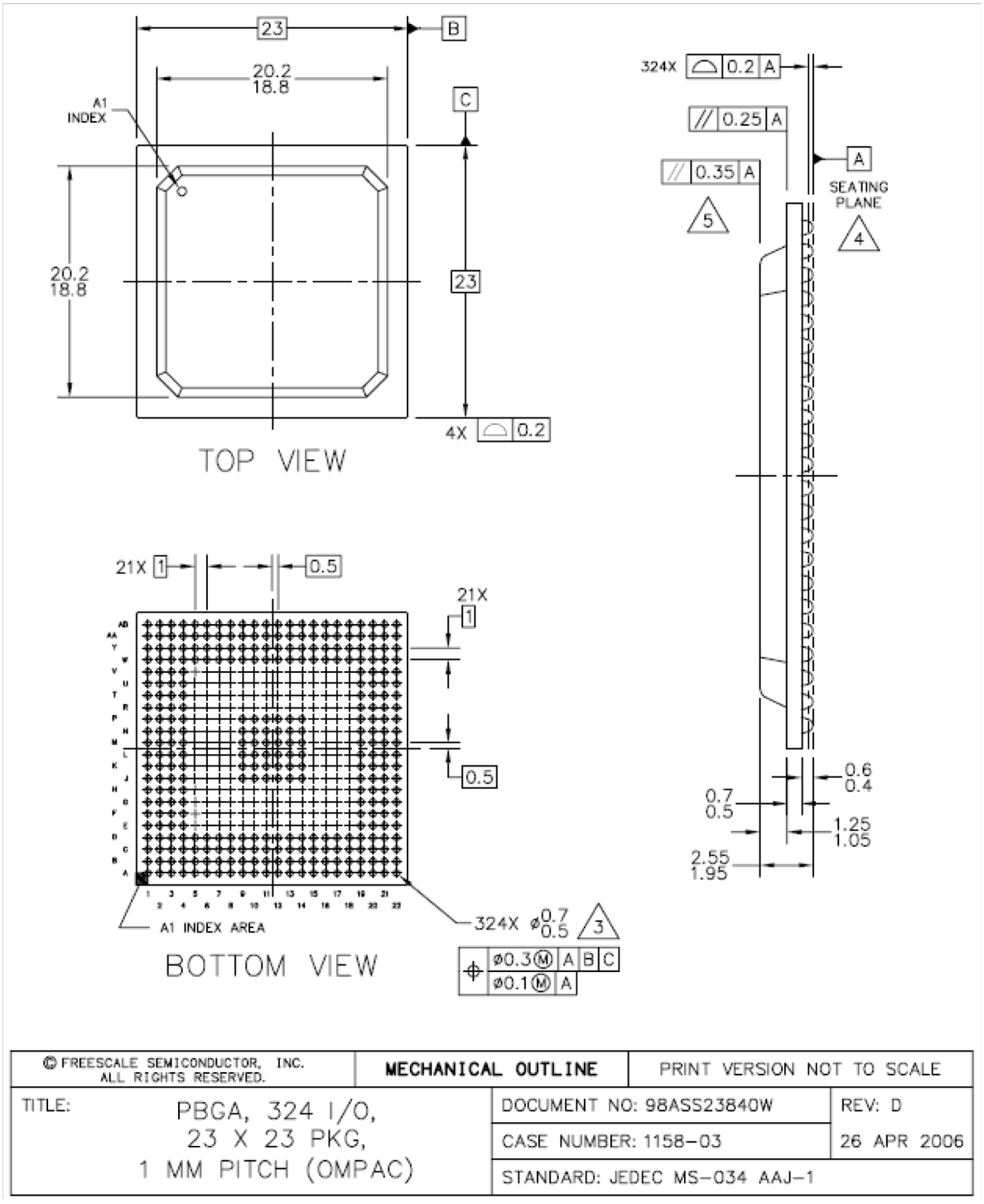


Figure 39. MPC5553 324 TEPBGA Package

4.2.3 MPC5553 208-Pin Package

Figure 40 is a package drawing of the MPC5553 208-pin MAP BGA package.

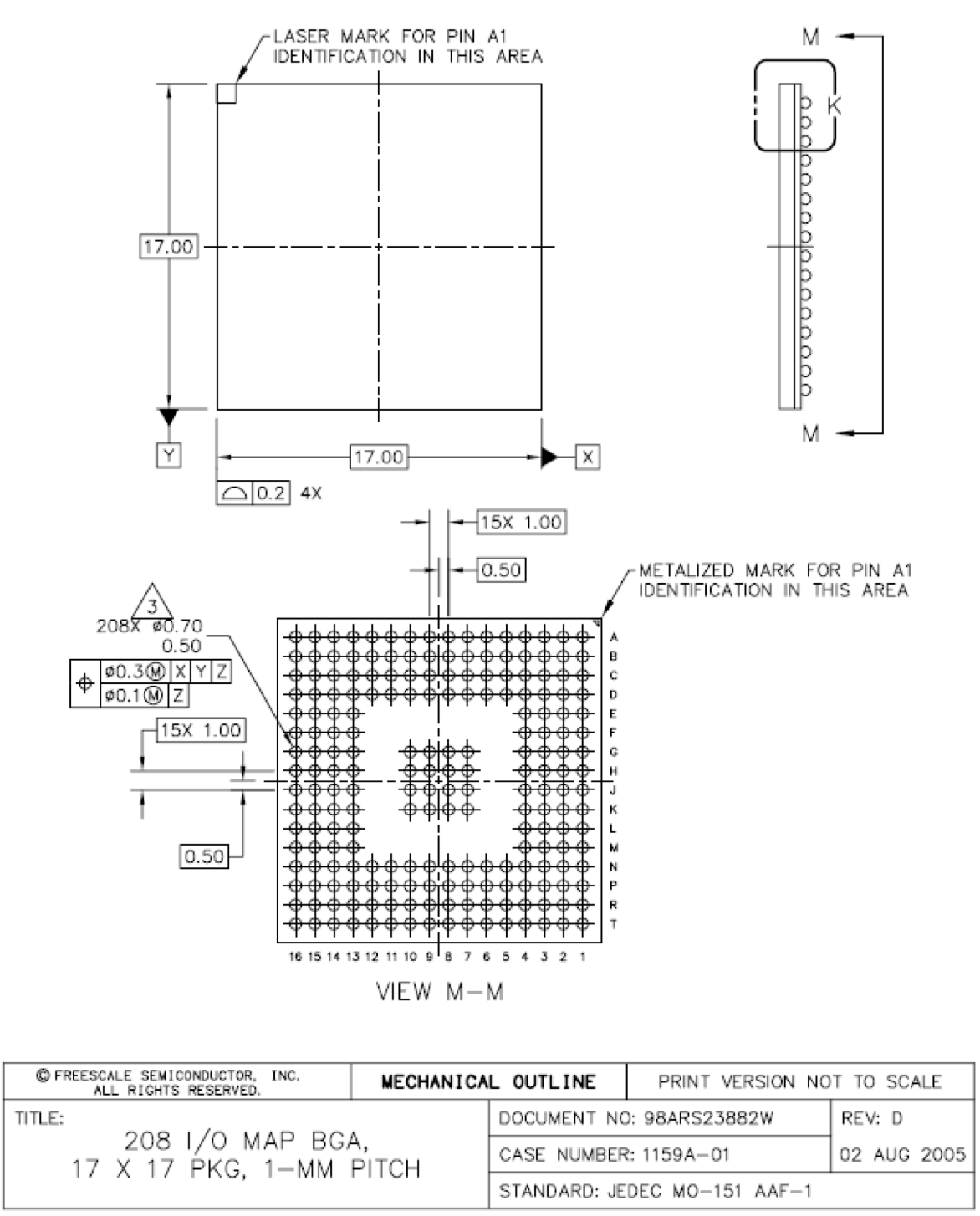


Figure 40. MPC5553 208 MAP BGA Package

5 Revision History

Table 32 provides a revision history of this document.

Table 32. Revision History

Revision	Location(s)	Substantive Change(s)
Rev. 0		This is the first released version of this document.

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