BR24C01A BR24C02F BR24C01AF BR24C04 BR24C02 BR24C04F

EEPROM, serial, 2 wire (for use with I²C bus)

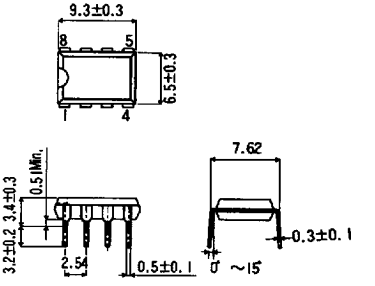
The BR24C01A/AF, BR24C02/F, and BR24C04/F are serial, 2-wire EEPROM ICs.

Features

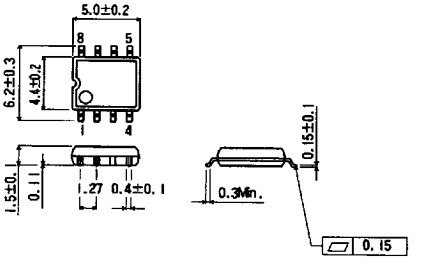
- available in DIP8 and SOP8 packages
- Available with the following memory:
  - — BR24C01A/AF: 1 kbit (128 × 8 bit)
  - — BR24C02/F: 2 kbit (256 × 8 bit)
  - — BR24C04/F: 4 kbit (512 × 8 bit)
- for use with I²C bus
- wide voltage supply range, 2.7 ~ 5.5 V (reading and writing)
- low current consumption, typically
  - — during operation: 0.2 mA at 5 V
  - — while standby: 1.0 μA at 5 V
- can be rewritten at least 10 000 times
- data can be stored for 10 years without corruption
- addresses can be incremented automatically during read operations
- auto erase and auto complete functions can be used during write operations
- page write mode function
  - — BR24C01A/AF: 4 bytes
  - — BR24C02/F: 4 bytes
  - — BR24C04/F: 16 bytes
- write protection when:
  - — V_{CC} is low
  - — IC is powered up
- includes noise filters on the SCL and SDA pins

Dimensions (Units : mm)

BR24C01A, BR24C02, BR24C04 (DIP8)



BR24C01AF, BR24C02F, BR24C04F (SOP8)

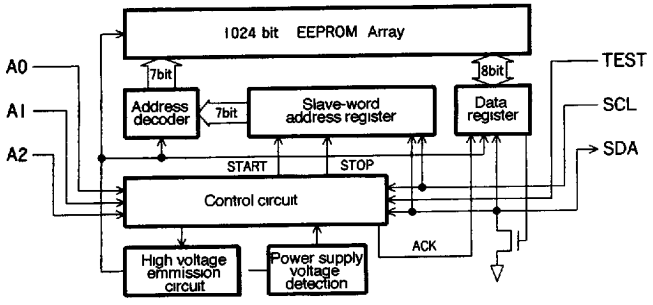


Applications

- video tape recorders
- televisions
- printers
- car stereo radio cassette players
- cordless telephones
- short wave radios
- programmable DIP switches

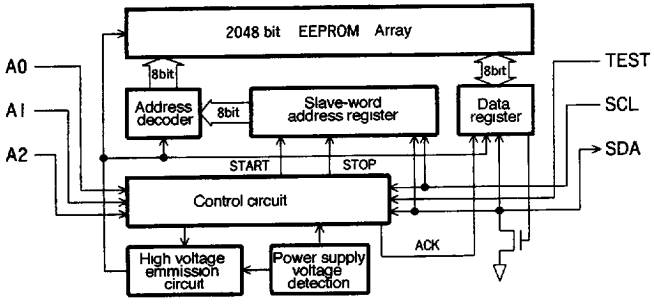
Note: I²C is a registered trademark of Phillips Co.

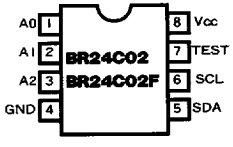
Block diagram and pin connections—BR24C01A and BR24C01AF



Pin name	Function
A0, A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input/output
TEST	Test connection
V_{CC}	Power supply
GND	Ground

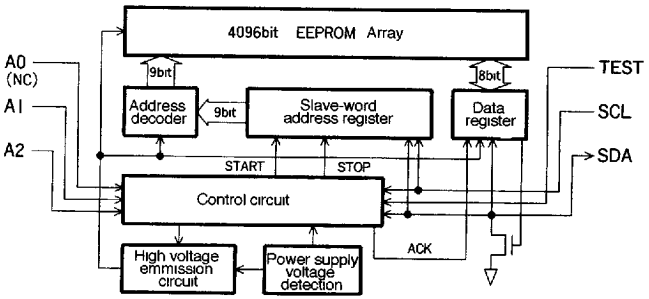
Block diagram and pin connections—BR24C02 and BR24C02F

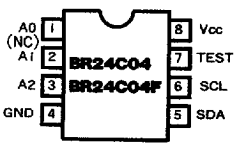




Pin name	Function
A0, A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input/output
TEST	Test connection
V_{CC}	Power supply
GND	Ground

Block diagram and pin connections—BR24C04 and BR24C04F

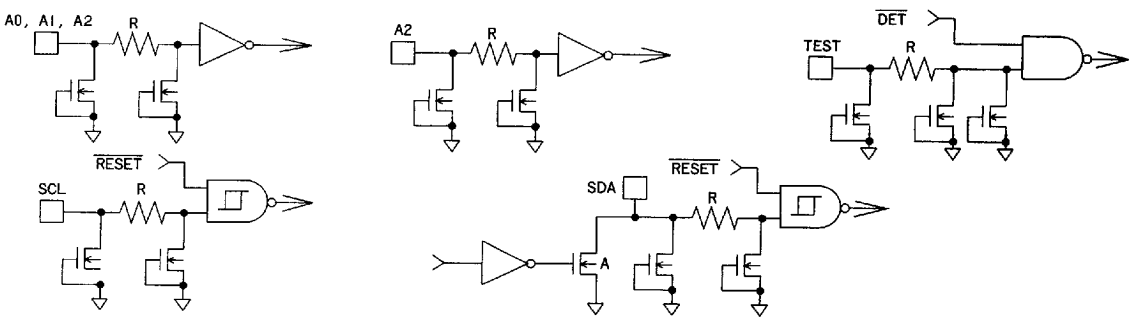




The SDA pin has an Nch open drain output. Therefore, make sure to use an external pull-up resistor.

Pin name	Function
A0	Not used
A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input/output
TEST	Test connection
V_{CC}	Power supply
GND	Ground

Input/output circuits



Absolute maximum ratings (T_a = 25°C)

Parameter		Symbol	Limits	Units	Conditions
Power supply		V_{CC}	−0.3 ~ +6.5	V	
Power dissipation	BR24C01A BR24C02 BR24C04	P_d	500	mW	Reduce power by 5.0 mW/°C for each degree above 25°C.
	BR24C01AF BR24C02F BR24C04F		350		Reduce power by 3.5 mW/°C for each degree above 25°C.
Voltage for each pin			−0.3 ~ V_{CC} +0.3	V	
Storage temperature		T_{stg}	−65 ~ +125	°C	
Operating temperature		T_{opr}	−40 ~ +85	°C	

Recommended operating conditions (T_a = 25°C)

Parameter		Symbol	Limits	Unit
Supply voltage	Read	V_{CC}	2.7 ~ 5.5	V
	Write		2.7 ~ 5.5	
Input voltage		V_{IN}	0 ~ V_{CC}	V

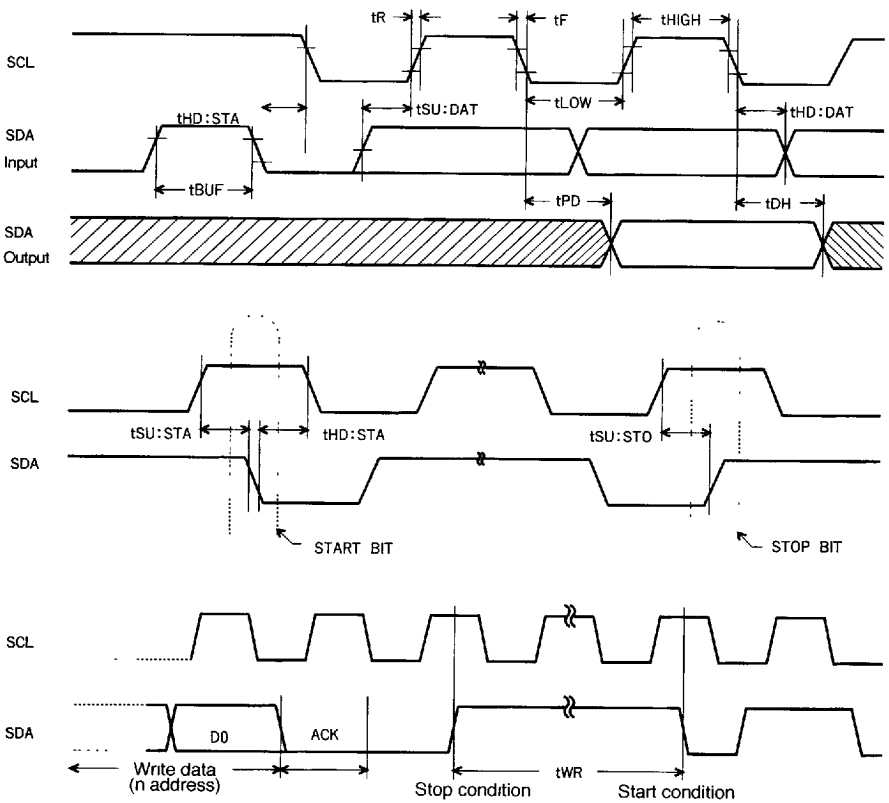
Electrical characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 2.7 V ~ 5.5 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Input voltage high	V_{IH}	0.7 V_{CC}			V	
Input voltage low	V_{IL}			0.3 V_{CC}	V	
Output voltage low	V_{OL}			0.4	V	I_{OL} = 3.0 mA (SDA)
Input leak current	I_{LI}	− 10		10	µA	V_{IN} = 0 V ~ V_{CC}
Output leak current	I_{LO}	−10		10	µA	V_{OUT} = 0 V ~ V_{CC}
Operating current consumed	I_{CC}			1.0	mA	V_{CC} = 5.5 V, f_{SCL} = 100 kHz
Stand-by current	I_{SB}			2.0	µA	V_{CC} = 5.5 V, SDA and SCL = V_{CC}
SCL frequency	f_{SCL}			100	kHz	

Timing characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 2.7 ~ 5.5 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Data clock time high	t_{HIGH}	4.0			µs	
Data clock time low	t_{LOW}	4.7			µs	
SDA and SCL rise time	t_R			1.0	µs	
SDA and SCL fall time	t_F			0.3	µs	
Start condition hold time	t_{HD}:STA	4.0			µs	
Start condition setup time	t_{SU}:STA	4.7			µs	
Input data hold time	t_{HD}:DAT	0			ns	
Input data setup time	t_{SU}:DAT	250			ns	
Output data delay time	t_{PD}	0.3		3.5	µs	
Output data hold time	t_{DH}	0.3			µs	
Stop condition setup time	t_{SU}:STO	4.7			µs	
Bus open time before start of transfer	t_{BUF}	4.7			µs	
Internal write cycle time	t_{WR1}			10	ms	V_{CC} = 4.5 ~ 5.5 V
	t_{WR2}			25	ms	V_{CC} = 2.7 ~ 3.3 V
Noise erase valid time (SCL or SDA pin)	t_I			0.1	µs	

Figure 1 Timing chart



Note: Data is input on the rising edge of SCL. Data is output on the falling edge of SCL

Circuit operation

Start condition (recognition of start bit)

Before executing any command, a start condition (start bit) is required. A start bit is recognized when SDA falls from HIGH to LOW with SCL HIGH.

Stop condition (recognition of stop bit)

To stop any command, the stop condition (stop bit) must be issued. A stop bit is defined as the condition when SDA is raised from LOW to HIGH with SCL HIGH.

Write command

In the WRITE mode, when the stop bit is not executed, the transferred data is not written to memory.

Device addressing—BR24C01A/AF, BR24C02/F

Make sure to output the slave address from the master immediately after the start condition.

The upper four bits of the slave address are used to determine the device type. This IC has its device code fixed at 1010.

The next three bits of the slave address (A2, A1, A0 device address) are used to select the device. This IC can address up to eight devices on the same bus.

The lowermost bit of the slave address (R/$\overline{W}$, READ/$\overline{WRITE}$) is used to set the write or read mode as follows:

R/W set to 0 = write: R/W set to 1 = read

(Random read word address setting is also 0)

Device addressing—BR24C04/F

Make sure to output the slave address from the master in continuation with the start condition.

The upper four bits of the slave address are used to determine the device type. This IC has its device code fixed at 1010.

The next two bits of the slave address (A2, A1 device address) are used to select the device. This IC can address up to four devices on the same bus.

The next bit of the slave address (PS page select) is used to select the page. As shown following, it can write or read to any of the 256 words in the 2 pages in memory.

PS set to 0 = page 1 (000 - 0FF): PS set to 1 = page 2 (100 – 1FF)

The lowermost bit of the slave address (R/$\overline{W}$: READ/$\overline{WRITE}$) is used to set the write or read mode as follows:

R/$\overline{W}$ set to 0 = write: R/$\overline{W}$ set to 1 = read

(Random read word address setting is also 0)

ACK signal

The acknowledge signal (ACK signal) is determined by software and is used to indicate whether or not a data transfer is proceeding normally.

The transmitting device, whether the master or slave, opens the bus after an 8-bit data output (μ-COM when a write or read command of the slave address input; this IC when reading data)

For the receiving device during the 9th clock cycle, SDA is set to LOW and an acknowledge signal (ACK signal) is sent to indicate that it received the 8-bit data (this IC when a write command or a read command of the slave address input, μ-COM when a read command data output).

This IC outputs a LOW acknowledge signal (ACK signal) after recognizing the start condition and slave address (8 bits).

When data is being written to this IC, a LOW acknowledge signal (ACK signal) is output after the receipt of each 8 bits of data (word address and write data).

When data is being read from the IC, 8 bits of data (read data) are output and the IC waits for a returned LOW acknowledge signal (ACK signal). When an acknowledge signal (ACK signal) is detected and a stop condition is not sent from the master (μ-COM) side, the IC sends the next 8 bits of data.

If an acknowledge signal (ACK signal) is not detected, the IC interrupts the data transfer and ceases read operations after recognizing the stop condition (stop bit). The IC enters a wait state.

Figure 2 Acknowledge (ACK) signal response (during read, write slave address input)

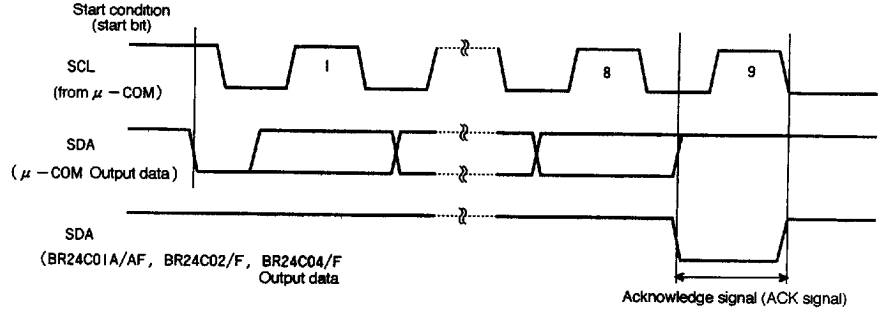


Figure 3 Byte write cycle—BR24C01A and BR24C01AF

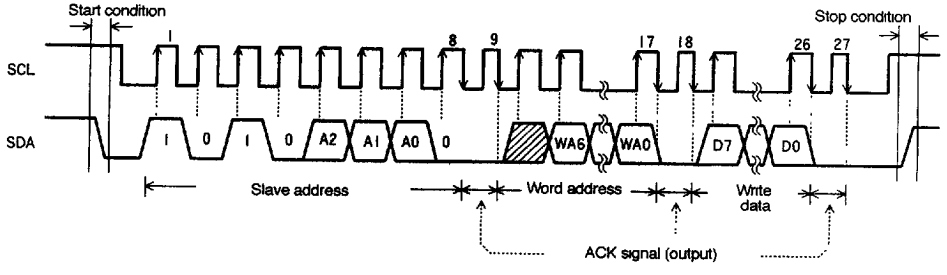


Figure 4 Byte write cycle—BR24C02 and BR24C02F

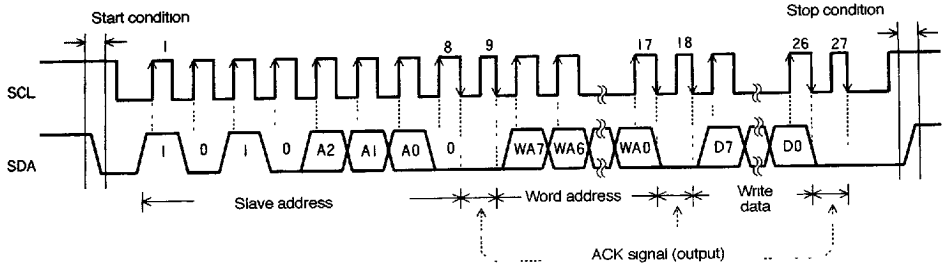
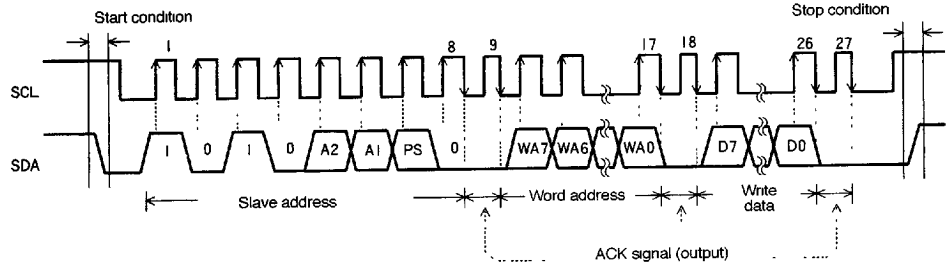


Figure 5 Byte write cycle—BR24C04 and BR24C04F

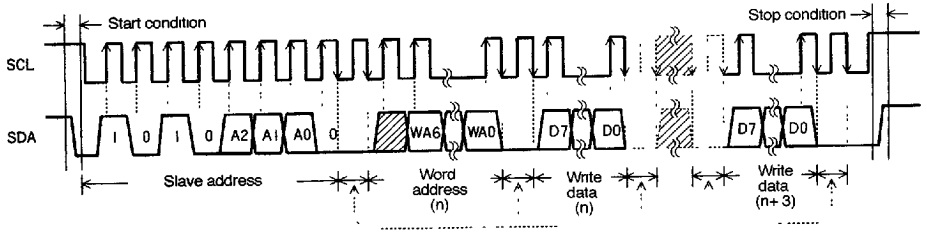


Data is written to the address designated by the word address (n address).

After 8 bits of data are input, the data is written to the memory cell by issuing the stop bit.

Page write

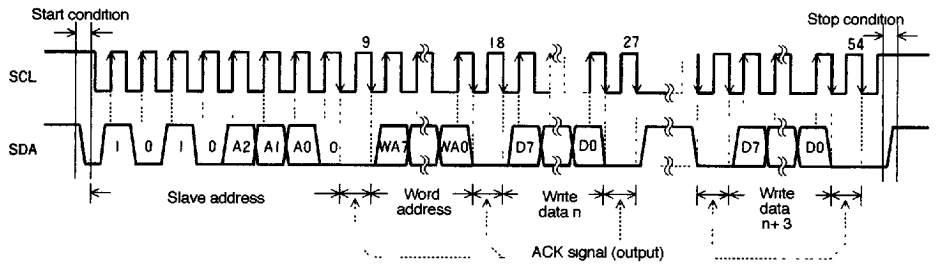
Figure 6 Page write cycle—BR24C01A and BR24C01AF



A 4-byte write is possible using this command.

The page write command arbitrarily sets the upper five bits (WA6 - WA2) of the word address. The lower two bits (WA1 - WA0) can write up to four bytes of data with the address being incremented internally.

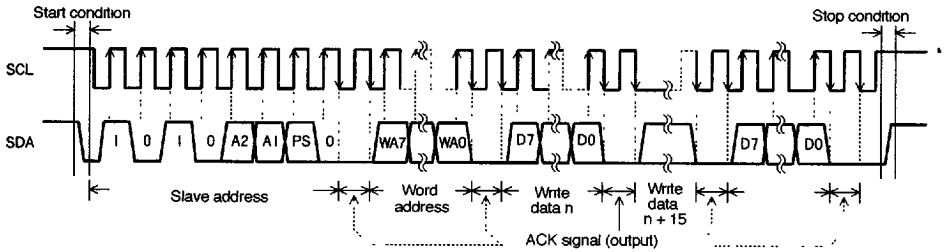
Figure 7 Page write cycle—BR24C02 and BR24C02F



A 4-byte write is possible using this command.

This page write command arbitrarily sets the upper six bits (WA7 - WA2) of the word address. The lower two bits (WA1 - WA0) can write up to four bytes of data with the address being incremented internally.

Figure 8 Page write cycle—BR24C04 and BR24C04F



A 16-byte write is possible using this command.

This page write command arbitrarily sets the upper four bits (WA7 - WA4) of the word address. The lower four bits (WA3 - WA0) can write up to 16 bytes of data with the address being incremented internally.

Current read

Figure 9 Current write cycle—BR24C01A and BR24C01AF

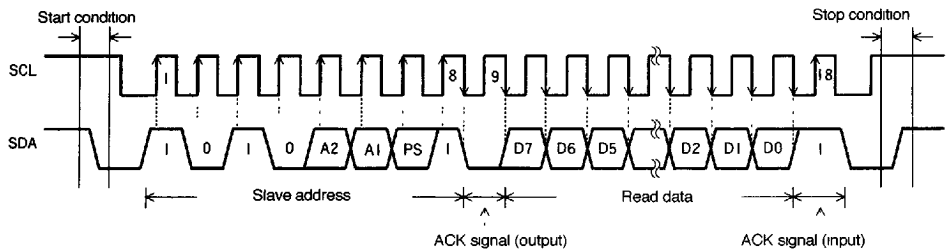


Figure 10 Current write cycle—BR24C02 and BR24C02F

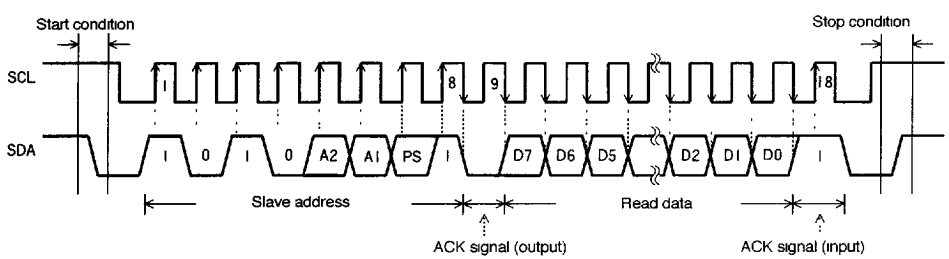
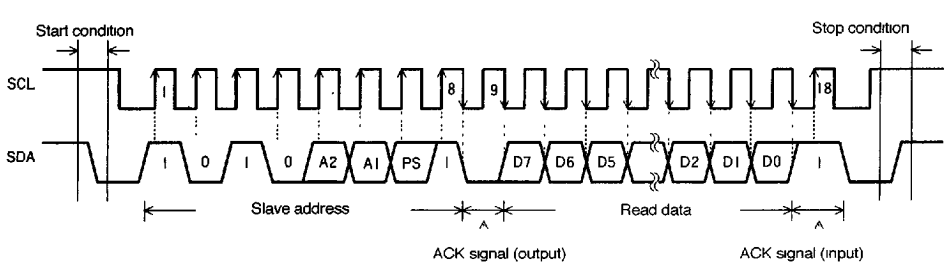


Figure 11 Current write cycle—BR24C04 and BR24C04F



This IC increments the address by one position by using the internal circuit address count. It records the final word address (n address) of the executed write - read command.

This command reads the data of the next word address (n + 1 address) of the final write word address after the execution of the previous command.

When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. (Refer to Figures 15 - 17):

This command is ended by inputting HIGH to the ACK signal after D0 and raising the SDA signal (stop condition) by setting SCL HIGH.

Figure 12 Random read—BR24C01A and BR24C01AF

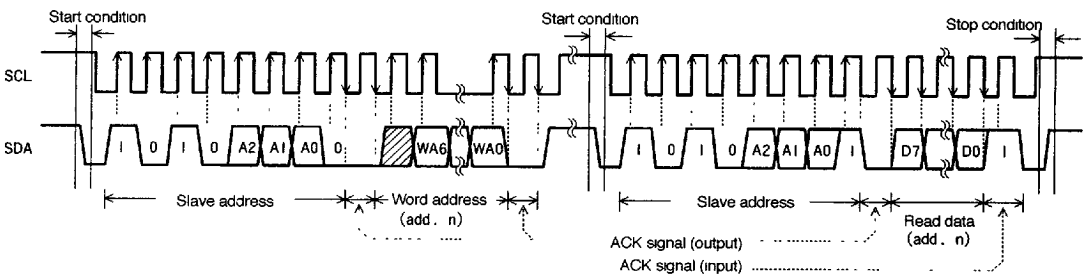


Figure 13 Random read—BR24C02 and BR24C02F

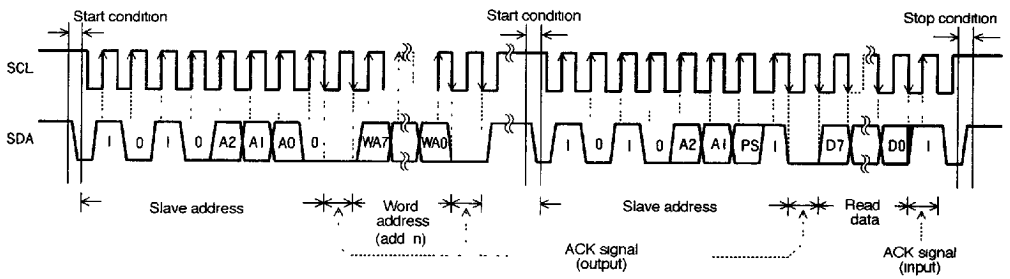
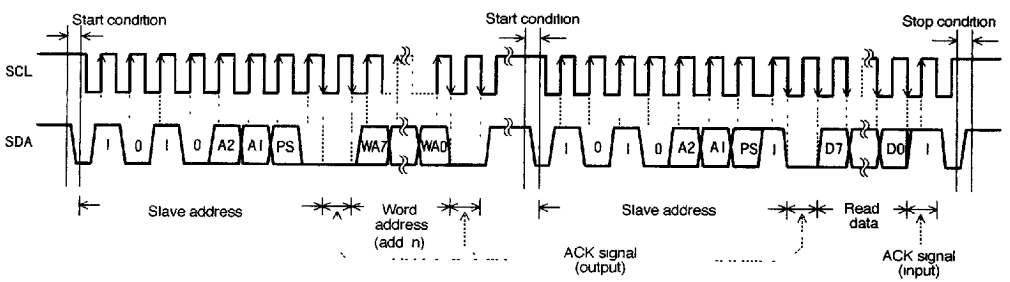


Figure 14 Random read—BR24C04 and BR24C04F



This command can read the designated word address data.

When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. (Refer to Figures 15 - 17).

This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) by raising SCL HIGH.

Figure 15 Sequential read—BR24C01A and BR24C01AF—Ex: for a current read

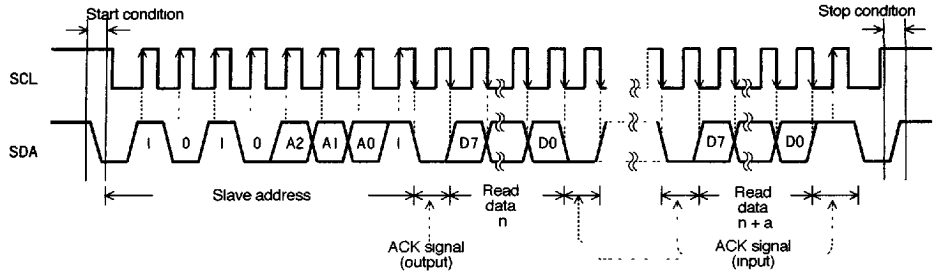


Figure 16 Sequential read—BR24C02 and BR24C02F—Ex: for a current read

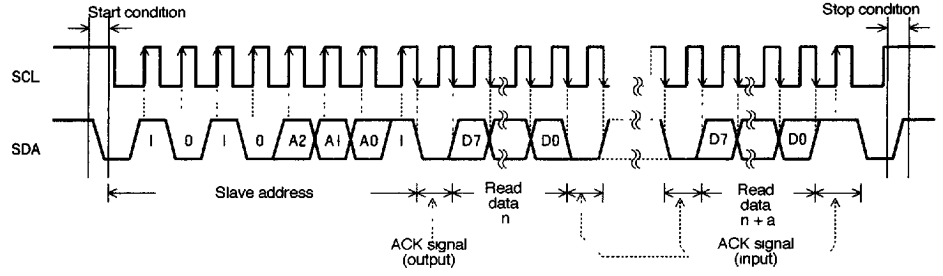
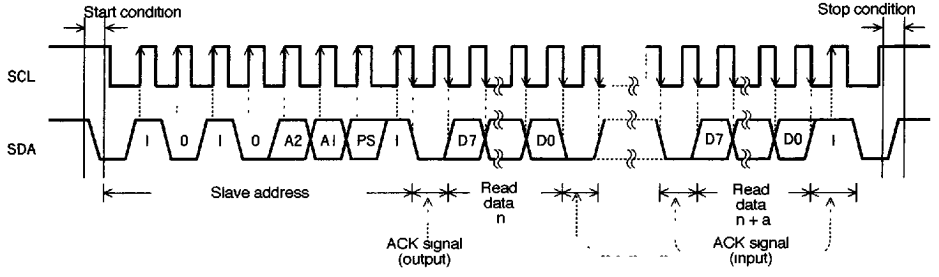


Figure 17 Sequential read—BR24C04 and BR24C04F—Ex: for a current read

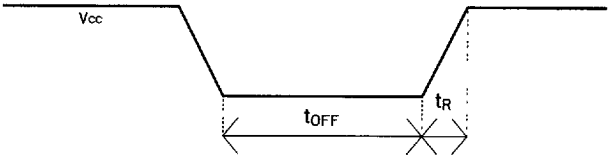


When an ACK signal "LOW" is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. (All words can be read)

This command is ended by inputting a HIGH to the ACK signal after D0 and raising the SDA signal (stop condition) using the SCL signal HIGH.

A sequential read is possible for a random read.

Figure 18



Precautions for use

Powering up the IC

When power is connected, V_{CC} rises through the low power supply voltage region in which the IC internal circuits do not operate. Thus, if the power supply voltage rises without completely resetting the internal logic, erroneous operation may occur. To avoid this, ensure the following sequence is followed:

- Set SCL = SDA = HIGH
- Raise the power supply voltage such that the Power on Reset (POR) circuit operates.

Note the following requirements to ensure that the POR functions correctly:

- Set the power supply voltage rise time (t_R) to less than 10 ms.
- Set the OFF period (t_{OFF}) after the power supply is isolated to greater than 100 ms.

SDA pin pull-up resistance

The SDA pin is an N channel open drain output. Therefore, a pull-up external resistor is required. Make sure to select an appropriate value for this pull-up resistance value based on the V_{OL} and I_{OL} characteristics of this IC, together with the measured data for V_{IL} and I_{LI} for personal computers and other devices that control this IC.

The recommended value for the resistor is 2.0 ~10 kΩ

Electrical characteristic curves

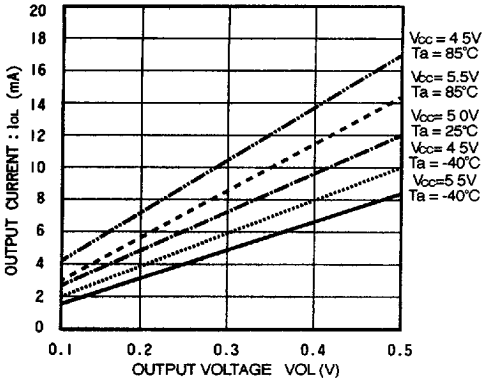


Figure 19

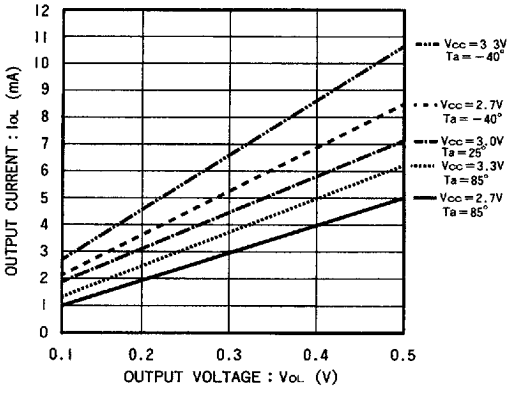


Figure 20

Note: The memory data array is in the "FF" state when shipped from ROHM.