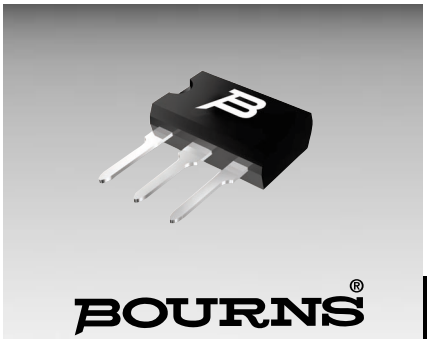
DUAL BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS



BOURNS®

TISP3600F3, TISP3700F3

IEEE Std 802.3 LAN and MAN Applications

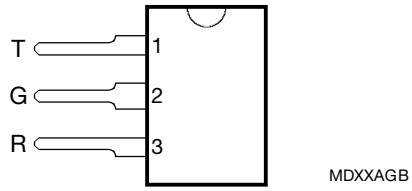
Ion-Implanted Breakdown Region
Precise and Stable Voltage

Terminals	T&G, R&G		T & R	
Device	V_{DRM} V	$V_{(BO)}$ V	V_{DRM} V	$V_{(BO)}$ V
'3600	420	600	840	1200
'3700	500	700	1000	1400

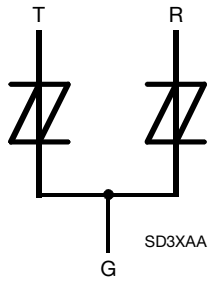
Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{TSP} A
2/10	GR-1089-CORE	190
8/20	IEC 61000-4-5	175
10/160	FCC Part 68	110
10/700	FCC Part 68 ITU-T K.20/21	70
10/560	FCC Part 68	50
10/1000	GR-1089-CORE	45

SL Package (Top View)



Device Symbol



Terminals T, R and G correspond to the alternative line designators of A, B and C

How To Order

Device	Package	Carrier	Order #
TISP3600F3	SL, Single-in-line	TUBE	TISP3600F3SL
TISP3700F3	SL, Single-in-line	TUBE	TISP3700F3SL

Description

These devices are designed to limit overvoltages between systems and so protect their insulation. A single device can be used in two ways; as a 3-point protector or as a 2-point protector. In the 3-point mode, the G terminal is connected to the system protective ground and the R and T terminals are connected to the two conductors being protected. For the TISP3600F3, each conductor will have its voltage limited to ±600 V from the protective ground. The maximum inter-conductor voltage will be limited to ±1200 V.

In the 2-point mode, only the outer R and T terminals are connected and the G terminal is unconnected. The TISP3700F3 limits the voltage between the two connection nodes to ±1400 V with voltage limiting beginning above ±1000 V. Two TISP3700F3 devices connected in series would allow insulation testing to ±2000 V (1400 Vrms).

The protector consists of two symmetrical voltage-triggered bidirectional thyristors with a common connection. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are coupled on to the system. These overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

The TISP3x00F3 is guaranteed to voltage limit and withstand the listed international lightning surges in both polarities.

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Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, (R-G or T-G value)	TISP3600F3	V_{DRM}	± 420	V
	TISP3700F3		± 500	
Non-repetitive peak on-state pulse current (see Notes 1 and 2)		I_{PPSM}		A
2/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape)			190	
1/20 (ITU-T K.22, 1.2/50 voltage wave shape, 25 Ω resistor)			100	
8/20 (IEC 61000-4-5, combination wave generator, 1.2/50 voltage wave shape)			175	
10/160 (FCC Part 68, 10/160 voltage wave shape)			110	
4/250 (ITU-T K.20/21, 10/700 voltage wave shape, simultaneous)			95	
5/310 (ITU-T K.20/21, 10/700 voltage wave shape, single)			70	
5/320 (FCC Part 68, 9/720 voltage wave shape, single)			70	
10/560 (FCC Part 68, 10/560 voltage wave shape)			50	
10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)			45	
Non-repetitive peak on-state current (see Notes 1 and 2) 50/60 Hz, 1 s		I_{TSM}	6	A
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value < 38 A		di_T/dt	250	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Initially, the TISP® device must be in thermal equilibrium with T_J = 25 °C.
2. These non-repetitive rated currents are peak values of either polarirty. The rated current values may be applied to the R or T terminals. Additionally, both R and T terminals may have their rated current values applied simultaneously (in this case the G terminal return current will be the sum of the currents applied to the R and T terminals). The surge may be repeated after the TISP returns to its initial conditions.

Recommended Operating Conditions

Component		Min	Typ	Max	Unit
R1, R2	Series resistor for GR-1089-CORE first-level surge survival	15			Ω
	Series resistor for ITU-T recommendation K.20 and K.21	0			
	Series resistor for FCC Part 68 9/720 survival	0			
	Series resistor for FCC Part 68 10/160, 10/560 survival	10			

Electrical Characteristics for the T and R Terminals, T_A = 25 °C

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = ±2V_{DRM}				±10	µA
$V_{(BO)}$	Breakover voltage	dv/dt = ±700 V/ms, R_{SOURCE} = 300 Ω	TISP3600F3			±1200	V
			TISP3700F3			±1400	
$I_{(BO)}$	Breakover current	dv/dt = ±700 V/ms, R_{SOURCE} = 300 Ω			±0.1		A
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms			±0.15		A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 1.7V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V				±10	µA

Electrical Characteristics for the T and R Terminals, T_A = 25 °C (Continued)

Parameter		Test Conditions	Min	Typ	Max	Unit
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0, (See Note 3)			0.1	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.

Electrical Characteristics for the T and G or the R and G Terminals, T_A = 25 °C

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$				±5	µA
$V_{(BO)}$	Breakover voltage	dv/dt = ±700 V/ms, R_{SOURCE} = 300 Ω	TISP3600F3			±600	V
			TISP3700F3			±700	
$I_{(BO)}$	Breakover current	dv/dt = ±700 V/ms, R_{SOURCE} = 300 Ω			±0.1		A
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15			A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V				±10	µA
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0, (See Note 4)			44	74	pF
		f = 100 kHz, V_d = 1 V rms, V_D = -50 V			11	20	

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 5)			50	°C/W

NOTE 5: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

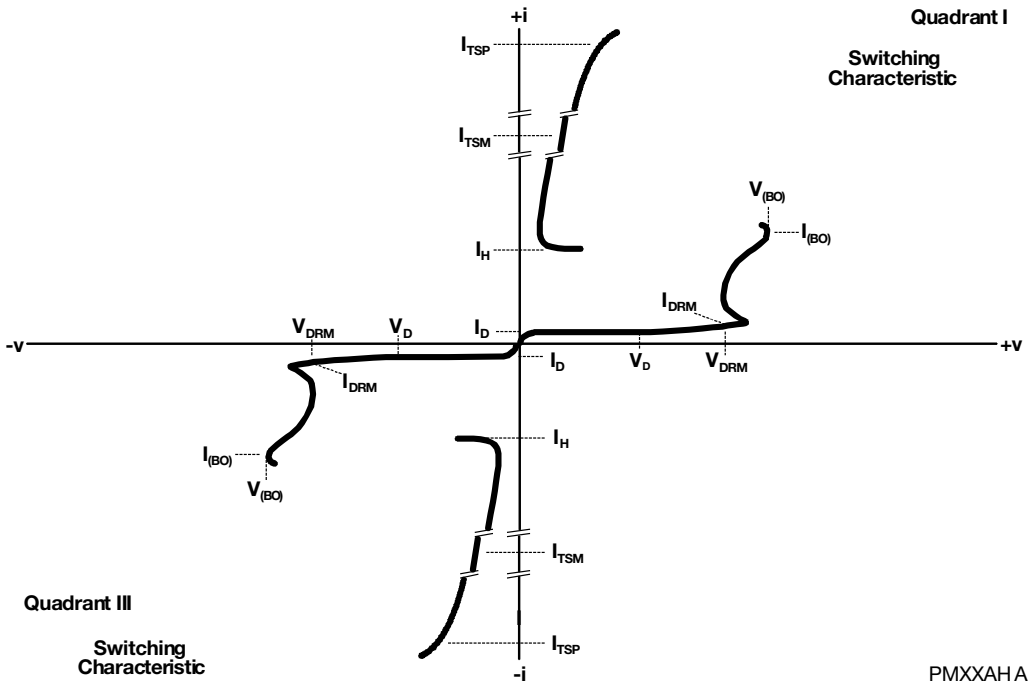

Figure 1. Voltage-Current Characteristic for R-G and T-G Terminal Pairs

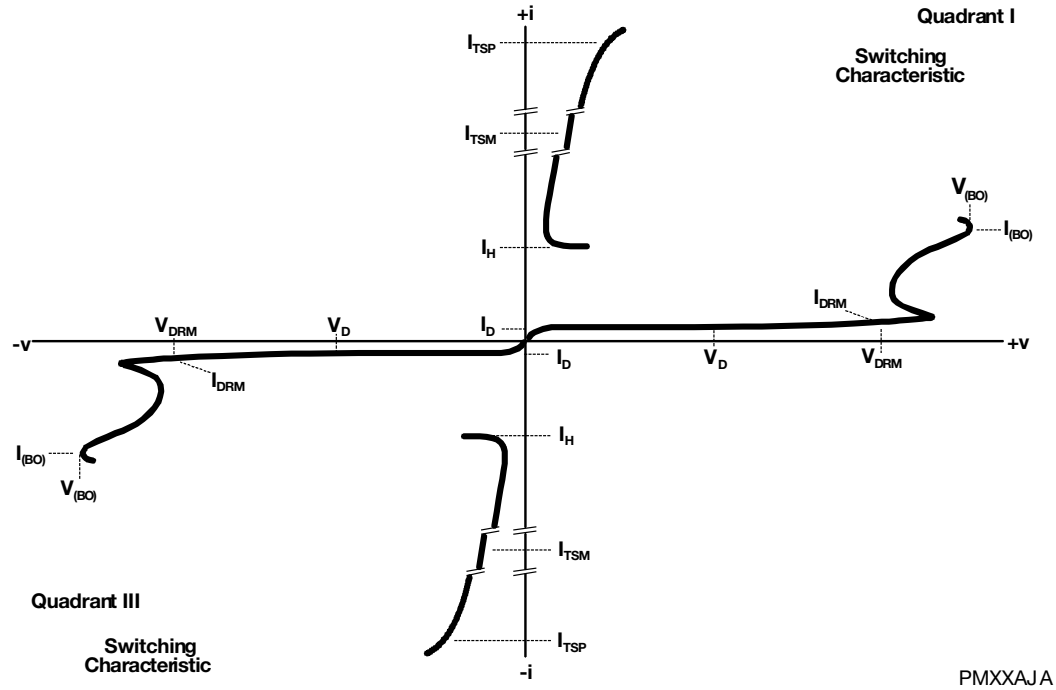

Figure 2. Voltage-Current Characteristic for R-T Terminal Pair

Typical Characteristics

OFF-STATE CURRENT
vs
JUNCTION TEMPERATURE

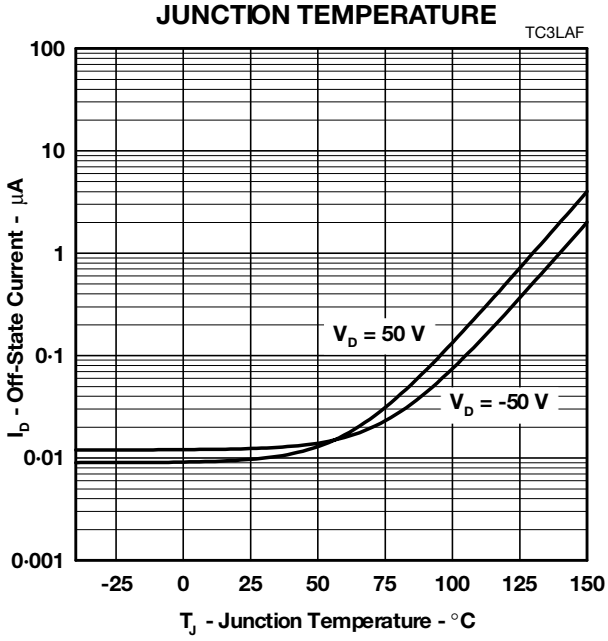

Figure 3.

NORMALIZED BREAKOVER VOLTAGE
vs
JUNCTION TEMPERATURE

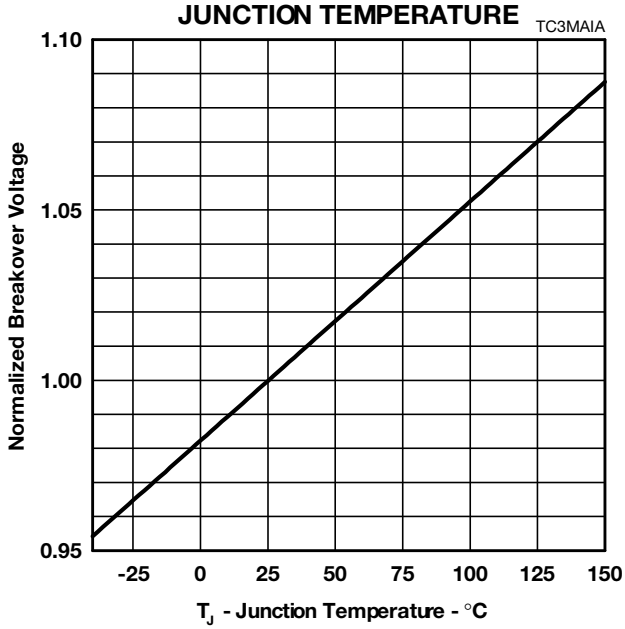

Figure 4.

HOLDING CURRENT
vs
JUNCTION TEMPERATURE

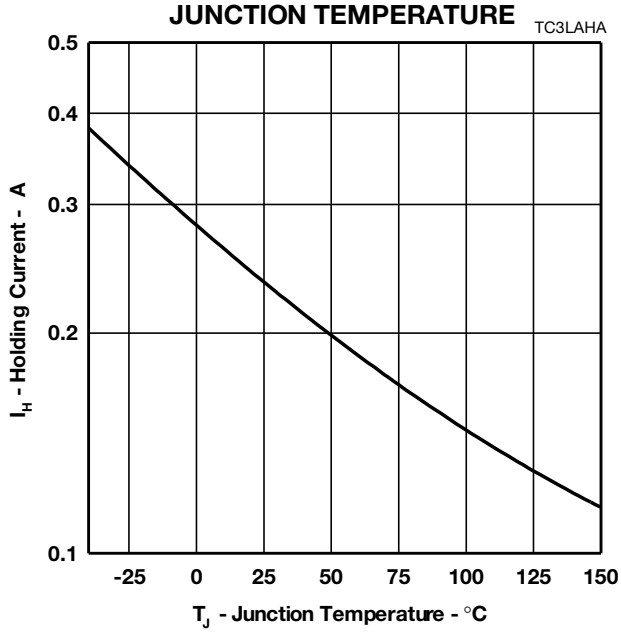

Figure 5.

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Thermal Information

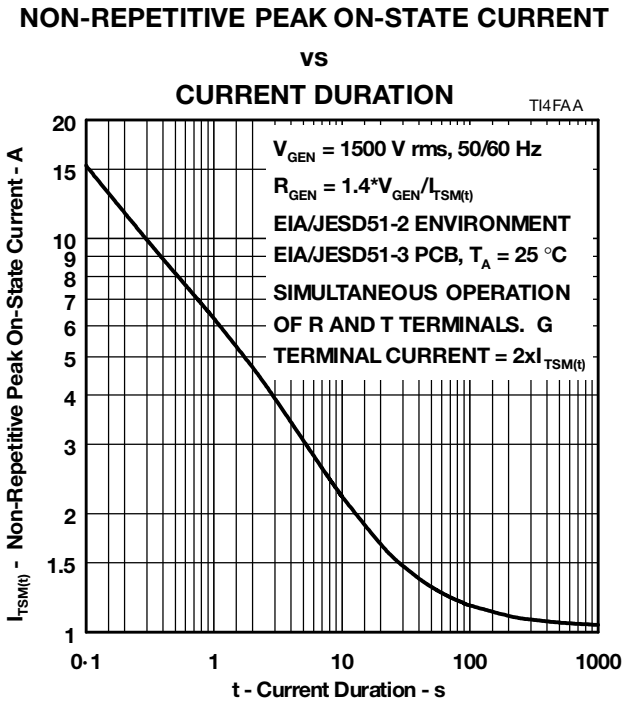

Figure 6.

APPLICATIONS INFORMATION

IEC 60950, EN 60950, UL 1950 and CSA 22.2 No.950

The '950 family of standards have certain requirements for equipment (EUT) with incoming lines of telecommunication network voltage (TNV). Any protector from a TNV conductor to protective ground must have a voltage rating of at least 1.6 times the equipment rated supply voltage (Figure 7). The intent is to prevent the possibility of the a.c. main supply voltage from feeding into the telecommunication network and creating a safety hazard. International and European equipment usually have a maximum rated voltage of 230 V rms, 240 V rms or 250 V rms. Multiplying the 250 V value by 1.6 gives a protector V_{DRM} value of 400 V. Allowing for operation down 0 °C gives a V_{DRM} requirement of 420 V at 25 °C. This need is met by the TISP3600F3.

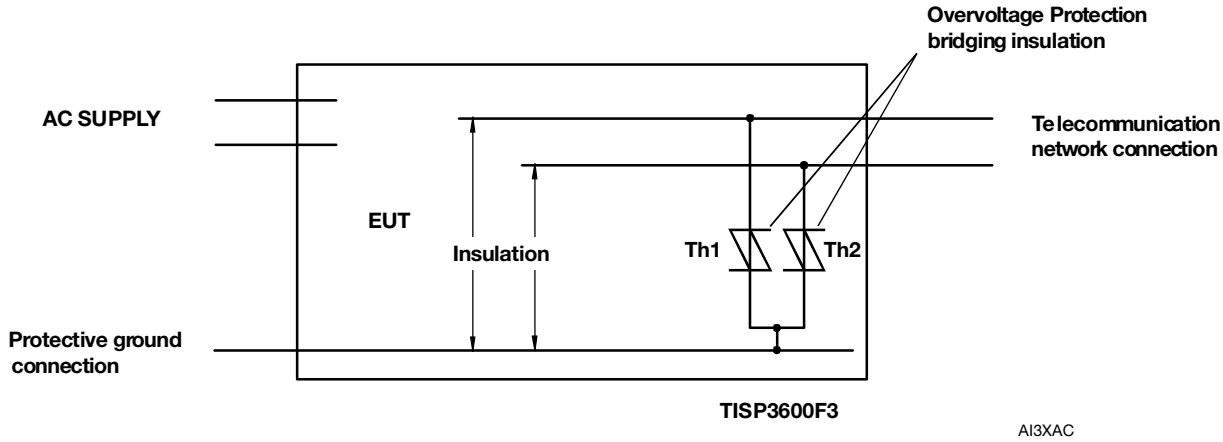

Figure 7. '950 TNV Network Insulation from Protective Ground

LAN System Insulation Protection

Some wired systems are not directly connected to ground and are either floating or have a high resistance to ground. Induced transients may cause high voltages relative to ground, resulting in arcing across insulation at wiring junctions. Arcing often leaves carbonized tracks which can degrade system performance. Where the system is carrying a power feed, current conduction through the carbonized track may cause a safety hazard.

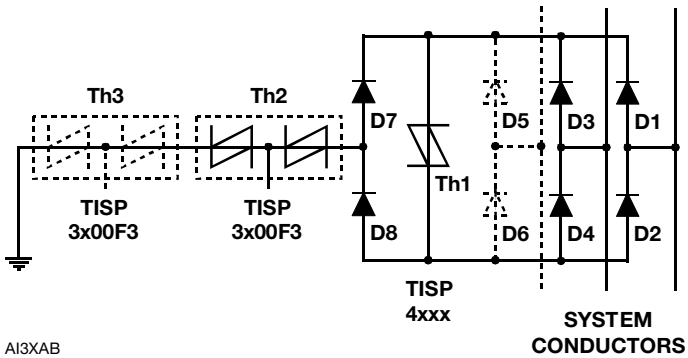

Figure 8. System Insulation Protection

In Figure 8, a low-protector, Th1, from a TISP4xxx series limits the differential conductor voltage of the system. The use of a diode bridge, D1 through D4, reduces the capacitive loading of the protectors on the system and can be extended to protect more conductors as shown by the dotted diodes D5 and D6. Low voltage diodes can be used as the maximum reverse voltage stress is limited to the $V_{(BO)}$ value of the TISP4xxx protector plus the diode forward recovery voltage. Steering diodes D7 and D8 and high-voltage protector Th2 limit the conductor voltage to ground. The limiting voltage is set by the choice of protector, TISP3600F3, 1200 V or TISP3700F3, 1400 V, and the number connected in series (one extra protector Th3 shown dotted).

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APPLICATIONS INFORMATION

LAN System Insulation Protection (continued)

IEEE Std 802.3, 2000 Edition *(IEEE Standard for Information technology— Telecommunications and information exchange between systems— Local and metropolitan area networks— Specific requirements, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications)* specifies three network insulation withstands: 1.5 kV rms a.c., 2.25 kV d.c. and 2.4 kV 1.2/50 impulse. Under these conditions there shall be no insulation breakdown, as defined in IEC 60950:1991. Also, there is a 2 MΩ insulation resistance minimum requirement measured at 500 V d.c. (250 μA maximum).

In Figure 8, at least one protection element of a TISP3700F3 must be used to give the 500 V working voltage (V_{DRM}) to meet the insulation resistance requirement. To avoid breakover during the 2.4 kV impulse test, five TISP3700F3 protection elements (2.5 kV V_{DRM}, 2-1/2 SL packages) or six TISP3600F3 elements (2.52 kV V_{DRM}, 3 SL packages) are required. Transmitters are required to withstand a 1 kV 0.3/50 common-mode impulse. A TISP3700F3 (1 kV V_{DRM}), from each conductor to ground at the transmitter, would not breakover during the impulse.

BOD Replacement

Figure 9a shows a traditional overvoltage protection scheme for a high power switching thyristor, Th1. The protection voltage level is set by a BOD (BreakOver Diode) thyristor. Potentially damaging voltage transients cause the BOD to crowbar which turns on thyristor Th1. The on state of thyristor Th1 causes the current drawn by the load from the d.c. voltage supply +V to continuously increase until the fast acting fuse F1 operates.

Resistor R1 limits the peak BOD current and diode D1 protects the unidirectional BOD against reverse polarity voltage. Resistor R2 provides a d.c. return, and with capacitor C1, forms a low pass network to prevent false triggering from noise. Further trigger voltage discrimination and isolation is given by the series combination of zener diode D2 and reverse blocking diode D3. Capacitor C2 and Resistor R3 form the normal snubber network for the thyristor Th1.

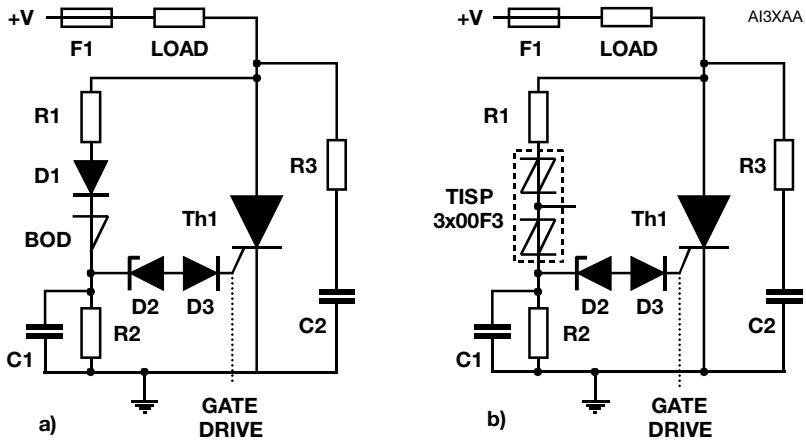

Figure 9. Thyristor Protection

Figure 9b shows the TISP3x00F3 replacing the unidirectional BOD and reverse polarity protection diode, D1. Reverse polarity protection is not needed for the TISP3x00F3 as it is bidirectional.

MECHANICAL DATA

Device Symbolization Code

Devices will be coded as follows:

DEVICE	SYMBOLIZATION CODE
TISP3600F3	SP3600F3
TISP3700F3	SP3700F3

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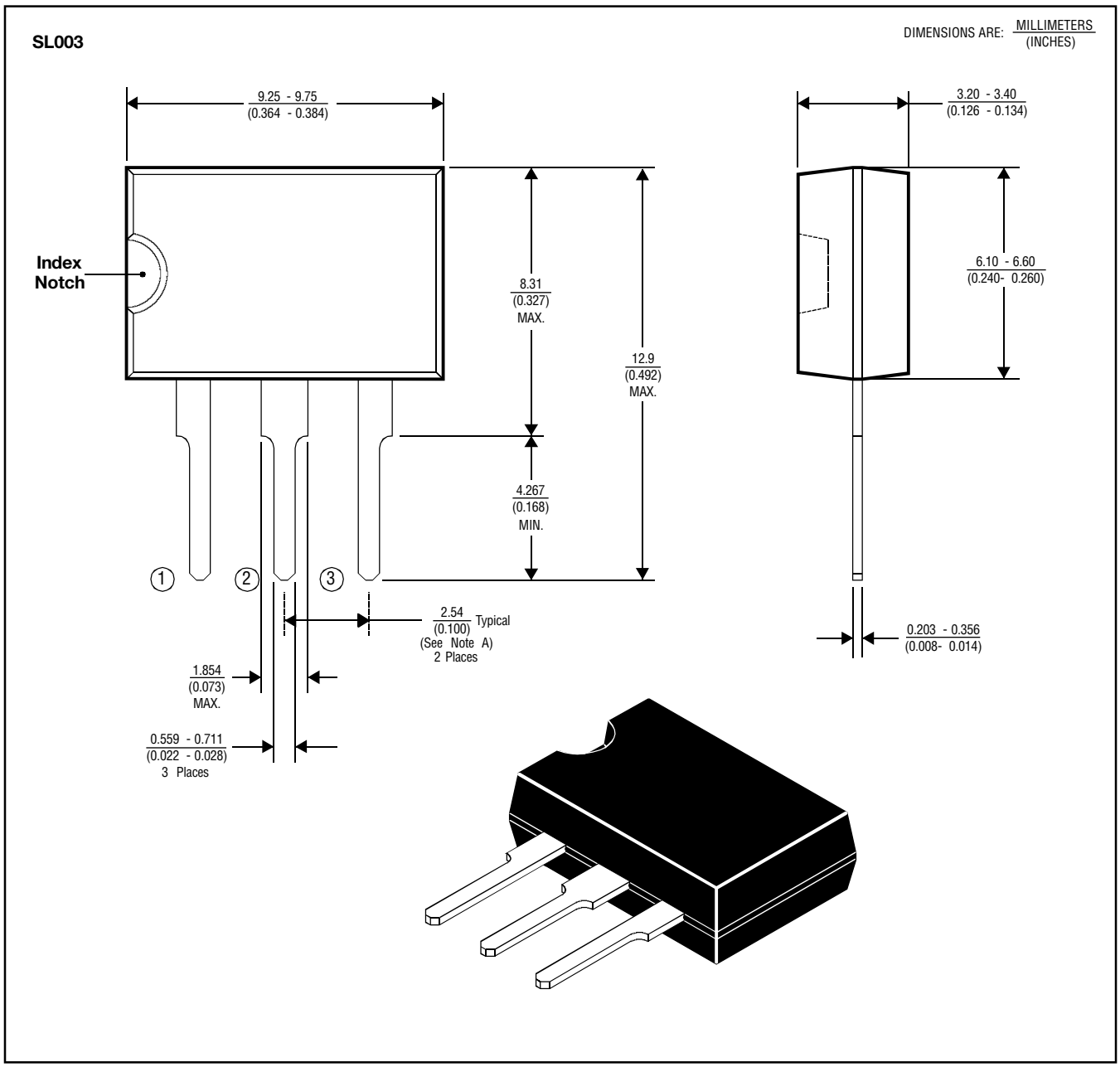
MECHANICAL DATA

SL003 3-pin Plastic Single-In-Line Package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



MDXXCEB

NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
B. Body molding flash of up to 0.15 (0.006) may occur in the package lead plane.