

MC10EL15, MC100EL15

5V ECL 1:4 Clock Distribution Chip

The MC10EL/100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable (EN) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

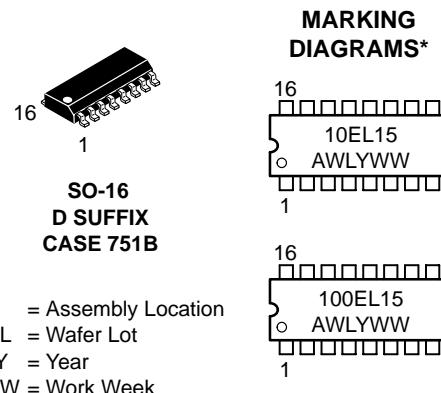
The 100 series contains temperature compensation.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors on CLKs, SCLK, SEL, and EN.



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*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC10EL15D	SO-16	48 Units / Rail
MC10EL15DR2	SO-16	2500 Tape & Reel
MC100EL15D	SO-16	48 Units / Rail
MC100EL15DR2	SO-16	2500 Tape & Reel

†For additional tape and reel information, refer to Brochure BRD8011/D.

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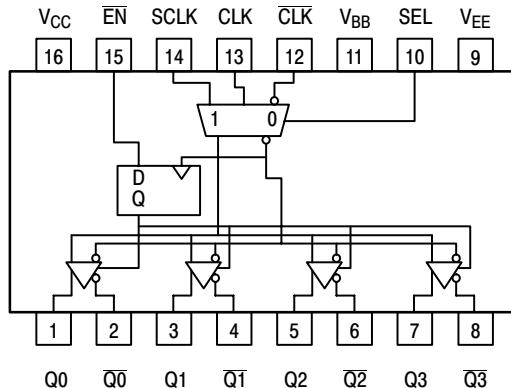


Figure 1. Logic Diagram and Pinout Assignment

PIN DESCRIPTION

PIN	FUNCTION
CLK, <u>CLK</u>	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
<u>EN</u>	ECL Sync Enable
SEL	ECL Clock Select Input
Q ₀₋₃ , <u>Q₀₋₃</u>	ECL Diff Clock Outputs
V _{BB}	Reference Voltage Output
V _{CC}	Positive Supply
V _{EE}	Negative Supply

FUNCTION TABLE

CLK*	SCLK*	SEL*	<u>EN</u> *	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L(1)

1. On next negative transition of CLK or SCLK
 *Pins will default low when left open.

ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	75 KΩ	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 KV > 100 V 2 KV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)	Level 1	
Flammability Rating Oxygen Index	UL 94 V-0 @ 0.125 in 28 to 34	
Transistor Count	103	
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

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MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0$ V		8	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0$ V		-8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0$ V $V_{CC} = 0$ V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-16 SO-16	130 75	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SO-16	33 to 36	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

3. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0$ V; $V_{EE} = 0.0$ V (Note 4)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	35		25	35		25	35	mA
V_{OH}	Output HIGH Voltage (Note 5)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 5)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.3			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.06 V / -0.5 V.
5. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2 volts.
6. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

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10EL SERIES NECL DC CHARACTERISTICS $V_{CC} = 0.0$ V; $V_{EE} = -5.0$ V (Note 7)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	35		25	35		25	35	mA
V_{OH}	Output HIGH Voltage (Note 8)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
V_{OL}	Output LOW Voltage (Note 8)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1230		-890	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1950		-1500	-1950		-1480	-1950		-1445	mV
V_{BB}	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 9)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μ A
I_{IL}	Input LOW Current	0.5			0.5			0.3			μ A

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.06 V / -0.5 V.

8. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2 volts.

9. V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

100EL SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0$ V; $V_{EE} = 0.0$ V (Note 10)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	35		25	35		25	38	mA
V_{OH}	Output HIGH Voltage (Note 11)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 11)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 12)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μ A
I_{IL}	Input LOW Current	0.5			0.5			0.5			μ A

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

10. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.

11. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2 volts.

12. V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

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100EL SERIES NECL DC CHARACTERISTICS $V_{CC} = 0.0$ V; $V_{EE} = -5.0$ V (Note 13)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	35		25	35		25	38	mA
V_{OH}	Output HIGH Voltage (Note 14)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 14)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 15)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μ A
I_{IL}	Input LOW Current	0.5			0.5			0.5			μ A

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

13. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.

14. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2 volts.

15. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

AC CHARACTERISTICS $V_{CC} = 5.0$ V; $V_{EE} = 0.0$ V or $V_{CC} = 0.0$ V; $V_{EE} = -5.0$ V (Note 16)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency				1.25						GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	460 410 410		660 710 710	470 420 420		670 720 720	500 450 470		700 750 750	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 17)			200 50			200 50			200 50	ps
t_{JITTER}	Random Clock Jitter (RMS)				2.6						ps
t_S	Setup Time \bar{EN}	150			150			150			ps
t_H	Hold Time \bar{EN}	400			400			400			ps
V_{PP}	Input Swing (Note 18)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	325		575	325		575	325		575	ps

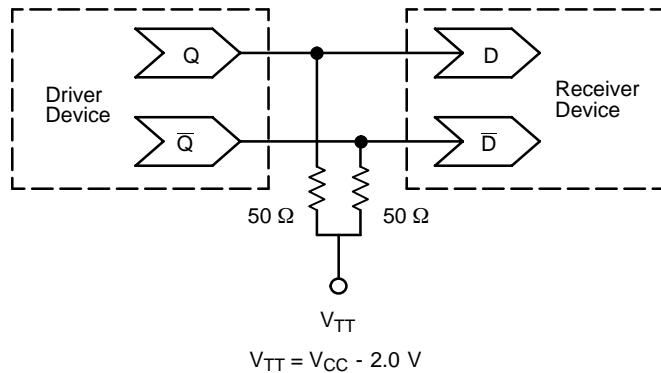
16. 10 Series: V_{EE} can vary +0.06 V / -0.5 V.

100 Series: V_{EE} can vary +0.8 V / -0.5 V.

17. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.

18. $V_{PP(min)}$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .

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**Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 - Termination of ECL Logic Devices.)**

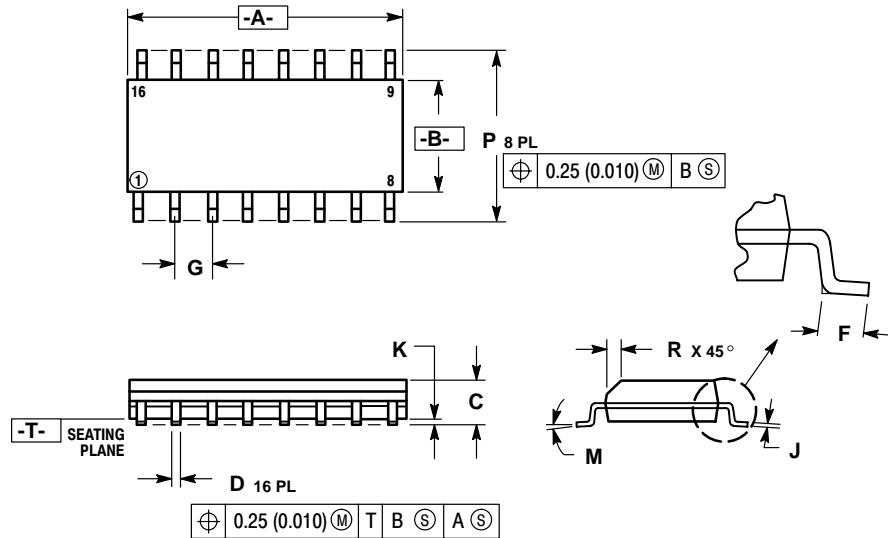
Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices
- AND8090** - AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SO-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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