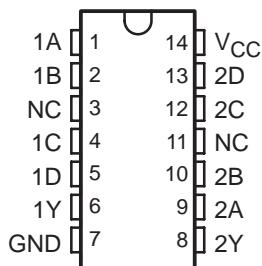
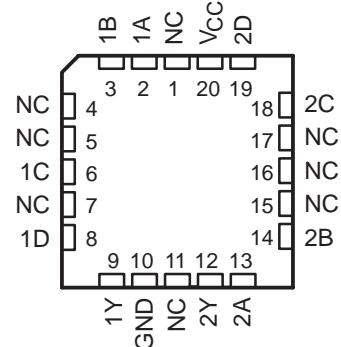


- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 11$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC20 . . . J OR W PACKAGE
SN74HC20 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC20 devices contain two independent 4-input NAND gates. They perform the Boolean function $Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC20N	SN74HC20N
	SOIC – D	Tube of 50	SN74HC20D	HC20
		Reel of 2500	SN74HC20DR	
		Reel of 250	SN74HC20DT	
	SOP – NS	Reel of 2000	SN74HC20NSR	HC20
	SSOP – DB	Reel of 2000	SN74HC20DBR	HC20
	TSSOP – PW	Tube of 90	SN74HC20PW	HC20
		Reel of 2000	SN74HC20PWR	
		Reel of 250	SN74HC20PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC20J	SNJ54HC20J
	CFP – W	Tube of 150	SNJ54HC20W	SNJ54HC20W
	LCCC – FK	Tube of 55	SNJ54HC20FK	SNJ54HC20FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC20, SN74HC20 DUAL 4-INPUT POSITIVE-NAND GATES

SCLS086F – DECEMBER 1982 – REVISED AUGUST 2003

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC20, SN74HC20
DUAL 4-INPUT POSITIVE-NAND GATES

SCLS086F – DECEMBER 1982 – REVISED AUGUST 2003

recommended operating conditions (see Note 3)

			SN54HC20			SN74HC20			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5			0.5		V
		V _{CC} = 4.5 V		1.35			1.35		
		V _{CC} = 6 V		1.8			1.8		
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/ΔV	Input transition rise/fall time	V _{CC} = 2 V		1000			1000		ns
		V _{CC} = 4.5 V		500			500		
		V _{CC} = 6 V		400			400		
T _A	Operating free-air temperature		-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC20		SN74HC20		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9		1.9		V	
			4.5 V	4.4	4.499	4.4		4.4			
			6 V	5.9	5.999	5.9		5.9			
		I _{OH} = -4 mA	4.5 V	3.98	4.3	3.7		3.84			
			6 V	5.48	5.8	5.2		5.34			
		I _{OL} = 20 μA	2 V		0.002	0.1	0.1		0.1		
V _{OL}	V _I = V _{IH} or V _{IL}		4.5 V		0.001	0.1	0.1		0.1		
			6 V		0.001	0.1	0.1		0.1		
			I _{OL} = 4 mA	4.5 V		0.17	0.26	0.4	0.33		
			I _{OL} = 5.2 mA	6 V		0.15	0.26	0.4	0.33		
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			2	40	20		20	μA	
C _i		2 V to 6 V		3	10		10		10	pF	

SN54HC20, SN74HC20 DUAL 4-INPUT POSITIVE-NAND GATES

SCLS086F – DECEMBER 1982 – REVISED AUGUST 2003

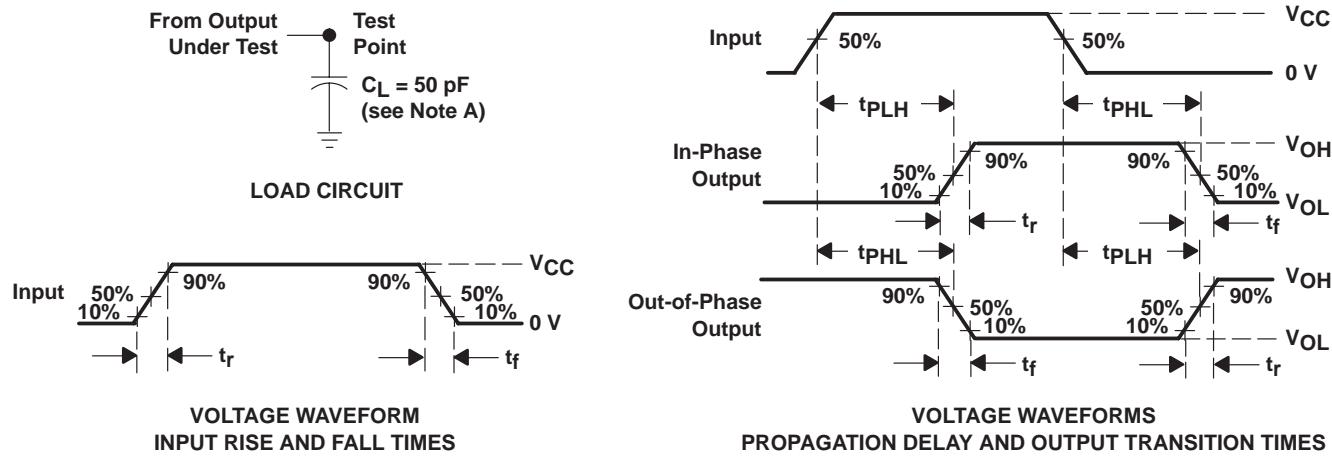
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC20		SN74HC20		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, C, or D	Y	2 V	45	110	165	140				ns
			4.5 V	14	22	33	28				
			6 V	11	19	28	24				
t _t		Y	2 V	27	75	110	95				ns
			4.5 V	9	15	22	19				
			6 V	7	13	19	16				

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES:

- C_L includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8403901VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8403901VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
84039012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8403901CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
8403901DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/65003BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54HC20J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74HC20D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC20N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI
SN74HC20NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC20NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HC20PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC20PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC20FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC20J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54HC20W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

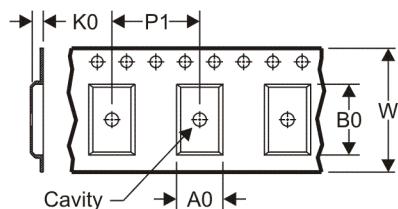
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

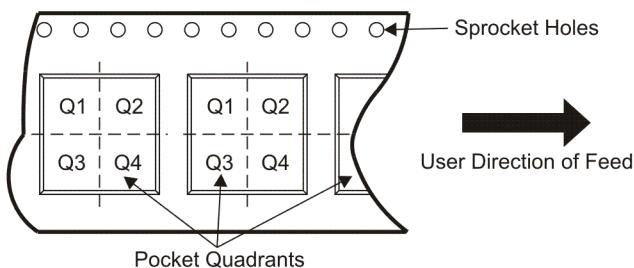
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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC20DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC20DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC20NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC20PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



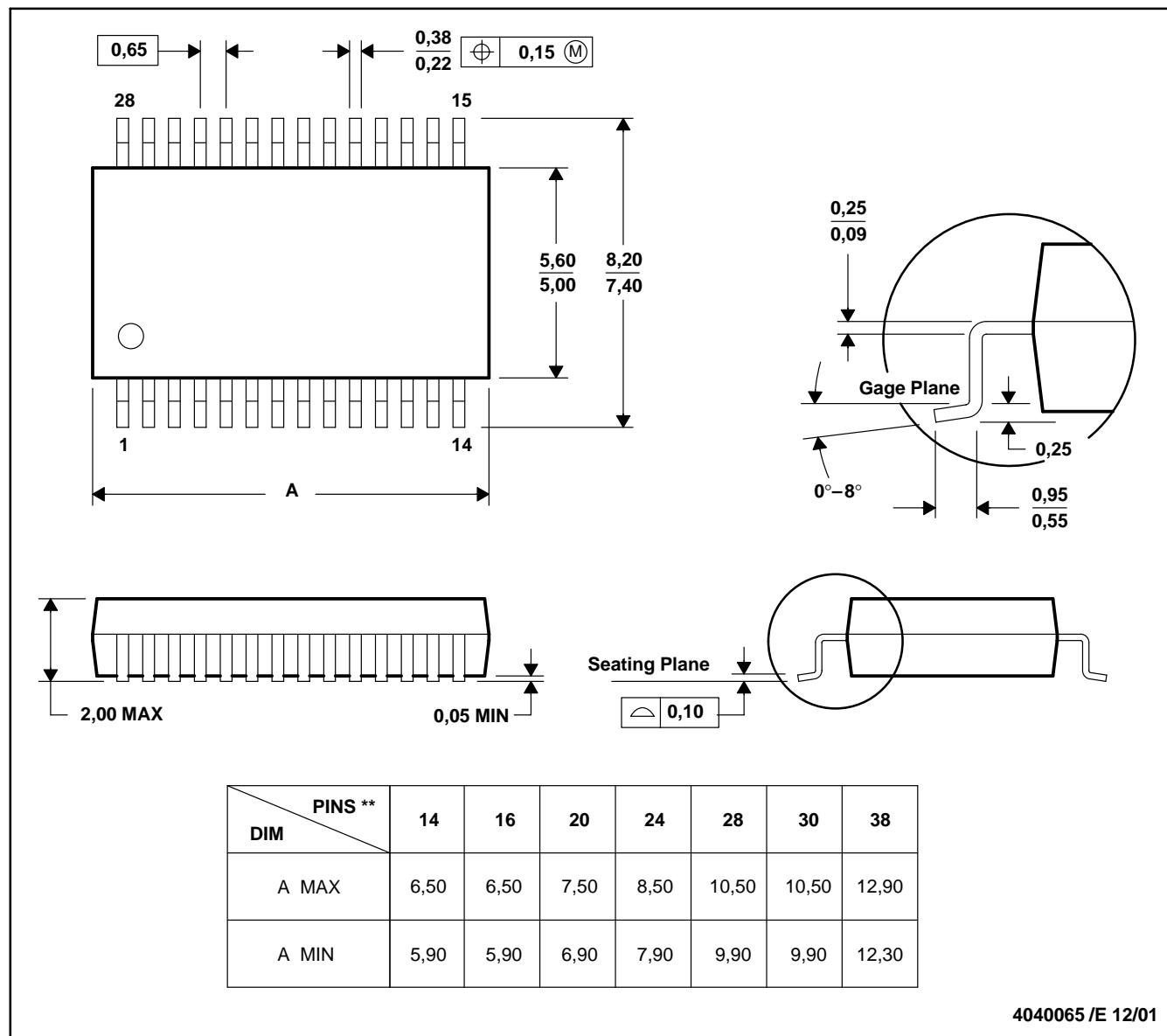
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC20DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74HC20DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HC20NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HC20PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

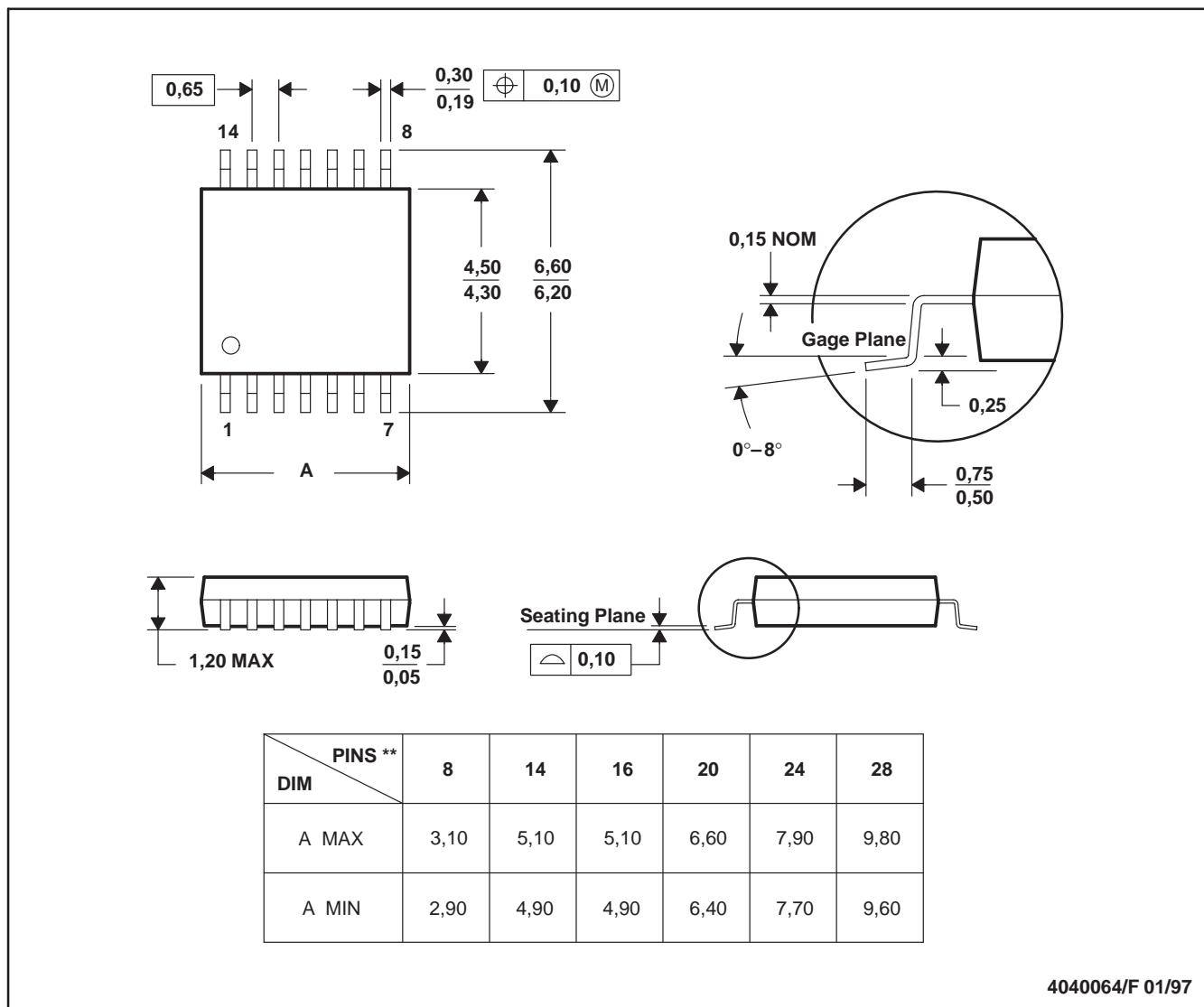


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G^{**})

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



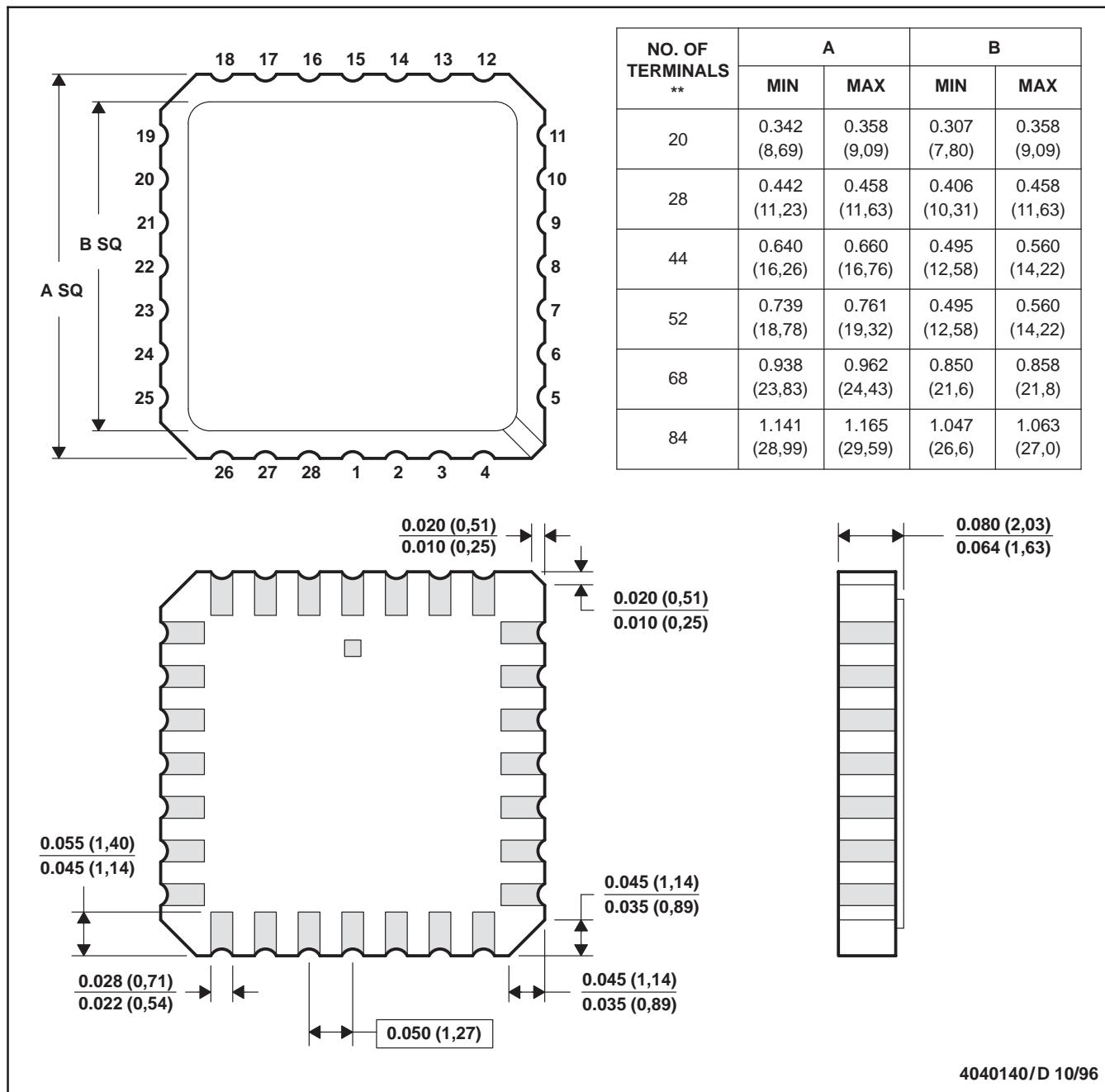
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



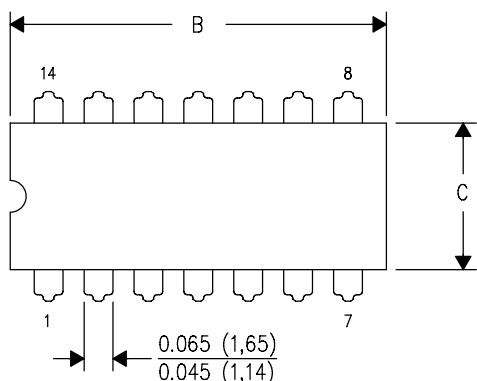
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

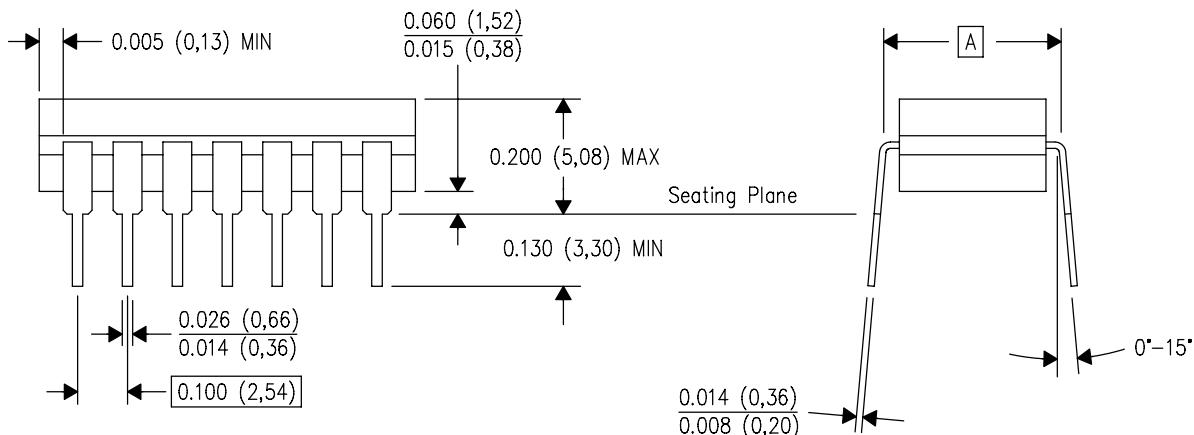
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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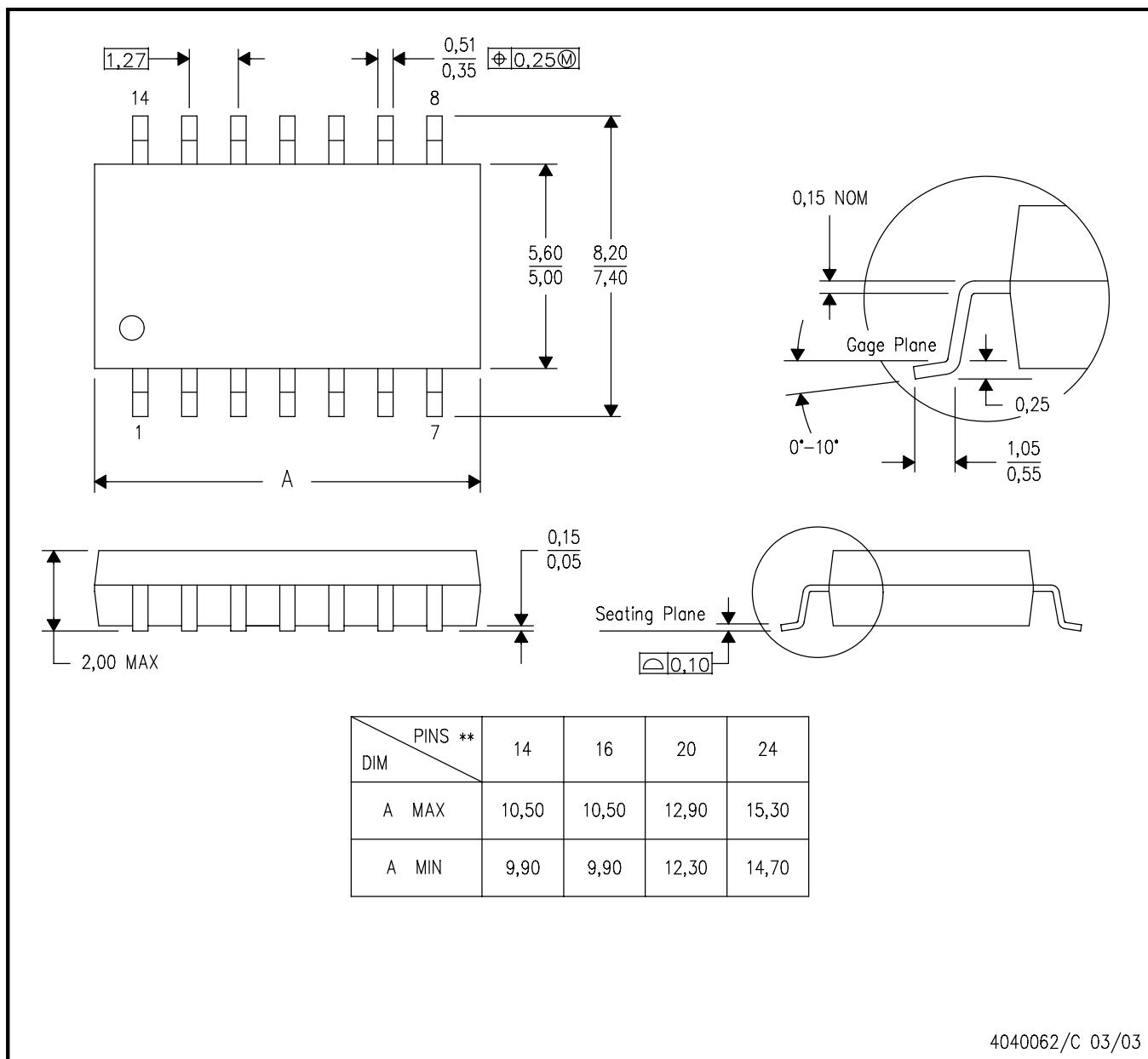
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

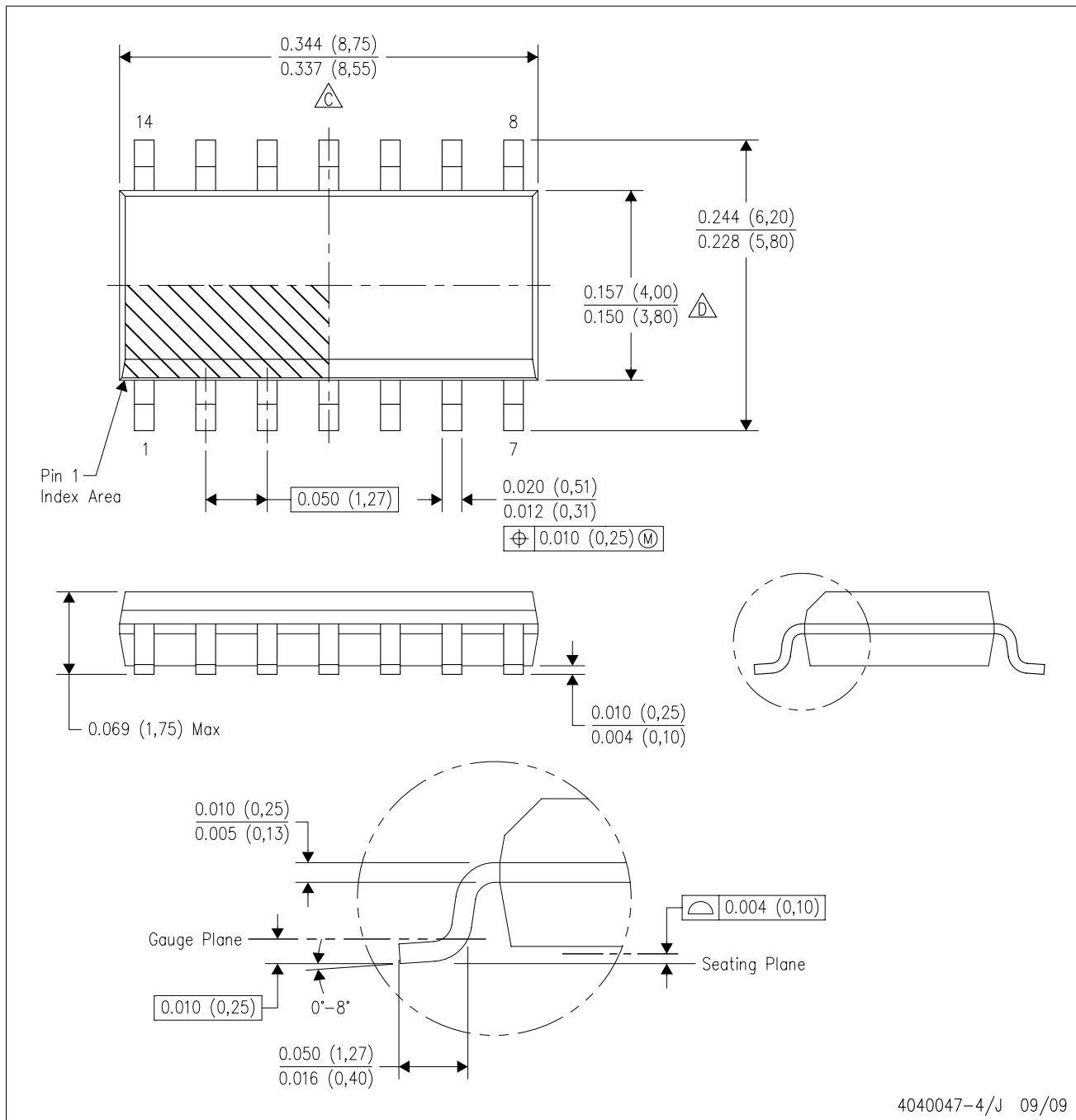


4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

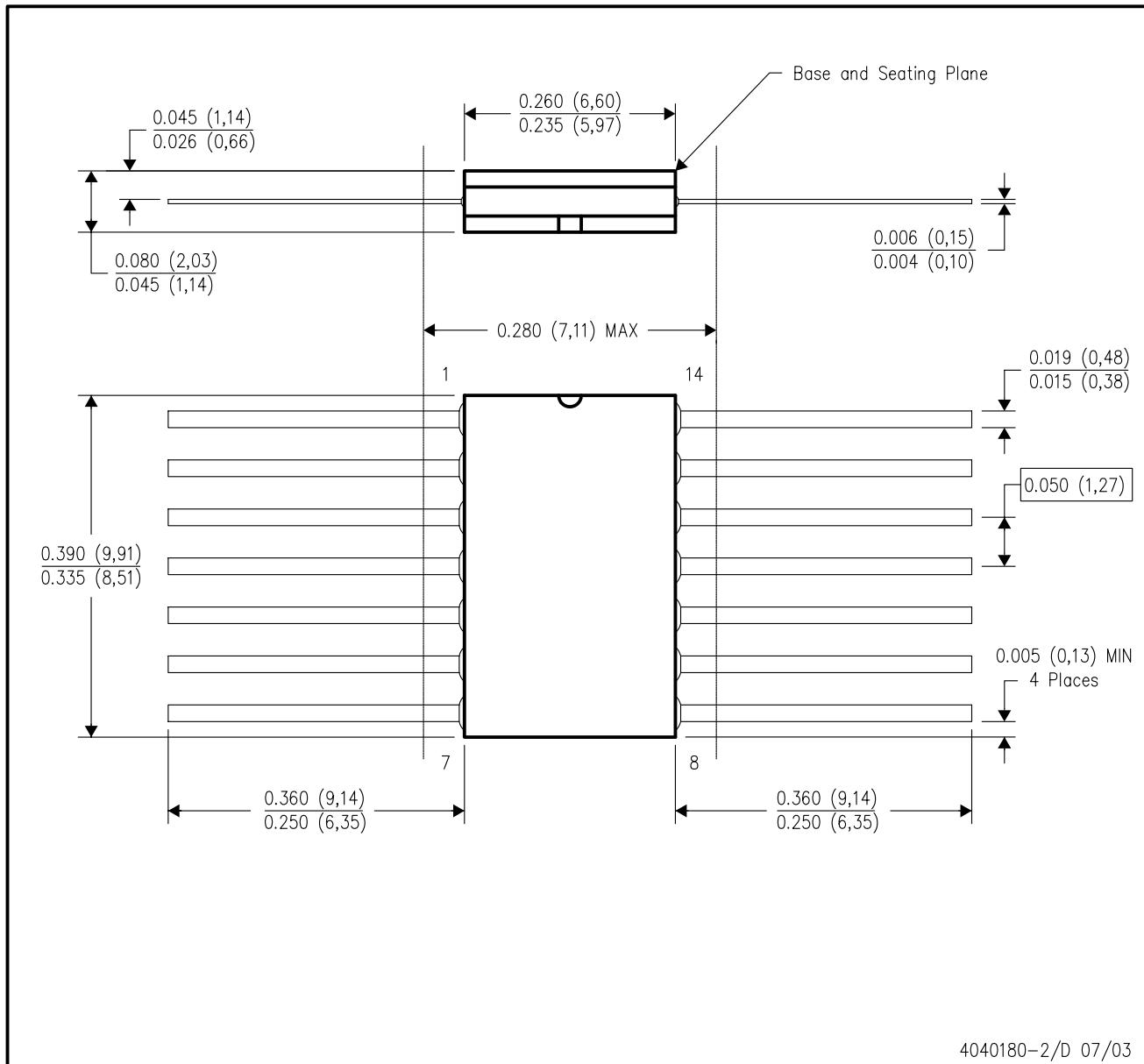
D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

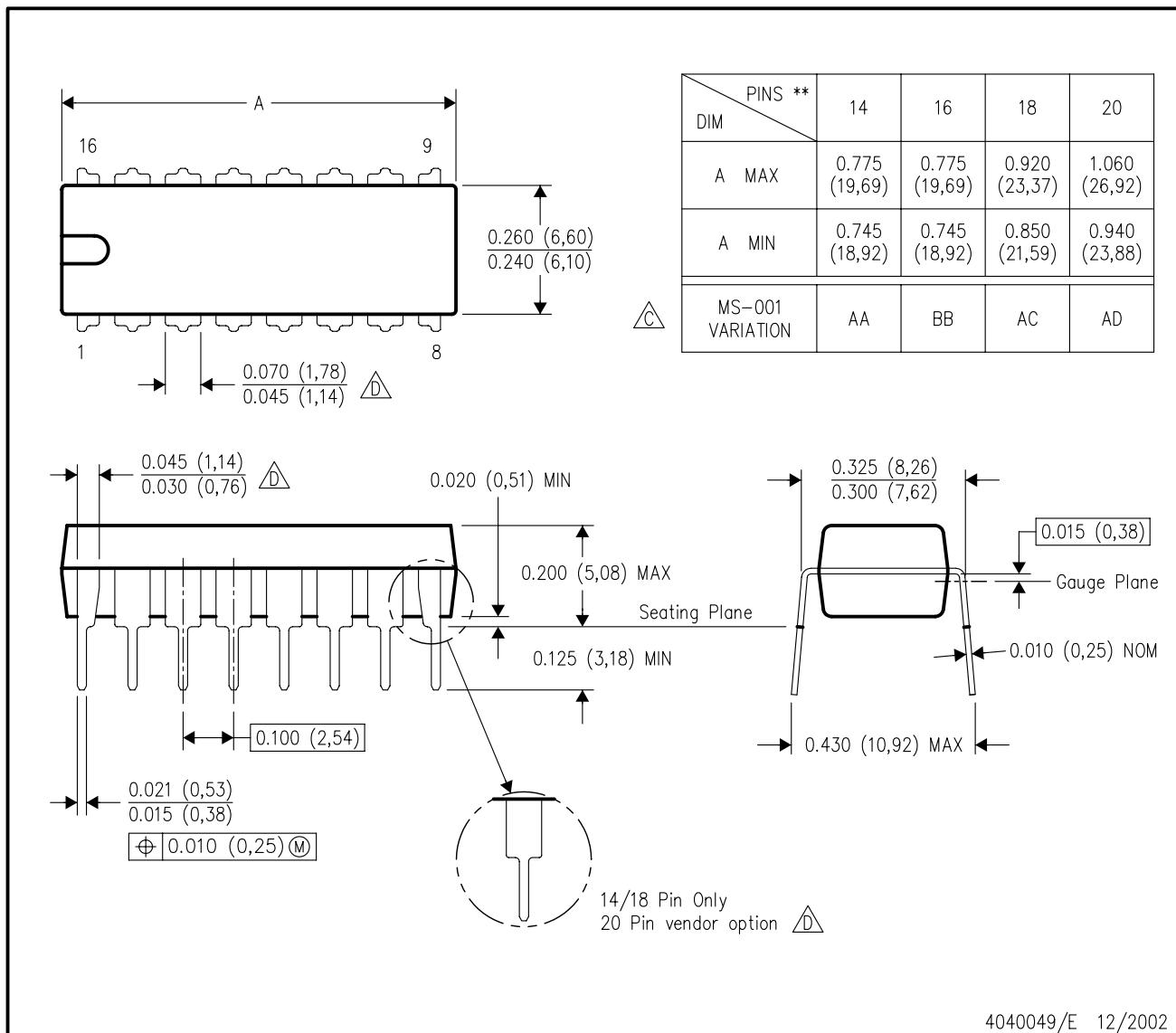
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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