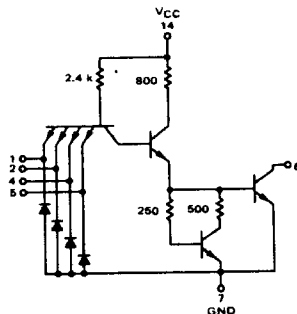


MTTL III MC3100/3000 series

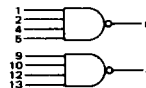
DUAL 4-INPUT "NAND" GATE
(Open Collector)

MC3112F • MC3012F
MC3112L • MC3012L,P
(54H22J) (74H22J,N)

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates with no output pull-up circuits. It can be used where the Wired-OR function is required or for driving discrete components.

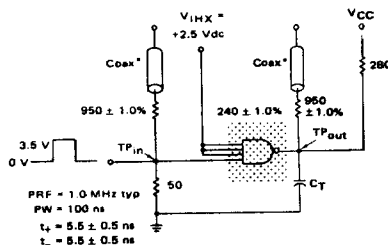


Positive Logic: $6 = 1 \cdot 2 \cdot 3 \cdot 4 \cdot 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

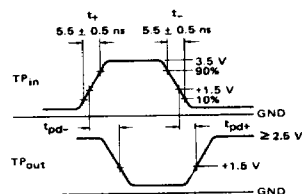
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS

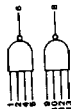


See General Information section for packaging.

MC3112F, MC3012F/MC3112L, MC3012L,P (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further test procedures are shown for only one output of the gate under test. To complete testing, sequence through remaining inputs.



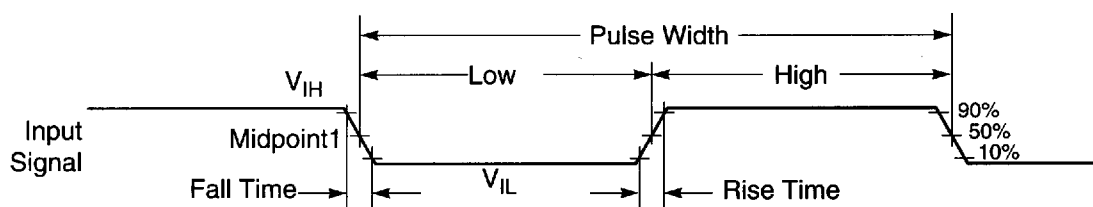
aining inputs.

Characteristic		MC3012 Test Limits												TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW												Gnd							
		-55°C						+25°C						+75°C						V _{pin}													
		Min		Max		Min		Max		Min		Max		Min		Max		I _{on}	I _{off}	V _{ih}	V _{il}	V _{oh}	V _{ol}	V _{cc1}	V _{cc2}		V _{cc3}	V _{cc4}	V _{cc5}	V _{cc6}			
Input	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	20	20	2.0	0.4	2.4	0.4	2.0	4.5	5.5	5.5	5.5	5.5	1*			
Forward Current	I _F	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-	-	-	-	-	-	-	-	-	-	-	1*			
Leakage Current	I _L	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	-	-	-	-	-	-	-	-	-	-	-	1*			
Breakdown Voltage	B _{Vin}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1*			
Clamp Voltage	V _D	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1*			
Output	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	20	20	2.0	0.4	2.4	0.4	2.0	4.5	5.5	5.5	5.5	5.5	5.5	1*		
Output Voltage	V _{OL}	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		
Output Leakage	I _{CEX}	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		
Power Requirements	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	20	20	2.0	0.4	2.4	0.4	2.0	4.5	5.5	5.5	5.5	5.5	5.5	1*		
(Total Device)	I _{max}	-	12.5	-	12.5	-	12.5	-	12.5	-	12.5	-	12.5	-	12.5	-	12.5	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		
Supply Current	I _{DD}	-	18	-	18	-	18	-	18	-	18	-	18	-	18	-	18	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		
Power Supply Drain	I _{DDL}	-	0.0	-	0.0	-	0.0	-	0.0	-	0.0	-	0.0	-	0.0	-	0.0	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		
Switching	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	20	20	2.0	0.4	2.4	0.4	2.0	4.5	5.5	5.5	5.5	5.5	5.5	1*		
Turn-On Delay	t _{pd}	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		
Turn-Off Delay	t _{pd}	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	-	-	-	-	-	-	-	-	-	-	-	-	1*		

* Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference