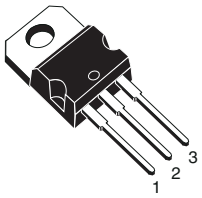
STP60NS04ZB

N-channel clamped - 10mΩ - 60A - TO-220
Fully protected Mesh Overlay™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP60NS04ZB	Clamped	< 0.015Ω	60A

- 100% avalanche tested
- Low capacitance and gate charge
- 175 °C maximum junction temperature

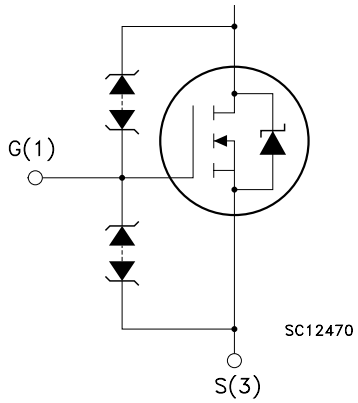


TO-220

Description

This fully clamped Power MOSFET is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP60NS04ZB	P60NS04ZB	TO-220	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	Clamped	V
V_{GS}	Gate- source voltage	Clamped	V
I_D	Drain current (continuous) at T_C = 25°C	60	A
I_D	Drain current (continuous) at T_C = 100°C	42	A
I_{DG}	Drain gate current (continuous)	±50	mA
I_{GS}	Gate source current (continuous)	±50	mA
I_{DM}(1)	Drain current (pulsed)	240	A
P_{tot}	Total dissipation at T_C = 25°C	150	W
	Derating factor	1	W/°C
$V_{ESD(G-S)}$	Gate-source ESD (HBM - C = 100pF, R=1.5 kΩ)	6	KV
$V_{ESD(G-D)}$	Gate-drain ESD (HBM - C = 100pF, R=1.5 kΩ)	4	KV
$V_{ESD(D-S)}$	Drain-source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	KV
T_{stg}	Storage temperature	-65 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	60	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 30 V)	400	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} =0 -40 < T_j < 175°C	33			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 16V; T_J =150°C V_{DS} = 16V; T_J =175°C			50 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±10V;T_j =175°C V_{GS} = ±16V;T_j =175°C			50 150	µA µA
V_{GSS}	Gate-source breakdown voltage	I_{GS} = 100µA	18			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1mA -40 < T_J < 150°C	1.7	3	4.2	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 30A V_{GS} = 16V, I_D = 30A		11 10	15 14	mΩ mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}= 15V, I_D=30A	20	40		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		1700 800 190	2100 1000 240	pF pF pF
$t_{r(Voff)}$ t_f t_c	Turn-on delay time Fall time Cross-over time	V_{clamp} = 30V, I_D = 60A R_G = 4.7Ω V_{GS} = 10V (see *Figure 14*)		60 45 100	75 60 130	ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 18V, I_D = 60A, V_{GS} = 10V, R_G = 4.7Ω (see *Figure 15*)		48 13 16	42	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				60 240	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 60A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 60A, di/dt = 100A/µs, V_{DD} = 15V, T_j = 150°C (see *Figure 16*)		50 62 2.6		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

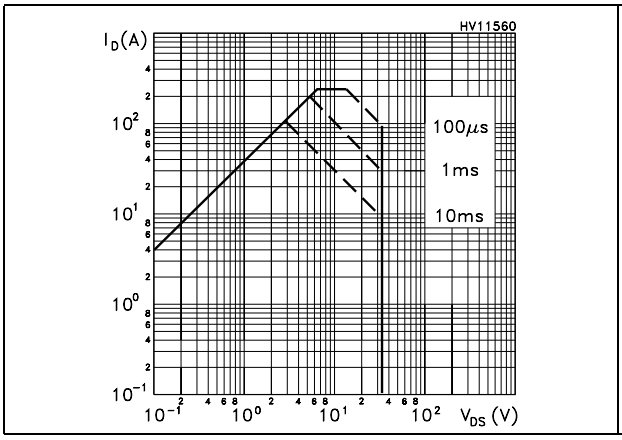


Figure 2. Thermal impedance

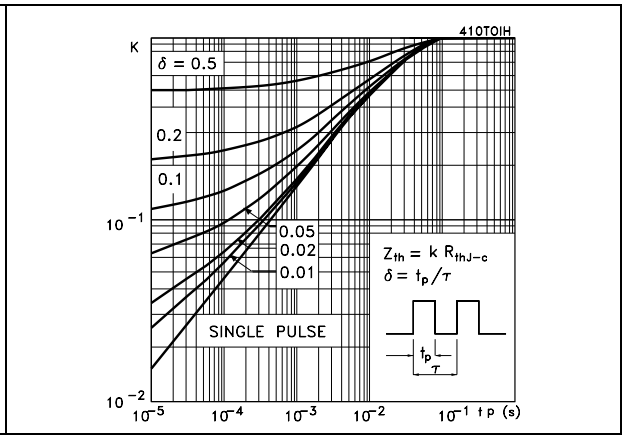


Figure 3. Output characterisics

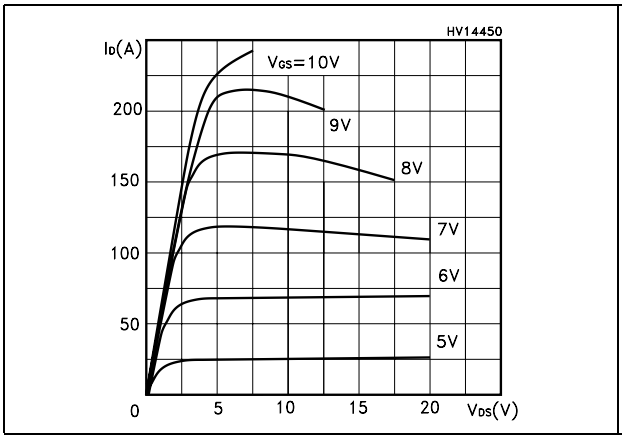


Figure 4. Transfer characteristics

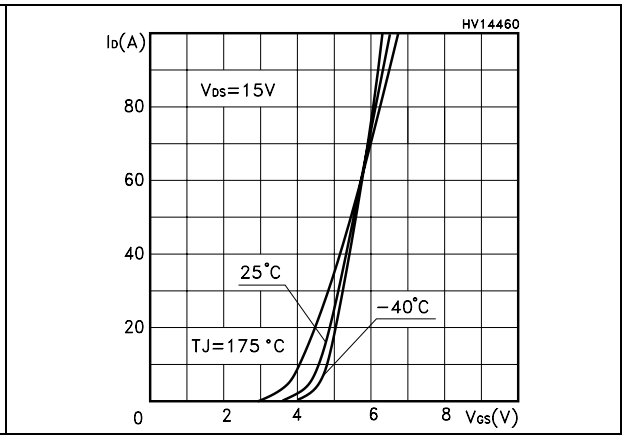


Figure 5. Transconductance

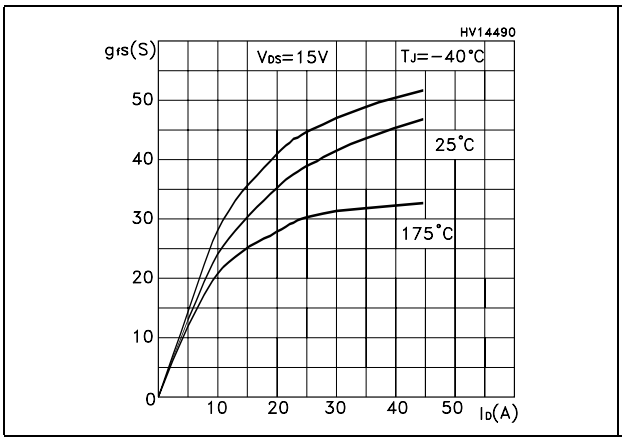


Figure 6. Static drain-source on resistance

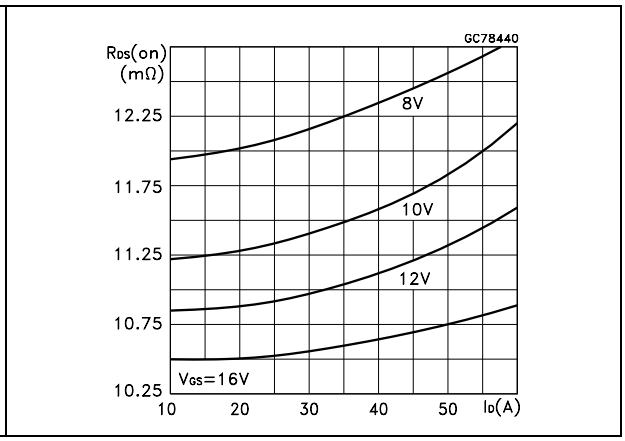


Figure 7. Gate charge vs gate-source voltage

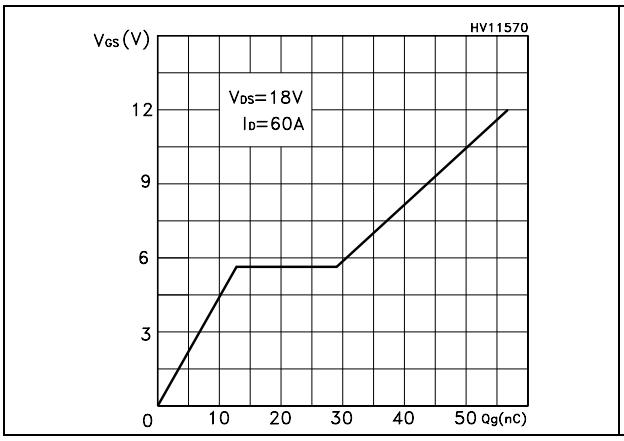


Figure 8. Capacitance variations

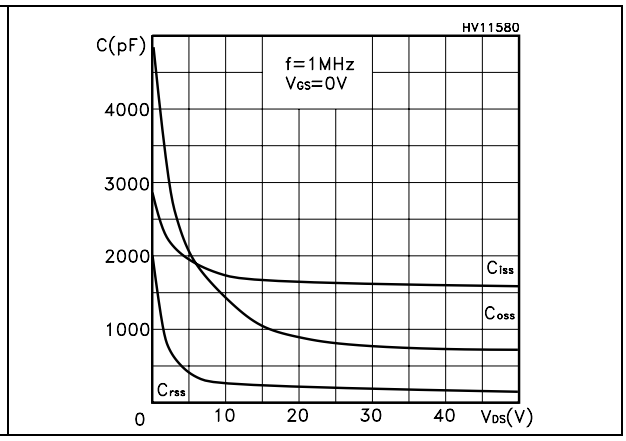


Figure 9. Normalized gate threshold voltage vs temperature

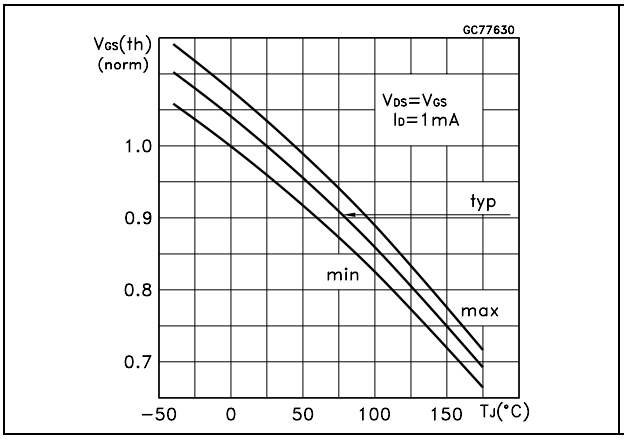


Figure 10. Normalized on resistance vs temperature

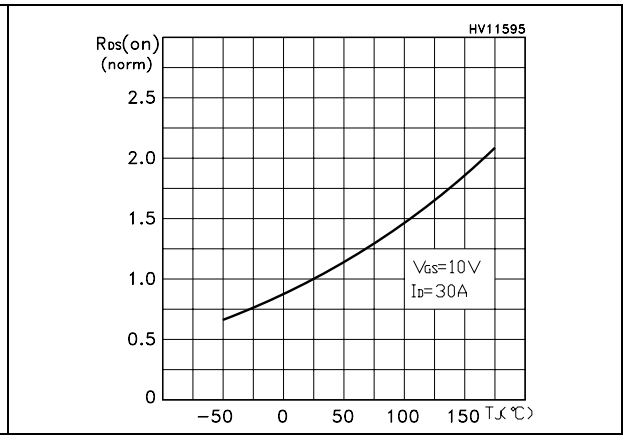


Figure 11. Source-drain diode forward characteristics

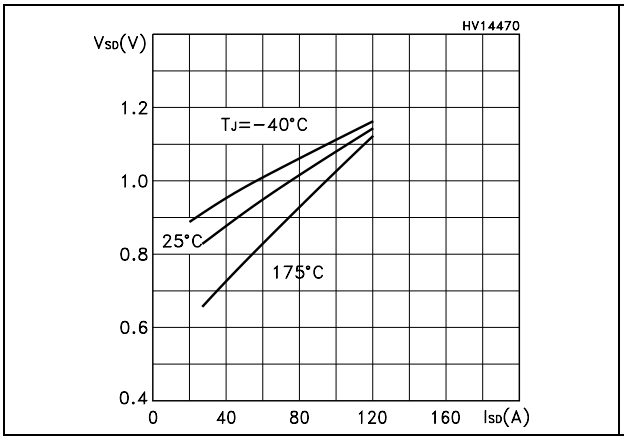


Figure 12. Zero gate voltage drain current vs temperature

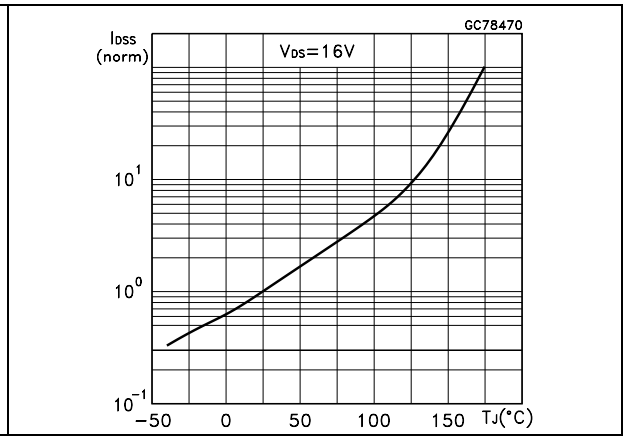
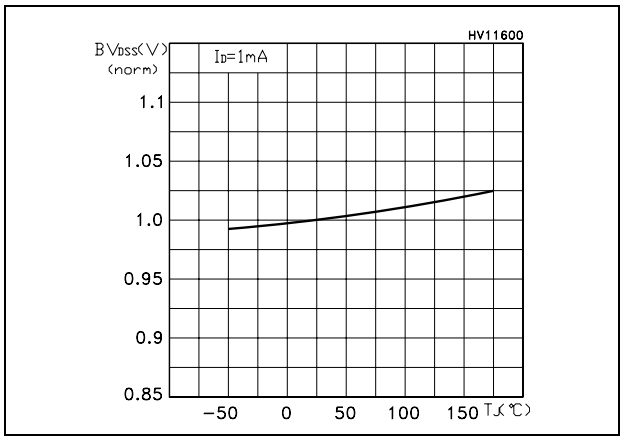


Figure 13. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

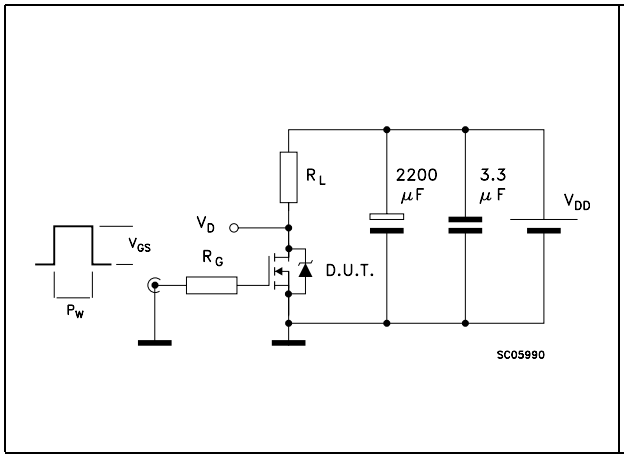


Figure 15. Gate charge test circuit

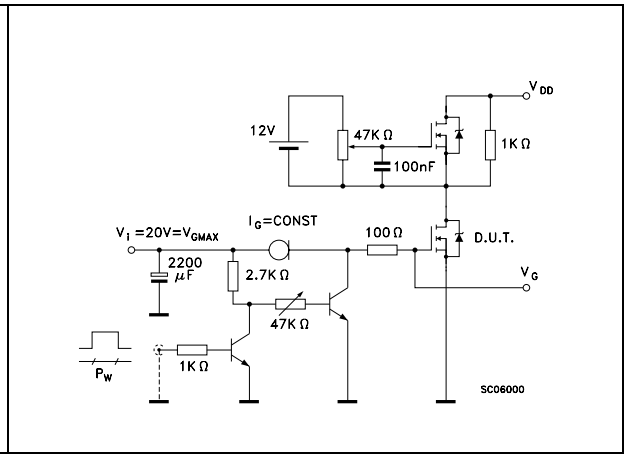


Figure 16. Test circuit for inductive load switching and diode recovery times

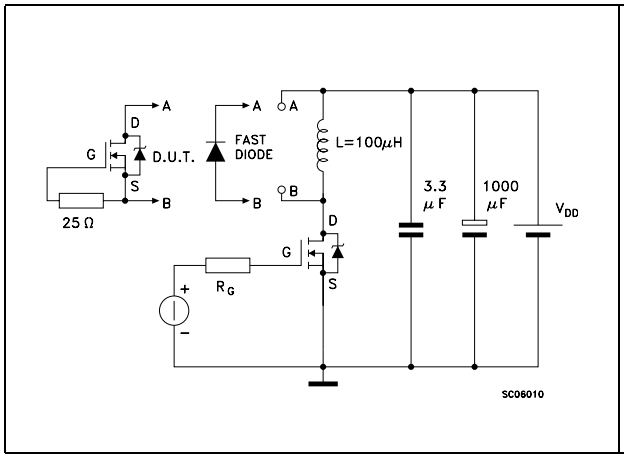


Figure 17. Unclamped Inductive load test circuit

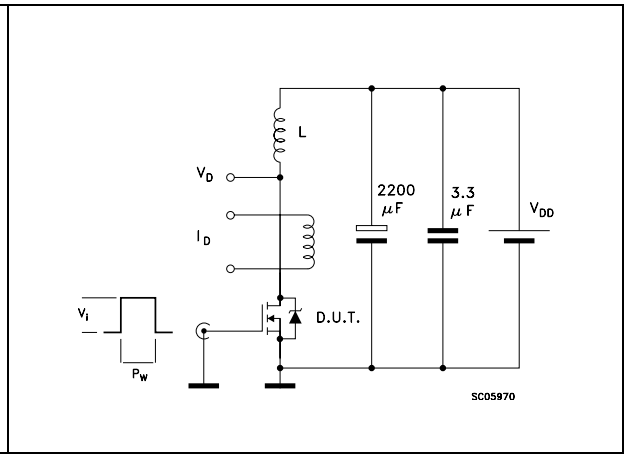


Figure 18. Unclamped inductive waveform

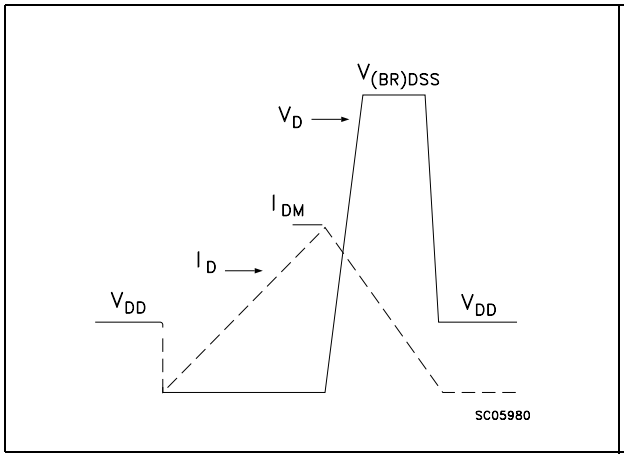
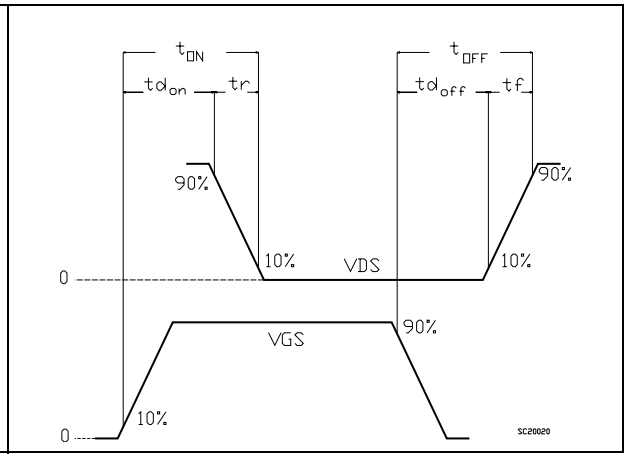


Figure 19. Switching time waveform

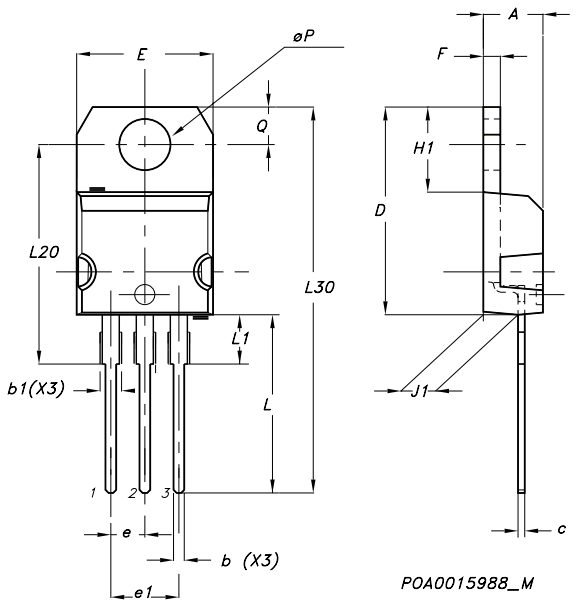


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	1	Complete document
04-Oct-2006	2	New template, no content change

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