AN5308NK

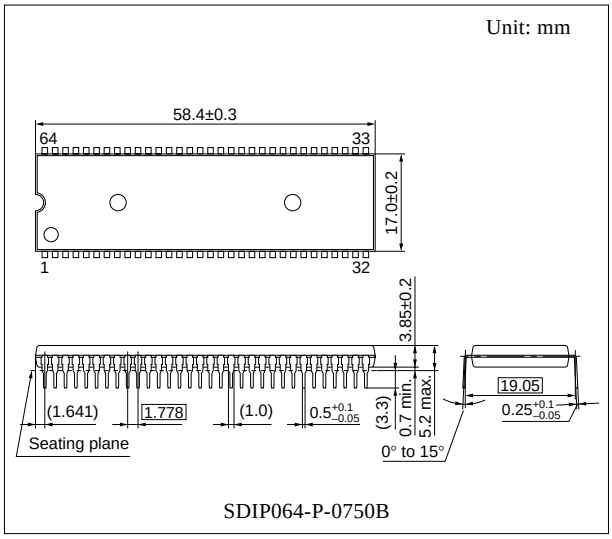
Single chip IC for color TV (Built-in I²C bus interface)

■ Overview

The AN5308NK is an IC in which NTSC video, chroma, RGB, sync. and deflection signal processing circuits are integrated on a single chip incorporating I²C bus controller.

■ Features

- Video block : Built-in wide band width filter, pre-shoot and over-shoot amount adjustment, aperture changeover possible and with ABL pin
- Chroma block : Built-in ACC filter and with color difference output pin
- RGB block : With color difference signal input pin and analog RGB
- Sync. block : With sync. BLK in/output pin, µ changeover and H center adjustment possible
- Deflection block: Built-in screen distortion correction circuit

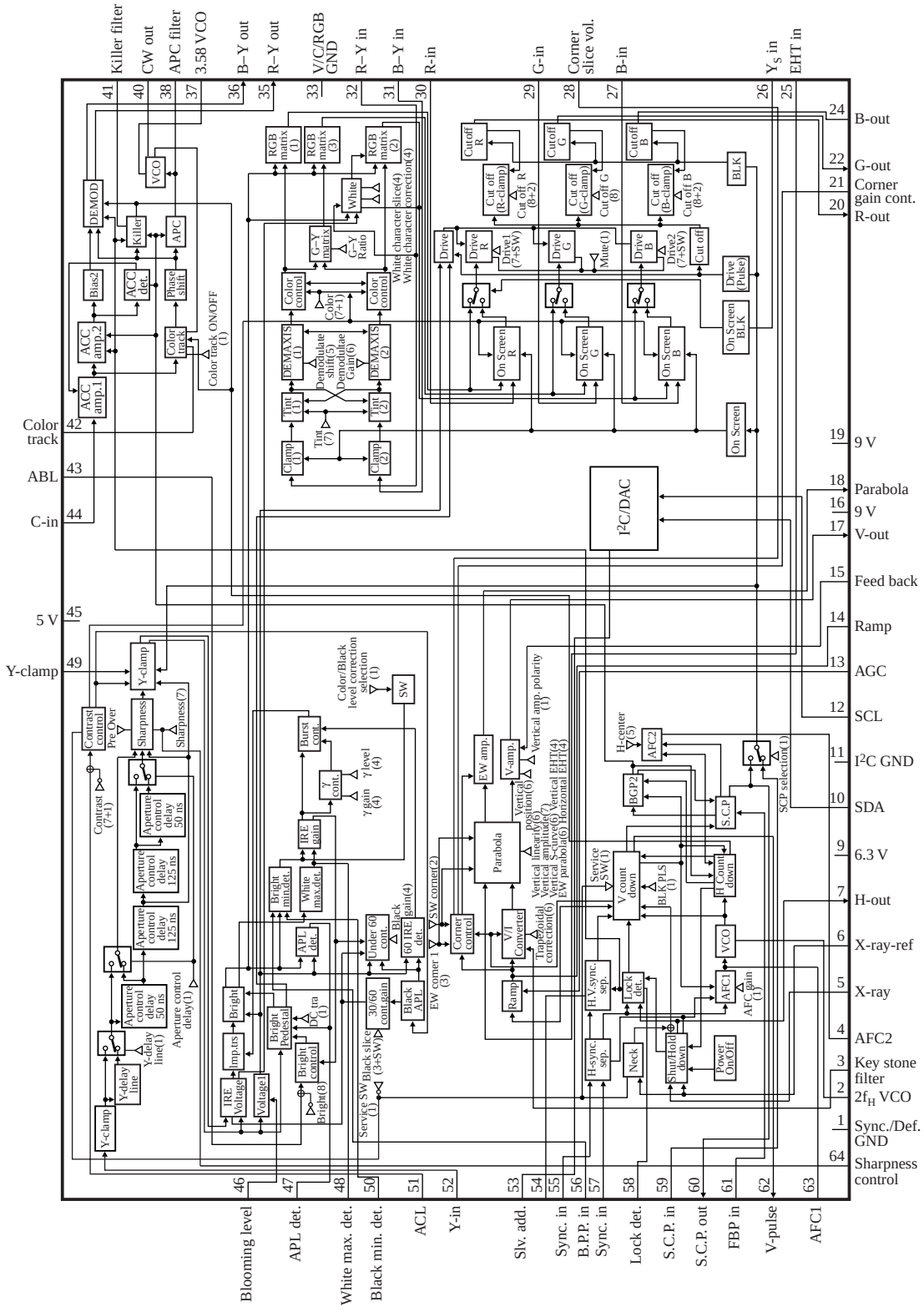


SDIP064-P-0750B

■ Applications

- TV

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Sync., Def. GND	35	R−Y output
2	503 kHz VCO	36	B−Y output
3	Vertical position transition DAC output	37	3.58 MHz VCO
4	AFC2 filter	38	Chroma APC filter
5	High-tention detection input (X-ray)	40	VCO output
6	High-tention detection reference voltage	41	Killer filter
7	Horizontal drive pulse output	42	Color track filter
9	Horizontal power supply (H V_{CC})	43	ABL input
10	I^2C SDA input	44	Chroma input
11	I^2C GND	45	5 V power supply (V_{CC2})
12	I^2C SCL input	46	Blooming level input
13	Reference ramp wave form AGC	47	APL detection use filter
14	Reference ramp wave form generation	48	White detection use filter
15	Corner slice level	49	Y-clamp
16	Sync. 9 V power supply	50	Black detection filter/color control
17	Vertical deflection sawtooth wave output	51	ACL input
18	EW output	52	Y-signal input
19	9 V power supply (V_{CC1})	53	Slave address changeover
20	R-output	54	V-sync. sep. filter
21	Corner gain control	55	H-sync. input
22	G-output	56	Black detection inhibition pulse input
24	B-output	57	V-sync. input
25	EHT voltage detection	58	Lock det. filter
26	Y_S input	59	Sandcastle pulse input
27	On-screen B-input	60	Sandcastle pulse output
28	Corner slice volume	61	Flyback pulse (FBP) input
29	On-screen G-input	62	V-pulse output
30	On-screen R-input	63	AFC1 filter
31	B−Y input	64	Sharpness control output
32	R−Y input	8, 23, 34, 39	Non-connection
33	V/C/RGB GND		

■ Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage	V_{CC}	V_{CC1}	9.6	V
		V_{CC2}	5.6	
Supply current	I_{CC}	I_{CC1} (I_{16}+I_{19})	113	mA
		I_{CC2} (I_{45})	89	
		I_9	26	
Power dissipation (T_a = 70°C)	P_D		947	mW
Operating ambient temperature *1	T_{opr}		–20 to +70	°C
Storage temperature *1	T_{stg}		–55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1} $V_{19–1, 11, 33}$	8.5 to 9.0 to 9.5	V
	V_{CC2} $V_{45–1, 11, 33}$	4.5 to 5.0 to 5.5	V
Supply current	I_9	15 to 20 to 25	mA

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics						
Supply current	I_{16+19}	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	74	90	106	mA
Supply current	I_{45}	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	59	71	83	mA
Sync. input pin voltage	$V_{55–1}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	0.8	1.3	1.8	V
Sync. input pin voltage	$V_{57–1}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	0.8	1.3	1.8	V
Video input pin voltage	$V_{7–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	2.7	3.2	3.7	V
ABL input pin voltage	$V_{43–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	2.5	3.0	3.5	V
ACL input pin voltage	$V_{51–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	2.5	3.0	3.5	V
Blooming level pin voltage	$V_{46–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	2.2	2.7	3.2	V
Chroma input pin voltage	$V_{44–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	1.5	2.0	2.5	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics (continued)						
B–Y output pin voltage	$V_{31–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	2.3	2.8	3.3	V
R–Y output pin voltage	$V_{32–33}$	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	2.3	2.8	3.3	V
Horizontal signal processing						
Horizontal stabilized supply voltage	HV_{CC}	V_{CC1}: 9 V, V_{CC2}: 5 V, pin 9: 12 V with 380 Ω	5.9	6.3	6.7	V
Constant voltage operating resistance	RHV_{CC}	I_9: 15 mA to 25 mA	—	—	30	Ω
Horizontal free-running oscillation frequency 1	f_{HO-1}		15.434	15.734	16.034	kHz
Horizontal free-running oscillation frequency 2	$f_{HO–2}$	At hold down	16.3	16.4	16.8	kHz
Variation of f_{HO}, when supply voltage start-up	$\frac{\Delta f_{HO}}{V_{CC3}}$	f_{HO} frequency difference, when other power supply off→on	0	100	200	Hz
Horizontal output pulse duty cycle	τH_O	Hold down off	34.4	37.5	40.6	%
Horizontal output starting voltage	$V_{fH(S)}$	f = 10 kHz to 20 kHz, when horizontal oscillation voltage is 1 V[p-p] or more	—	—	5.2	V
Horizontal output level	V_{fH}		2.4	2.9	3.4	V
Horizontal pull-in range	f_{PH}	f_{HO} = 15.73 kHz	±400	—	—	Hz
H-center changeable range 1	T_{DH}	Phase lead of 1A[10]→[00]	1.8	2.5	3.2	µs
H-center changeable range 2	T_{DH}	Phase lead of 1A[10]→[1F]	–3.0	–2.3	–1.6	µs
Lock detector output voltage 1	$V_{58–M}$	Synchronous	5.1	5.8	6.5	V
Lock detector output voltage 2	$V_{58–L}$	Asynchronous	– 0.1	0	0.5	V
Lock detector output voltage 3	$V_{58–T}$	Hold down	7.6	8.3	9.0	V
Burst gate pulse width	T_{BGP}	Sandcastle output	1.8	2.5	3.2	µs
Sandcastle pulse output level (BGP)	V_{BGP}	V_{CC}: typ.	4.0	4.3	4.6	V
Sandcastle pulse output level (HBLK)	V_{HBLK}	V_{CC}: typ.	2.7	3	3.3	V
Sandcastle pulse output level (VBLK)	V_{VBLK}	V_{CC}: typ.	1.2	1.5	1.8	V
Vertical signal processing						
Vertical output pulth width	τV_O		360	380	400	µs
Vertical output level	V_{62H}		3.8	4.3	4.8	V
Vertical output free-running frequency	f_{VO}		58.8	60.0	61.2	Hz
Vertical blanking pulse width	τ_{VBLK}		1.09	1.12	1.15	ms

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-signal processing (continued)						
Video voltage gain	AY_G	Cont.: max., Sharp.: min.	17	20	23	dB
Video voltage gain relative ratio	AY	Ratio between channels, Drive: typ.	−2.5	0	2.5	dB
Video voltage gain relative ratio DL	AY_{GD1}	Y delay line on/off	−1.5	0	1.5	dB
Sharpness 1	AG_{SH1}	f = 4 MHz, Aperture control SW: 00	11.5	14.5	17.5	dB
Sharpness 2	AG_{SH2}	f = 3 MHz, Aperture control SW: 02	11.5	14.5	17.5	dB
Contrast control range max. value	AG_{CON}	Sharp.: min., Cont.: typ.	3.5	6.0	8.5	dB
Contrast control range min. value	yG_{CONmin}	Contrast: min.	—	30	100	mV
Brightness changeable amount	V_{BR}	No input, Bright: min.→max.	3.0	3.7	4.4	V
DC re-generation factor 1	TDC1	APL10%→90% DC transmission amount changeover: − direction	90	96	102	%
DC re-generation factor 2	TDC2	APL10%→90% DC transmission amount changeover: + direction	96	103	110	%
Y-signal delay time 1	τ_{DL1}	Y delay line: On	260	325	390	ns
Y-signal delay time 2	τ_{DL2}	Y delay line: Off	160	205	250	ns
Y-frequency characteristics 1	Δy_{1Y}	10 MHz attenuation amount DL: On for f = 3 MHz	−6	−3	1	dB
Y-frequency characteristics 2	Δy_{2Y}	10 MHz attenuation amount DL: Off for f = 3 MHz	−5	−2	2	dB
ACL characteristics	Δy_{ACL}	Pin 51: 3 V→3.5 V	8	11	14	dB/V
ABL characteristics	Δy_{ABL}	Pin 43: 2.7 V→3.5 V	2.7	3.4	4.1	V/V
Black extension amount 1	ΔYBL1	Input: Whole black, pin 50: 5 V→ CR filter	− 0.1	0	0.1	V
Black extension gain	ΔYBL2	Input: Whole black, pin 50: 3 V black gain: min.→max.	1.60	1.95	2.3	V
Black extension start point	ΔYBL3	Pin 50: 5 V, set contrast to 2.7 V[p-p], after that with pin 50 CR filter	− 0.12	0	0.12	V
Black extension amount 2	ΔYBL4	Black level: min., set contrast to 0.8 V[p-p], after that with pin 50 CR filter	0.08	0.18	0.28	V
γ correction amount min. to max.	Y_γ	White γ gain: max., white γ gain: min. to max.	0.50	0.85	1.20	V
Blooming level variation amount	ΔYBLM	Blooming DC pin 46: 0.5 V→4.5 V	3.2	3.9	4.6	V
Pedestal level (typical)	Y_G	Cut off: 80	2.0	2.4	2.8	V
Chroma signal processing						
ACC characteristics 1	ACC1	Color bar signal (Burst 300 mV[p-p])	−1	0	1	dB
ACC characteristics 2	ACC2	Color bar signal (Burst 15 mV[p-p])	−4	−1.5	1	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chroma signal processing (continued)						
Killer tolerance on	eK	Color bar burst 0 dB = 150 mV[p-p]	–48	–43	–38	dB
Killer tolerance off	eK	Color bar signal hysteresis	—	2	4	dB
Detection output amplitude B-Y	e_{OB}	Color bar signal (Burst 150 mV[p-p])	1.04	1.57	2.1	V[p-p]
Detection output amplitude R-Y	e_{OR}	Color bar signal (Burst 150 mV[p-p])	0.82	1.26	1.7	V[p-p]
De-modulated output ratio	R/B	Rainbow signal R–Y/B–Y output ratio	0.48	0.56	0.64	Time
De-modutation angle (B–Y)	∠B		–8.0	–2.5	3.0	degree
De-modutation angle (R–Y)	∠R		83	88	93	degree
Color residual	e_{KILLER}	Killer filter pin, grounded with 20 kΩ	—	—	50	mV[p-p]
Detection output residual carrier	e_{CAR}	No-signal input	—	—	50	mV[p-p]
APC pull-in range low	f_{PULL}	Burst frequency change	500	600	—	Hz
APC pull-in range high	f_{PULL}	Burst frequency change	–500	–600	—	Hz
CW output amplitude	e_{CW}		600	800	1 100	mV[p-p]
Free running frequency	f_{CO}	Deviation from 3.579545 MHz	–200	0	200	Hz
RGB processing circuit						
Tint center *1	θ_T	Pin 31: 356 mV[p-p], pin 32: 200 mV[p-p], DAC value, when R, B output are equal	[2F]	[3A]	[4A]	—
Tint variable range max. *1	$\Delta\theta_1$	Tint: typ.→max.	40	65	—	degree
Tint variable range min. *1	$\Delta\theta_2$	Tint: typ.→min.	–37	–50	—	degree
R–Y demodulation axis variable range max. *1	$\Delta\theta_{DEM}$	Demodulation axis: min.→max.	16	28	39	degree
B–Y ratio variable range 1 *1	$AB–Y_{min}$	Demodulation ratio: typ.→min.	—	0	0.25	Time
B–Y ratio variable range 2 *1	$AB–Y_{min}$	Demodulation ratio: typ.→min.	1.25	1.50	1.75	Time
R–Y/B–Y ratio *1	eR/eB	Pin 31: 356 mV[p-p], pin 32: 200 mV[p-p]	0.65	0.79	0.94	Time
G–Y/R–Y ratio 1 *1	eG/eR_1	G–Y ratio changeover: type2	0.47	0.57	0.67	Time
G–Y/R–Y ratio 2 *1	eG/eR_2	G–Y ratio changeover: type1	0.27	0.35	0.44	Time
G–Y/B–Y ratio 1 *1	eG/eB_1	G–Y ratio changeover: type2	0.18	0.27	0.36	Time
G–Y/B–Y ratio 2 *1	eG/eB_2	G–Y ratio changeover: type1	0.30	0.36	0.42	Time
RGB output blanking voltage	E_{BLK}	Brightness: typ., cutoff	0.7	1.1	1.5	V
Color control range max. *1	$A_{B–YCLmax}$	Cont.: typ., Color: typ.→max.	3.4	5.0	6.6	dB
Color control min. value *1	$A_{B–YCLmin}$	Cont.: typ., Color: typ.→min.	—	25	50	mV
Color difference signal contrast variable range *1	$A_{B(CON)}$	Color: typ., Cont.: typ.→max.	3.5	6.0	8.5	dB

Note) *1: Under the condition that pin 52 is adjusted for the Drive I, II by inserting Y-signal, and R and B-output amplitude equal that of G-output.

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RGB processing circuit (continued)						
Drive control range	$A_{R(DR)}$	Drive SW: 00→04, drive: min.→max.	4	6	8	dB
Cut-off R.B control range	V_{CO}	Cutoff SW, cutoff: min.→max.	1.6	2.1	2.6	V
Cut-off G control range	$V_{(CO)G}$	Cutoff: min. to max.	0.6	1.1	1.6	V
On-screen voltage gain	A_{yG}	Y_S = 1 V, contrast: max.	8	10	12	dB
On-screen contrast range	$A_{yG(ON)}$	Y_S = 1 V typ.→max.	0	1.5	3.5	dB
On-screen contrast min. value	$A_{yG(ON)min}$	0.5 V input	0.1	0.3	0.5	V[p-p]
On-screen frequency characteristics	Δe	Attenuation amount of f = 10 MHz to f = 3 MHz	–6	–3	1	dB
Deflection signal processing						
Standard vertical output amplitude	V_{OUT}		2.2	2.6	3.0	V[p-p]
Standard EW output amplitude	V_{EW}		1.8	2.2	2.6	V[p-p]
Color track						
Color track off/on variation amount 1 Blue *1	Δe_{BB}	B–Y: 1.39 V, R–Y: 1.1 V After tint color adjustment	–160	0	160	mV
Color track off/on variation amount 2 Red *1	Δe_{BR}	Variation amount at color track On, 0E : 03→04	–100	100	300	mV
Color track off/on variation amount 3 Yellow *1	Δe_{RY}		–350	–200	–16	mV
C/Y ratio	$V_{C/Y}$	Y: 0.36 V_{B-W}, C: Color bar typ., Color: typ., contrast: typ. G–Y/Y zero peak ratio at G-output	0.285	0.42	0.56	Time

Note) ∗1: Under the condition that pin 52 is adjusted for the Drive I, II by inserting Y-signal, and R and B-output amplitude equal that of G-output.

- Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal signal processing						
Sync. separation possible input	V_{IN}	Input: Whole black sync. level	0.2	1.0	—	V[p-p]
Ambient temperature dependence of f_{HO}	$\frac{Df_{HO}}{T_a}$	T_a = –20°C to +70°C	—	5.5	—	Hz/°C
Horizontal oscillation frequency control sensitivity	β_H		—	1.2	—	Hz/mV
AFC1 reference current 1	$I_{63(1)}$	0D[30]	—	0.83	—	mA
AFC1 reference current 2	$I_{63(2)}$	0D[20]	—	1.33	—	mA
AFC1 reference current 3	$I_{63(3)}$	0D[10]	—	1.83	—	mA
AFC1 reference current 4	$I_{63(4)}$	0D[00]	—	2.33	—	mA

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal signal processing (continued)						
F.B.P slice level (blanking)	V_{FBP-1}		—	0.7	—	V
F.B.P slice level (AFC1)	V_{FBP-2}		—	2.5	—	V
F.B.P delay time range	T_{H-FBP}	H-center: typ. From H_{OUT} rising edge to FBP center	—	—	19	µs
B.G.P start position		From H. sync. rear edge to burst gate pulse front edge	—	0.3	—	µs
Sandcastle pulse output temperature characteristics	$\Delta V_{60(Ta)}$		—	1.8	—	mV/deg
Sandcastle pulse input threshold level temperature characteristics	$\Delta V_{59(Ta)}$		—	0	—	mV/deg
F.B.P input threshold level temperature characteristics (HBLK)	$\Delta V_{61(Ta)}$		—	–1.8	—	mV/deg
F.B.P input threshold level temperature characteristics (AFC1)			—	1	—	mV/deg
X-ray inside reference temperature characteristics		Zener temperature characteristics: +1.8 mV/deg	—	0	—	mV/deg
Sandcastle pulse output vs. supply voltage dependence (BGP)		V_{CC2}: 5 V ± 0.5 V	—	1	—	V/V
Sandcastle pulse output vs. supply voltage (HBLK)		V_{CC2}: 5 V ± 0.5 V	—	0.74	—	V/V
Sandcastle pulse output vs. supply voltage (VBLK)		V_{CC2}: 5 V ± 0.5 V	—	0.44	—	V/V
Hold down operation voltage	V_{HTH}	V_{REF} (= pin 6) = 6.2 V	2.71	2.81	2.91	V
Vertical signal processing						
Vertical BLK phase (wide)	PVBLK(W)	Period from VBLK rising edge to vertical sync. falling edge	—	3.87	—	ms
Vertical BLK phase (normal)	PVBLK	Period from VBLK rising edge to vertical sync. falling edge	—	0.2	—	ms
Neck break operation pin 60 voltage	V_{60}	Pin 6: 1.5 V	1.5	—	—	V
Vertical BLK pulse width (wide)	TVBLK(W)		—	5.05	—	ms
Y-signal processing						
Contrast variable range	$Ay_{G(CON)min}$	Contrast: min.	—	40	—	dB
Y-output amplitude V_{CC} dependence	$\Delta y_{G(V_{CC})}$		—	0.4	—	dB/V
Y-output DC voltage V_{CC} dependence	$\Delta y_{G(V_{CC})}$		—	0.18	—	V/V
Y-noise level	VY_{NL}		—	7	50	mV
Delay line dynamic range	V_{DLmax}		—	0.7	—	V

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-signal processing (continued)						
Y-output amplitude vs. ambient temperature (R)	$\Delta y_{R(Ta)}$	−20°C to +70°C	—	−6	—	%
Y-output amplitude vs. ambient temperature (G)	$\Delta y_{G(Ta)}$	−20°C to +70°C	—	−8	—	%
Y-output amplitude vs. ambient temperature (B)	$\Delta y_{B(Ta)}$	−20°C to +70°C	—	−6	—	%
APL detection voltage	A_{APL}	Detection voltage ratio at APL 50%→100%	1	2	4	Time
Sharpness output voltage	V_{64}	Sharpness: typ.	1.8	2.1	2.4	V
Sharpness output variable range	ΔV_{64}	Sharpness: min.→max.	2.7	3.0	3.3	V
Chroma signal processing						
Detection output amplitude V_{CC} dependence	e_{O-V}		—	0	—	dB/V
VCO V_{CC} dependence	Δf_{CO-V}		—	220	—	Hz/V
Allowance of ratio between burst and chroma	$\Delta e_{O(bst)}$	Burst compression tolerance for color bar chroma	—	−40	—	%
Demodulated output ambient temperature dependeney (R−Y)	$\Delta e_{R-Y(Ta)}$	−20°C to +70°C	—	−3	—	%
Demodulated output ambient temperature dependeney (B−Y)	$\Delta e_{B-Y(Ta)}$	−20°C to +70°C	—	−3	—	%
RGB signal processing						
Y→RGB cross talk	eCT_1	Crosshatch	—	−45	—	dB
RGB→Y cross talk	eCT_2	Crosshatch	—	−40	—	dB
Color difference input dynamic range	AV_{max}		—	2.2	—	V
Internal-external pedestal difference voltage	ΔE_{YS}		−100	0	100	mV
OSD input dynamic range	AV_{max}		—	1.5	—	V
RGB output amplitude V_{CC} dependence	$\Delta e_{G(V_{CC})}$	V_{CC1}: 8.5 V to 9.5 V, V_{CC2}: 4.5 V to 5.5 V	—	0.4	—	V/V
OSD output amplitude V_{CC} dependence	$\Delta e_{g(V_{CC})}$	V_{CC1}: 8.5 V to 9.5 V, V_{CC2}: 4.5 V to 5.5 V	—	0	—	V/V
RGB color difference amplitude temperature dependence	$\Delta e_{G(Ta)}$	−20°C to +70°C	—	20	—	%
OSD color difference amplitude temperature dependence	$\Delta e_{g(Ta)}$	−20°C to +70°C	—	6	—	%

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RGB signal processing (continued)						
Color control range (External)	Δe_{COLOR}	0E: [40] versus DAC control ratio	—	28	—	%
White character slice level range	V_W	Blooming: DC 2.5 V, color difference no-input	0.6	0.8	1.0	V
White character correction amount	ΔV_W	Blooming: DC 2.5 V, color difference no-input	0.6	0.8	1.0	V
Demodulation angle R *1	$\angle R_{OUT}$	Tint: Tint center	—	87	—	degree
Demodulation angle G 1 *1	$\angle G_{OUT1}$	Tint: Tint center, G-Y ratio changeover: Type1	—	216	—	degree
Demodulation angle G 2 *1	$\angle G_{OUT2}$	Tint: Tint center, G-Y ratio changeover: Type2	—	236	—	degree
Deflection signal processing						
Vertical amplitude min. value	V_{AMPmin}		1.75	2.0	2.25	V[p-p]
Vertical amplitude max. value	V_{AMPmax}		2.8	3.2	3.6	V[p-p]
Vertical amplitude variation ratio	ΔV_{AMP}	Vertical amplitude: typ.→max.,min.	±10	±19	±28	%
Vertical linearity variation width	ΔV_{LIN}	Vertical linearity: typ.→max.,min.	±5	±12	±19	%
Vertical S letter amplitude variation ratio	ΔV_{SC}	Vertical S letter: max.→min.	−33	−18	−3	%
Vertical position center voltage	V_{CENTER}		2.53	2.85	3.17	V
Vertical position variation width	ΔV_{SHIFT}	Vertical S position: min.→max.	0.6	0.8	1.0	V
Vertical EHT amplitude variation ratio	ΔV_{EHT}	Pin 25 = 0 V vertical EHT: typ.→max., min.	±3	±11	±19	%
EW parabola amplitude min. value	$V_{PARAmin}$		0.02	0.29	0.59	V[p-p]
EW parabola amplitude max. value	$V_{PARAmax}$		3.0	4.3	5.6	V[p-p]
EW parabola variation width	$\Delta V_{PARABOLA}$	EW parabola amplitude: min.→max.	2.0	3.2	4.4	V[p-p]
Horizontal amplitude variation width	$\Delta V_{H-WIDTH}$	Horizontal amplitude: min.→max.	3.4	4.6	5.8	V
Horizontal amplitude min. DC value	$V_{H-WIDTH}$		1.5	1.9	2.3	V
Trapezoidal distortion correction variation ratio	ΔV_{TRAPZ}	Trapezoidal distortion correction: typ.→max., min.	±48	±72	±96	%
Corner correction variation ratio 1	ΔV_{CORNER}	EW corner 1: min.→max.	−40	−28	−16	%
Corner correction variation ratio 2	ΔV_{CORNER}	EW corner 2: min.→max.	−38	−26	−14	%
Horizontal EHT correction variable range	ΔV_{H-EHT}	Pin 25 = 1 V, horizontal EHT:	1.4	2.2	3.0	V

Note) ∗1: Under the condition that pin 52 is adjusted for the Drive I, Ⅱ by inserting Y-signal, and R and B-output amplitude equal that of G-output.

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deflection signal processing (continued)						
Horizontal EHT correction min. DC value	V_{H-EHT}		1.8	2.8	3.8	V
Vertical position variation width at trapezoidal correction	$\Delta V_{SH-TRAP}$	Trapezoidal correction: min.→max.	0.4	0.65	0.9	V
Corner correction slice level pin voltage	V_{28}		—	0.55	—	V
Corner correction gain adjustment pin voltage	V_{20}		—	2.5	—	V
EW output V_{CC} variation	$\Delta V_{EW(V_{CC})}$	V_{CC1}: 8.5 V to 9.5 V, V_{CC2}: 4.5 V to 5.5 V	—	0	—	%
Ramp waveform (normal)	ΔV_{RAMP}	0D[00]	—	2.5	—	V[p-p]
Ramp waveform (wide)	$\Delta V_{RAMP(W)}$	0D[40]	—	2.5	—	V[p-p]
AGC input/output current	I_{13}	Service SW: On, pin 14 sweep	—	±140	—	µA
Ramp input/output current 1	I_{14}	Pin 13: 1.5 V, pin 14: 2.5 V, V_{PULSE}: On	—	4.4	—	mA
Ramp input/output current 2	I_{14}	Pin 13: 1.5 V, pin 14: 2.5 V, V_{PULSE}: Off	—	–90	—	µA
Ramp wave pin voltage at V-OSC stopping	V_{14-SW}	0D[80]	—	1.2	—	V
Input signal						
Chroma input allowable level	e_{CIN}	Color bar chroma, 330 mV[p-p] burst level	90	150	—	mV[p-p]
Y-input allowable level	y_{IN}	Sync. to white 100%	—	0.5	0.7	V[p-p]
H-sync. input allowable level	V_{HIN}	Sync. to pedestal	0.5	1.0	2.0	V[p-p]
V-sync. input allowable level	V_{VIN}	Sync. to pedestal	0.5	1.0	2.0	V[p-p]
Sandcastle pulse external input BGP	V_{BGPIN}	V_{CC}: typ.	4.0	4.3	4.6	V[p-p]
Sandcastle pulse external input HBLK	V_{HBLKIN}	V_{CC}: typ.	2.7	3.0	3.3	V[p-p]
Sandcastle pulse external input VBLK	V_{VBLKIN}	V_{CC}: typ.	1.2	1.6	1.8	V[p-p]
FBP input	V_{FBPIN}	V_{CC}: typ.	—	—	3.5	V
Y_S input threshold voltage	V_{26}	V_{CC}: typ.	0.4	0.7	1.2	V
On-screen input R	e_{30}		—	0.71	1.0	V[p-p]
On-screen input G	e_{29}		—	0.71	1.0	V[p-p]
On-screen input B	e_{27}		—	0.71	1.0	V[p-p]

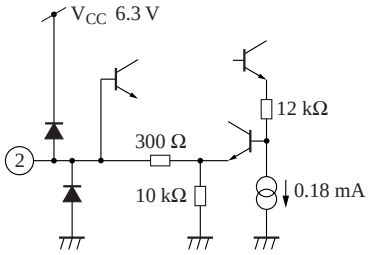
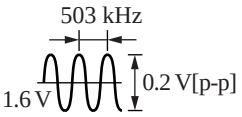
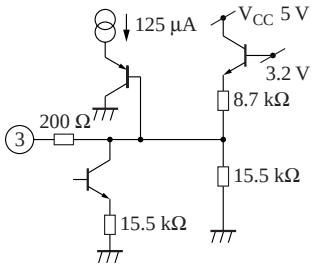
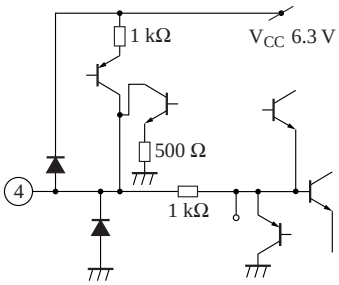
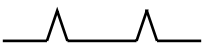
■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

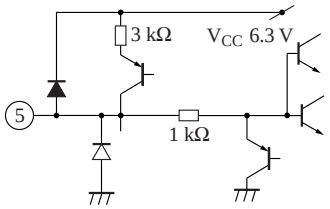
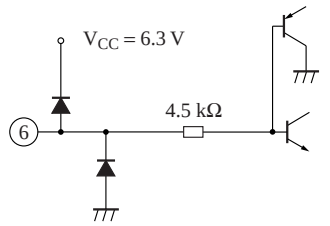
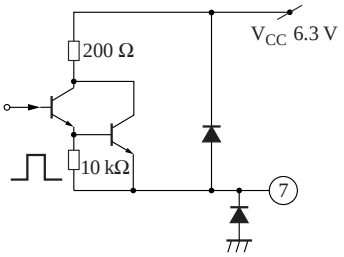
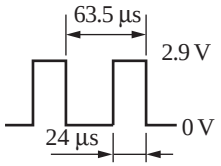
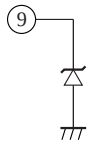
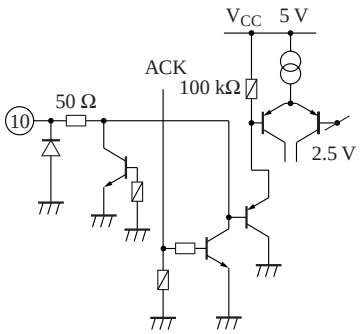
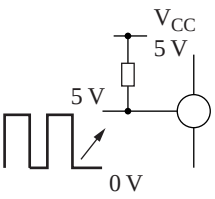
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input signal (continued)						
I^2C bus SDA input level high	V_{10}	V_{CC2} (= 5 V)	4.0	—	V_{CC2}	V
I^2C bus SDA input level low	V_{10}	V_{CC2} (= 5 V)	0	—	0.7	V
I^2C bus SCL input level high	V_{12}	V_{CC2} (= 5 V)	4.0	—	V_{CC2}	V
I^2C bus SCL input level low	V_{12}	V_{CC2} (= 5 V)	0	—	0.7	V
ACL pin voltage range	V_{51}	V_{CC}: Typ.	2.7	—	4.5	V

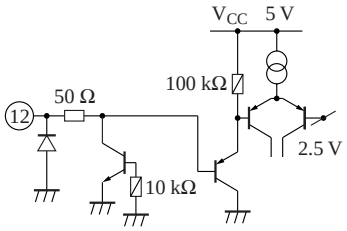
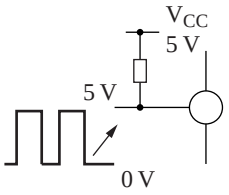
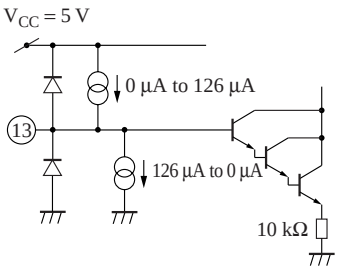
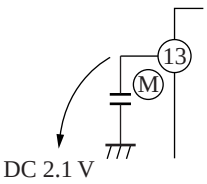
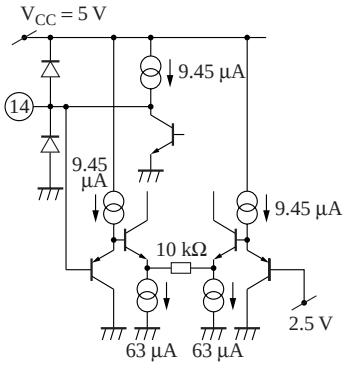
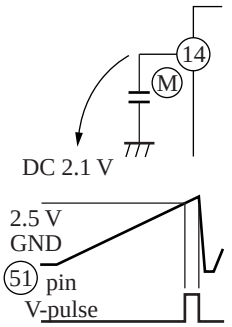
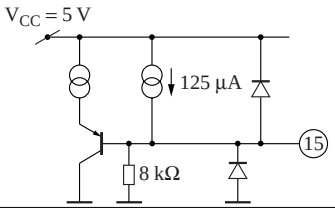
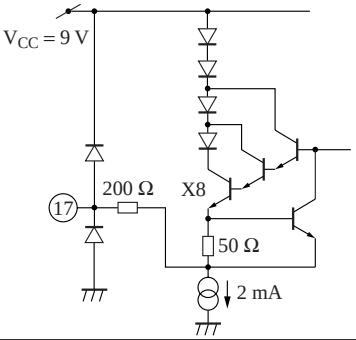
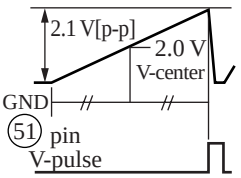
■ Terminal Equivalent Circuits

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
1	GND	—	Sync. and DEF GND	—
2	503 kHz VCO		Horizontal oscillation pin • Oscillates by connecting crystal oscillator of 503 kHz • DC = 1.6 V	
3	Vertical position movement DAC output		Trapezoidal correction control DAC output	DC
4	AFC2 filter		Phase detection filter for picture position adjustment • Phase adjustment High: Phase Lead Low: Phase Lag	

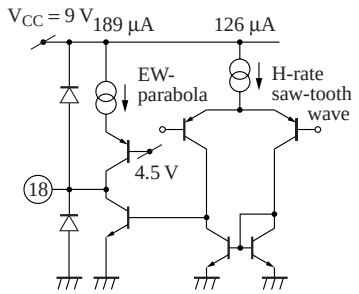
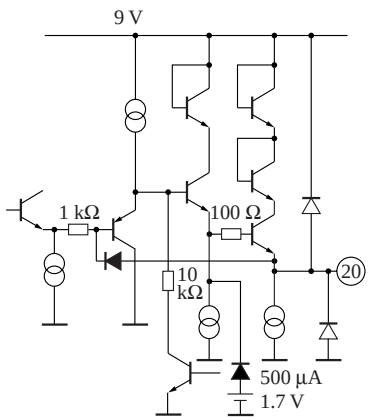
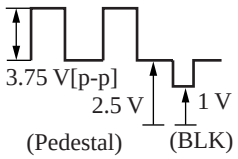
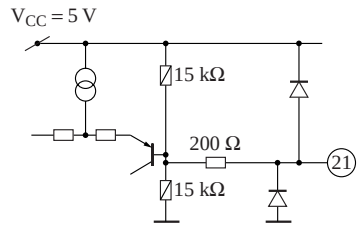
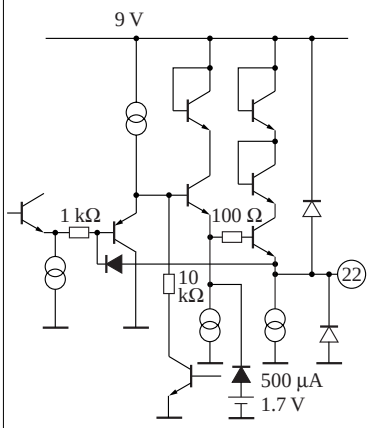
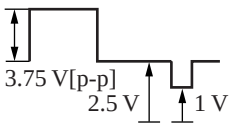
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
5	High tension detection input (X-ray)		Hold-down input pin • Threshold voltage 2.81 V	DC
6	High tension reference voltage		Hold-down reference (comparison) voltage • DC = 6.2 V	DC
7	Horizontal drive pulse output		Output pin of horizontal drive pulse • High: 2.9 V Low: 0 V	
8	N.C.	—	—	—
9	H V_{CC}		Power supply voltage pin of horizontal block • With an external resistor, V_{CC} of 6.3 V are generated in advance.	DC
10	I^2C SDA input		SDA signal input pin for I^2C and ACK signal output pin	
11	I^2C Ground	—	Ground pin for I^2C	—

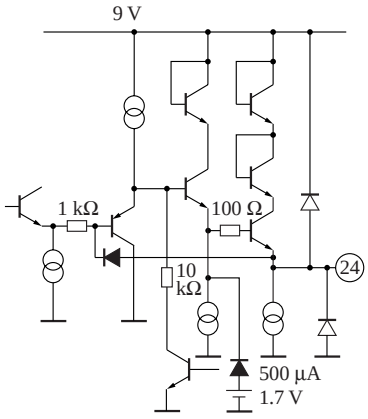
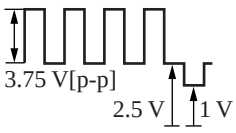
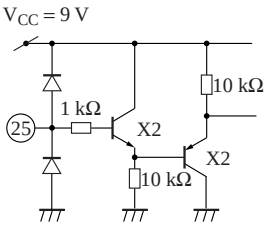
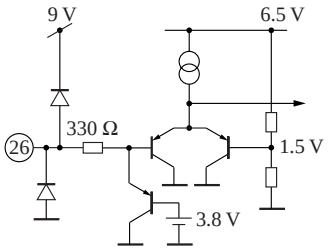
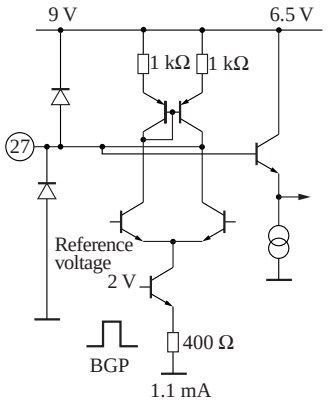
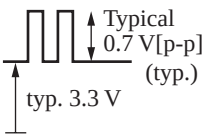
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
12	I^2C SCL input		SCL signal input pin for I^2C	
13	Reference ramp waveform AGC pin (Ramp-AGC)		AGC capacitor connection pin to make the amplitude of saw-tooth wave generating at pin 14 constant.	Connect a capacitor of 0.47 µF to pin 13. 
14	Reference ramp waveform (Ramp-Gen)		Capacitor pin to generate reference saw-tooth wave performed AGC.	Connects 0.33 µF of capacitor to pin 14 
15	Corner slice level		Corner slice level correction use pin	—
16	9 V power supply (V_{CC1})	—	9 V power supply	—
17	Vertical deflection saw-tooth wave output (V-ramp)		Pin for vertical deflection saw-tooth output with various deflection corrections	

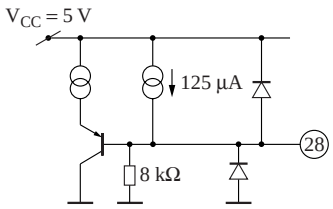
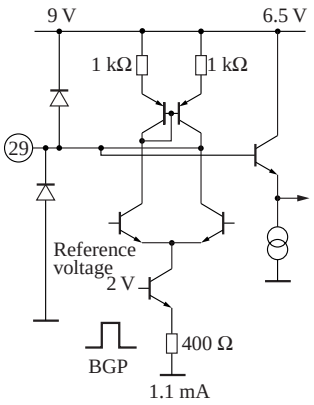
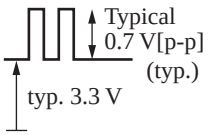
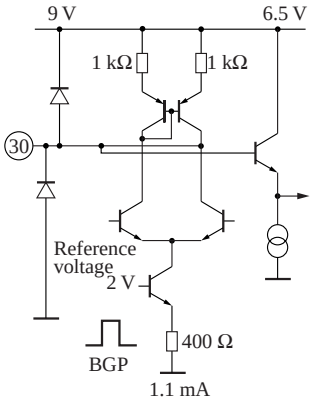
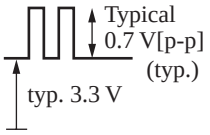
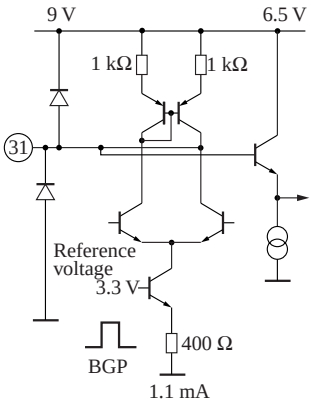
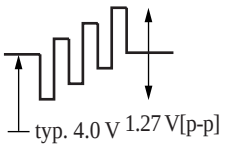
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
18	Pincushion distortion correction wave output pin (EW-out)		Pin for pincushion correction with various deflection corrections	
19	9 V power supply (V_{CC1})	—	9 V power supply	—
20	R-output		R-signal output	At contrast max. of input (R–Y: 1.0 V[p-p], Y: 0.5 V[p-p]) 
21	Corner gain control		Picture corner correction gain adjustment pin • Adjustable with an external resistor	—
22	G-output		G-signal output	At contrast max. of Y: 0.5 V[p-p] (R–Y: 1.0 V[p-p], B–Y: 1.27 V[p-p]) 

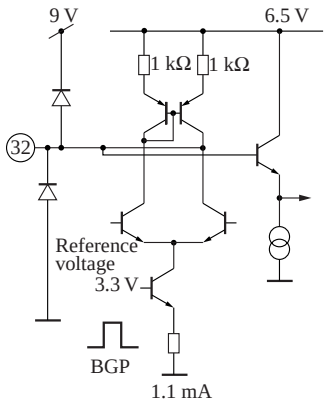
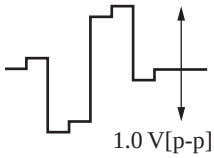
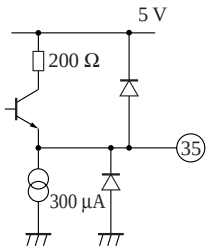
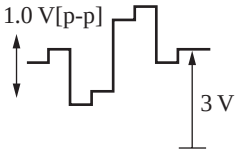
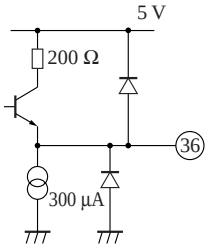
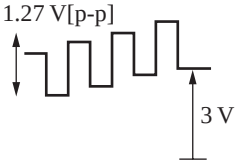
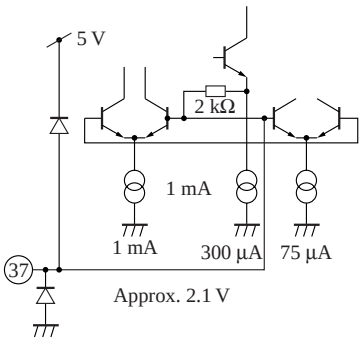
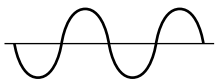
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
23	N.C.	—	—	—
24	B-output		B-signal output	When contrast max. of Y: 0.5 V[p-p], B–Y: 1.27 V[p-p] 
25	EHT voltage detection pin		High tension variation detection input pin for vertical and horizontal EHT correction	Move linearly with 4.0 V to 2.0 V of DC voltage (Normally 4.0 V or more)
26	Y_S input		TV/on-screen change-over pin at on-screen input Threshold level: 0.7 V(typ.)	—
27	On-screen B-input		On-screen B-input	On-screen data 

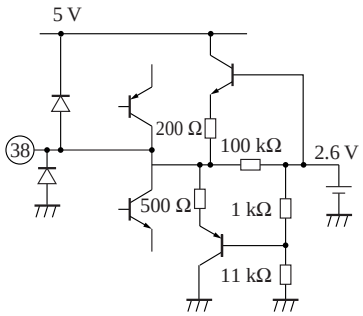
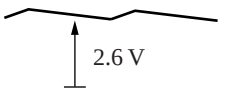
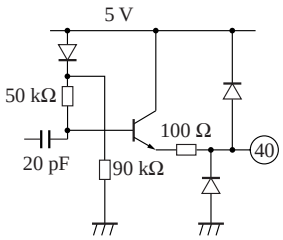
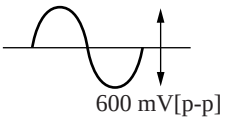
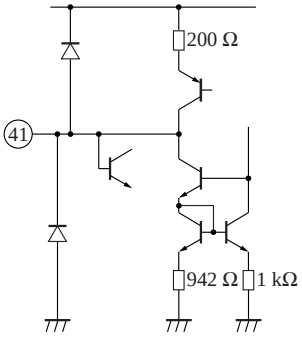
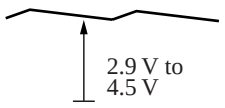
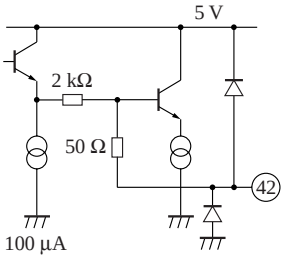
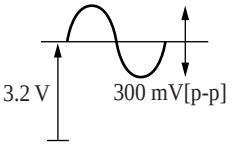
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
28	Corner slice level		Connects to pin 15	—
29	On-screen G-input		On-screen G-input	
30	On-screen R-input		On-screen R-input	
31	Color difference B–Y input		Color difference B–Y input	

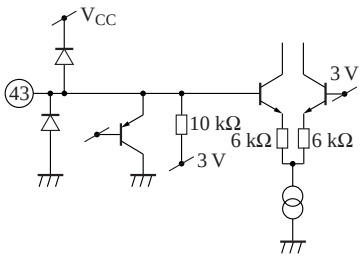
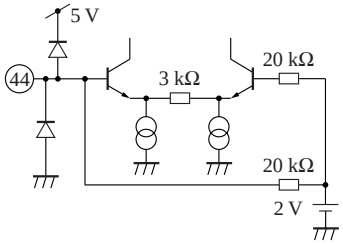
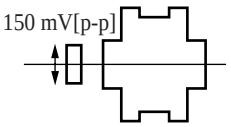
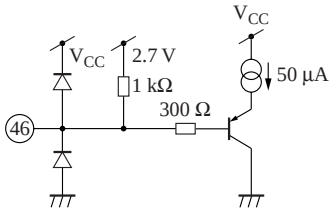
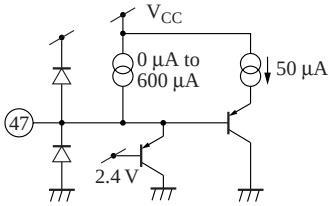
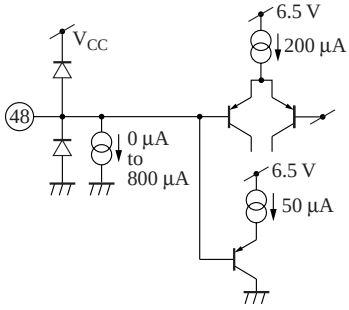
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
32	Color difference R−Y input		Color difference R−Y input	
33	Ground for V/C/RGB	—	GND pin for video, chroma and RGB block	—
34	N.C.	—	—	—
35	Color difference R−Y output		Color difference signal R−Y output	
36	Color difference B−Y output		Color difference signal B−Y output	
37	3.58 MHz oscillator pin		3.58 MHz VCO oscillator pin	 Oscillation waveform

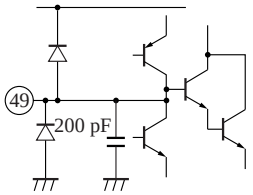
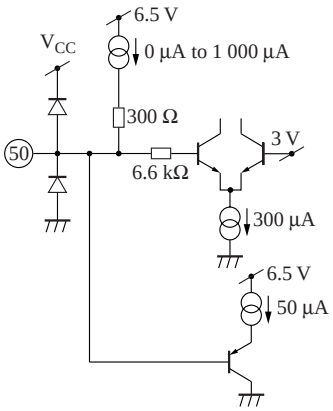
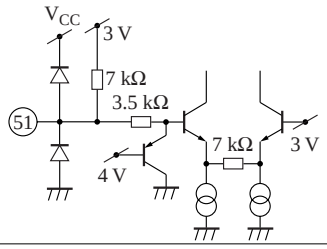
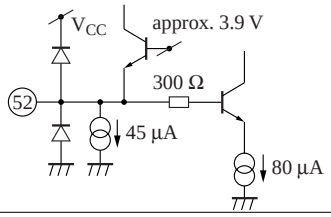
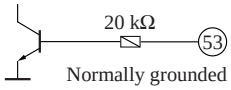
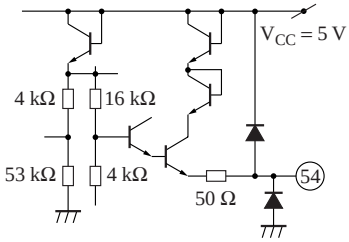
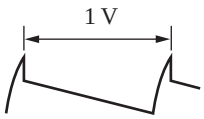
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
38	APC filter		Chroma APC filter pin	
39	N.C.	—	—	—
40	3.58 MHz CW output		3.58 MHz VCO oscillation output	
41	Killer filter		Killer detection filter pin • Killer detection at 3.5 V or less	
42	Color track filter		Filter pin for phase shift	

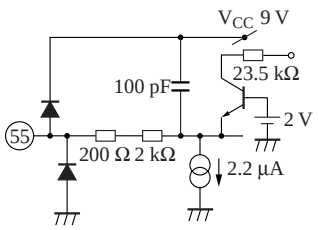
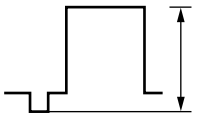
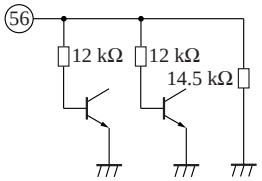
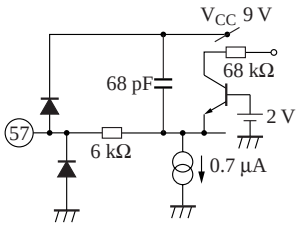
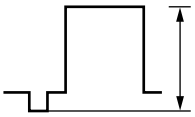
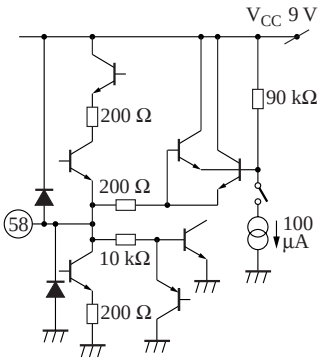
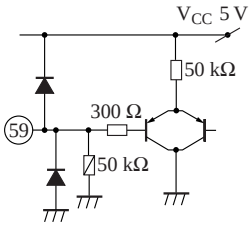
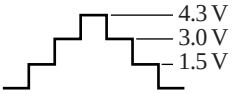
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
43	ABL input pin for brightness		Brightness variable pin	Has adjustment range of 3 V ± 0.8 V at DC input
44	Chroma input		Chroma input pin	Color bar signal  Burst reference 0 dB = 150 mV[p-p]
45	5 V power supply (V_{CC2})	—	5 V power supply	—
46	Blooming level input pin		Input pin to determine blooming level	DC 2.7 V at open
47	Filter pin for APL detection		Filter pin to detect APL of video signal	DC voltage of 0 V to 3 V
48	Filter pin for white detection		Filter pin to detect white max. value of video signal	DC voltage of 2 V to 4 V

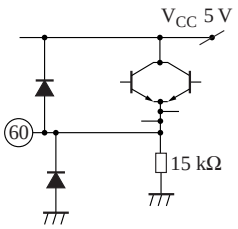
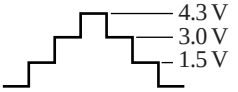
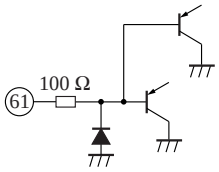
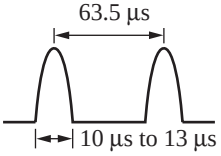
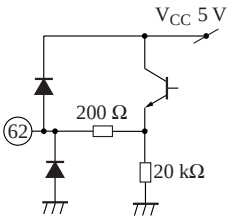
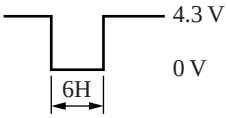
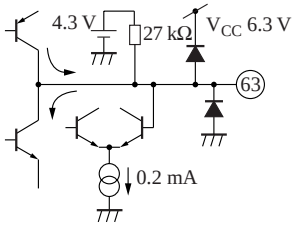
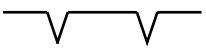
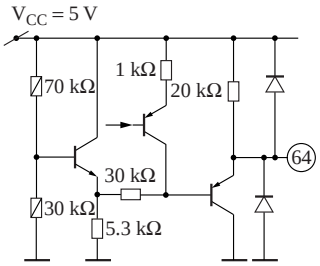
■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
49	Y-clamp filter		Luminance clamp filter pin	DC voltage 2.5 V to 8 V
50	Filter pin for black detection Color control input pin		1. Filter pin to detect black min. value of video signal 2. Input pin to control color	1. Case of black detection pin DC voltage 2 V to 4 V 2. Color control voltage 2 V to 4V
51	ACL input pin for contrast		Contrast variable pin	With adjustment range of DC input 2.7 V to 4.5 V
52	Y-signal input pin		Y-signal input pin	0.5 V[p-p] typical input 0.36 V (Pedestal to white)
53	Slave address setting		<table><tr><th>Pin</th><th>53</th></tr><tr><td>8A</td><td>Low</td></tr><tr><td>8C</td><td>High</td></tr></table> 8A has been registered by Philips Semiconductors.	—
54	V-sync. Sep.		Integrating filter pin for vertical sync. signal	

■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
55	Sync. in (H)		Input pin for sync. separation	
56	Black detection inhibition		—	—
57	Sync. in (V)		Input pin for sync. separation	
58	Lock det. filter		Filter pin for horizontal oscillation frequency and sync. detection of input sync., common use as hold-down detection.	At sync.: 6 V At async.: 0 V At hold-down: 8.3 V
59	Sandcastle pulse input For AFC FBP input		Input pin for vertical and horizontal blanking pulses on which a burst gate pulse has been super-imposed. • Threshold voltage Burst gate pulse : 3.5 V Horizontal blanking pulse : 2.2 V Vertical blanking pulse : 1.0 V	

■ Terminal Equivalent Circuits (continued)

Pin No.	Pin name	Equivalent circuit	Description	Pin waveform
60	Sandcastle pulse output		Output pin for vertical and horizontal blanking pulse and pulse which is superimposed burst gate pulse in order to synchronize with AN5308NK and other IC. • Threshold voltage : 3.5 V	
61	Flyback pulse input		Input pin of flyback pulse • Threshold voltage AFC: 2.5 V Blanking: 0.7 V	
62	V_{OUT}		Output pin of vertical oscillation pulse	
63	AFC1 filter		Output pin of horizontal AFC current • Horizontal AFC is operated when RC for filter is connected. • Frequency adjustment High: Frequency to low Low: Frequency to high	
64	Sharpness control		External sharpness control pin • Interlocks to internal sharpness	—

■ Application Circuit Example