

P-channel -60 V, 0.13 Ω typ., -3 A STripFET™ F6 Power MOSFET in a SOT-223 package

Datasheet - production data

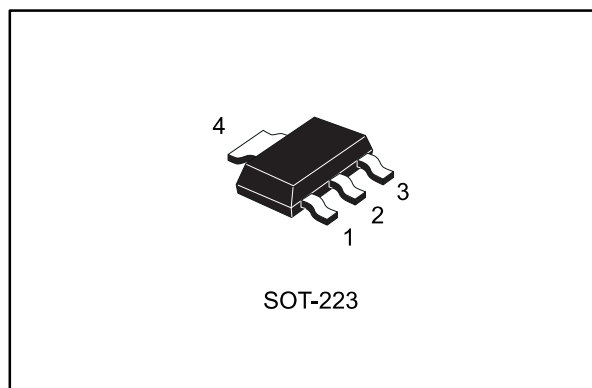
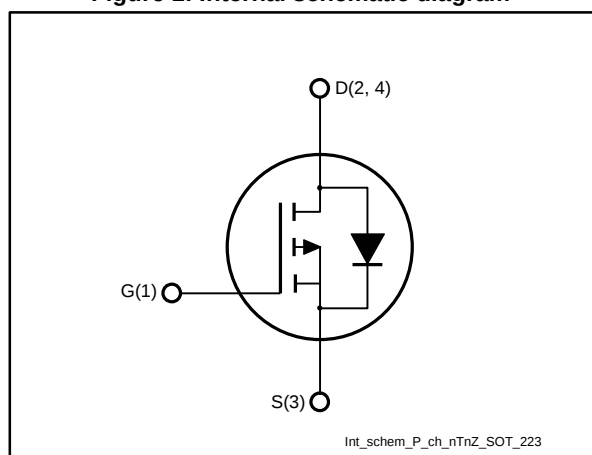


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STN3P6F6	-60 V	0.16 Ω	-3 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STN3P6F6	3P6F6	SOT-223	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	-3	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	-2	A
I_{DM}	Drain current (pulsed)	-12	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.6	W
T_j	Operating junction temperature range	- 55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width is limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	57	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2 Oz Cu, $t < 10\text{ s}$

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage(V _{GS} = 0)	I _D = -250 μA	-60			V
I _{DSS}	Zero gate voltage Drain current (V _{GS} = 0)	V _{DS} = -60 V			-1	μA
		V _{DS} = -60 V, T _C = 125 °C ⁽¹⁾			-10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ± 20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = -250 μA	-2		-4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = -10 V, I _D = -1.5 A		0.13	0.16	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = -48 V, f = 1 MHz, V _{GS} = 0	-	340	-	pF
C _{oss}	Output capacitance		-	40	-	pF
C _{rss}	Reverse transfer capacitance		-	20	-	pF
Q _g	Total gate charge	V _{DD} = -48 V, I _D = -3 A, V _{GS} = -10 V (see Figure 14: "Gate charge test circuit")	-	6.4	-	nC
Q _{gs}	Gate-source charge		-	1.7	-	nC
Q _{gd}	Gate-drain charge		-	1.7	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = -48 V, I _D = -1.5 A, R _G = 4.7 Ω, V _{GS} = -10 V (see Figure 13: "Switching times test circuit for resistive load")	-	6.4	-	ns
t _r	Rise time		-	5.3	-	ns
t _{d(off)}	Turn-off delay time		-	14	-	ns
t _f	Fall time		-	3.7	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		-3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		-12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = -3\text{ A}$, $V_{GS} = 0$	-		-1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = -5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = -16\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	20		ns
Q_{rr}	Reverse recovery charge		-	17.8		nC
I_{RRM}	Reverse recovery current		-	-1.8		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Figure 2: Safe operating area

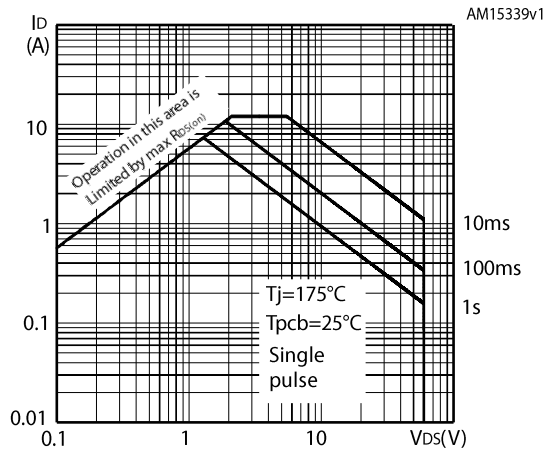


Figure 3: Thermal impedance

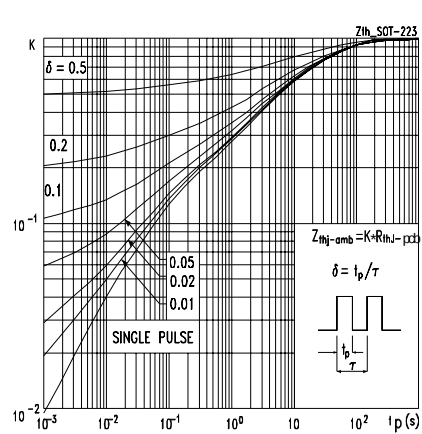


Figure 4: Output characteristics

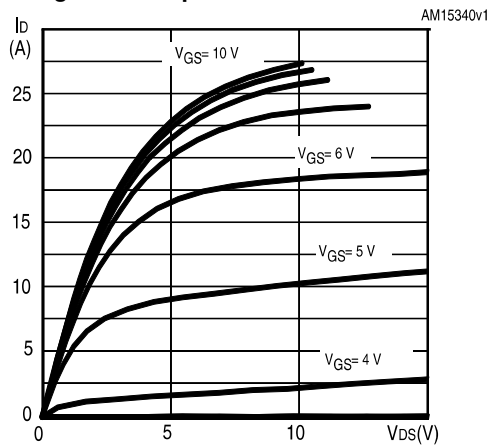


Figure 5: Transfer characteristics

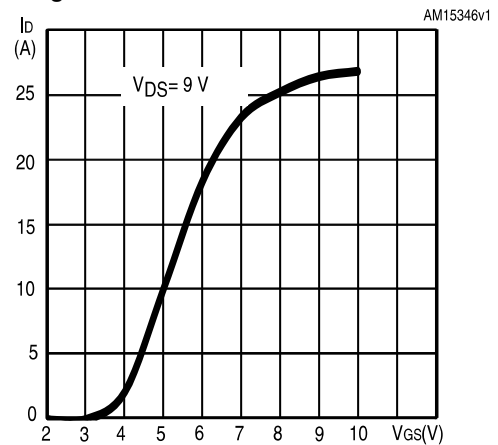


Figure 6: Gate charge vs gate-source voltage

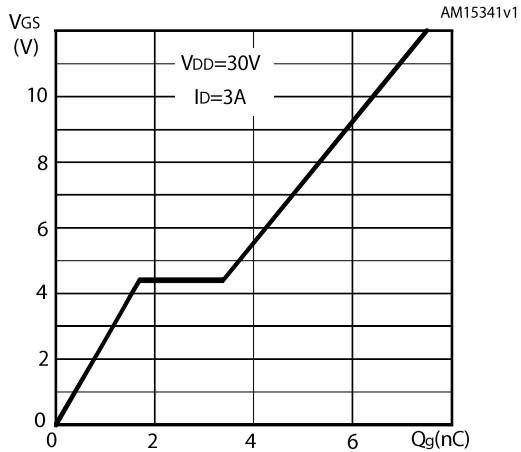


Figure 7: Static drain-source on-resistance

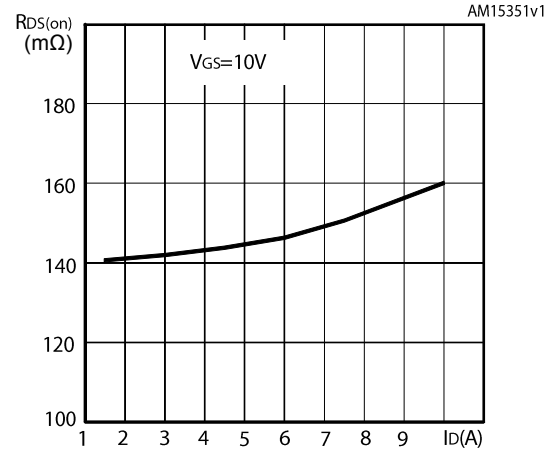


Figure 8: Capacitance variations

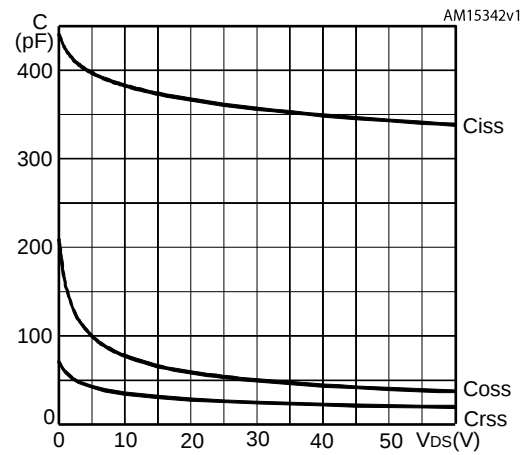
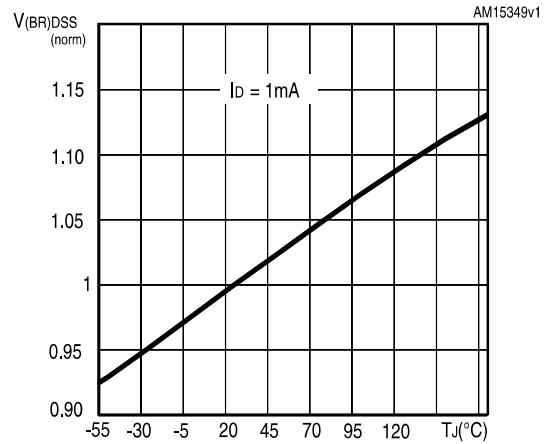
Figure 9: Normalized $V(BR)_{DSS}$ vs. temperature

Figure 10: Normalized gate threshold voltage vs temperature

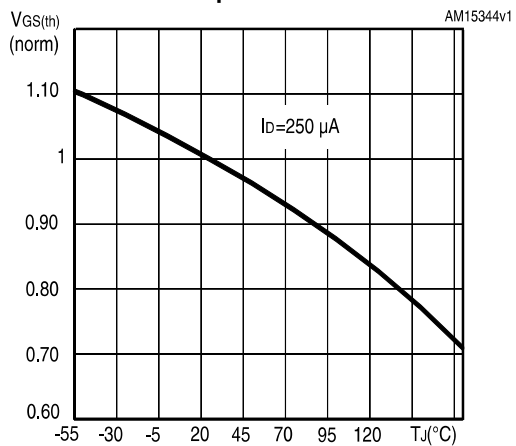


Figure 11: Normalized on-resistance vs. temperature

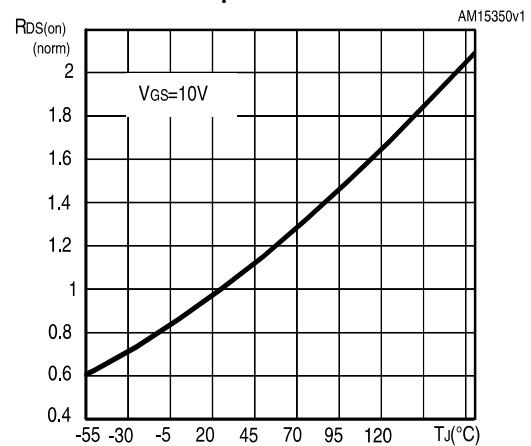
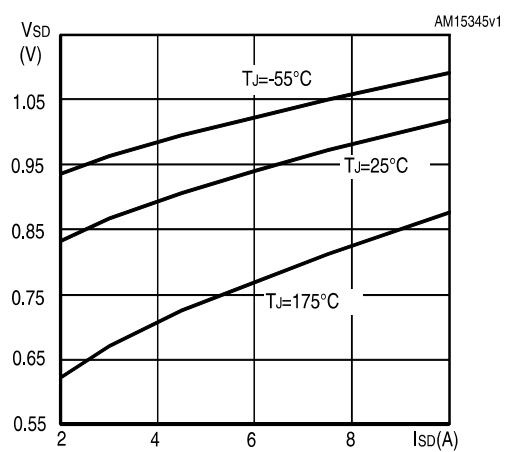


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

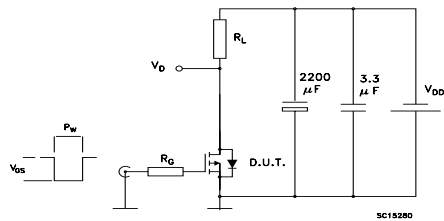


Figure 14: Gate charge test circuit

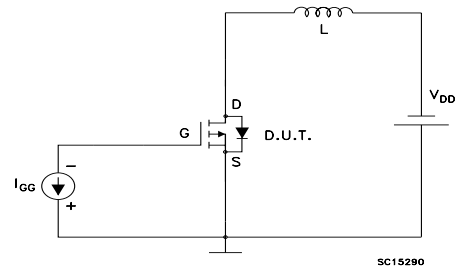
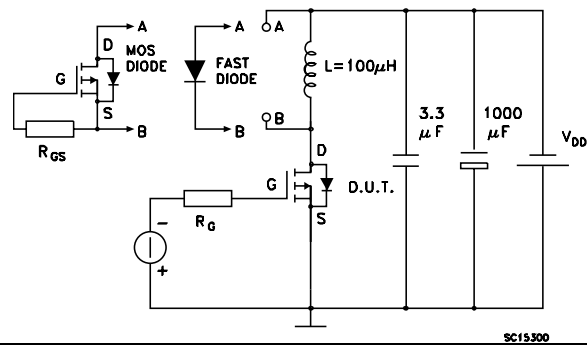


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 16: SOT-223 package outline

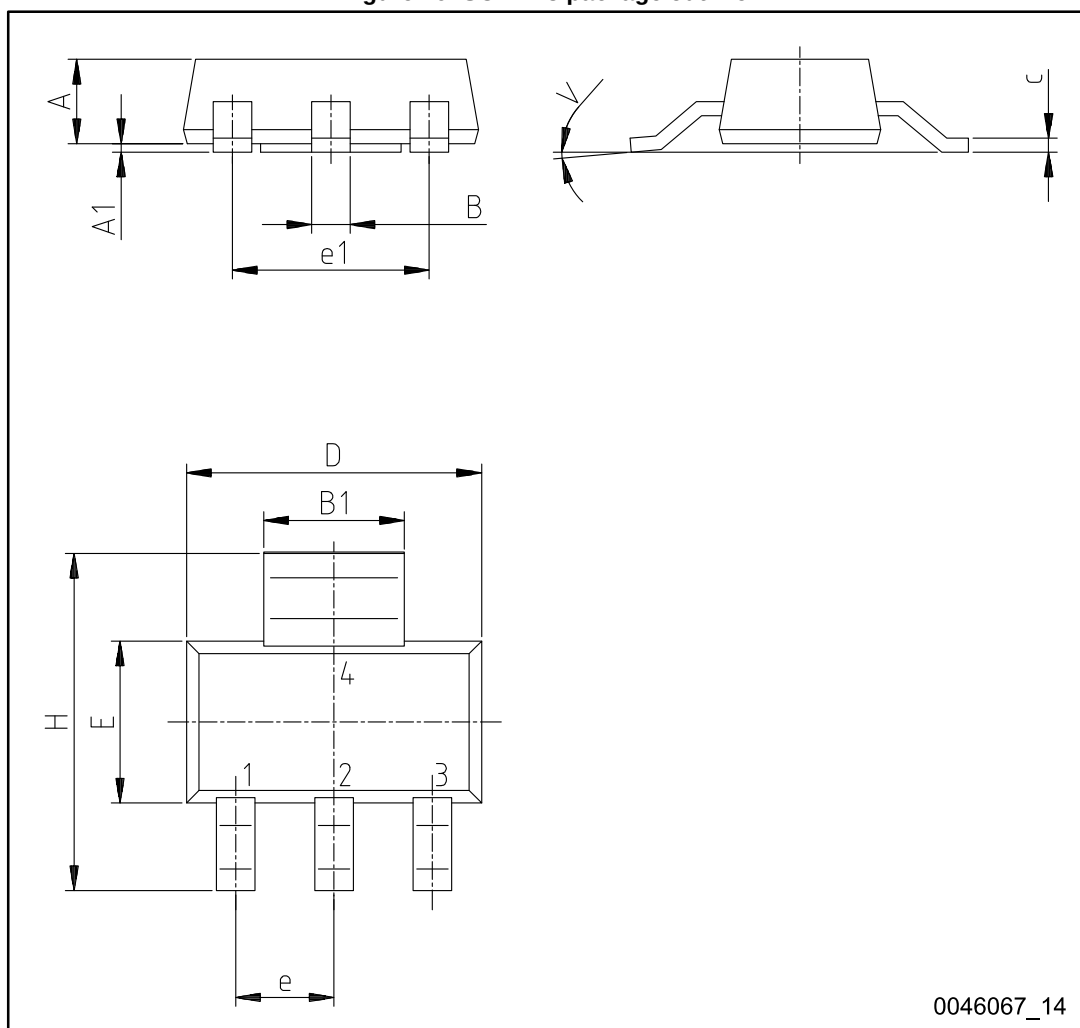
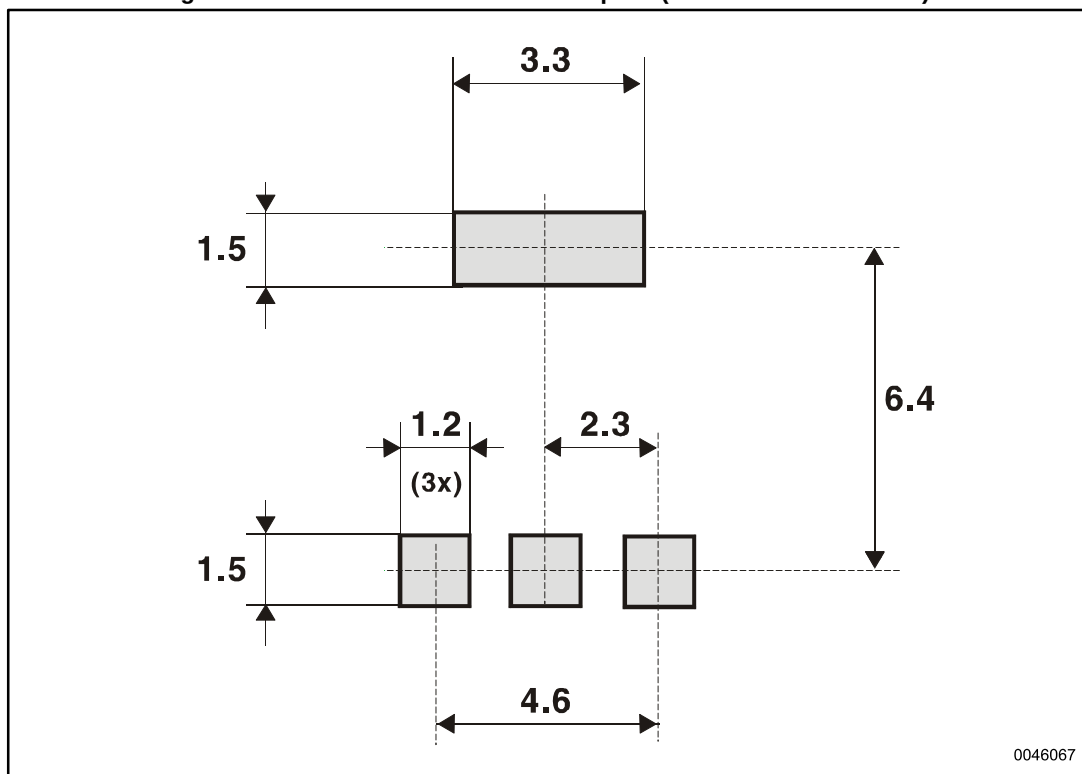


Table 8: SOT-223 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.8
A1	0.02		0.1
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7.0	7.3
V			10°

Figure 17: SOT-223 recommended footprint (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
31-Oct-2012	1	First release.
09-Nov-2012	2	Modified: note 1 in Table 3
16-Jan-2013	3	Document status promoted from preliminary data to production data
14-Mar-2013	4	Modified: Figure 1, 3, Ciss, Coss, Crss typical values in Table 5
07-Oct-2016	5	Updated title, features and description in cover page. Updated silhouette and Figure 1: "Internal schematic diagram" . Updated Figure 16: "SOT-223 package outline" . Minor text changes.

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