LINFINITY
A MICROSEMI COMPANY
THE INFINITE POWER OF INNOVATION

UltraMAX™ LX5245 / 5246

9-LINE LVD SCSI TERMINATOR

PRELIMINARY DATA SHEET

DESCRIPTION

The LX5245/5246 ICs are Low Voltage Differential (LVD) Terminators designed to comply with the LVD termination specification in the SPI-4 document. The LX5245/5246 are designed specifically for LVD applications. Because the LX5245/ 5246 support only LVD, they have lower output capacitance than multimode terminators such as the LX5241.

The LX5245/5246 Utilize Linfinity's UltraMAX Technology which delivers the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduces channel-to-channel noise and cross talk. The high-bandwidth UltraMAX architecture insures ULTRA-2 performance, while providing a clear migration path to ULTRA-3 and beyond.

When The LX5245/5246 Are Enabled, The Differential Sense (DIFFSENSE) Pin Supplies A Voltage Between 1.2V And 1.4V. In application, the terminator DIFFSENSE output is connected to the system DIFFSENSE line. If there are no single ended or HVD devices attached to the system the LVD output will be enabled. If the DIFFSENSE line is LOW, indicating a single ended device, the LX5245/ 5246 output will be HiZ. If the DIFFSENSE line is HIGH, indicating a high voltage differential device the LX5245/5246 output will be HiZ.

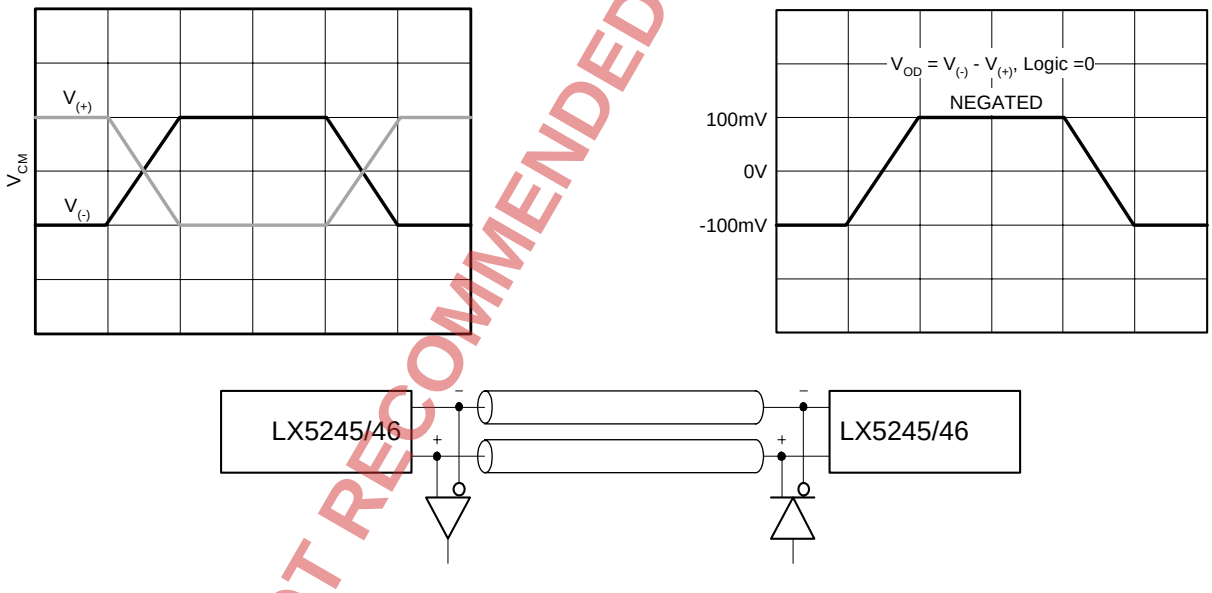
The LX5245/5246 ICs Have A TTL Compatible DISCONNECT Pin. The LX5245 is active LOW and the LX5246 is active HIGH. During sleep mode, power dissipation is reduced to a meager 5µA, while also placing all outputs in a HI Z state. Also during sleep mode, the DIFFSENSE function is disabled and is placed in a HI Z state.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- 2.5pF Typical Disabled Output Capacitance
- Fast Response, No External Capacitors Required
- 5µA Supply Current In Disconnect Mode
- 20mA Supply Current During Normal Operation
- Logic Command Disconnects All Termination Lines
- Diffsense Line Driver
- Current Limit And Thermal Protection
- Compliant With SPI-2 (Ultra2), SPI-3 (Ultra160),
- Mention 5249 as LVD Only Terminator With Pinout Compatible With Industry Standard Multi-mode Terminators
- Pin Compatible With Unitrode UCC5640

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	PW Plastic TSSOP 24-Pin RoHS / Pb-free Transition DC: 0442
0 to 70	**LX5245CPW**
	LX5246CPW

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX5245CPW-TR)

Rev. 0.8a,2005-03-02

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ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage ..... +6.5V
Signal Line Voltage ..... 0V to 6.5V
Differential Voltage ..... 0V to 6.5V
Operating Junction Temperature
Plastic (PW Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Peak Package Solder Reflow Temperature (40 second maximum exp.)....260°C(+0, -5)

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

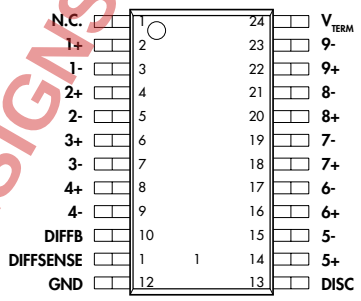
PW PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUTS

LX5245/46 CPW



24L PW PACKAGE (Top View)
("N.C." = No Internal Connections)

RoHS / Pb-free 100% Matte Tin Lead Finish

DIFFSENSE / POWER UP / POWER DOWN FUNCTION TABLE

LX5245 DISCONNECT	LX5246 DISCONNECT	DIFFSENSE	Outputs Status	Outputs Type	Quiescent Current
L	H	L < 0.5V	Disable	HiZ	2mA
L	H	0.7V to 1.9V	Enable	LVD	21mA
L	H	H > 2.4V	Disable	HiZ	2mA
H	L	X	Disable	HiZ	10µA
Open	Open	X	Disable	HiZ	10µA

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termpwr Voltage	V_{TERM}	3.0		5.25	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Junction Temperature Range					
LX5245 / 5246		0		70	°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperature range of $0°C \le T_A \le 70°C$. TermPwr = 3.3V, DISCONNECT: LX5245 = L, LX5246 = H. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	LX5245 / 5246			Units
			Min.	Typ.	Max.	
LVD Terminator Section						
TermPwr Supply Current	LVD I_{CC}	All term lines = Open		21	25	mA
		DISCONNECT: LX5245 = H, LX5246 = L		5	10	µA
Common Mode Voltage	V_{OM}		1.125	1.25	1.375	V
Offset Voltage (fail safe bias voltage)	V_{OS}	Open circuit between - and + (see Note 3)	100	112	125	mV
Differential Terminator Impedance	Z_D	V_{OD} = -1V to 1V	100	105	110	Ω
Common Mode Impedance	Z_{CM}	0V to 2.5V	100	200	300	Ω
Output Capacitance	C_o	DISCONNECT: LX5245 = H, LX5246 = L		2.5		pF
Output Leakage	I_{Leak}	DISCONNECT: LX5245 = H, LX5246 = L, V_{LINE} = 0 to 4V, T_A=25°C		0	2	µA
		DISCONNECT: LX5245 = H, LX5246 = L, V_{TERM} = 0V, V_{LINE} = 2.7V		1		µA
Mode Change Delay	t_{DF}	DIFFSENSE = 1.4V to 0V	100	150		ms
DIFFSENSE Section						
DIFFSENSE Output Voltage	V_{DIFF}		1.2	1.3	1.4	V
DIFFSENSE Output Source Current	I_{DIFF}	DIFFSENSE = 0V	5.0		15.0	mA
DIFFSENSE Sink Current	$I_{SINK(DIFF)}$	V_{IN} = 2.75V			200	µA
DIFFSENSE Output Leakage	$I_{LEAK(DIFF)}$	DISCONNECT: LX5245 = H, LX5246 = L, T_A = 25°C			10	µA
DISCONNECT Section						
DISCONNECT Threshold	V_{TH}		0.8		2.0	V
Input Current	I_{IH}	DISCONNECT: LX5245 = 0V			10	µA
		DISCONNECT: LX5246 = 3.3V			10	µA

Note 3. Open circuit failsafe voltage.

BLOCK DIAGRAM

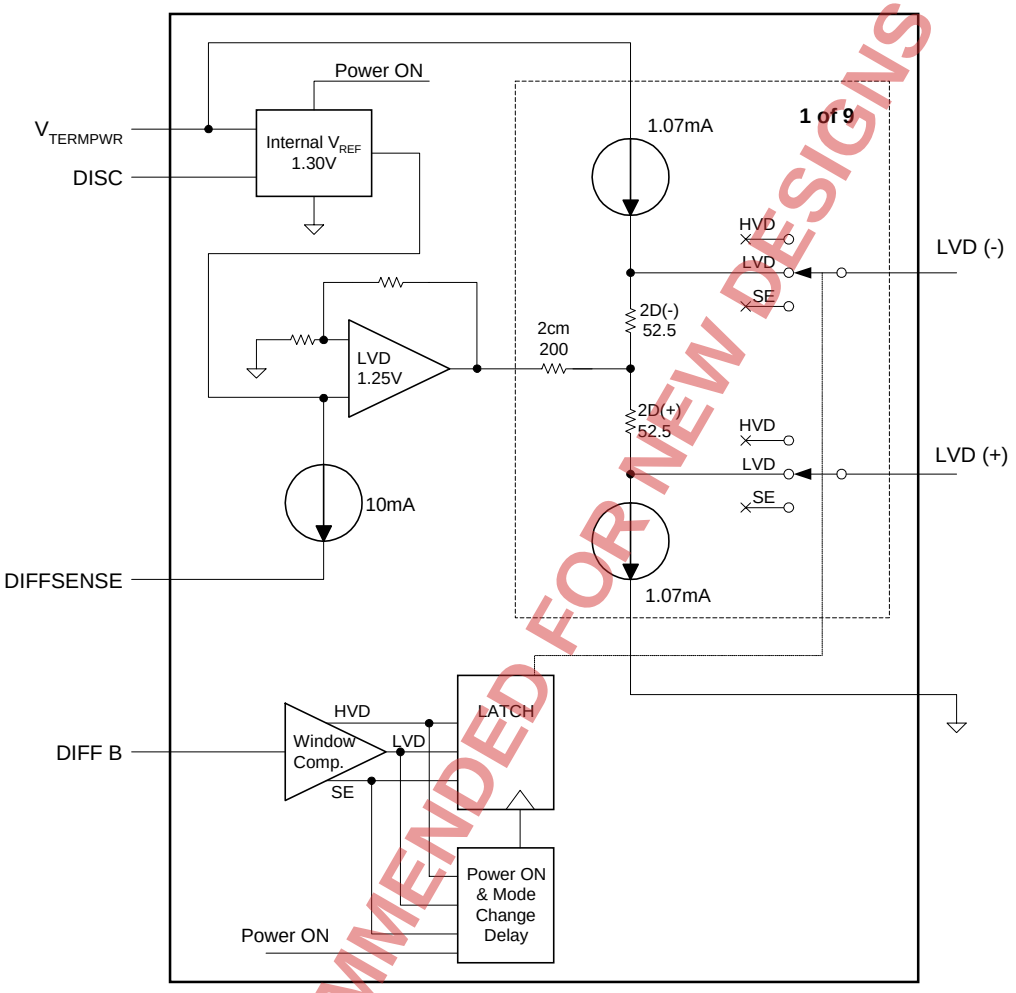


FIGURE 1 — LX5245 Block Diagram

FUNCTIONAL PIN DESCRIPTION

Pin Designator	Description
1-, 2-, 3-, 4-, 5-, 6-, 7-, 8-, 9-	Negative signal termination lines.
1+, 2+, 3+, 4+, 5+, 6+, 7+, 8+, 9+	Positive signal termination lines.
V_{TERM}	Power supply pin for terminator. Connect to SCSI bus TERMPWR. Must be decoupled by one 4.7µF low-ESR capacitor for every three terminator devices. It is absolutely necessary to connect this pin to the decoupling capacitor through a very low impedance (big traces on PCB). Keeping distances very short from the decoupling capacitors to the V_{TERM} pin is also critical. The value of the decoupling capacitor is somewhat layout dependant and some applications may benefit from high-frequency decoupling with 0.1µF capacitors right at V_{TERM} pin.
DISC	Enables / disables terminator. See Power Down Function Table for logic levels per device.
GND	Terminator ground pin. Connect to ground.
DIFFB	Used to detect the SCSI BUS mode (LVD, HVD, SE). Should be connected to 4.7µF to ground and 50k Ohm resistor to DIFFSENSE pin (See Figure 3).
DIFFSENSE	Differential sense pin connected to system DIFFSENSE line.

APPLICATION SCHEMATIC

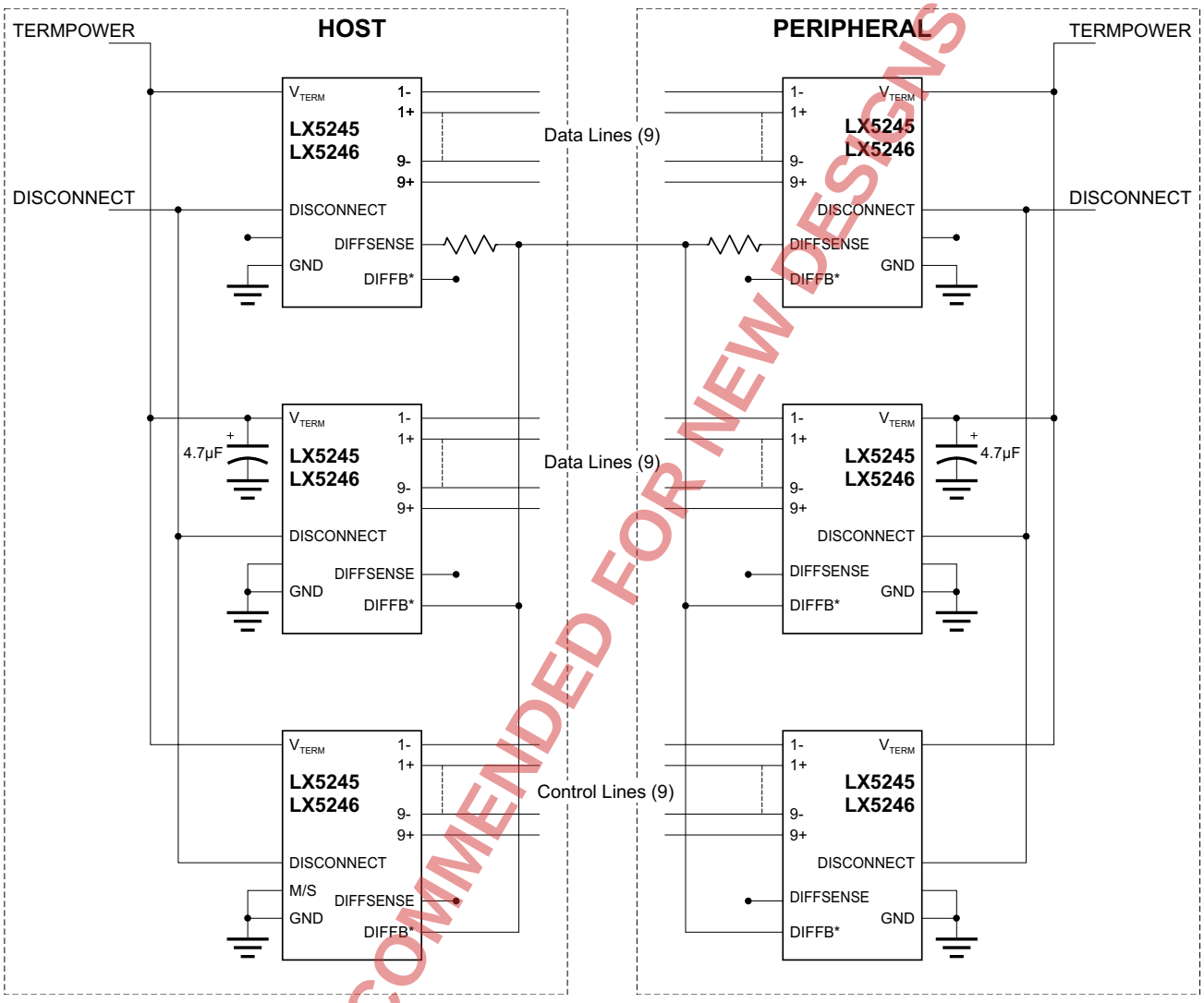
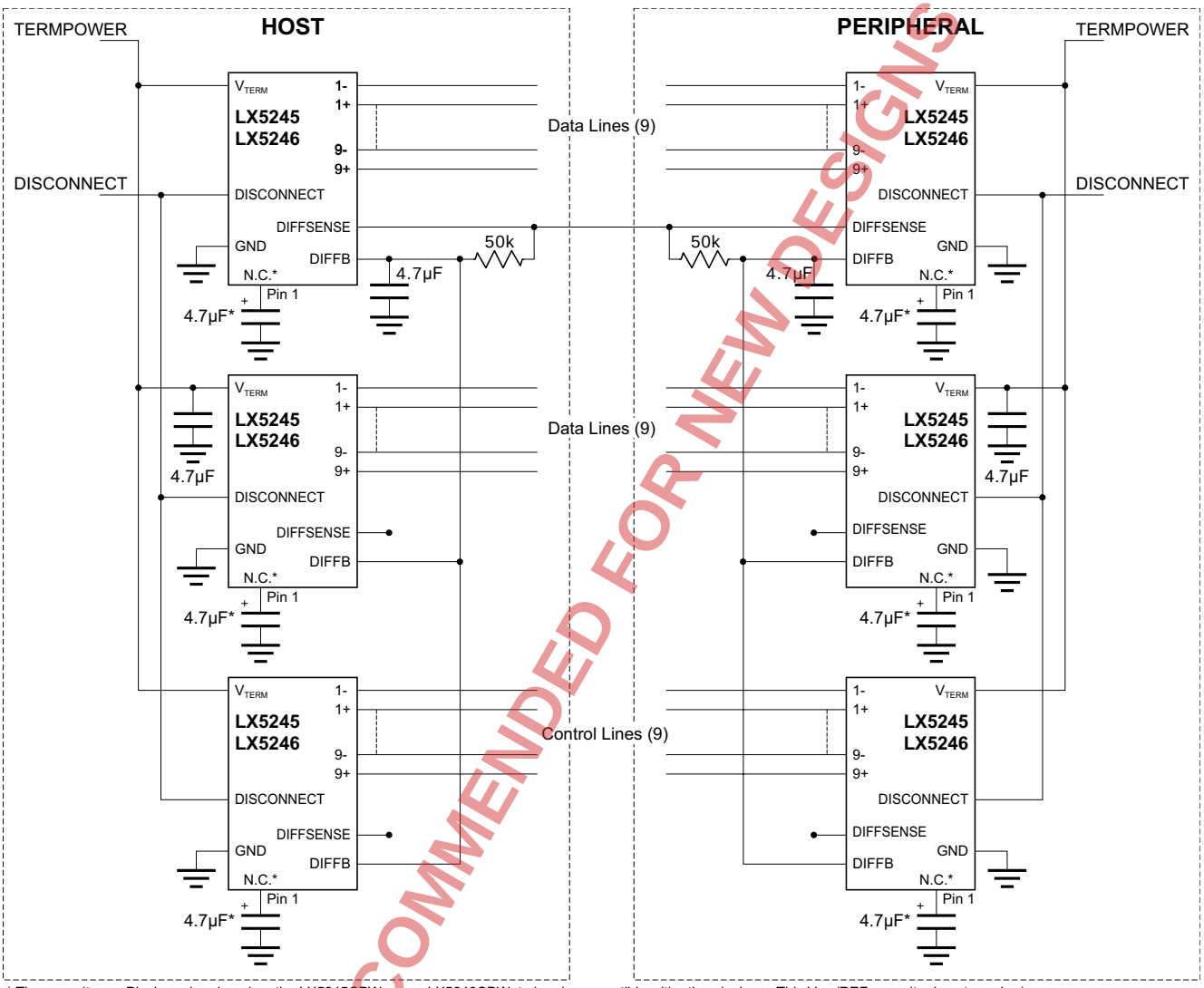


FIGURE 2 — Linfinity ONLY Application Schematic

APPLICATION SCHEMATIC



* The capacitor on Pin 1 can be placed on the LX5245CPW or LX5246CPW to be pin-compatible with other devices. This V_{REQ}/REF capacitor is not required.

FIGURE 3 — Suggested Linfinity LX5245/5246 Universal Application Schematic
(Please Reference Manufacturer's Current Data Sheet To Ensure Compatibility)