# CCD

## LINEAR IMAGE SENSORS

A typical linear image sensor is composed of a row of image sensing elements (photosites), two analog transport registers, and an output amplifier *(Figure 1)*. Light energy falls on the photosites and generates charge packets proportional to the light intensity. These charge packets are then transferred in parallel to two analog transport registers, which are clocked by 2-phase clocks. The packets are next delivered to an on-chip output amplifier where they are converted to proportional voltage levels. A series of pulses, amplitude modulated with the optical information, appear at the output.

*Table 1* summarizes the features of the CCD110F 256-element, CCD131 1024-element and CCD121H 1728-element linear image sensors. The CCD110F and CCD121H have similar cell size and number of output amplifiers. The CCD131 has two separate output amplifiers, one for each 512-stage analog transport register, which permit higher total output data rate. The linear image sensors are packaged in hermetically sealed ceramic packages with a high quality optical glass window.

Linear sensors find applications ranging from simple optical character recognition (OCR) using the 256 x 1 device to high speed facsimile sensing using the 1728 x 1. The precise location of the photosites on the sensors allows the device to be used in high precision non-contact measurement applications such as dimensional measurements of objects, shape recognition and sorting, defect detection and so on. The three linear sensors have the same sensing element center-to-center spacing; selection is determined by the user's resolution requirement.

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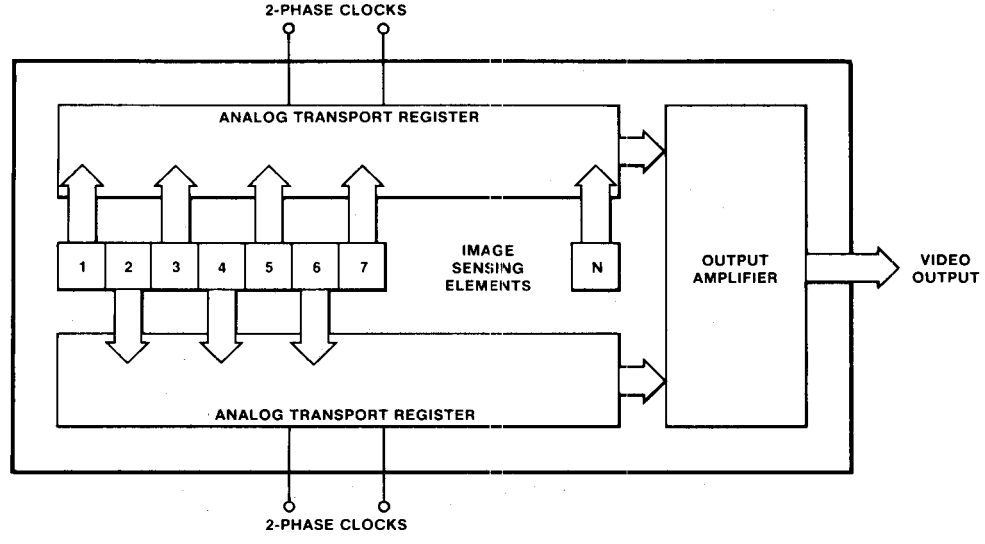


**Fig. 1. Typical Block Diagram for a Linear Image Sensor**

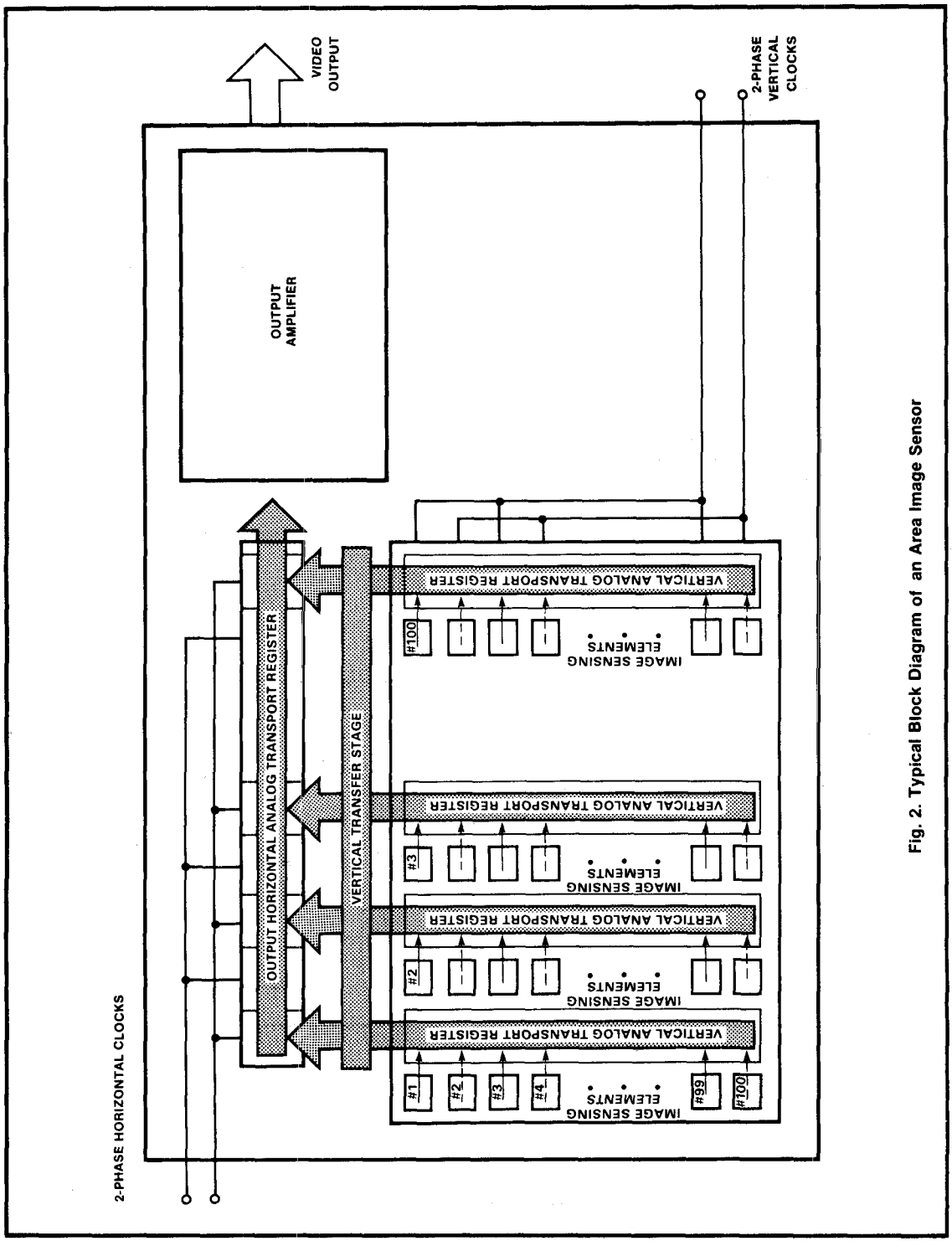


Fig. 2. Typical Block Diagram of an Area Image Sensor

| PARAMETERS | CCD110F | CCD131 | CCD121H |
|---|---|---|---|
| Number of Elements | 256 | 1024 | 1728 |
| Dynamic Range | 500:1 | 500:1 | 500:1 |
| Number of Output Amplifiers | 1 | 2 | 1 |
| Package Type | Non-Herrnetic | Hermetic | Hermetic |
| Number of Pins | 18 | 24 | 24 |
| Saturation Exposure | 1.0 $\mu J/cm^2$ | 1.0 $\mu J/cm^2$ | 1.0 $\mu J/cm^2$ |
| Saturation Output Voltage | 150 mV | 750 mV | 750 mV |
| Photo Element Dimensions | 13 $\mu$ X 17 $\mu$ | 13 $\mu$ X 13 $\mu$ | 13 $\mu$ X 17 $\mu$ |
| Video Data Rate | 10 MHz | 24 MHz | 10 MHz |
| Design Development Board | **CCD110FB** | **CCD131DB** | **CCD121HB** |

**Table 1. Linear Image Sensors**

| PARAMETERS | CCD202 | CCD211 |
|---|---|---|
| Number of Elements | 100 X 100 | 244 X 190 |
| Dynamic Range | 300:1 | 300:1 |
| Package Type | Hermetic | Hermetic |
| Number of Pins | 24 | 24 |
| Saturation Exposure | 0.4 $\mu J/cm^2$ | 0.2 $\mu J/cm^2$ |
| Saturation Output Voltage | 1,600 mV | 200 mV |
| Photoelements Dimensions | 18 $\mu$m X 30 $\mu$m | 14 $\mu$m X 18 $\mu$m |
| Video Data Rate | 2 MHz | 7 MHz |
| Design Development Boards | **CCD202DB** | — |

**Table 2. Area Image Sensors**

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## AREA IMAGE SENSORS

Area arrays are similar to the linear sensors except that the photosites are arranged in a matrix format and the opaque transport registers are located between the photosite columns *(Figure 2)*. The charge packets are transferred to the output amplifier in two separate fields, line by line. This technique is called the interline transfer approach.

*Table 2* summarizes the features of the CCD202 100 x 100 element and CCD211 244 x 190 element devices. The x-y format of the area sensors was selected to provide a 4 x 3 image aspect ratio. The highly precise location of the photosites allows precise identification of each component of the image signal, an important feature for applications requiring exact dimensional measurements. The devices are also well suited for use in video cameras that require low power, small size, high sensitivity and high reliability. Both devices are packaged in a hermetically sealed package with a high quality optical glass window.

## ANALOG SHIFT REGISTERS

The capability to manipulate information in the form of charge packets makes CCD technology ideal for analog signal processing. In a CCD analog shift register, electrical inputs are applied to the charge-injection port which samples the input signal at a rate determined by the input signal bandwidth.

This signal is then transformed into a charge packet and injected into the register. The clocks shift the charge packet through the register to the output amplifier for conversion to an output signal voltage. A filtering or sample-and-hold technique is usually required to recover the analog information. The time delay between the input and output signals is equal to the number of elements in the CCD register (N) divided by the clock rate frequency. Since N is fixed, varying the clock rate provides a variable delay that makes the CCD shift register a powerful device for applications requiring highly precise delay of analog information.

## DESIGN DEVELOPMENT BOARDS AND MODULES

Fairchild offers a series of printed circuit boards for use as construction aids for experimental systems using CCD linear and area image sensors. These design development boards are fully assembled and tested, and require only power supplies and an oscilloscope to display the video information corresponding to the image positioned in front of the sensor. A typical board *(Figure 4)* includes an on-board variable-frequency clock generator that can be overrun by an external input, logic circuitry for timing drive signals, drivers to interface the TTL logic to CCD levels, a socket for mounting the device at 90° on the edge of the board, video buffer circuits and simple video processing electronics. Design development boards are available for the CCD110F, CCD131, CCD121H and the CCD202.

To operate the board, supply +5 V, +15 V and -15 V through a 22-pin standard edge connector to the pc board. Video information, typically 1.0 V peak-to-peak, as well as synchronization pulses are supplied to the connector for display on an oscilloscope. The CCD202 board also includes sweep waveform generators for driving an x-y monitor.

In addition, Fairchild offers the CCD321VM video delay module which includes the CCD321A-2 analog shift register plus driver electronics package with VCO, drivers, device socket, video amplifiers and filters. A 1.0 V peak-to-peak input comes out 1.0 V peak-to-peak, delayed by 455 or 910 divided by the clock frequency. The CCD321VM module is capable of storing a full video line (1H) at a 14.3 MHz clock rate with a 58 dB signal-to-noise ratio and excellent linearity. Assembled and thoroughly tested, the module requires only a single power supply. Also available is the CCD321AM audio module which includes the CCD321A-4 plus driver package and processing electronics.

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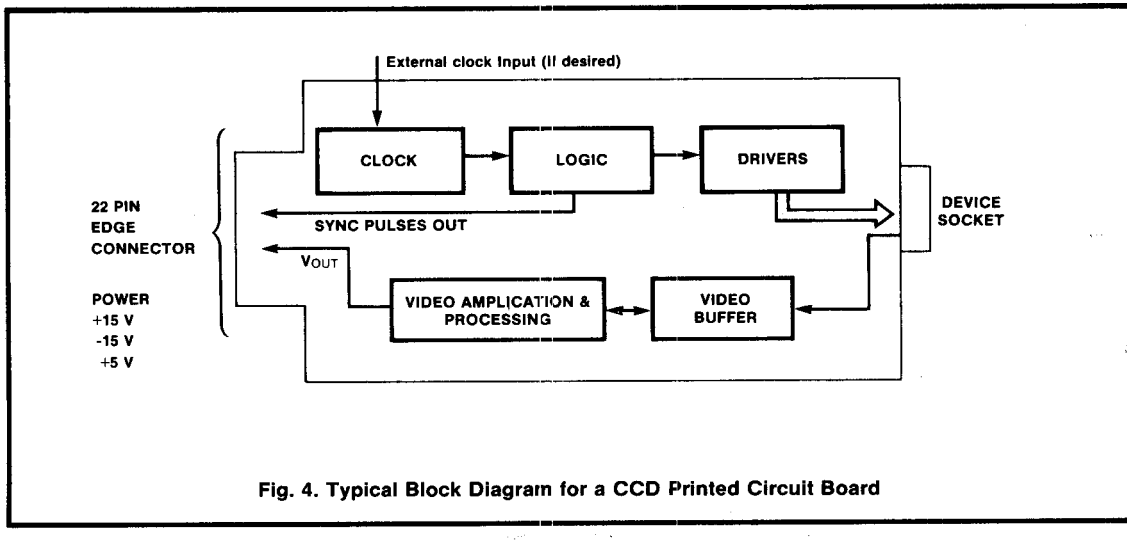


**Fig. 4. Typical Block Diagram for a CCD Printed Circuit Board**

## LINE-SCAN CAMERA SUBSYSTEMS

There are presently three models of the line-scan camera sub-systems—the 256-element CCD1100, the 1024-element CCD1300 and the 1728-element CCD1400. The choice among them is determined primarily by resolution requirements, since each camera model offers essentially equivalent performance in other respects. The line-scan camera can be ordered with a C-mount lens with a focal length to meet the specific application.

Each camera subsystem includes a line-scan camera, a camera-control unit and interconnecting cables. Within the camera is a CCD image sensor, a logic board to provide clock signals for controlling sensor operation, and a video processing assembly to generate an analog-video and a binary-video output signal. The analog-video signal is a continuous analog representation of the spacial distribution of image brightness, obtained by sample-and-hold processing of the raw sensor output. The binary-video output, provided by a comparator, is a digital version of the analog video waveform and corresponds to black-to-white and white-to-black transitions of the analog-video signal across the threshold. The threshold adjustment can be varied across the full dynamic range of the camera.