

## 128K x 8 Static RAM

### Features

- High speed  
—  $t_{AA} = 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  options
- Functionally equivalent to CY7C1019

### Functional Description

The CY7C1019BN is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ), an active LOW Output Enable ( $\overline{\text{OE}}$ ), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

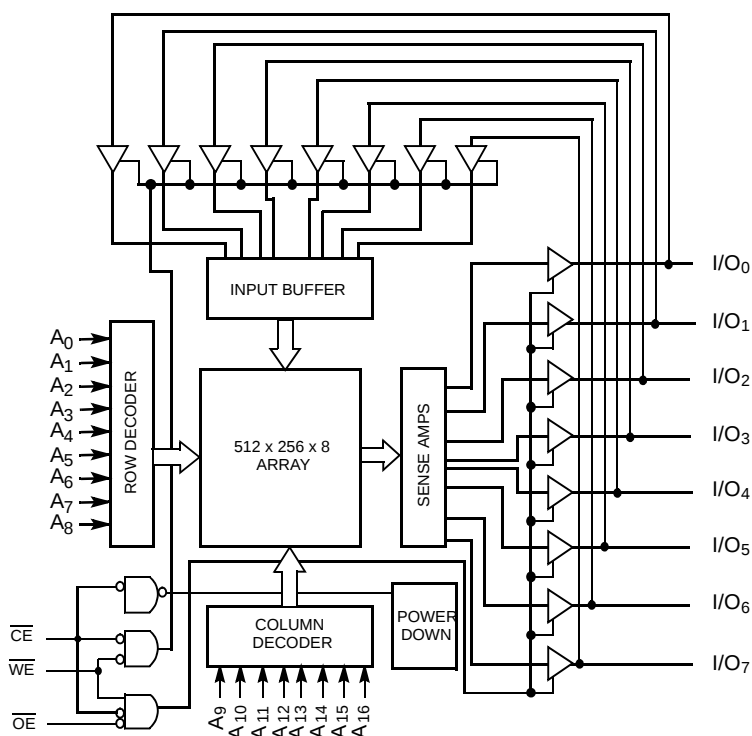
Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1019BN is available in standard 32-pin TSOP Type II and 400-mil-wide SOJ packages.

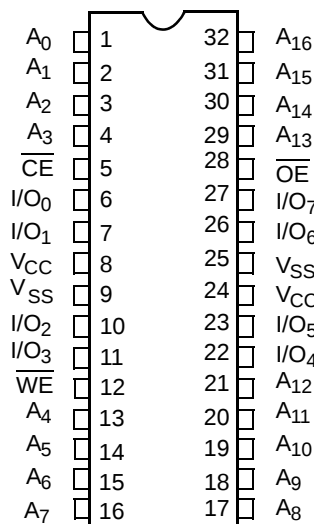
### Logic Block Diagram



### Pin Configurations

#### SOJ / TSOP II

#### Top View



## Selection Guide

|                           |   | 7C1019BN-12 | 7C1019BN-15 | Unit |
|---------------------------|---|-------------|-------------|------|
| Maximum Access Time       |   | 12          | 15          | ns   |
| Maximum Operating Current |   | 140         | 130         | mA   |
| Maximum Standby Current   |   | 10          | 10          | mA   |
|                           | L | 1           | 1           | mA   |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature <sup>[2]</sup> | $V_{CC}$ |
|------------|------------------------------------|----------|
| Commercial | 0°C to +70°C                       | 5V ± 10% |
| Industrial | -40°C to +85°C                     | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description                                  | Test Conditions                                                                                                             | -12  |                | -15  |                | Unit |
|-----------|----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------|----------------|------|----------------|------|
|           |                                              |                                                                                                                             | Min. | Max.           | Min. | Max.           |      |
| $V_{OH}$  | Output HIGH Voltage                          | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$                                                                            | 2.4  |                | 2.4  |                | V    |
| $V_{OL}$  | Output LOW Voltage                           | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$                                                                             |      | 0.4            |      | 0.4            | V    |
| $V_{IH}$  | Input HIGH Voltage                           |                                                                                                                             | 2.2  | $V_{CC} + 0.3$ | 2.2  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW Voltage <sup>[1]</sup>             |                                                                                                                             | -0.3 | 0.8            | -0.3 | 0.8            | V    |
| $I_{IX}$  | Input Leakage Current                        | $GND \leq V_I \leq V_{CC}$                                                                                                  | -1   | +1             | -1   | +1             | μA   |
| $I_{OZ}$  | Output Leakage Current                       | $GND \leq V_I \leq V_{CC}$ ,<br>Output Disabled                                                                             | -5   | +5             | -5   | +5             | μA   |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current            | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}$ ,<br>$f = f_{MAX} = 1/t_{RC}$                                                |      | 140            |      | 130            | mA   |
| $I_{SB1}$ | Automatic CE Power-Down Current —TTL Inputs  | Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$<br>$V_{IN} \geq V_{IH}$ or<br>$V_{IN} \leq V_{IL}$ , $f = f_{MAX}$              |      | 40             |      | 40             | mA   |
|           |                                              | L                                                                                                                           |      | 20             |      | 20             |      |
| $I_{SB2}$ | Automatic CE Power-Down Current —CMOS Inputs | Max. $V_{CC}$ ,<br>$\overline{CE} \geq V_{CC} - 0.3V$ ,<br>$V_{IN} \geq V_{CC} - 0.3V$ ,<br>or $V_{IN} \leq 0.3V$ , $f = 0$ |      | 10             |      | 10             | mA   |
|           |                                              | L                                                                                                                           |      | 1              |      | 1              |      |

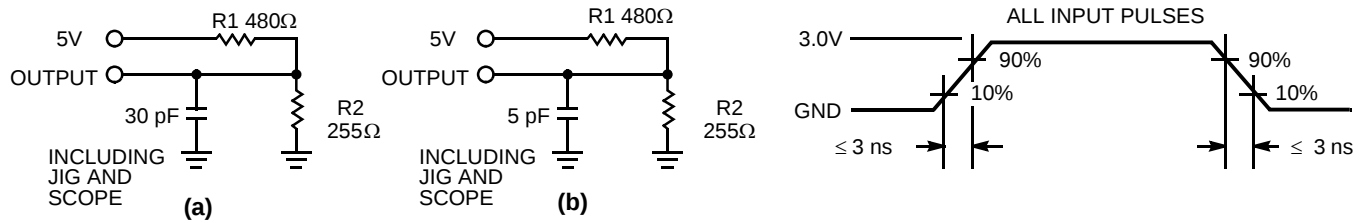
## Capacitance<sup>[3]</sup>

| Parameter | Description        | Test Conditions                                                     | Max. | Unit |
|-----------|--------------------|---------------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ ,<br>$V_{CC} = 5.0V$ | 6    | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                     | 8    | pF   |

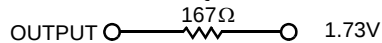
### Notes:

1.  $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
2.  $T_A$  is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics<sup>[4]</sup> Over the Operating Range

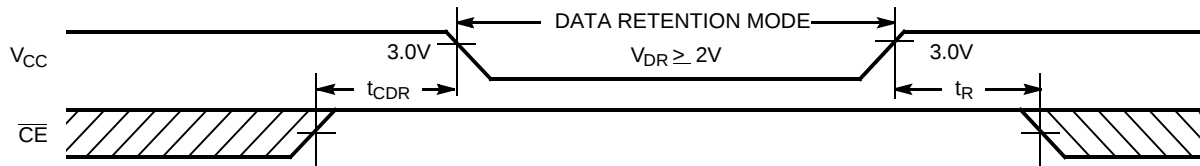
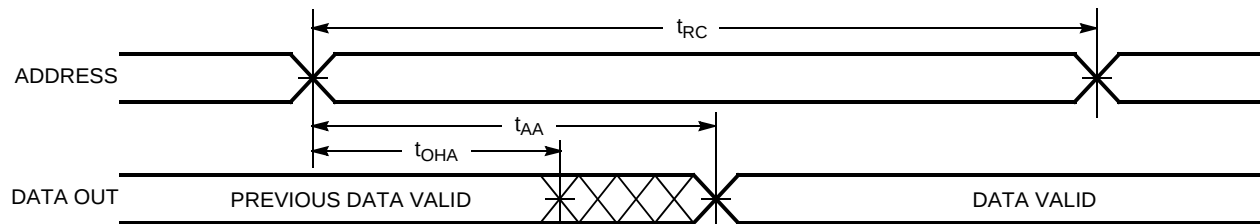
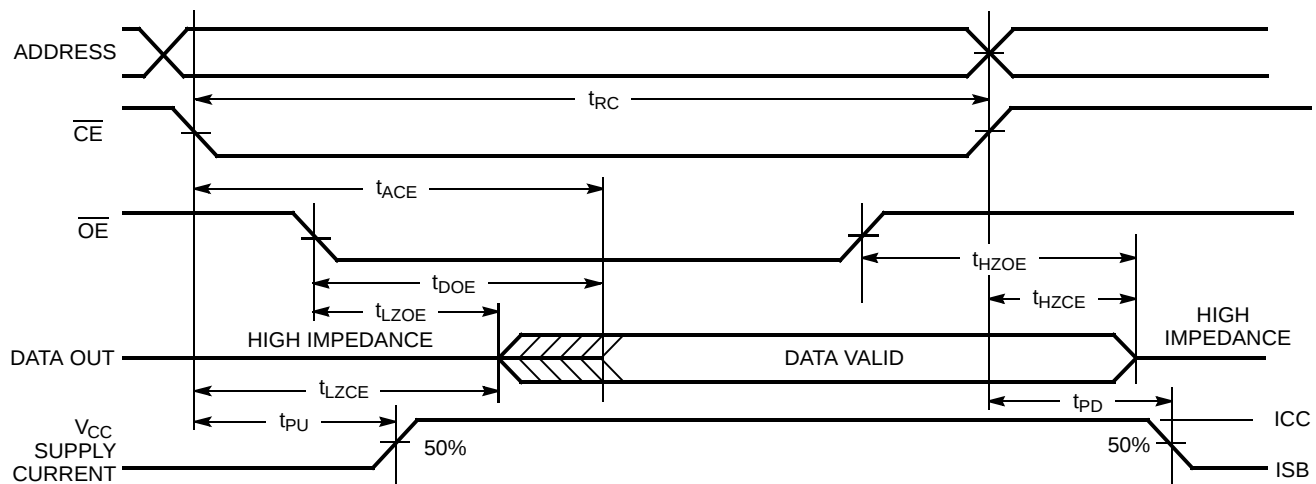
| Parameter                     | Description                                      | -12  |      | -15  |      | Unit |
|-------------------------------|--------------------------------------------------|------|------|------|------|------|
|                               |                                                  | Min. | Max. | Min. | Max. |      |
| Read Cycle                    |                                                  |      |      |      |      |      |
| t <sub>RC</sub>               | Read Cycle Time                                  | 12   |      | 15   |      | ns   |
| t <sub>AA</sub>               | Address to Data Valid                            |      | 12   |      | 15   | ns   |
| t <sub>OHA</sub>              | Data Hold from Address Change                    | 3    |      | 3    |      | ns   |
| t <sub>ACE</sub>              | $\overline{CE}$ LOW to Data Valid                |      | 12   |      | 15   | ns   |
| t <sub>DOE</sub>              | $\overline{OE}$ LOW to Data Valid                |      | 6    |      | 7    | ns   |
| t <sub>LZOE</sub>             | $\overline{OE}$ LOW to Low Z                     | 0    |      | 0    |      | ns   |
| t <sub>HZOE</sub>             | $\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup> |      | 6    |      | 7    | ns   |
| t <sub>LZCE</sub>             | $\overline{CE}$ LOW to Low Z <sup>[6]</sup>      | 3    |      | 3    |      | ns   |
| t <sub>HZCE</sub>             | $\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup> |      | 6    |      | 7    | ns   |
| t <sub>PU</sub>               | $\overline{CE}$ LOW to Power-Up                  | 0    |      | 0    |      | ns   |
| t <sub>PD</sub>               | $\overline{CE}$ HIGH to Power-Down               |      | 12   |      | 15   | ns   |
| Write Cycle <sup>[7, 8]</sup> |                                                  |      |      |      |      |      |
| t <sub>WC</sub>               | Write Cycle Time                                 | 12   |      | 15   |      | ns   |
| t <sub>SCE</sub>              | $\overline{CE}$ LOW to Write End                 | 9    |      | 10   |      | ns   |
| t <sub>AW</sub>               | Address Set-Up to Write End                      | 8    |      | 10   |      | ns   |
| t <sub>HA</sub>               | Address Hold from Write End                      | 0    |      | 0    |      | ns   |
| t <sub>SA</sub>               | Address Set-Up to Write Start                    | 0    |      | 0    |      | ns   |
| t <sub>PWE</sub>              | $\overline{WE}$ Pulse Width                      | 8    |      | 10   |      | ns   |
| t <sub>SD</sub>               | Data Set-Up to Write End                         | 6    |      | 8    |      | ns   |
| t <sub>HD</sub>               | Data Hold from Write End                         | 0    |      | 0    |      | ns   |
| t <sub>LZWE</sub>             | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3    |      | 3    |      | ns   |
| t <sub>HZWE</sub>             | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  |      | 6    |      | 7    | ns   |

### Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range (L Version Only)

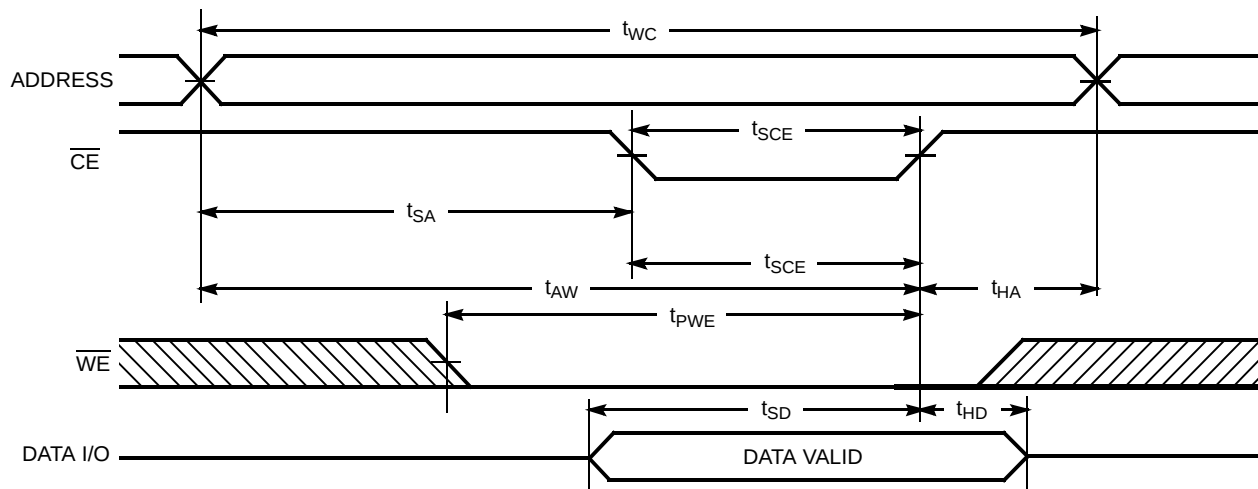
| Parameter       | Description                          | Conditions                                                                                                              | Min. | Max. | Unit    |
|-----------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------|------|------|---------|
| $V_{DR}$        | $V_{CC}$ for Data Retention          | No input may exceed $V_{CC} + 0.5V$                                                                                     | 2.0  |      | V       |
| $I_{CCDR}$      | Data Retention Current               | $V_{CC} = V_{DR} = 2.0V$ ,<br>$\overline{CE} \geq V_{CC} - 0.3V$ ,<br>$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ |      | 300  | $\mu A$ |
| $t_{CDR}^{[3]}$ | Chip Deselect to Data Retention Time |                                                                                                                         | 0    |      | ns      |
| $t_R$           | Operation Recovery Time              |                                                                                                                         | 200  |      | $\mu s$ |

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[9, 10]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>**

**Notes:**

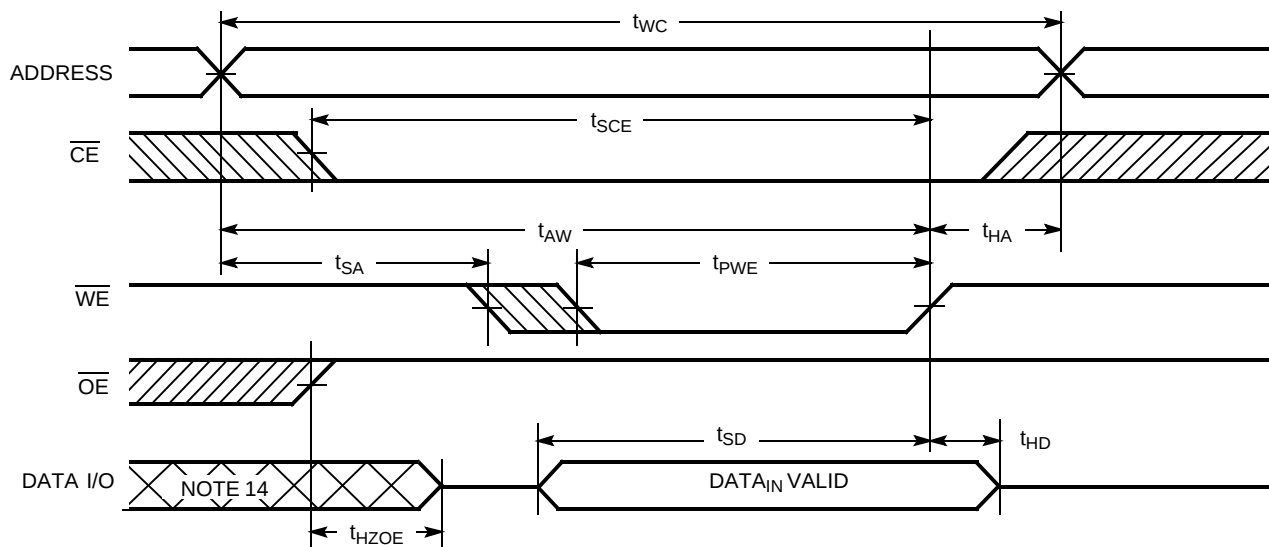
9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
10.  $\overline{WE}$  is HIGH for read cycle.
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 ( $\overline{\text{CE}}$ Controlled)<sup>[12, 13]</sup>

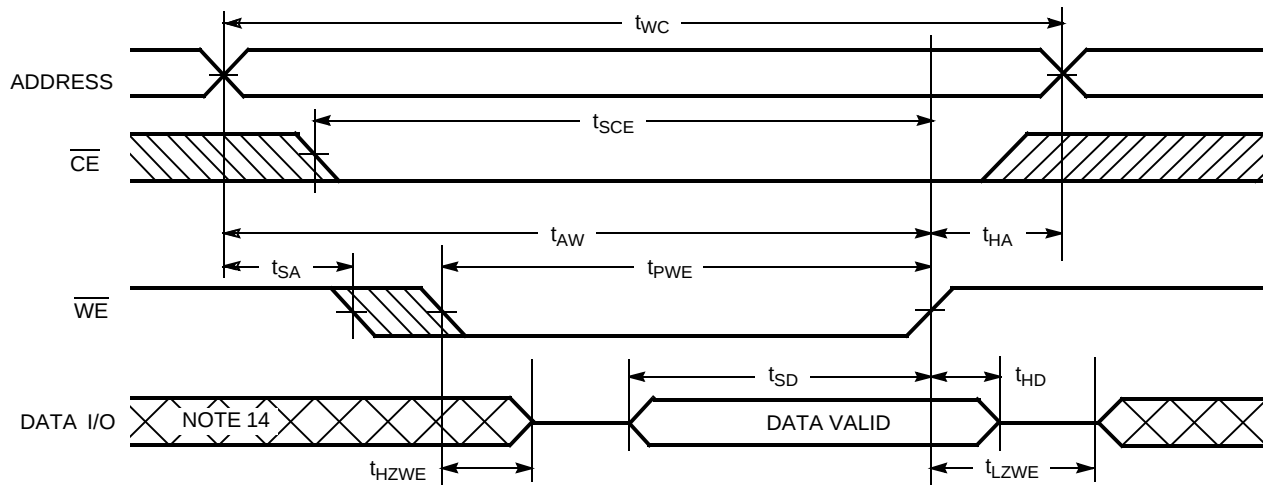


### Write Cycle No. 2 ( $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)<sup>[12, 13]</sup>



#### Notes:

12. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[13]</sup>**

**Truth Table**

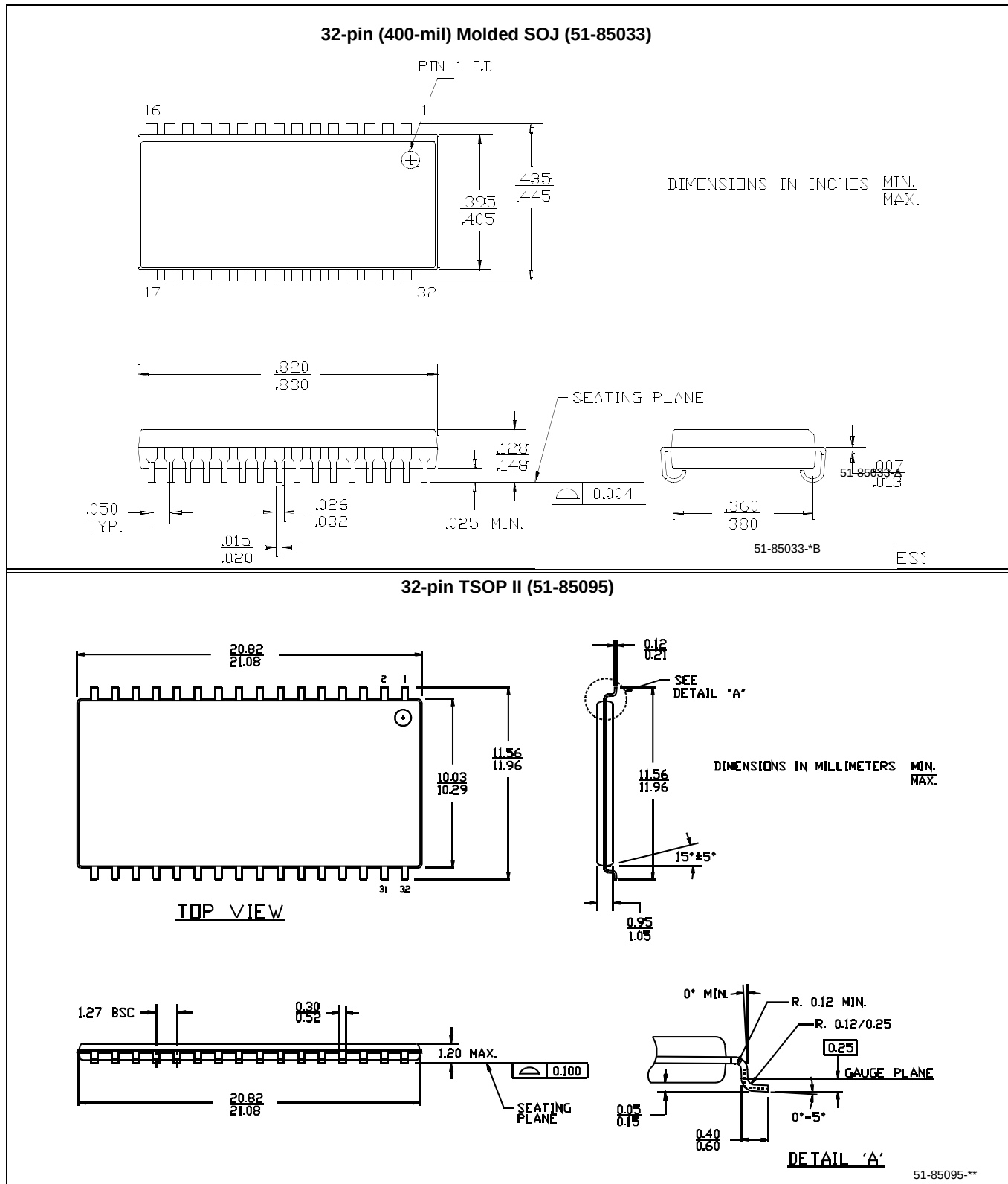
| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O <sub>0</sub> -I/O <sub>7</sub> | Mode                       | Power                |
|-----------------|-----------------|-----------------|------------------------------------|----------------------------|----------------------|
| H               | X               | X               | High Z                             | Power-Down                 | Standby ( $I_{SB}$ ) |
| L               | L               | H               | Data Out                           | Read                       | Active ( $I_{CC}$ )  |
| L               | X               | L               | Data In                            | Write                      | Active ( $I_{CC}$ )  |
| L               | H               | H               | High Z                             | Selected, Outputs Disabled | Active ( $I_{CC}$ )  |

**Ordering Information**

| Speed (ns) | Ordering Code    | Package Diagram | Package Type                   | Operating Range |
|------------|------------------|-----------------|--------------------------------|-----------------|
| 12         | CY7C1019BN-12VC  | 51-85033        | 32-Lead 400-Mil Molded SOJ     | Commercial      |
|            | CY7C1019BN-12ZC  | 51-85095        | 32-Lead TSOP Type II           |                 |
|            | CY7C1019BN-12ZXC | 51-85095        | 32-Lead TSOP Type II (Pb-free) |                 |
| 15         | CY7C1019BN-15VC  | 51-85033        | 32-Lead 400-Mil Molded SOJ     | Commercial      |
|            | CY7C1019BN-15ZXC | 51-85095        | 32-Lead TSOP Type II (Pb-free) |                 |

Please contact local sales representative regarding availability of these parts

## Package Diagrams



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**Document History Page**

| <b>Document Title: CY7C1019BN 128K x 8 Static RAM</b><br><b>Document Number: 001-06425</b> |                |                   |                        |                              |
|--------------------------------------------------------------------------------------------|----------------|-------------------|------------------------|------------------------------|
| <b>REV.</b>                                                                                | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b> |
| **                                                                                         | 423847         | See ECN           | NXR                    | New Data Sheet               |