32MB EDO-SIMM

PN :
SAE00832E2AF2OK-60R

32MB EDO RAM in SOJ Technique
RoHS compliant

Options:

§	Access Time 60ns	Marking -60
§	Module densities 16MB with 8 chips and 1 rank 32MB with 16 chips and 2 ranks	
§	Standard Grade	0°C to 70°C

Features:

- § 72-pin 32-bit SIMM Module
- § EDO RAM component base
  OKI: MSM5117405F-60J3
- § V_{DD} = 5V ±0.5V
- § Standard access time: 60ns
- § Extended Data Output (EDO)
- § /CAS Before /RAS Refresh (CBR), /RAS Only Refresh,
  and Hidden Refresh capability
- § Double-sided module
- § 2K Refresh cycle
- § Low active and stand-by current consumption
- § Decoupling capacitors at each memory device
- § TTL-compatible inputs and outputs
- § 25.4mm (1 inch) height
- § Tin card edge fingers

Environmental Requirements:

- § Operating temperature (ambient)
  Standard Grade 0°C to 70°C
- § Operating Humidity
  10% to 90% relative humidity, noncondensing
- § Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- § Storage Temperature
  -55°C to 150°C
- § Storage Humidity
  5% to 95% relative humidity, noncondensing
- § Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

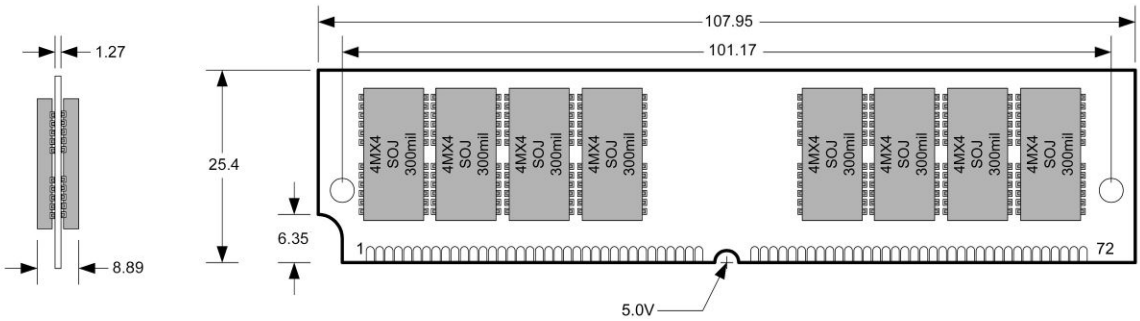


Figure1: mechanical dimensions

This Swissbit module is an industry standard 72-pin 8-byte SIMM Memory Module which is organized as x32 high speed CMOS memory arrays.
The module achieves high integration, high-speed operation, and low-power consumption.

The SIMM is assembled in SOJ Technology.

Module Configuration

Organization	SDRAMs used	Refresh	Addr.
8M x 32bit	16 x 4M x 4bit	2k	10

Module Dimensions in mm
107.95 (long) x 25.4 (high) x 8.90 [max] (thickness)

Timing Parameters

Part Number	Chip vendor	Module Density	Access Time
SAE00832E2AF2OK-60R	OKI	32 MB	60ns

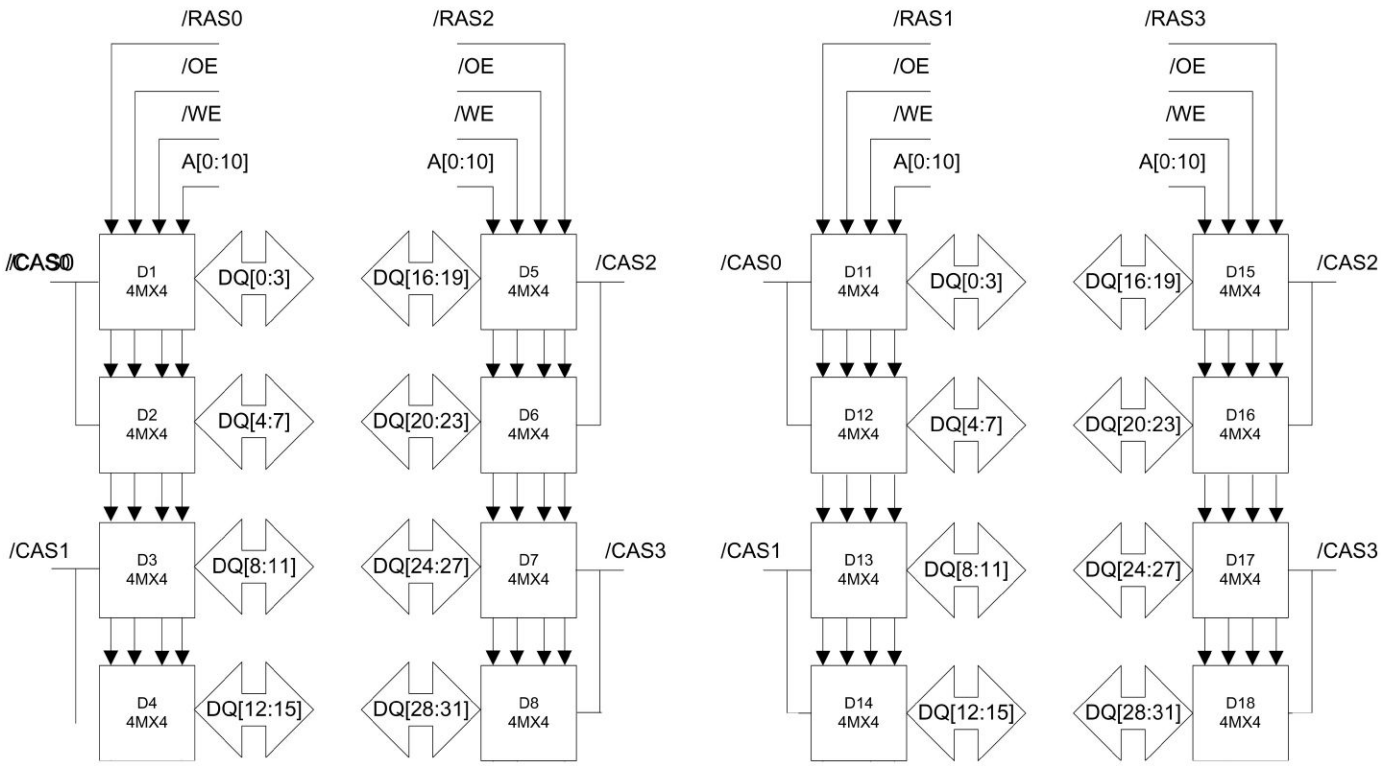
Pin Name

A0-A10	Address Inputs
DQ0 – DQ31	Data Input / Output
/RAS0 - /RAS3	Row Address Strobe
/CAS0 - /CAS3	Column Address Strobe
/WE	Write Enable
PB1 – PB4	Parity
PD1 – PD4	Present Detect
V_{DD}	Supply Voltage (5V± 0.5V)
V_{SS}	Ground
NC	No Connection

Pin Configuration

PIN #	Description	PIN #	Description	PIN #	Description	PIN #	Description
1	VSS	19	A10	37	PB1 | NC	55	DQ11
2	DQ0	20	DQ4	38	PB3 | NC	56	DQ27
3	DQ16	21	DQ20	39	VSS	57	DQ12
4	DQ16	22	DQ5	40	/CAS0	58	DQ28
5	DQ17	23	DQ21	41	/CAS2	59	VDD
6	DQ2	24	DQ6	42	/CAS3	60	DQ29
7	DQ18	25	DQ22	43	/CAS1	61	QD13
8	DQ3	26	DQ7	44	/RAS0	62	DQ30
9	DQ19	27	DQ23	45	/RAS1	63	DQ14
10	VDD	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	/WE	65	DQ15
12	A0	30	VDD	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	/RAS3	51	DQ9	69	PD3
16	A4	34	/RAS2	52	DQ25	70	PD4
17	A5	35	PB2 | NC	53	DQ10	71	NC
18	A6	36	PB0 | NC	54	DQ26	72	VSS

FUNCTIONAL BLOCK DIAGRAMM 32MB EDO RAM SIMM, 16 COMPONENTS



NOTE
/OE is tied directly to ground

Absolute Maximum Ratings*

Item		Symbol	Rating	Unit
Voltage on any pin relative to Vss		V_{IN}, V_{OUT}	-1 – 7	V
Storage Temperature		t_{STG}	-55 - +150	°C
Short Circuit Output Current		I_{OS}	50	mA
Power Dissipation	8MX36	P_D	20	W

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS** (T_A = 0 to 70 OC)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{DD}+1.0	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

** All voltages are referenced to Vss

DC AND OPERATING CHARACTERISTICS+

Item	Condition	Symbol	Refresh Rate 2k		Unit
			Min	Max	
Average Power Supply Current (Operating)	/RAS, /CAS cycling, t_{RC} = min	I_{CC1}*	-	760	mA
Power Supply Current (Standby)	/RAS, /CAS = V_{IH}	I_{CC2}	-	16	mA
	/RAS, /CAS ≥ V_{CC} - 0,2V		-	8	
Average Power Supply Current (/RAS Only Refresh)	/CAS = V_{IH} /RAS Cycling t_{RC} = min	I_{CC3}*	-	760	mA
Power Supply Current (Standby)	/RAS = V_{IH} /CAS = V_{IL} DQ 0 enable	I_{CC5}	-	40	mA
Average Power Supply Current (/CAS Before /RAS Refresh)	/RAS cycling /CAS Before /RAS	I_{CC6}*	-	760	mA
Power Supply Current (Fast Page Mode)	/RAS = V_{IL} /CAS Cycling t_{HPC} = min	I_{CC7}*	-	760	mA
Input Leakage Current	0 < V_{IN} < 6.5 V all other Pins not under test	I_{L1}	-80	80	µA
Output Leakage Current	Data out is disabled, 0 < V_{OUT} < 5.5V	I_{L0}	-10	10	µA
Output High Voltage Level	I_{OH} = -5mA	V_{OH}	2.4	V_{CC}	V
Output Low Voltage Level	I_{OL} = 4.2mA	V_{OL}	0	0.4	V

+ I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.
*one bank in standby (I_{CC5})

Capacitance (T_A=25°C)

Item	Config	Symbol	Min	Max	Unit
Input Capacitance [A0 – A10]	8MX36	C_{IN1}	-	80	pF
Input Capacitance [/WE]	8MX36	C_{IN2}	-	112	pF
Input Capacitance [/RAS0 - /RAS3]	8MX36	C_{IN3}	-	28	pF
Input Capacitance [/CAS0 - /CAS3]	8MX36	C_{IN4}	-	28	pF
Output Capacitance [/WE]	8MX36	C_{DQ}	-	14	pF

AC Characteristics (T_A=0-70°C, V_{CC}=5V+/-0,5V)

Standard Operation	Symbol	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	104	-	ns	
Read-modify-write cycle time	t_{RWC}	135	-	ns	
Access time from /RAS	t_{RAC}	-	60	ns	4,5,6
Access time from /CAS	t_{CAC}	-	15	ns	4,5
Access time from column address	t_{AA}	-	30	ns	4,6
/CAS to output in low-Z	t_{CLZ}	0	-	ns	4
Output buffer turn-off delay from /CAS	t_{CEZ}	0	15	ns	7,8
Transition time (rise and fall)	t_T	1	50	ns	3
/RAS precharge time	t_{RP}	40	-	ns	
/RAS pulse width	t_{RAS}	60	10 000	ns	
/RAS hold time	t_{RSH}	10	-	ns	
/CAS hold time	t_{CSH}	40	-	ns	
/CAS pulse width	t_{CAS}	10	10 000	ns	
/RAS to /CAS delay time	t_{RCD}	14	45	ns	5
/RAS to column address delay time	t_{RAD}	12	30	ns	6
/CAS to /RAS precharge	t_{CRP}	5	-	ns	
Row address setup time	t_{ASR}	0	-	ns	
Row address hold time	t_{RAH}	10	-	ns	
Column address setup time	t_{ASC}	0	-	ns	
Column address hold time	t_{CAH}	10	-	ns	
Column address to /RAS lead time	t_{RAL}	30	-	ns	
Read command set-up time	t_{RSC}	0	-	ns	
Read command hold time referenced to /CAS	t_{RCH}	0	-	ns	9
Read command hold time referenced to /RAS	t_{RRH}	0	-	ns	9
Write command hold time	t_{WCH}	10	-	ns	
Write command pulse width	t_{WP}	10	-	ns	
Write command to /RAS lead time	t_{RWL}	10	-	ns	
Write command to /CAS lead time	t_{CWL}	10	-	ns	
Data setup time	t_{DS}	0	-	ns	11
Data hold time	t_{DH}	10	-	ns	11
Refresh period	t_{REF}	-	32	ms	
Write command setup time	t_{WCS}	0	-	ns	10
/CAS to /W delay time	t_{CWD}	34	-	ns	10
/RAS to /W delay time	t_{RWD}	79	-	ns	10
Column address to /W delay time	t_{AWD}	49	-	ns	10
/CAS precharge to /W delay time	t_{CPWD}	54	-	ns	10
/CAS setup time (CBR Refresh)	t_{CSR}	5	-	ns	
/CAS hold time (CBR Refresh)	t_{CHR}	10	-	ns	
/RAS to /CAS precharge time	t_{RPC}	5	-	ns	
/RAS hold time reference to /OE	t_{ROH}	10	-	ns	
Access time from /CAS precharge	t_{CPA}	-	35	ns	4
EDO mode cycle time	t_{HPC}	25	-	ns	
EDO mode read-modify-write cycle time	t_{PRWC}	68	-	ns	
/CAS precharge time (EDO cycle)	t_{CP}	10	-	ns	
/RAS pulsewidth (EDO cycle)	t_{RASP}	60	100 000	ns	
/RAS holdtime from /CAS precharge	t_{RHCP}	35	-	ns	
/OE access time	t_{OEA}	-	15	ns	
/OE command hold time	t_{OEH}	10	-	ns	
Output buffer turn off delay time from /OE	t_{OEZ}	0	15	ns	7
/OE command hold time	t_{OCH}	10	-	ns	

Standard Operation	Symbol	Min	Max	Unit	Notes
Output data hold time	t_{DOH}	5	-	ns	
Output buffer turn off delay from /RAS	t_{REZ}	0	15	ns	7,8
Output buffer turn off delay from /W	t_{WEZ}	0	15	ns	7
/OE to data-in delay time	t_{OED}	15	-	ns	
/OE hold time to /CAS (DQ disable)	t_{CHO}	5	-	ns	
/OE to data-in delay time	t_{OED}	15	-	ns	
/OE precharge time	t_{OEP}	10	-	ns	
/W pulse width (EDO cycle)	t_{WPE}	10	-	ns	
/W to /RAS precharge time (/CAS before /RAS)	t_{WRP}	10	-	ns	
/W hold time /RAS (/CAS before /RAS)	t_{WRH}	10	-	ns	

NOTES:

1. A start-up delay of 200µs is required after power-up, followed by a minimum of eight initialization cycles (/RAS-only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T=2 ns.
3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring input timing signals. Transition time (t_T) are measured bet/WEen V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the t_{RCD}(Max.) limit ensures that t_{RAC}(Max.) can be met. t_{RCD} (Max.) is specified as a reference point only . If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only . If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.
7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition .
9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only . If $t_{WCS} \geq t_{WCS}$(Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(Min.), $t_{RWD} \geq t_{RWD}$(Min.) , $t_{AWD} \geq t_{AWD}$(Min.) and $t_{CPWD} \geq t_{CPWD}$(Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to /CAS leading edge in an early write cycle, and to /WE leading edge in an /OE control write cycle or a read modify write cycle .
12. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 8-bit locations .Since all 4 DQ pins are used, a total of 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal the DQ pin will indicate a high level. If the 8 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a /RAS-only refresh cycle or a /CAS before /RAS refresh cycle.
13. In a test mode read cycle , the value of access time parameters is delayed for 5 ns for the specified value . These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

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