

DATA SHEET

74F166

8-bit bidirectional universal shift register

Product specification

1991 Feb 14

IC15 Data Handbook

8-bit bidirectional universal shift register

74F166

FEATURES

- High impedance NPN base inputs for reduced loading (20µA in high and low states)
- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- Expandable to 16 bits in 8-bit increments
- Industrial temperature range available (−40°C to +85°C)

DESCRIPTION

The 74F166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active low parallel enable ($\overline{PE}$) input. When the $\overline{PE}$ is low one setup time before the low-to-high clock transition, parallel data is entered into the register.

When $\overline{PE}$ is high, data is entered into internal bit position Q0 from serial data input (Ds), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2, etc.) with each positive going clock transition.

For expansion of the register in parallel to serial converters, the Q7 output is connected to the Ds input of the succeeding stage. The clock input is gated OR structure which allows one input to be used as an active-low clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The low-to-high transition of $\overline{CE}$ input should only take place while the CP is high for predictable operation. A low on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a low state.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F166	175MHz	50mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
16-pin plastic DIP	N74F166N	I74F166N	SOT38-4
16-pin plastic SO	N74F166D	I74F166D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Parallel data inputs	1.0/0.033	20µA/20µA
Ds	Serial data input (shift right)	2.0/0.066	40µA/40µA
CP	Clock input (active rising edge)	1.0/0.033	20µA/20µA
$\overline{CE}$	Clock enable input (active low)	1.0/0.033	20µA/20µA
$\overline{PE}$	Parallel enable input (active low)	1.0/0.033	20µA/20µA
$\overline{MR}$	Master reset input (active low)	2.0/0.066	40µA/40µA
Q7	Data output	50/33	1.0mA/20mA

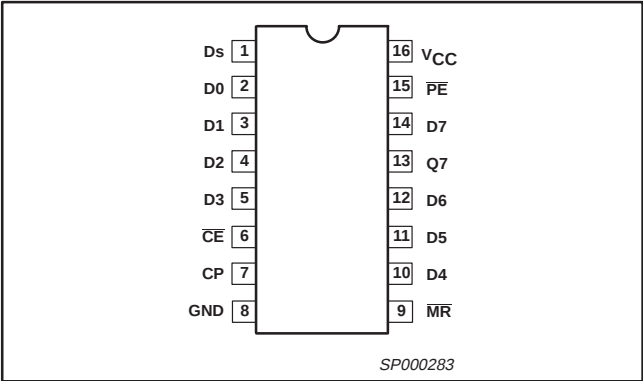
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

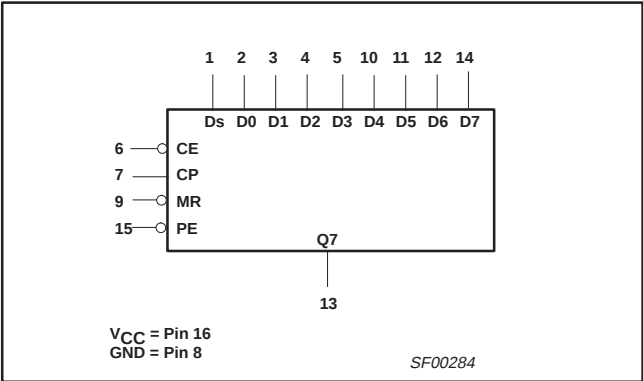
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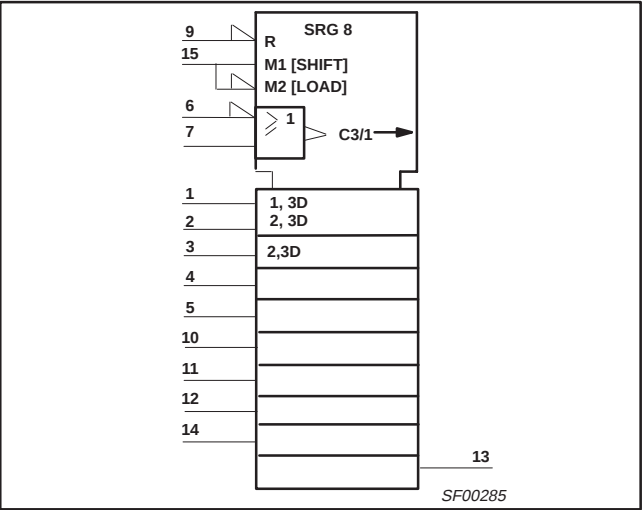
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



FUNCTION TABLE

INPUTS					Qn REGISTER		OUTPUT	OPERATING MODE
PE	CE	CP	DS	D0 – D7	Q0	Q1 – Q6	Q7	
L	L	↑	X	L – L	L	L – L	L	Parallel load
L	L	↑	X	h – h	H	H – H	H	
h	L	↑	L	X – X	L	q0 – q5	q6	Serial shift
h	L	↑	h	X – X	H	q0 – q5	q6	
X	h	X	X	X – X	qn	q1 – q6	q7	Hold (do nothing)

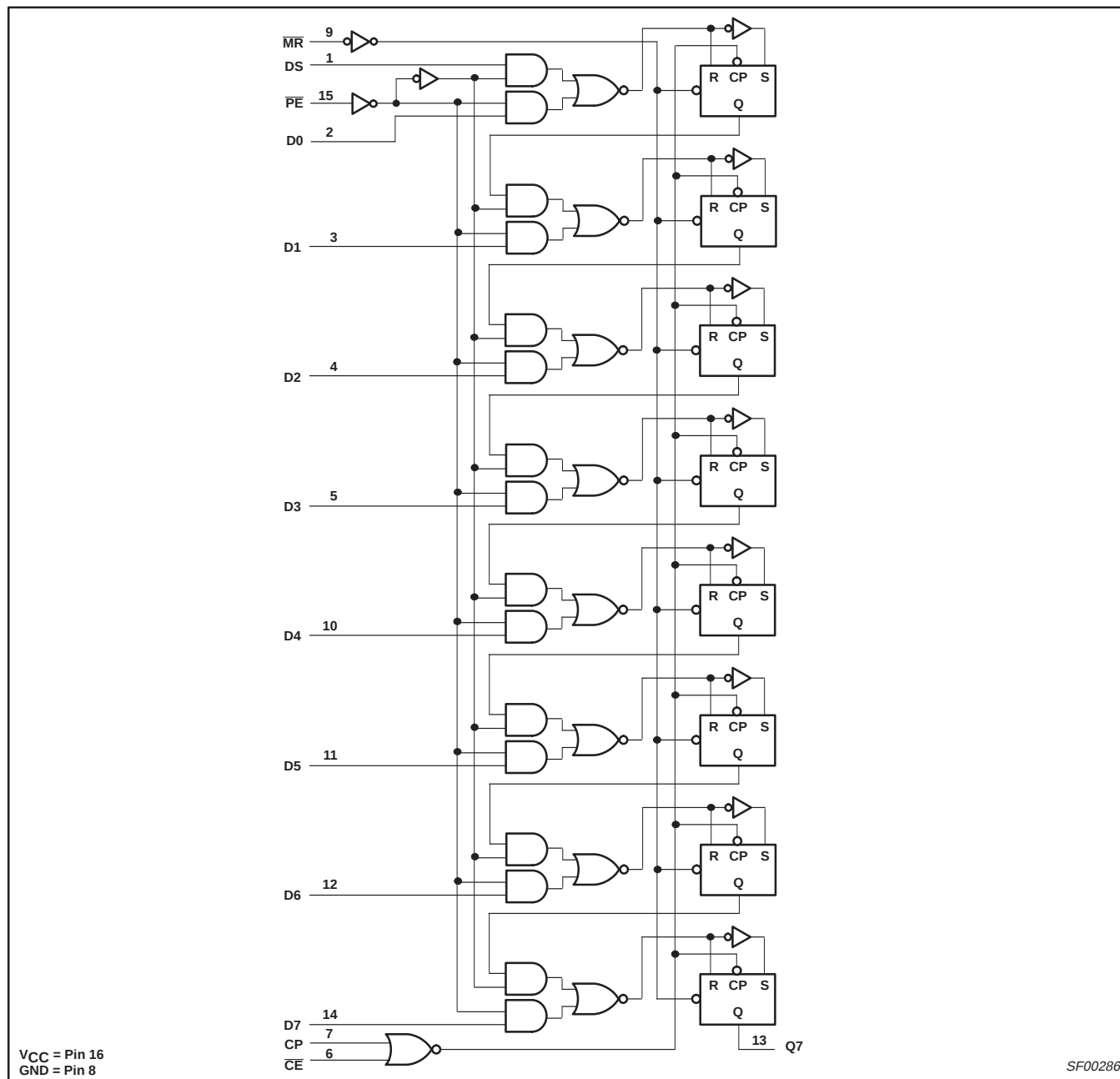
Notes to function table

- 1. H = High-voltage level
- 2. h = High voltage level one setup time before the low-to-high clock transition
- 3. L = Low-voltage level
- 4. l = Low voltage level one setup time before the low-to-high clock transition
- 5. qn = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the low-to-high clock transition
- 6. X = Don't care
- 7. ↑ = Low-to-high clock transition

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LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	−40		+85	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS ¹			LIMITS			UNIT
							MIN	TYP ²	MAX	
V _{OH}	High-level output voltage			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = MAX	±10%V _{CC}	2.5			V
						±5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}		0.30	0.50	V
						±5%V _{CC}		0.30	0.50	V
V _{IK}	Input clamp voltage			V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximum input voltage	others CE, CP ³		V _{CC} = 0.0V, V _I = 7.0V					100	μA
I _{IH}	High-level input current	others		V _{CC} = MAX, V _I = 2.7V					20	μA
		MR, Ds							40	μA
		Industrial only	others						40	μA
		MR, Ds							80	μA
I _{IL}	Low-level input current		others	V _{CC} = MAX, V _I = 0.5V					-20	μA
			MR, Ds						-40	μA
I _{OS}	Short-circuit output current ⁴			V _{CC} = MAX			-60		-150	mA
I _{CC}	Supply current (total)			V _{CC} = MAX, PE = CE = Dn = GND, MR = Ds = 4.5V, CP = ↑				50	70	mA

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- When testing CP, CE must remain in high state, whereas CP must remain in high state when testing CE.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			T _{amb} = +25°C			T _{amb} = 0°C to +70°C		T _{amb} = -40°C to +85°C			
			V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}	Maximum clock frequency	Waveform 1	135	175		110		100		ns	
t _{PLH} t _{PHL}	Propagation delay CP to Q7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	5.0 3.5	13.0 9.0	ns	
t _{PHL}	Propagation delay MR to Q7	Waveform 2	4.0	6.5	8.5	4.0	9.5	4.0	9.5	ns	

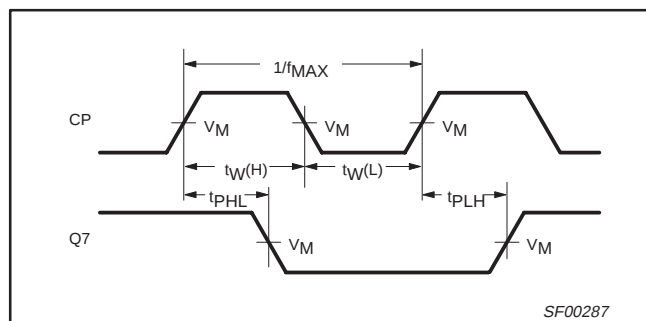
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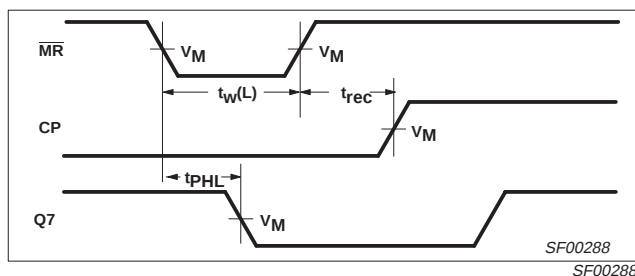
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T _{amb} = +25°C			T _{amb} = 0°C to +70°C		T _{amb} = −40°C to +85°C		
			V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{su} (H) t _{su} (L)	Setup time, high or low Dn, Ds to CP, $\overline{\text{CE}}$	Waveform 3	3.0 2.5			4.0 3.0		4.0 3.0		ns
t _h (H) t _h (L)	Hold time, high or low Dn, Ds to CP	Waveform 3	0.0 0.0			1.0 0.0		1.0 0.0		ns
t _h (H) t _h (L)	Hold time, high or low Dn, Ds to $\overline{\text{CE}}$	Waveform 3	1.5 0.0			2.0 0.0		2.0 0.0		ns
t _{su} (L)	Setup time, low $\overline{\text{CE}}$ to CP	Waveform 3	5.0			6.0		6.0		ns
t _h (H)	Hold time, high $\overline{\text{CE}}$ to CP	Waveform 3	0.0			0.0		0.0		ns
t _{su} (H) t _{su} (L)	Setup time, high or low $\overline{\text{PE}}$ to CP, $\overline{\text{CE}}$	Waveform 3	3.0 3.0			4.0 4.0		4.0 6.0		ns
t _h (H) t _h (L)	Hold time, high or low $\overline{\text{PE}}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		0.0 0.0		ns
t _w (H) t _w (L)	CP pulse width, high or low	Waveform 1	3.0 4.5			3.5 5.0		3.5 6.0		ns
t _w (L)	$\overline{\text{MR}}$ pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t _{rec}	Recovery time: $\overline{\text{MR}}$ to CP	Waveform 2	4.0			4.5		4.5		ns

AC WAVEFORMS



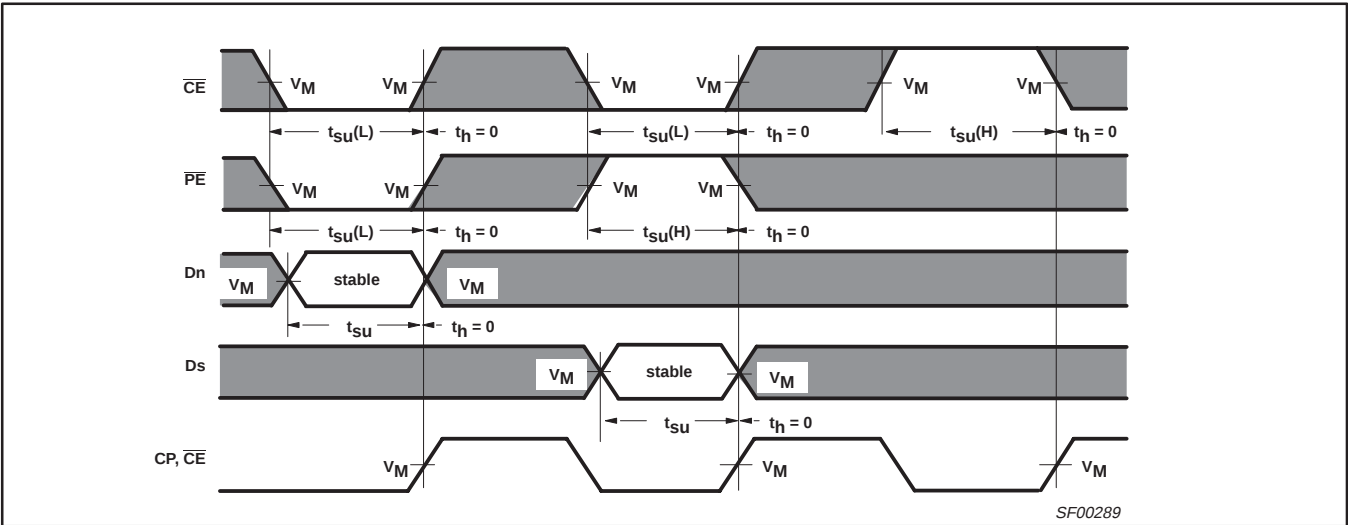
Waveform 1. Propagation delay for clock input to output,
clock pulse width, and maximum clock frequency



Waveform 2. Master reset pulse width, master reset to output
delay and master reset to clock recovery time

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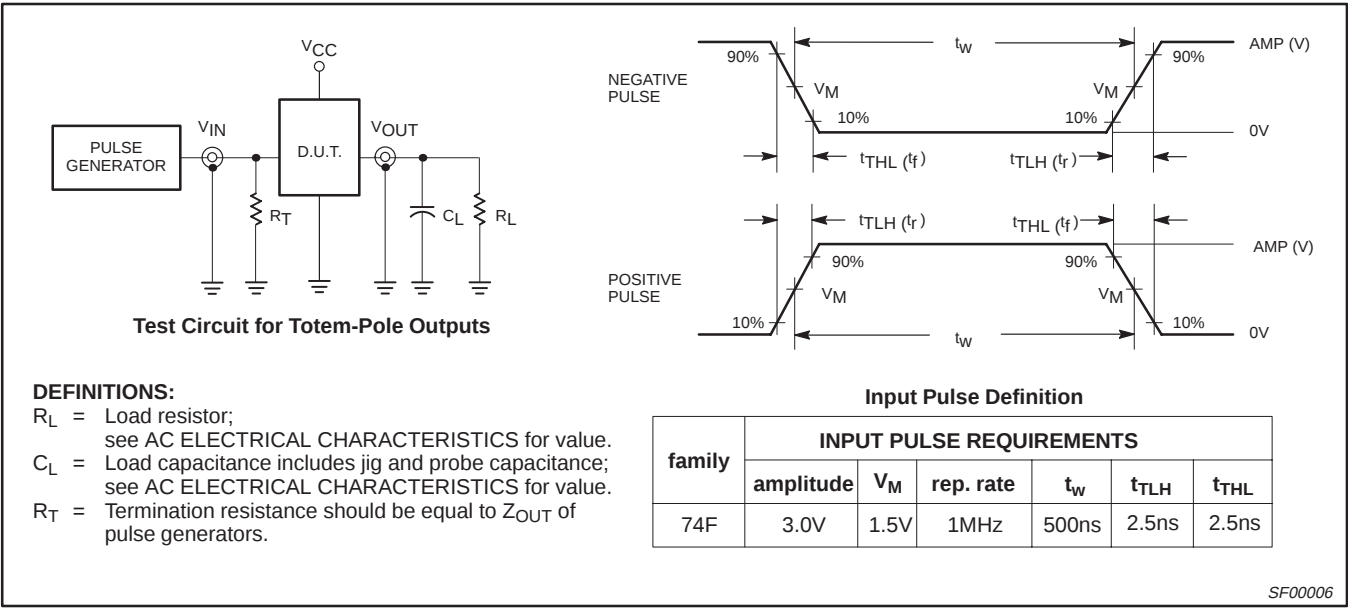


Waveform 3. Setup and hold times

Notes to AC waveforms

- 1. For all waveforms, $V_M = 1.5V$.
- 2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

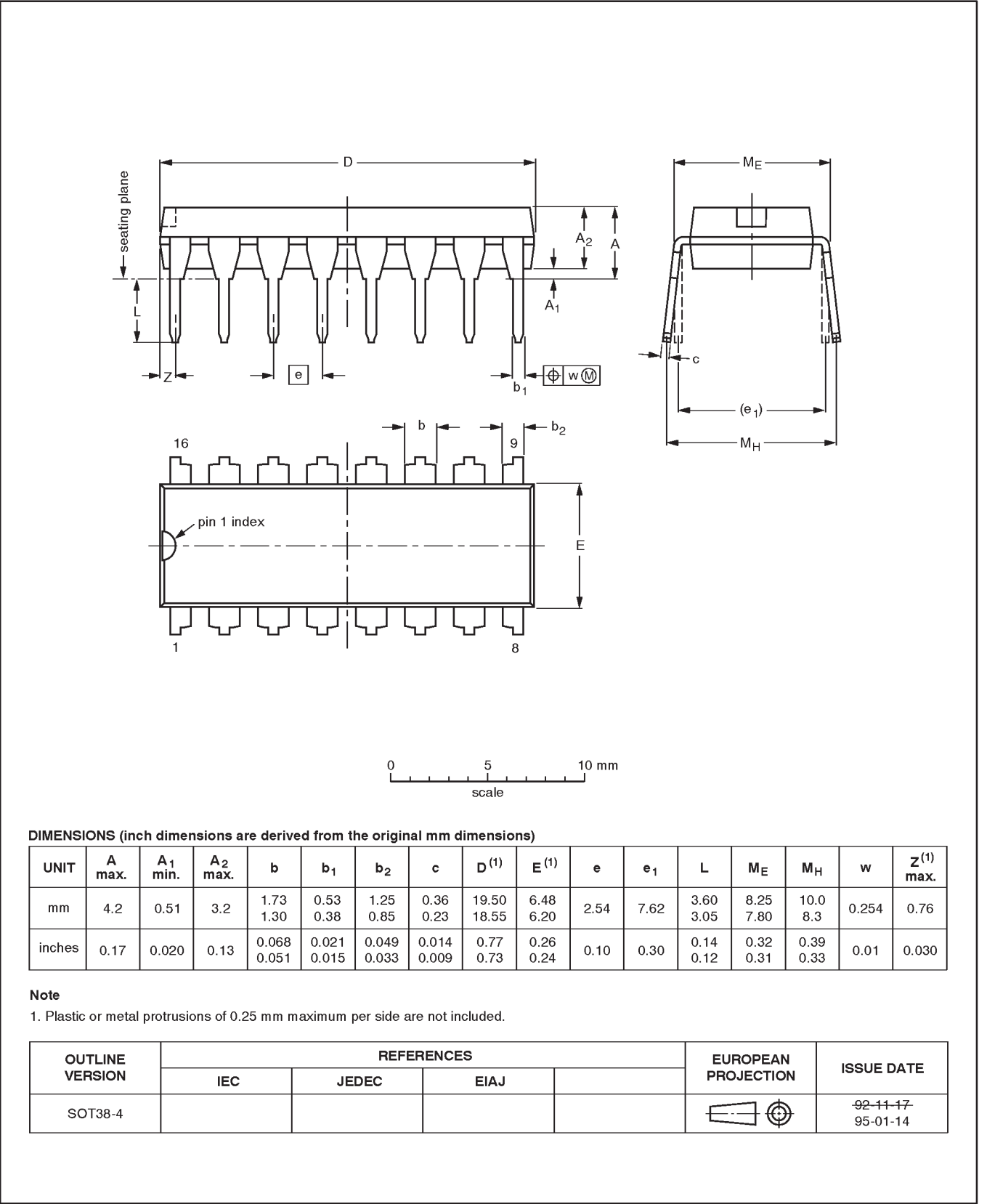


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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

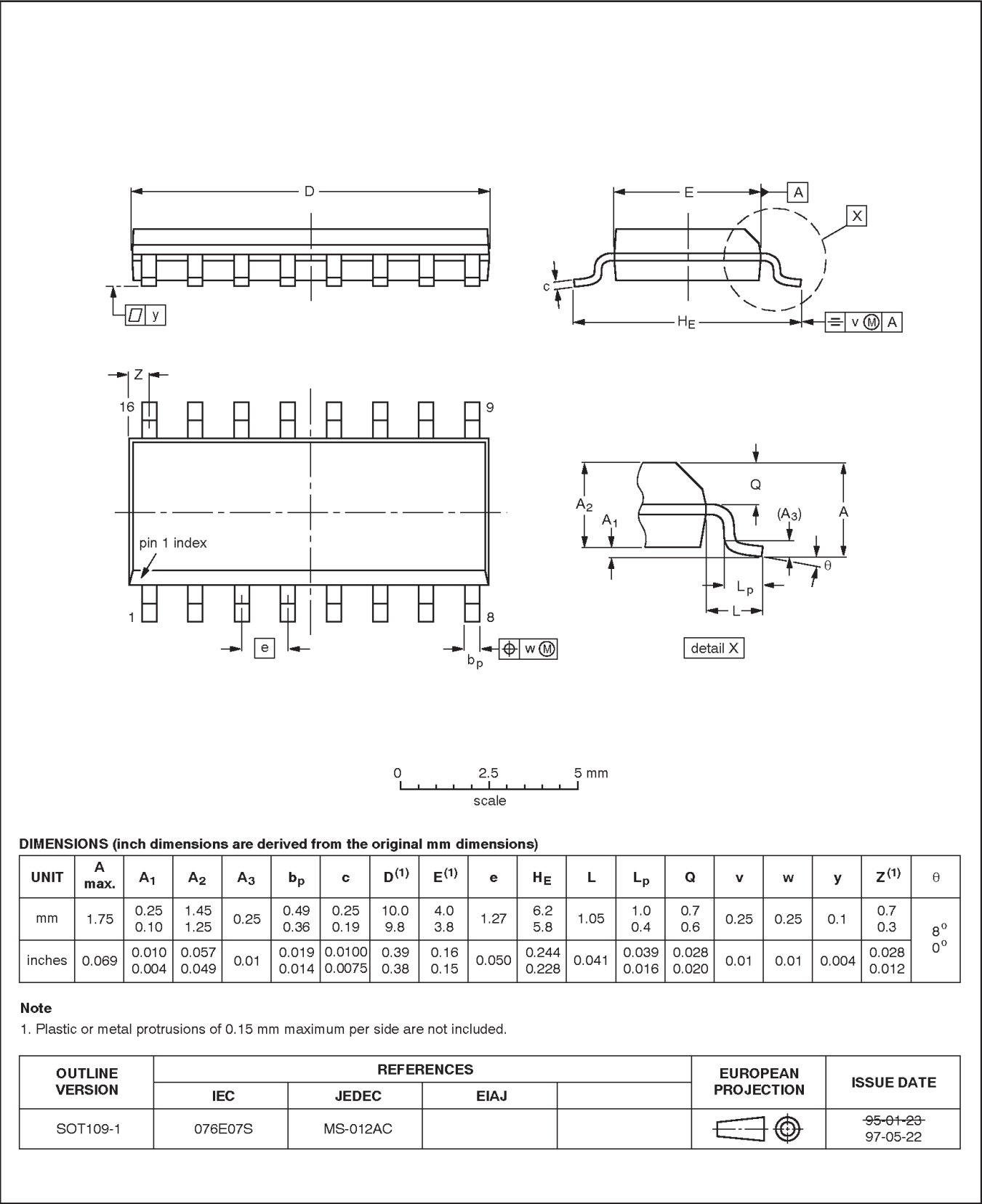


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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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