Three Phase Inverter Automotive Power MOSFET Module

NXV08V080DB1

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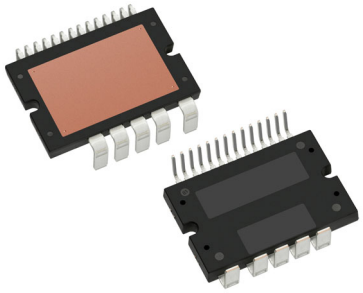


19LD, APM, PDD STD
CASE MODCD

Features

- Three−Phase Inverter Bridge for Variable Speed Motor Drive
- RC Snubber for Low EMI
- Current Sensing and Temperature Sensing
- Electrically Isolated DBC Substrate for Low Thermal Resistance
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- AEC Qualified − AQG324
- PPAP Capable
- This Device is Pb−free, RoHS and UL94−V0 Compliant

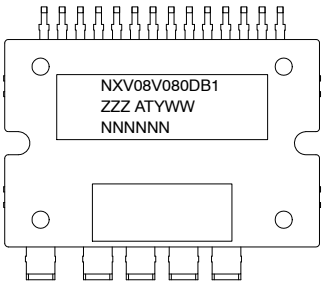
Applications

- 24 V and 48 V Motor Control
- DC−DC Converter

Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO_2 Emission
- Simplified Vehicle Assembly
- Enable Low Thermal Resistance to Junction−to−Heat Sink by Direct Mounting via Thermal Interface Material between Module Case and Heat Sink

MARKING DIAGRAM



NXV08V080DB1	= Specific Device Code
ZZZ	= Lot ID
AT	= Assembly & Test Location
Y	= Year
WW	= Work Week
NNN	= Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Package	Pb−Free and RoHS Compliant	Operating Temperature Range	Packing Method
NXV08V080DB1	APM19−CBC	Yes	−40 ~ 125°C	Tube

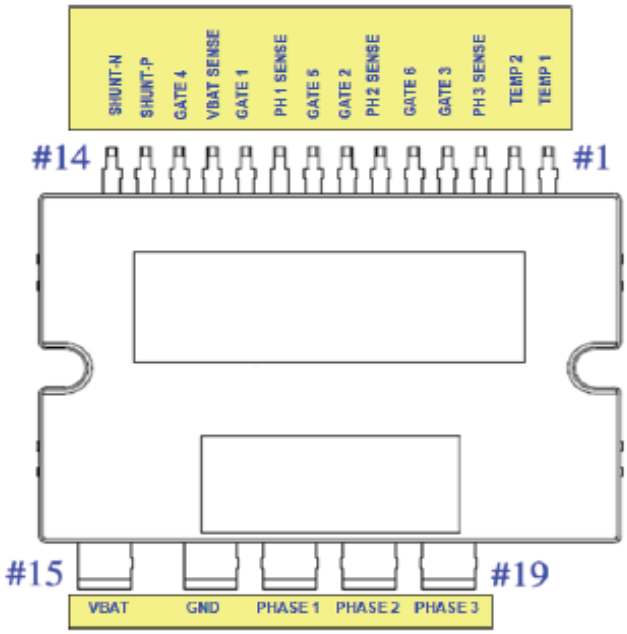


Figure 1. Pin Configuration

PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE 3 SENSE	Source of Q3 and Drain of Q6
4	GATE 3	Gate of Q3, high side Phase 3 MOSFET
5	GATE 6	Gate of Q6, low side Phase 3 MOSFET
6	PHASE 2 SENSE	Source of Q2 and Drain of Q5
7	GATE 2	Gate of Q2, high side Phase 2 MOSFET
8	GATE 5	Gate of Q5, low side Phase 2 MOSFET
9	PHASE 1 SENSE	Source of Q1 and Drain of Q4
10	GATE 1	Gate of Q2, high side Phase 1 MOSFET
11	VBAT SENSE	Sense pin for battery voltage and Drain of high side MOSFETs
12	GATE 4	Gate of Q4, low side Phase 1 MOSFET
13	SHUNT P	Positive CSR sense pin and source connection for low side MOSFETs
14	SHUNT N	Negative CSR sense pin and sense pin for battery return
15	VBAT	Battery voltage power lead
16	GND	Battery return power lead
17	PHASE 1	Phase 1 power lead
18	PHASE 2	Phase 2 power lead
19	PHASE 3	Phase 3 power lead

Schematic Diagram

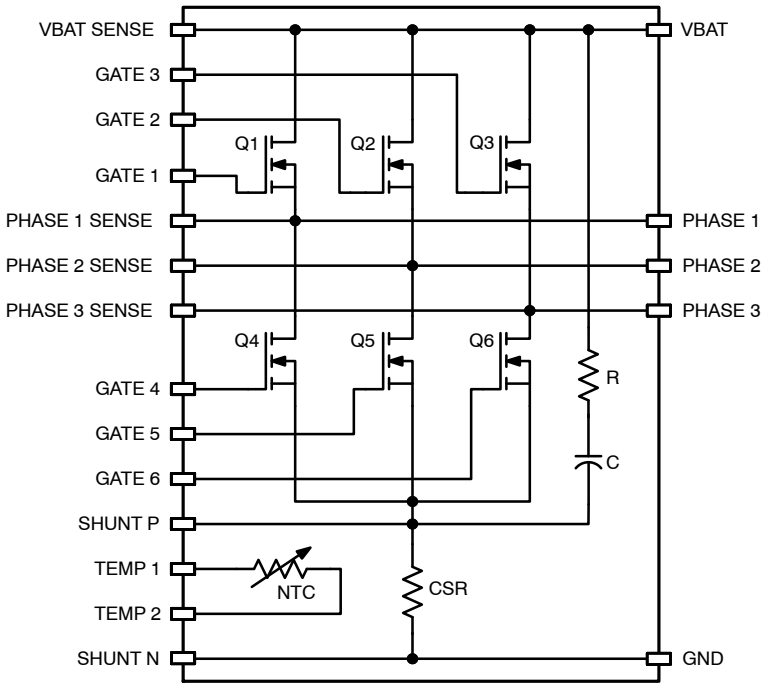


Figure 2. Schematic

Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0 or higher.

Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

Solder

Solder used is a lead free SnAgCu alloy.

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Max.	Unit
V_{DS}	Drain−to−Source Voltage	80	V
V_{GS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, T_J = 175°C) (Note 1)	130	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	190	mJ
$T_{J(max)}$	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature Range	125	°C
V_{ISO}	Isolation Voltage	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Defined by design, not subject to production testing. The value is the result of the calculation, Min (package limit max current, Silicon limit max current) where the silicon limit current is calculated based on the maximum value which is not to exceed T_J = 175°C on maximum thermal limitation and on resistance.
2. Starting T_J = 25°C, L = 0.08 mH, I_{AS} = 69 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0 V during time in avalanche.

THERMAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 3)	–	–	1.3	K/W

3. Test method compliant with MIL−STD−883−1012.1, case temperature measured below the package at the chip center. Cosmetic oxidation and discolor on the DBC surface is allowed.

MODULE SPECIFIC CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameters	Test Conditions	Symbol	Min	Typ	Max	Unit
Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	B_{VDSS}	80	–	–	V
Drain−to−Source Leakage Current	V_{DS} = 80 V, V_{GS} = 0 V	I_{DSS}	–	–	2	μA
Gate−to−Source Leakage Current	V_{GS} = ±20 V	I_{GSS}	−100	–	+100	nA
Gate−to−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	$V_{GS(th)}$	2.0	–	4.0	V
Body Diode Forward Voltage of MOSFET	I_S = 80 A, V_{GS} = 0 V	V_{SD}	–	–	1.25	V
Drain−to−Source On Resistance, Q1	I_D = 80 A, V_{GS} = 10 V (Note 4)	$R_{DS(ON)Q1}$	–	2.4	3.0	mΩ
Drain−to−Source On Resistance, Q2		$R_{DS(ON)Q2}$	–	2.5	3.1	mΩ
Drain−to−Source On Resistance, Q3		$R_{DS(ON)Q3}$	–	2.5	3.1	mΩ
Drain−to−Source On Resistance, Q4		$R_{DS(ON)Q4}$	–	2.6	3.2	mΩ
Drain−to−Source On Resistance, Q5		$R_{DS(ON)Q5}$	–	2.9	3.5	mΩ
Drain−to−Source On Resistance, Q6		$R_{DS(ON)Q6}$	–	3.2	3.8	mΩ
VBAT to PHASE 1	I_D = 80 A, V_{GS} = 10 V	$R_{DS(ON)MQ1}$	–	3.3	3.8	mΩ
VBAT to PHASE 2		$R_{DS(ON)MQ2}$	–	3.4	3.9	mΩ
VBAT to PHASE 3		$R_{DS(ON)MQ3}$	–	3.5	4.0	mΩ
PHASE1 to GND		$R_{DS(ON)MQ4}$	–	3.5	4.0	mΩ
PHASE2 to GND		$R_{DS(ON)MQ5}$	–	3.7	4.3	mΩ
PHASE3 to GND		$R_{DS(ON)MQ6}$	–	4.0	4.6	mΩ
Total loop resistance VBAT ≥ Phase ≥ GND	I_D = 80 A, V_{GS} = 10 V		–	6.5	8.5	mΩ

4. All MOSFETs have same size and on resistance. However, the different values listed due to the different access points available inside the module for on resistance measurement. Q1 has the shortest measurement path in the layout, in this reason, on resistance of Q1 can be used for simple power loss calculation.

COMPONENTS

Symbol	Spec	Quantity	Size
RESISTOR	1.0 Ω	1	142 × 55 mil
CAPACITOR	100 V, 0.022 μF	1	79 × 49 mil
CURRENT SENSING RESISTOR	0.5 mΩ	1	250 × 120 mil
NTC	NCP18XH103F0SRB, 10 kΩ	1	63 × 32 mil

ELECTRICAL CHARACTERISTICS

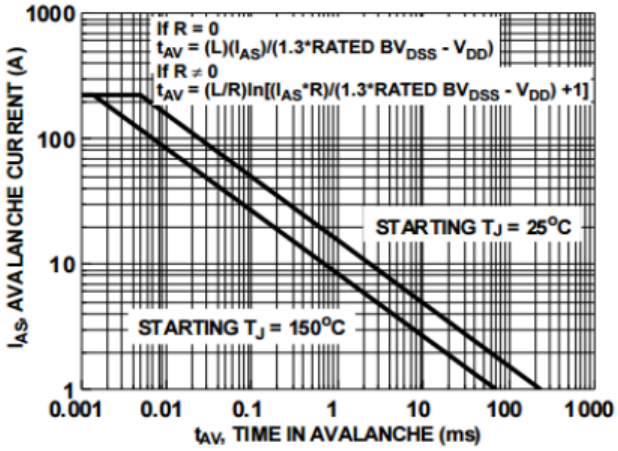
(T_J = 25°C unless otherwise noted, Reference typical characteristics of FDBL86366−F085, TOLL)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	6320	–	pF
C_{oss}	Output Capacitance		–	1030	–	pF
C_{rss}	Reverse Transfer Capacitance		–	32	–	pF
R_g	Gate Resistance	f = 1 MHz	–	2.1	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V; V_{DD} = 64 V, I_D = 80 A	–	86	112	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 10 V; V_{DD} = 64 V, I_D = 80 A	–	12	18	nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 64 V, I_D = 80 A	–	30	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge	V_{DD} = 64 V, I_D = 80 A	–	18	–	nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn−On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	–	98	ns
$t_{d(on)}$	Turn−On Delay Time		–	30	–	ns
t_r	Turn−On Rise Time		–	34	–	ns
$t_{d(off)}$	Turn−Off Delay Time		–	40	–	ns
t_f	Turn−Off Fall Time		–	17	–	ns
t_{off}	Turn−Off Time		–	–	86	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(Graphs are generated using the die assembled in discrete package for reference purposes only. Datasheet of FDBL86366−F085 is available in the web)



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 3. Unclamped Inductive Switching Capability

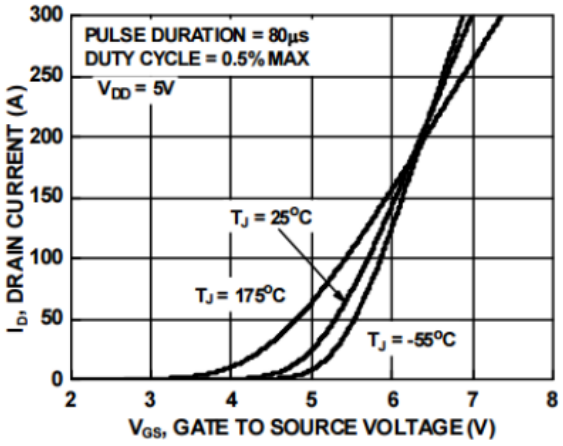


Figure 4. Transfer Characteristics

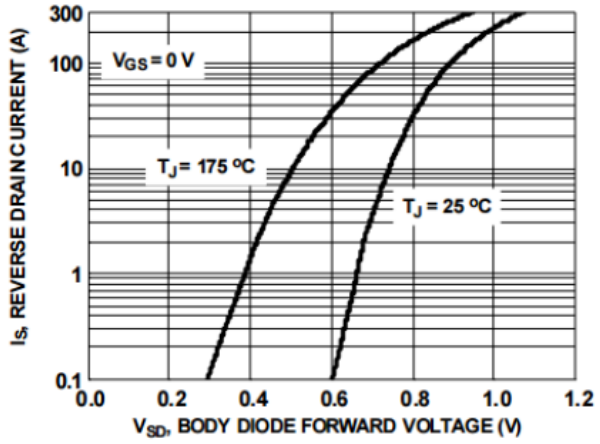


Figure 5. Forward Diode Characteristics

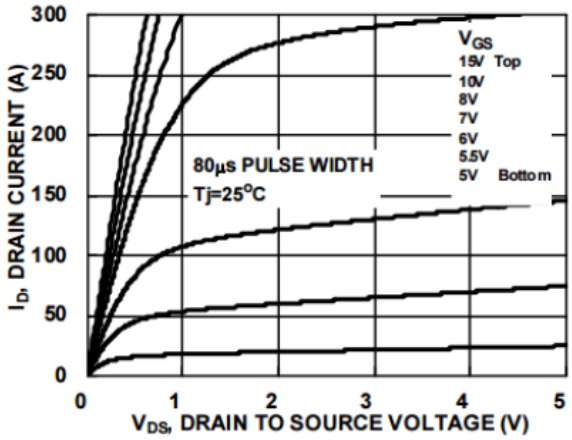


Figure 6. Saturation Characteristics

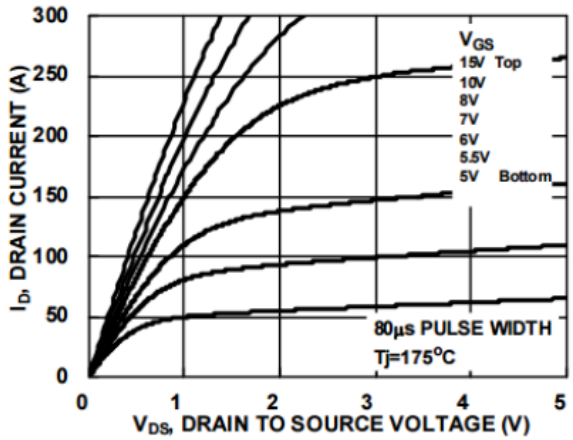


Figure 7. Saturation Characteristics

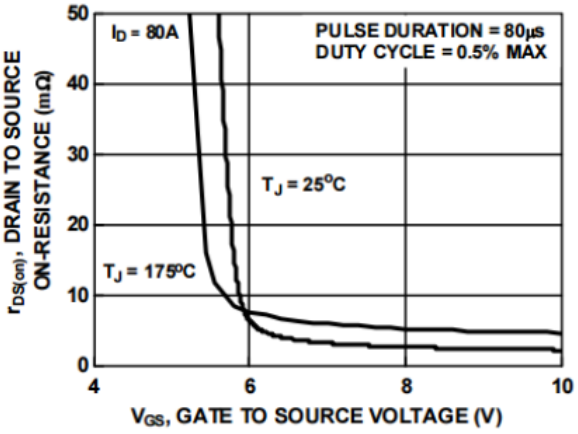


Figure 8. $R_{DS(on)}$ vs, Gate Voltage

TYPICAL CHARACTERISTICS (continued)

(Graphs are generated using the die assembled in discrete package for reference purposes only. Datasheet of FDBL86366−F085 is available in the web)

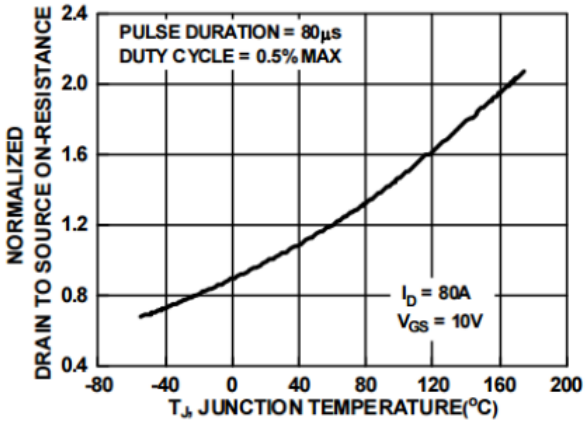


Figure 9. Normalized $R_{DS(on)}$ vs. Junction Temperature

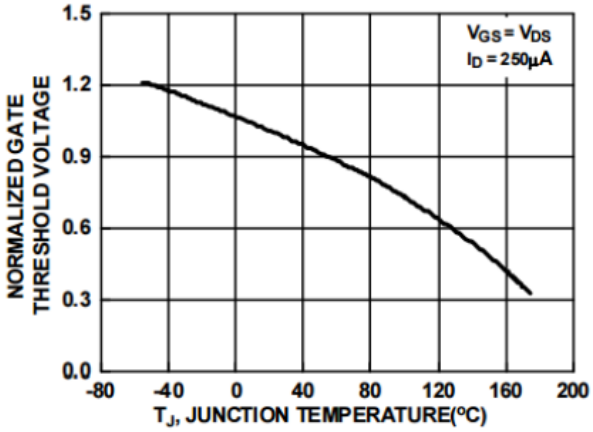


Figure 10. Normalized Gate Threshold Voltage vs. Temperature

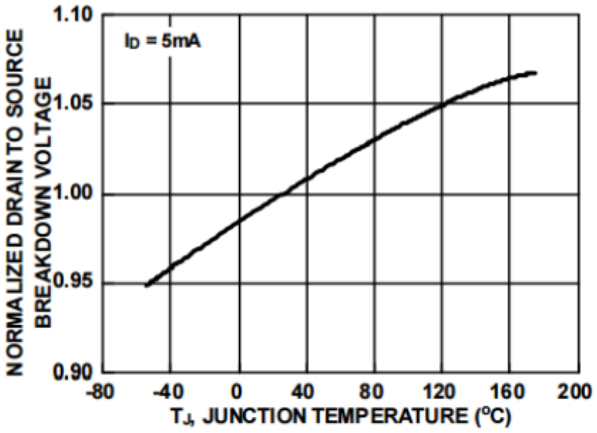


Figure 11. Normalized Drain−to−Source Breakdown Voltage vs. Junction Temperature

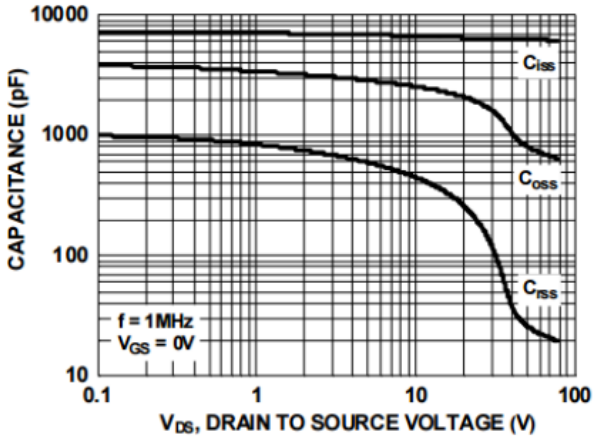


Figure 12. Capacitance vs. Drain−to−Source Voltage

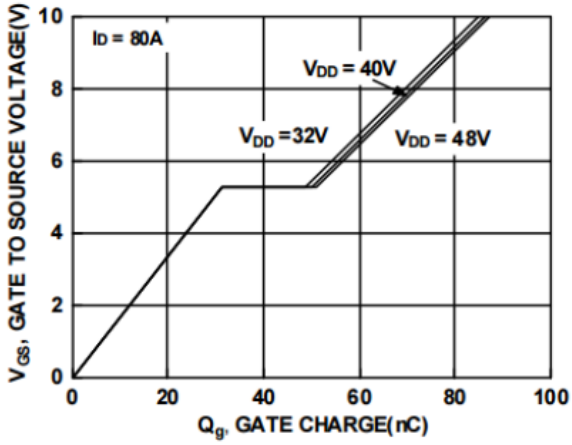


Figure 13. Gate Charge vs. Gate−to−Source Voltage

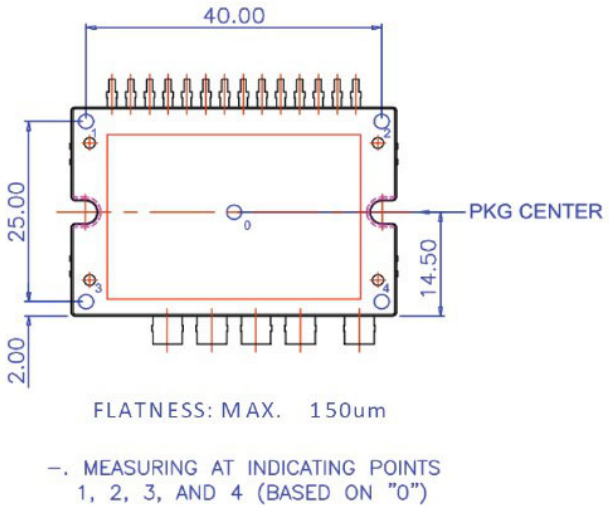


Figure 14. Flatness Measurement Position

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Device Flatness	Refer to the package dimensions	0	–	150	um
Mounting Torque	Mounting screw: M3, recommended 0.7 N•m	0.4	–	0.8	N•m
Weight		–	20	–	g

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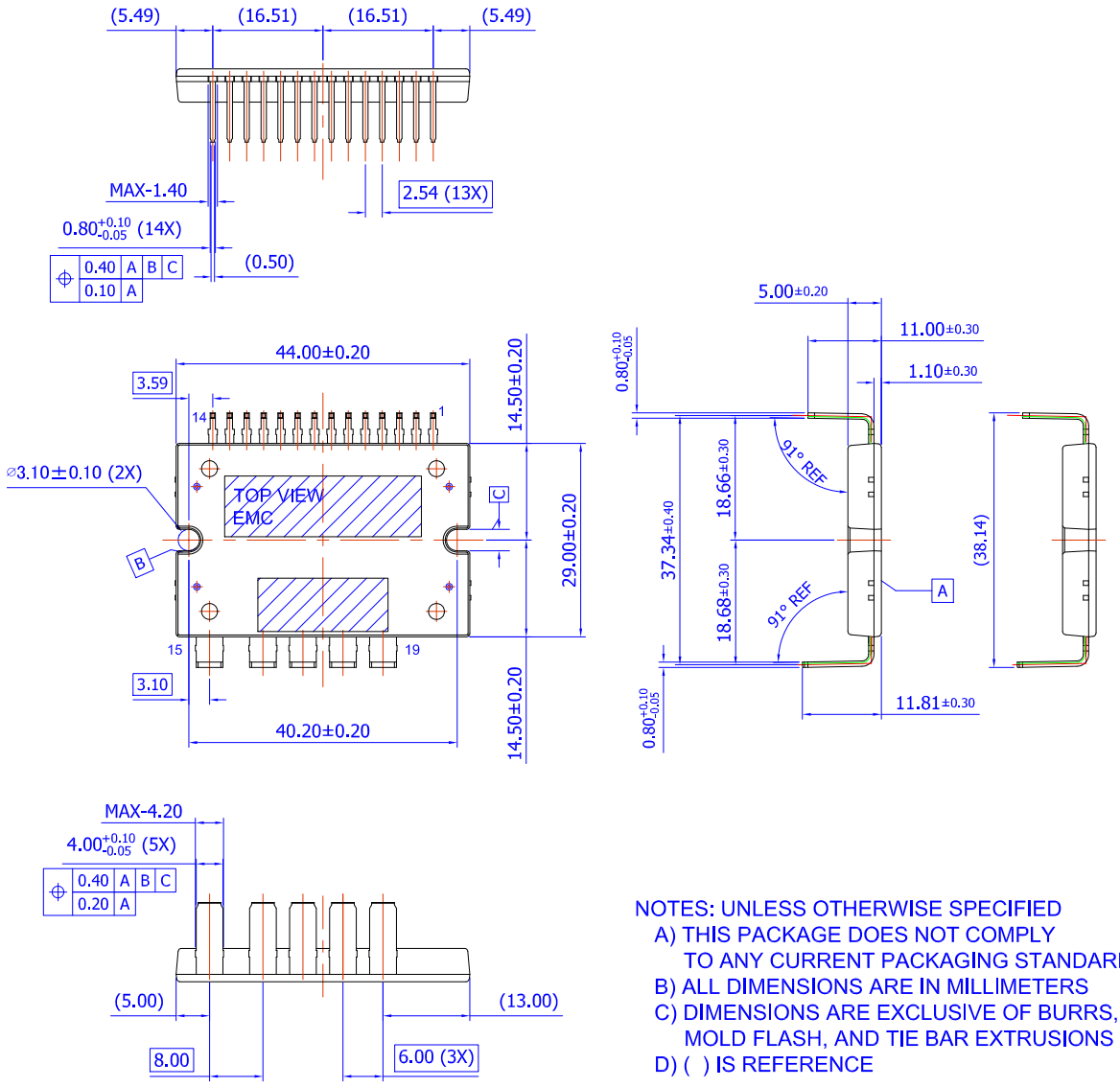

NOTES: UNLESS OTHERWISE SPECIFIED
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B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

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