

SN54ACT533, SN74ACT533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS553B – NOVEMBER 1995 – REVISED JANUARY 2000

- Inputs Are TTL-Voltage Compatible
- 3-State Inverting Outputs Drive Bus Lines Directly
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

description

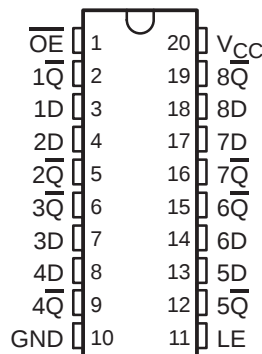
The 'ACT533 devices are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the $\bar{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\bar{Q}$ outputs are latched at the inverted levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

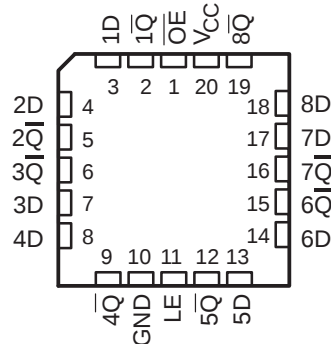
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT533 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ACT533 is characterized for operation from -40°C to 85°C .

SN54ACT533 . . . J OR W PACKAGE
SN74ACT533 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ACT533 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z



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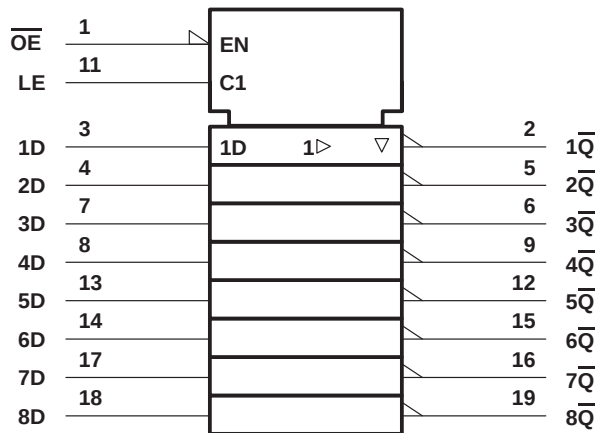
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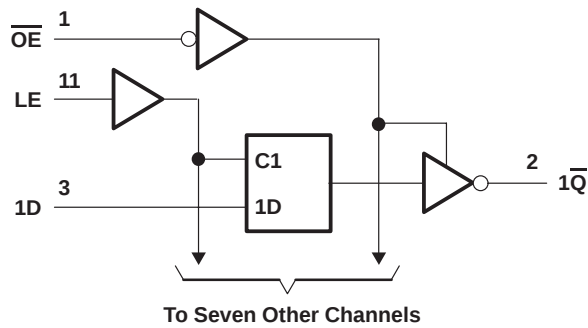
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN54ACT533, SN74ACT533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS553B – NOVEMBER 1995 – REVISED JANUARY 2000

recommended operating conditions (see Note 3)

		SN54ACT533		SN74ACT533		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–24		–24	mA
I _{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	8	0	8	ns/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT533		SN74ACT533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OH} = –24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I _{OH} = –50 mA [†]	5.5 V				3.85				
	I _{OH} = –75 mA [†]	5.5 V						3.85		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±5		±2.5	μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6			1.6		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		4.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54ACT533		SN74ACT533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	5		7.5		6		ns
t _{su}	Setup time, data before LE↓	3		5.5		4		ns
t _h	Hold time, data after LE↓	2		4		2.5		ns

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SN54ACT533, SN74ACT533

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCAS553B – NOVEMBER 1995 – REVISED JANUARY 2000

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN54ACT533		SN74ACT533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	2.5	10.5	1.5	13	2	11.5	ns
t_{PHL}			2.5	10	1.5	12.5	2	11	
t_{PLH}	LE	$\overline{Q}$	2.5	10.5	1.5	13	2	11.5	ns
t_{PHL}			2.5	10.5	1.5	13	2	11.5	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	2	10	1	12.5	1.5	11	ns
t_{PZL}			2	10	1	12.5	1.5	11	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2	10	1	12.5	1.5	11	ns
t_{PLZ}			2	10	1	12.5	1.5	11	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

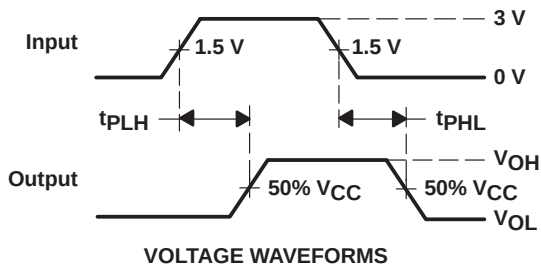
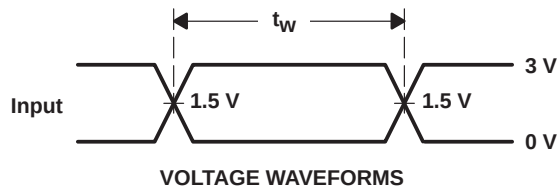
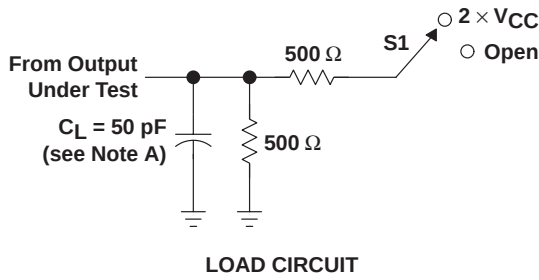
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	40	pF

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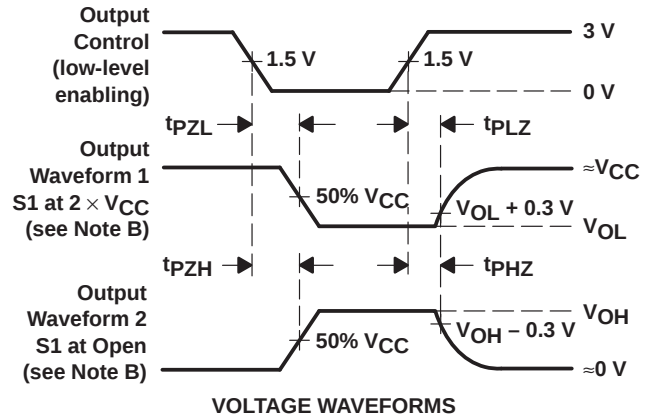
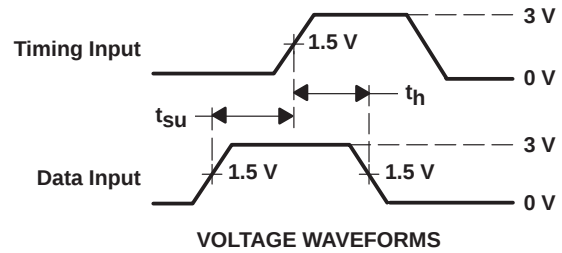


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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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