PPMU Circuit

AD53508

FEATURES

Dual Measurement Channels
Precision Four-Quadrant-Per-Pin V/I Source
Programmable Current Force Ranges
±204.8 μA and ±2.048 mA
Five Current Measurement Ranges
204.8 nA to ±2.048 mA
Output Voltage Range: –4 V to +9 V
Power Supplies: +15 V, +5 V, and –10 V
44-Lead Plastic J-Leaded Chip Carrier Package

APPLICATIONS

Can Be Used with the AD53032 DCL to Extend Current Force Range to 35 mA

GENERAL DESCRIPTION

The AD53508 is a custom dual-channel parametric measurement circuit for use in semiconductor automatic test equipment. It contains programmable modes to force a pin voltage and measure its current or to integrate and hold a current value. Alternatively, a current can be forced and the compliance voltage measured.

The device provides a remote force/sense capability to ensure accuracy at the tester pin. A guard output is available to drive the shield of a force/sense pair.

Two input references per channel permit controlled switching to different voltage or current levels. The forced voltage or current levels can be switched back to the measurement system to read back the analog levels for system calibration.

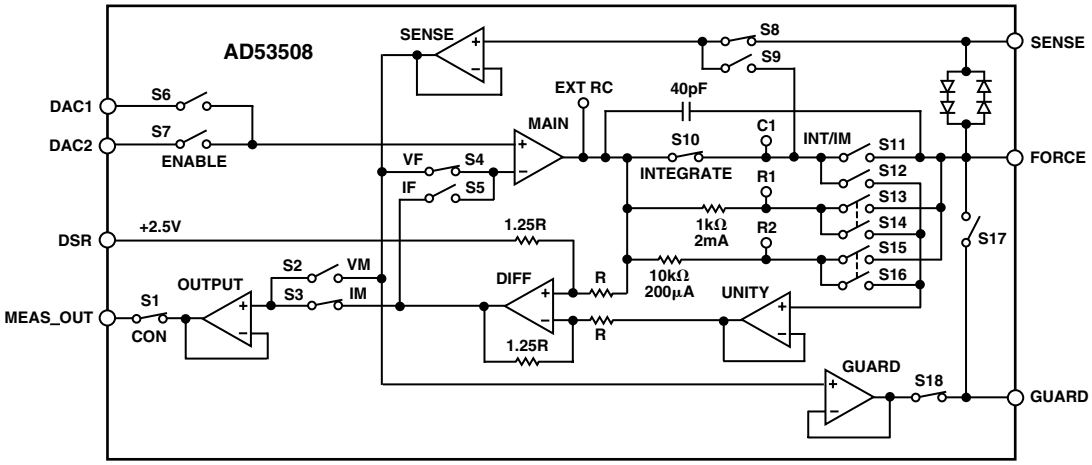
The circuit is powered by +15 V, +5 V, and –10 V supplies and dissipates 230 mW nominally.

Recommended Use of the PPMU with AD53032 DCL

The PPMU can be used with the AD53032 DCL to extend the Current Force Range beyond 2 mA VCOM can be set to the maximum spec allowance of 8 V, which would allow the maximum Current Force of IOL of 35 mA. The combination of the PPMU and the DCL would have a few benefits including:

1. Accurately measuring low currents.
2. Can take parallel measurements by using one PMU per pin.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD53508* PRODUCT PAGE QUICK LINKS

Last Content Update: 09/16/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD53508: PPMU Circuit Data Sheet

DESIGN RESOURCES

- AD53508 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD53508 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD53508–SPECIFICATIONS (T_A = 25°C, rated power supplies unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit[1]
VOLTAGE FORCE/MEASURE MODE					
Voltage Swing, ±2 mA Range					
±2 mA Drive		–4		+9	V
±100 µA Drive		–5		+12	V
ACCURACY					
Gain (±0.1% Tolerance)		0.999		1.001	V/V
Offset Error				±15	mV
Gain Nonlinearity (Relative to Endpoints)				±0.02	% of Span
Current Measure CMRR (at MEAS_OUT)				±0.31	mV/V
DRIFT					
Gain Error Temperature Coefficient				±20	ppm (PV or MV)/°C
Offset Drift				±100	µV/°C
CURRENT FORCE/MEASURE MODE RANGES					
0 (High)			±2.0		mA
1 (Low)			±200		µA
ACCURACY—HIGH RANGE					
Transconductance (±3% Tolerance)	Force Mode	0.776	0.8	0.824	mA/V
Transresistance (±3% Tolerance)	Measure Mode	1.21	1.25	1.29	V/mA
Offset Error				±40	µA
Gain Nonlinearity (Relative to Endpoints)				±0.05	% of Span
Output Compliance Voltage-Induced Transconductance/Error	Force Mode	–0.2		+0.4	µA/V
DRIFT—HIGH RANGE					
Gain Error Temperature Coefficient				+10/–60	ppm (PV or MV)/°C
Offset Drift				±400	nA/°C
ACCURACY—LOW RANGE					
Transconductance (±3% Tolerance)	Force Mode	77.6	80	82.4	µA/V
Transresistance (±3% Tolerance)	Measure Mode	12.1	12.5	12.9	V/mA
Offset Error				±4	µA
Gain Nonlinearity (Relative to Endpoints)				±0.05	% of Span
Output Compliance Voltage-Induced Transconductance/Error	Force Mode	–0.02		+0.04	µA/V
DRIFT—LOW RANGE					
Gain Error Temperature Coefficient				+10/–60	ppm (PV or MV)/°C
Offset Drift				±40	nA/°C
CURRENT MEASURE INTEGRATE MODE RANGES					
High			±20.0		µA
Medium			±2.0		µA
Low			±200		nA
ACCURACY—HIGH RANGE					
Transresistance Error (±3% Tolerance)		0.121	0.125	0.129	V/µA
Offset Error				±400	nA
Gain Nonlinearity (Relative to Endpoints)				±0.05	% of Span
Output Compliance Voltage-Induced Transresistance Error				±2.5	nA/V of Output
DRIFT—HIGH RANGE					
Gain Error Temperature Coefficient				±20	ppm MV/°C
Offset Drift				±2	nA/°C
ACCURACY—MEDIUM RANGE					
Transresistance Error (±3% Tolerance)		1.21	1.25	1.29	V/µA
Offset Error				±40	nA
Gain Nonlinearity (Relative to Endpoints)				±0.05	% of Span
Output Compliance Voltage-Induced Transresistance Error				±0.25	nA/V of Output
DRIFT— MEDIUM RANGE					
Gain Error Temperature Coefficient				±20	ppm MV/°C
Offset Drift				±250	pA/°C

Parameter	Condition	Min	Typ	Max	Unit[1]
ACCURACY—LOW RANGE					
Transresistance Error (±3% Tolerance)		0.0121	0.0125	0.0129	V/nA
Offset Error				±4	nA
Gain Nonlinearity (Relative to Endpoints)				±0.05	% of Span
Output Compliance Voltage-Induced Transresistance Error				±0.025	nA/V of Output
DRIFT—LOW RANGE					
Gain Error Temperature Coefficient				±20	ppm MV/°C
Offset Drift				±70	pA/°C
DISABLE MODE[2]					
Voltage Swing, ±2 mA Range					
±2 mA Drive		–4		+9	V
±100 µA Drive		–5		+12	V
ACCURACY					
Gain (±0.1% Tolerance)		0.999		1.001	V/V
Offset Error				±15	mV
Gain Nonlinearity (Relative to Endpoints)				±0.02	% of Span
Current Measure CMRR (at MEAS_OUT)				±0.31	mV/V
DRIFT					
Gain Error Temperature Coefficient				±20	ppm (PV or MV)/°C
Offset Drift				±100	µV/°C
OTHER SPECIFICATIONS					
Power Supply Rejection Ratio	f < 40 Hz, V_{CC}	70			dB
	f < 40 Hz, V_{EE}	60			dB
	f = 40 kHz, V_{CC}	35			dB
	f = 40 kHz, V_{EE}	25			dB
CURRENT MEASURE HOLD MODE LEAKAGE	T_{AMB} = 70°C			±1.2	nA
CROSSTALK[3]				±0.02	% of Span
SETTLING TIMES TO 0.01%					
Voltage Force and Guard Voltage	C_{LOAD} = 100 pF			20	µs
	C_{LOAD} = 2000 pF			2	ms
Current Force (200 µA Range)	Z_{LOAD} = 100 pF‖50 kΩ			50	µs
MEAS_OUT Pin	C_{LOAD} = 20 pF			2	µs
SHORT CIRCUIT CURRENT LIMIT MAGNITUDE	Any Output Except Guards	8.5		20	mA
GUARD SCC LIMIT MAGNITUDE		2.5		10	mA
GUARD OFFSET (FROM SENSE INPUT PIN)		–65	–25	0	mV
I_B (DAC1, DAC2) CURRENT				±1.0	µA
DIGITAL INPUTS					
V_{IH}		2.4			V
V_{IL}				0.8	V
I_{IN} (Input leakage current)				10	µA
POWER SUPPLIES					
V_{CC} (Positive Analog Supply Voltage)		14.0	15.0	15.75	V
V_{EE} (Negative Analog Supply Voltage)		–10.5	–10.0	–9.0	V
V_{DD} (Logic Supply Voltage)		4.75	5.0	5.25	V
I_{CC} (Positive Analog Supply Current)		5		15	mA
I_{EE} (Negative Analog Supply Current)		–15		–5	mA
I_{DD} (Logic Supply Current Is 0 with Inputs at Rails, Worst Case @ 2.4 V_{IN})				8	mA

NOTES

[1]PV = Programmed Value, MV = Measured Value, FSR = Full-Scale Range = span.

[2]Output connected: DAC2 and 2 mA range selected, unconditionally.

[3]f < 40 Hz, both channels in current force mode; other channel output voltage swinging rail to rail.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

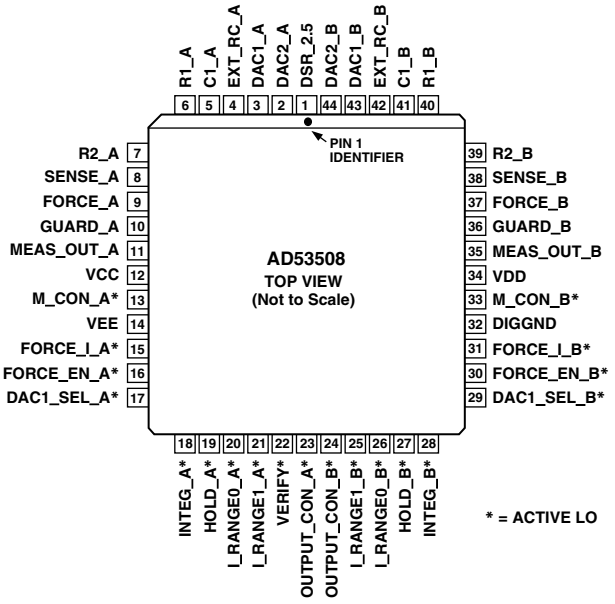
	Min	Max	Unit	Condition
VDD to VEE	–0.3	+26.4	V	
VCC to VEE	–0.3	+26.4	V	
VDD to DGND	–0.3	+6	V	
Digital Inputs to DGND	–0.3	VCC+0.3	V	
Power Dissipation		700	mW	$T_A \le 75°C$
Operating Temperature Range	25	70	°C	
Storage Temperature	–60	+125	°C	
Lead Temperature		300	°C	Soldering (10 sec)
Force/Sense Outputs	VEE–0.8	VCC+0.8	V	Or 75 mA, Whichever Is Less

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD53508JP	25°C to 70°C	Plastic Leaded Chip Carrier	P-44A

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Name	Description
1	DSR_2.5	2.5 V Reference Input
2	DAC2_A	First of Two Switchable Inputs
3	DAC1_A	Second of Two Switchable Inputs
4	EXT_RC_A	External R_S and C Common
5	C1_A	External Capacitor
6	R1_A	External Resistor
7	R2_A	External Resistor
8	SENSE_A	Sense Input
9	FORCE_A	Force Output
10	GUARD_A	Guard Drive Output
11	MEAS_OUT_A	Measurement Output
12	VCC	+15 V Analog Supply
13	M_CON_A*	Connect Measure Output to Bus
14	VEE	–10 V Analog Supply
15	FORCE_I_A*	Force V (When Hi) or I (When Lo)
16	FORCE_EN_A*	Control Input
17	DAC1_SEL_A*	Select DAC1 (When Lo) or DAC2
18	INTEG_A*	Control Input
19	HOLD_A*	Control Input
20	I_RANGE0_A*	Select 2 mA Range (Active Lo)
21	I_RANGE1_A*	Select 200 μA Range (Active Lo)
22	VERIFY*	Measure Forced Voltage or Current
23	OUTPUT_CON_A*	Connect Pin Drive (Active Lo)
24	OUTPUT_CON_B*	Connect Pin Drive (Active Lo)
25	I_RANGE1_B*	Select 200 μA Range (Active Lo)
26	I_RANGE0_B*	Select 2 mA Range (Active Lo)
27	HOLD_B*	Control Input
28	INTEG_B*	Control Input
29	DAC1_SEL_B*	Select DAC1 (When Lo) or DAC2
30	FORCE_EN_B*	Control Input
31	FORCE_I_B*	Force V (When Hi) or I (When Lo)
32	DIGGND	Digital Ground
33	M_CON_B*	Connect Measure Output to Bus
34	VDD	+5 V Digital Supply
35	MEAS_OUT_B	Measurement Output
36	GUARD_B	Guard Drive Output
37	FORCE_B	Force Output
38	SENSE_B	Sense Input
39	R2_B	External Resistor
40	R1_B	External Resistor
41	C1_B	External Capacitor
42	EXT_RC_B	External R_S and C Common
43	DAC1_B	Second of Two Switchable Inputs
44	DAC2_B	First of Two Switchable Inputs

* = Active Lo

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53508 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. Data Table

Data Latch Bits S1	S2	S3	S4	S5	S6	S7	S9	S17	S8	S10	S13, S14	S15, S16	S11	S12	S18
Voltage Force/Current Measure															
Irange 0															
On	Off	On	On	Off	On	Off	Off	Off	On	On	On	Off	Off	Off	On
Irange 1															
On	Off	On	On	Off	On	Off	Off	Off	On	On	Off	On	Off	Off	On
Integrate Range															
On	Off	On	On	Off	On	Off	Off	Off	On	On	Off	Off	On	On	On
Integrate															
On	Off	On	On	Off	On	Off	Off	Off	On	Off	Off	Off	On	On	On
Hold/Measure															
On	Off	On	On	Off	On	Off	On	On	Off	Off	Off	Off	Off	On	On
Current Force/Voltage Measure															
Irange 0															
On	On	Off	Off	On	On	Off	Off	Off	On	On	On	Off	Off	Off	On
Irange 1															
On	On	Off	Off	On	On	Off	Off	Off	On	On	Off	On	Off	Off	On
Disable Mode: Output Connected															
X	X	X	On	Off	Off	On	Off	Off	On	X	On	Off	Off	Off	On
Verify/Voltage Force															
On	On	Off	On	Off	On	Off	Off	Off	On	On	On	Off	Off	Off	On
Verify/Current Force															
On	Off	On	Off	On	On	Off	Off	Off	On	On	On	Off	Off	Off	On
Disconnect															
X	X	X	On	Off	X	X	On	Off	Off	On	Off	Off	Off	On	Off
DAC2 Select: Enabled															
X	X	X	X	X	Off	On	X	X	X	X	X	X	X	X	X

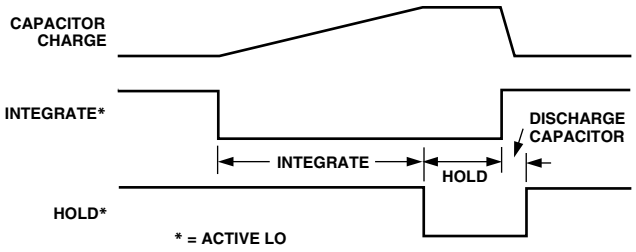


Figure 1. Integrate/Current Measure Timing Diagram

Table II. Truth Table

* = Active LO	FV/MI 2 mA		FV/MI 200 mA		FV/MI Integrate DAC1			FV/MI Integrate DAC 2			FI/MV 2 mA		FI/MV 200 µA		FV/Verify		FI/Verify		Disconnect	Disable
Control Input	DAC1	DAC2	DAC1	DAC2	Voltage Settle	Inte-grate	Hold	Voltage Settle	Inte-grate	Hold	DAC1	DAC2	DAC1	DAC2	DAC1	DAC2	DAC1	DAC2		Output Connected
M_CON*	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	X	X
VERIFY*	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	LO	LO	LO	LO	X	X
FORCE_I*	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	LO	LO	LO	LO	HI	HI	LO	LO	X	X
FORCE_EN*	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	X	HI
DAC1_SEL*	LO	HI	LO	HI	LO	LO	LO	HI	HI	HI	LO	HI	LO	HI	LO	HI	LO	HI	X	X
INTEG*	HI	HI	HI	HI	HI	LO	LO	HI	LO	LO	HI	HI	HI	HI	HI	HI	HI	HI	X	X
HOLD*	HI	HI	HI	HI	HI	HI	LO	HI	HI	LO	HI	HI	HI	HI	HI	HI	HI	HI	X	X
I_RANGE0*	LO	LO	HI	HI	HI	HI	HI	HI	HI	HI	LO	LO	HI	HI	X	X	X	X	X	X
I_RANGE1*	HI	HI	LO	LO	HI	HI	HI	HI	HI	HI	HI	HI	LO	LO	X	X	X	X	X	X
OUTPUT_CON*	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	HI	LO

PPMU APPLICATION NOTES

The PPMU can be used in two modes: 1. VOLTAGE FORCE with CURRENT MEASURE or VERIFY CURRENT FORCE; 2. CURRENT FORCE with VOLTAGE MEASURE or VERIFY VOLTAGE FORCE. In both modes the following setup is recommended:

1. The value of the external integrate capacitor (EXT_RC to C1) is 10 nF.
2. MEAS_OUT pin is loaded with 1 MΩ to ground.
3. V_{CC} = 15.0 V, V_{DD} = 4.5 V, DIGGND = 0.0 V, V_{EE} = –10 V, DSR = 2.5 V unless otherwise stated.
4. A 10 Ω resistor in series with the FORCE pin.
5. A 1 kΩ resistor in series with the SENSE pin.

IN VOLTAGE FORCE WITH CURRENT MEASURE OR VERIFY CURRENT FORCE

To measure the leakage in the current measure and hold mode, the PPMU has to be into the Force Voltage/Measure Current Integrate mode.

1. The FORCE_A (Force Output) pin has to be programmed to 9 V.
2. The PPMU has to be programmed to INTEGRATE mode.
3. The PPMU has to be programmed to HOLD mode.
4. Sample MEAS_OUT.
5. Wait 100 ms.
6. Sample MEAS_OUT again.
7. The difference between 2 and 4 must be less than 15 mV.

The linearity tests for forcing voltage are as follows (at the FORCE pin):

1. The four ranges of CURRENT MEASURE ranges (200 nA, 20 μA, 200 μA, and 2 mA) correspond to F1, F2, F3, and F4.
2. The endpoints of the linearity curve are determined by –full scale (or LOW), and the +full scale (or HIGH) readings at the same FORCE pin current.
3. Using these endpoints, gain nonlinearity is computed and tested at the 1/4 scale, 1/2 scale, and 3/4 scale points.
4. Computations for F1 are:
   F1 × 0.25 = LOW + 1 × (HIGH – LOW)/4
   F1 × 0.50 = LOW + 2 × (HIGH – LOW)/4
   F1 × 0.75 = LOW + 3 × (HIGH – LOW)/4

   Where LOW = –Full Scale and HIGH = +Full Scale.

The linearity tests for measuring current are as follows (at the MEAS_OUT pin):

1. The voltage is constant for these measurements.
2. The four ranges (M1, M2, M3, M4) correspond to CURRENT MEASURE ranges (200 nA, 20 μA, 200 μA, and 2 mA respectively).
3. The endpoints of the linearity curve are determined by the –full scale (or LOW), and the +full scale (or HIGH) readings at the same FORCE pin voltage.
4. Using these endpoints, gain nonlinearity is computed and tested at the 1/4 scale, 1/2 scale, and 3/4 scale points.
5. Computations for M1 are:
   M1 × 0.25 = LOW + 1 × (HIGH – LOW)/4
   M1 × 0.50 = LOW + 2 × (HIGH – LOW)/4
   M1 × 0.75 = LOW + 3 × (HIGH – LOW)/4

   Where LOW = –Full Scale, and HIGH = +Full Scale.

The M_CON pin can be used for disconnecting the MEAS_OUT pin by:

1. Raising M_CON to 2.4 V.
2. Measuring MEAS_OUT (which is loaded with 100 kΩ).
3. MEAS_OUT should ideally be 0 V.

The OUTPUT_CON pin can be used for disconnecting the DUT by:

1. Disabling the SENSE pin (OUTPUT_CON = 2.4 V).
2. Loading FORCE_OUT with 2 kΩ to ground.
3. Programming the DAC1 input to +FS (+9 V) and measuring the FORCE_OUT voltage (FV1).
4. Programming the DAC1 input to –FS (–4 V) and measuring the FORCE_OUT voltage (FV2).
5. FV1–FV2 < 1.3 mV.
6. A change of 1.3 mV implies a switch off-resistance of 20 MΩ.

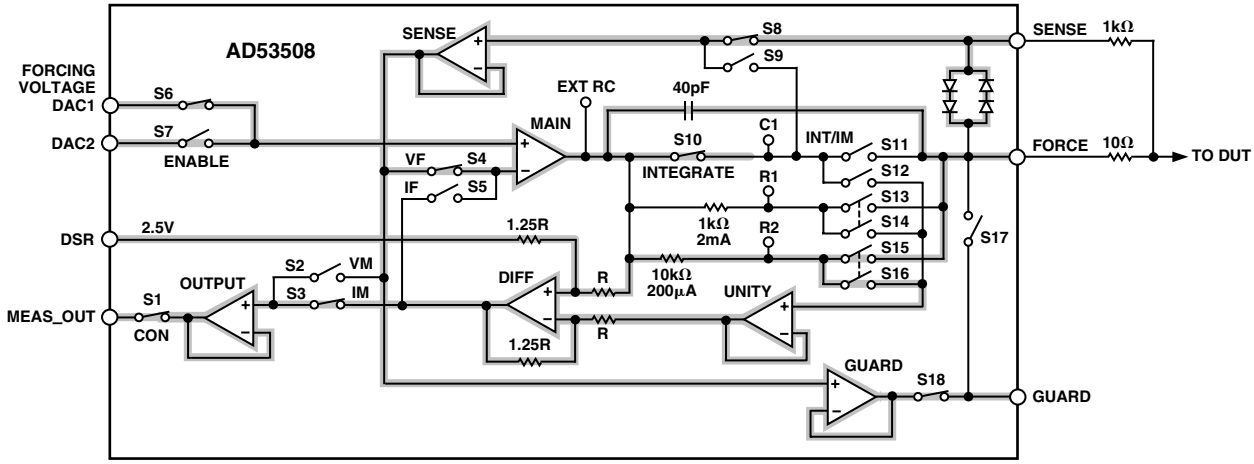


Figure 2. Guarded Voltage Force/Current Measure, $I_{RANGE\ 1}$: I ≤ 2 mA

IN CURRENT FORCE WITH VOLTAGE MEASURE OR VERIFY CURRENT FORCE

The linearity tests for forcing current at the FORCE pin:

1. The FORCE pin is loaded with a voltage source.
2. The two ranges of CURRENT FORCE ranges (2 mA and 200 μA) correspond to F1 and F2. The endpoints of the linearity curve are determined by full scale (or LOW), and the full scale (or HIGH) readings at the same FORCE pin voltage.
3. Using these endpoints, gain nonlinearity is computed and tested at the 1/4 scale, 1/2 scale, and 3/4 scale points.
4. Computations for F1 are:
   F1 × 0.25 = LOW + 1 × (HIGH – LOW)/4
   F1 × 0.50 = LOW + 2 × (HIGH – LOW)/4
   F1 × 0.75 = LOW + 3 × (HIGH – LOW)/4

   Where LOW = –Full Scale and HIGH = +Full Scale.

The linearity test for measuring voltage is as follows (at the MEAS_OUT pin):

1. The endpoints of the linearity curve are determined by the –full scale (or LOW), and the +full scale (or HIGH) readings.
2. Using these endpoints, gain nonlinearity is computed and tested at the 1/4 scale, 1/2 scale, and 3/4 scale points.
3. Computations for M1 are:
   M1 × 0.25 = LOW + 1 × (HIGH – LOW)/4
   M1 × 0.50 = LOW + 2 × (HIGH – LOW)/4
   M1 × 0.75 = LOW + 3 × (HIGH – LOW)/4

   Where LOW = –Full Scale, and HIGH = +Full Scale.

CURRENT FORCE WITH VOLTAGE MEASURE (2 mA RANGE)

1. DAC1 = 5 V.
2. FORCE pin loaded with 9 V source.
3. Measure current at FORCE.
4. Measure voltage at MEAS_OUT.
5. V_{CC} = 15 V.
6. Measure current at FORCE and compare to 3.
7. Measure voltage at MEAS_OUT and compare to 4.
8. V_{CC} = 15 V.
9. DAC1 = 0 V.
10. FORCE pin loaded with –4 V source.
11. Measure current at FORCE.
12. Measure voltage at MEAS_OUT.
13. V_{EE} = –9.5 V.
14. Measure current at FORCE and compare to 11.
15. Measure voltage at MEAS_OUT and compare to 12.
16. V_{EE} = –10 V.

VOLTAGE FORCE WITH CURRENT MEASURE (2 mA RANGE)

1. DAC1 = 9 V.
2. FORCE pin loaded with 2 mA current source.
3. Measure voltage at FORCE.
4. Measure current at MEAS_OUT.
5. V_{CC} = 14.25 V.
6. Measure voltage at FORCE and compare to 3:
   Limit = ±237 μV.
7. Measure current at MEAS_OUT and compare to 4:
   Limit = ±237 μV.
8. V_{CC} = 15 V.
9. DAC1 = –4 V.
10. FORCE pin loaded with 2 mA current sink.
11. Measure voltage at FORCE.
12. Measure current at MEAS_OUT.
13. V_{EE} = –9.5 V.
14. Measure voltage at FORCE and compare to 11:
   Limit = ±474 μV.
15. Measure current at MEAS_OUT and compare to 12.
16. V_{EE} = –10 V.

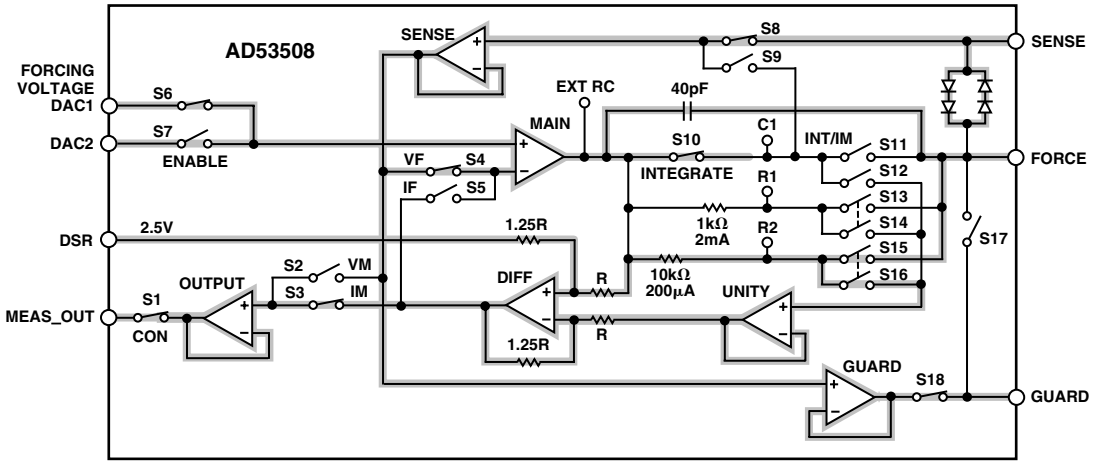


Figure 3. Guarded Current Force/Voltage Measure, $I_{RANGE\ 1}$: I ≤ 2 mA

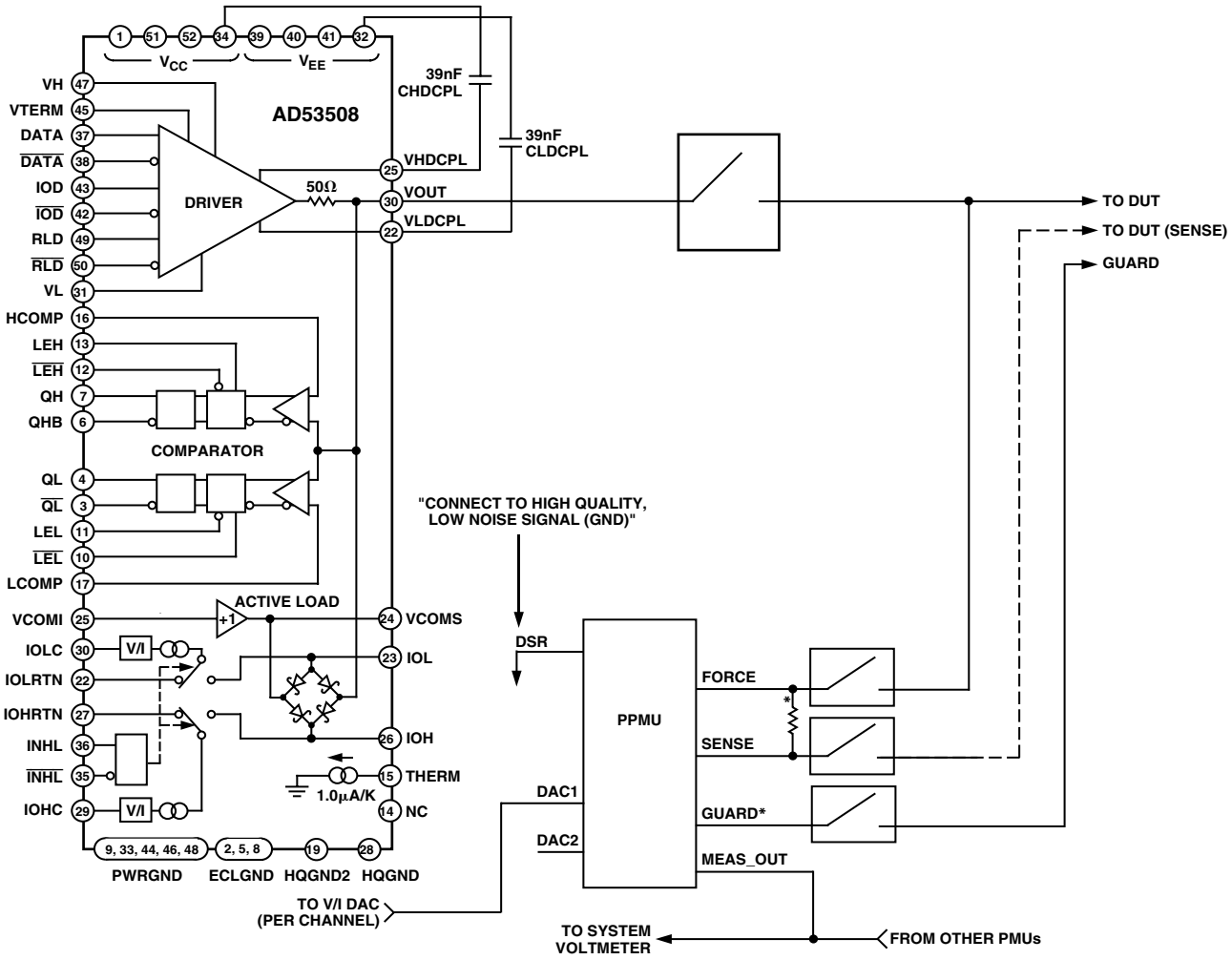


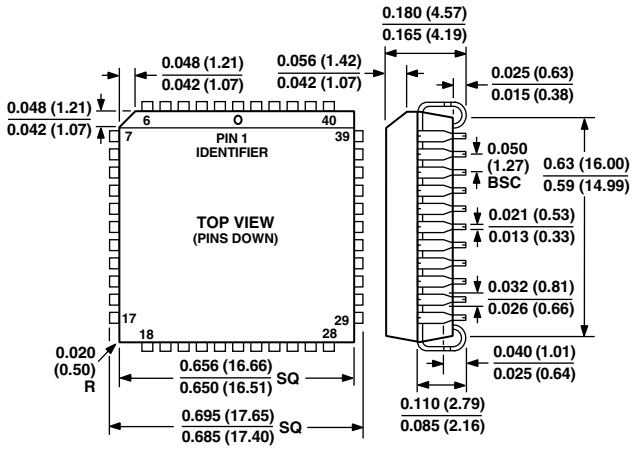
Figure 4. Recommended Use of the PPMU with a DCL

C00684–0–6/01(A)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Leaded Chip Carrier (PLCC)
(P-44A)



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