TLF35584

Multi Voltage Safety Micro Processor Supply

TLF35584QVVS1
TLF35584QVVS2
TLF35584QKVS1
TLF35584QKVS2

Data Sheet

Rev. 2.0, 2017-03-16

Automotive Power

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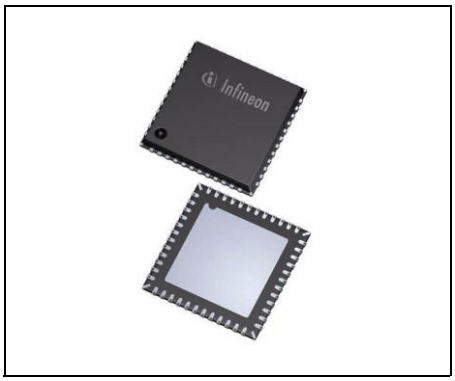
1 Overview



PG-VQFN-48

PG-LQFP-64

Features

- High efficient multi voltage power supply chip
- Serial step up and step down pre regulator for wide input voltage range from 3.0 to 40 V with full performance and low over all power loss
- Low drop post regulator 5.0V/200mA for communication supply (named LDO_Com)
- Low drop post regulator 5.0 V/600 mA (TLF35584xxVS1) or 3.3 V/600 mA (TLF35584xxVS2) for µC supply (named LDO_µC)
- Provides enable, sync out signal and voltage monitoring (inside device to be added to reset function) for an optional external post regulator for core supply
- Voltage reference 5.0 V +/- 1% for ADC supply, 150 mA current capability (named Volt_Ref)
- Two trackers for sensor supply following voltage reference 150 mA current capability each (named Tracker 1 and Tracker 2)
- Standby regulator 5.0 V/10 mA (TLF35584xxVS1) or 3.3 V/10 mA (TLF35584xxVS2) (named LDO_Stby)
- Independent voltage monitoring block with reset function
- Configurable functional and window watchdog
- 16-bit SPI
- Safe state control with two safe state signals with programmable delay
- Input voltage monitoring (over voltage switch off)
- Green Product (RoHS compliant)
- ISO26262 compliant
- AEC Qualified

Type	Package	Marking (Line1 / Line2)
TLF35584QVVS1 (5.0 V Variant)	PG-VQFN-48	35584 / VS1
TLF35584QVVS2 (3.3 V Variant)	PG-VQFN-48	35584 / VS2
TLF35584QKVS1 (5.0 V Variant)	PG-LQFP-64	TLF35584 / QK VS1
TLF35584QKVS2 (3.3 V Variant)	PG-LQFP-64	TLF35584 / QK VS2

2 Block Diagram

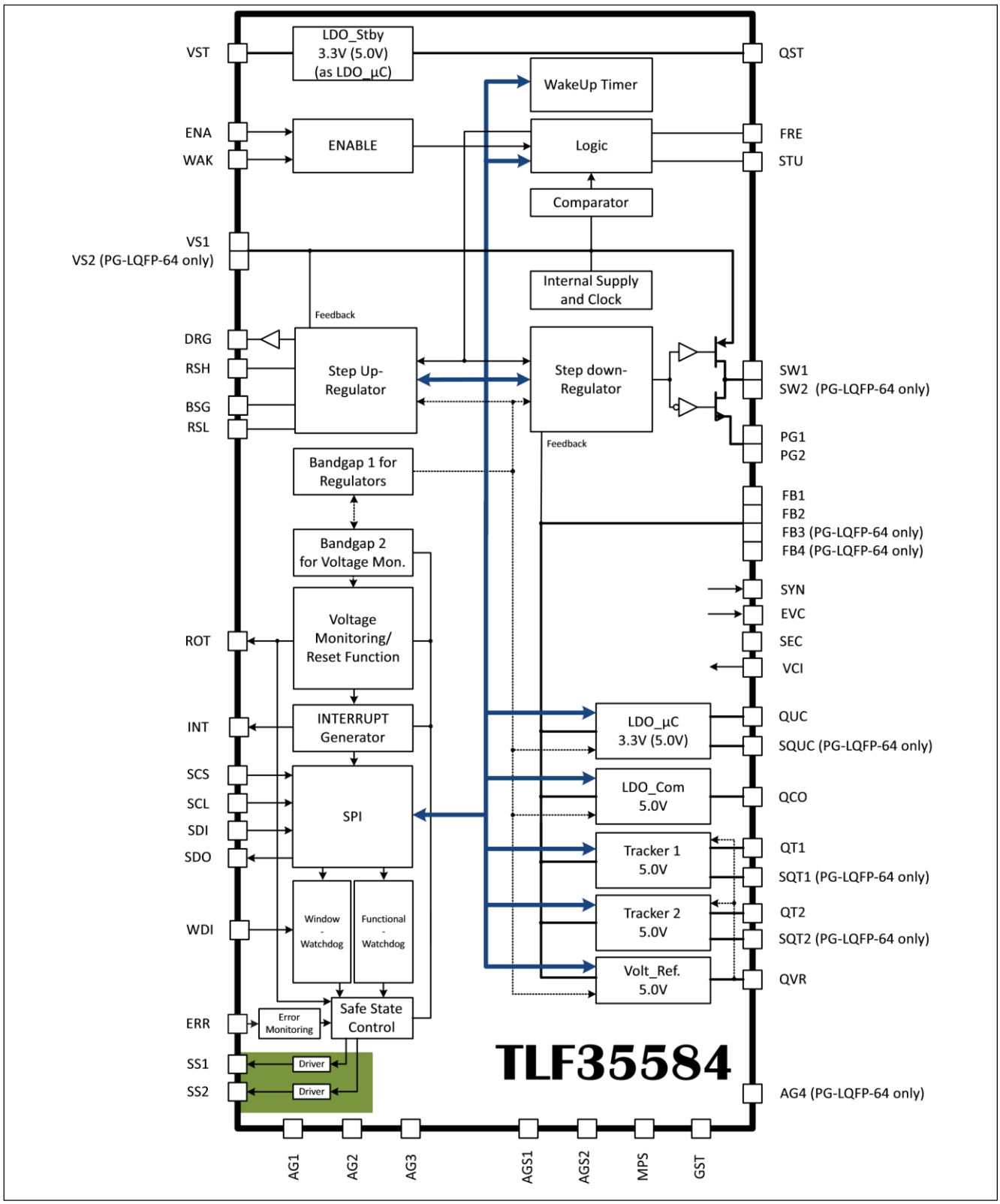


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment - PG-VQFN-48

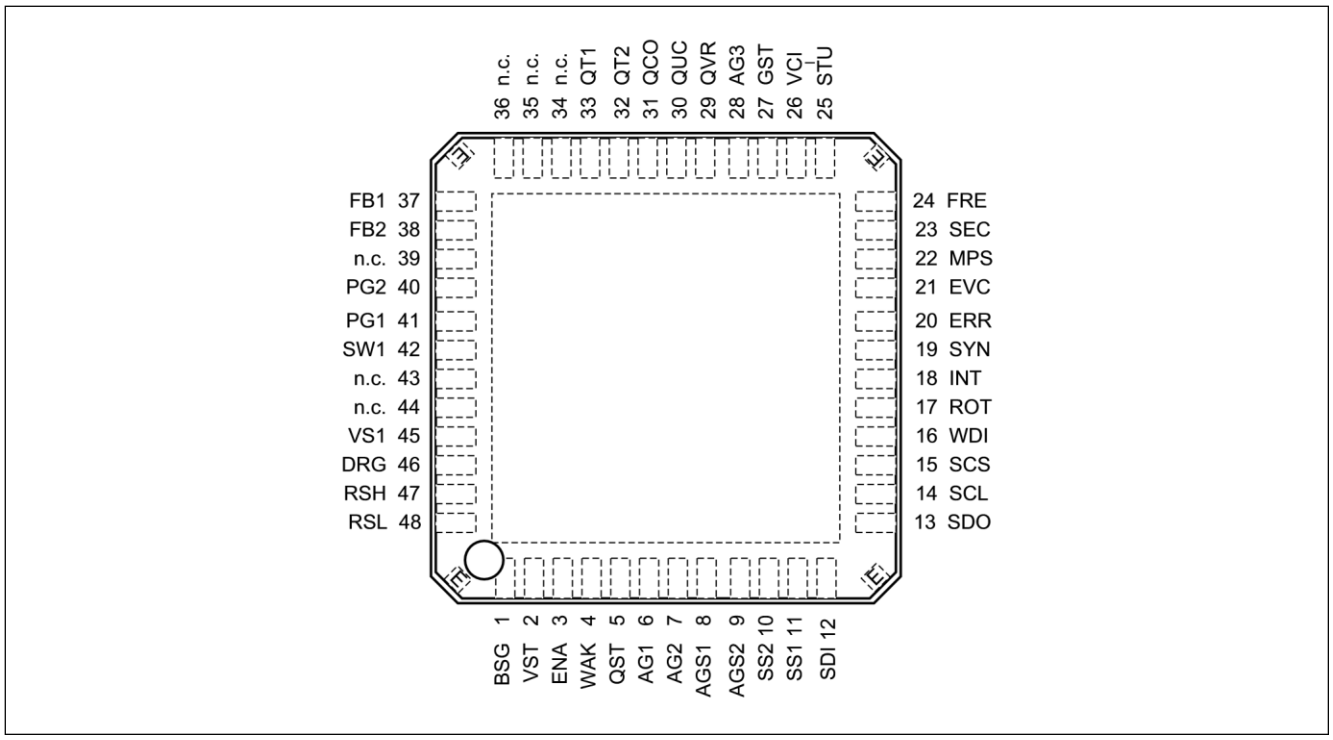


Figure 2 Pin Configuration - PG-VQFN-48

3.2 Pin Definitions and Functions - PG-VQFN-48

Pin	Symbol	Function
1	BSG	**Boost driver ground:** Connect this pin to ground at the low side of an external current sense resistor to decouple the driver noise from the sensitive ground. If step up pre regulator option is not used, connect to ground.
2	VST	**Supply voltage standby regulator, input:** Connect this input to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
3	ENA	**Enable Input:** A positive edge signal at this pin will wake the device. In case of not used connect to ground.
4	WAK	**Wake/Inhibit Input:** A high level signal of defined length at this pin will wake the device. In case of not used, connect to ground.

Pin	Symbol	Function
5	QST	**Output standby LDO:** Connect a capacitor as close as possible to pin.
6	AG1	**Analogue ground, pin 1:** Connect this pin directly (low ohmic and low inductive) to ground.
7	AG2	**Analogue ground, pin 2:** Connect this pin directly (low ohmic and low inductive) to ground.
8	AGS1	**Analogue ground, safety, pin 1:** Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
9	AGS2	**Analogue ground, safety, pin 2:** Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
10	SS2	**Safe state signal 2:** Safe state output signal 2, sets the application into a safe state. Signal is delayed against SS1, delay can be adjusted via SPI command.
11	SS1	**Safe state signal 1:** Safe state output signal 1, sets the application into a safe state.
12	SDI	**Serial peripheral interface, signal data input:** SPI signalling port, connect to SPI port “data output” of micro processor to receive commands during SPI communication.
13	SDO	**Serial peripheral interface, signal data output:** SPI signalling port, connect to SPI port “data input” of micro processor to send status information during SPI communication.
14	SCL	**Serial peripheral interface, signal clock:** SPI signalling port, connect to SPI port “clock” of micro processor to clock the device for SPI communication.
15	SCS	**Serial peripheral interface, signal chip select:** SPI signalling port, connect to SPI port “chip select” of micro processor to address the device for SPI communication.
16	WDI	**Watchdog input, trigger signal:** Input for trigger signal, connect the “trigger signal output” of the micro processor to this pin. In case of not used, leave open (internal pull-down).
17	ROT	**Reset output:** Open drain structure with internal pull-up current source. A low signal at this pin indicates a reset event.
18	INT	**Interrupt signal:** Push-pull-stage. A low pulse at this pin indicates an interrupt, the micro processor shall read out the SPI status registers. Connect to a non maskable interrupt port (NMI) of the micro processor core supply voltage.

19	SYN	**Synchronization output signal:** Connect this output to the optional external switch mode post regulator synchronization input. The signal delivers the step down regulator switching frequency either in phase or shifted by 180° (selectable via SPI command). The switch mode post regulator shall synchronize to the rising edge. If not used, leave open.

Pin	Symbol	Function
20	ERR	**Error signal input:** Input for error signal from micro processor safety managing unit (SMU, internal failure detection of the micro processor). Connect the “error signal output” of the micro processor to this pin.
21	EVC	**Enable external post regulator for core supply:** Connect this pin to the enable input of the external post regulator. If not used, leave open.
22	MPS	**Microcontroller programming support pin**: Pull down this pin to ground for operation. Optionally, this pin can be used for microcontroller debugging and programming purposes. For details please refer to **Chapter 11.7**.
23	SEC	**Configuration pin for external post regulator for core supply:** Connect this pin to ground if the option external post regulator is not used. If the option external post regulator is used, leave open.
24	FRE	**Frequency adjustment pin:** Connect pin to ground for low frequency range or leave open for high frequency range.
25	STU	**Configuration pin for step up converter:** Connect this pin to ground if the option step up pre regulator is not used. If the option step up pre regulator is used, leave open.
26	VCI	**Input for optional external post regulator output voltage (core supply):** Connect an external resistor divider to adjust the over and under voltage thresholds of reset output signal ROT. If the option external post regulator is not used, leave open.
27	GST	**Gate stress pin:** Not for customer use. Connect this pin directly (low ohmic and low inductive) to ground.
28	AG3	**Analogue ground, pin 3:** Connect this pin directly (low ohmic and low inductive) to ground.
29	QVR	**Output voltage reference:** Connect a capacitor as close as possible to pin.
30	QUC	**Output LDO_uC supply (micro processor supply):** Connect a capacitor as close as possible to pin.
31	QCO	**Output LDO_communication supply:** Connect a capacitor as close as possible to pin.
32	QT2	**Output tracker 2:** Connect a capacitor as close as possible to pin.

33	QT1	**Output tracker 1:** Connect a capacitor as close as possible to pin.
34	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.

Pin	Symbol	Function
35	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
36	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
37	FB1	**Step down pre regulator feedback input plus input for linear post regulators and trackers, pin 1:** Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB2.
38	FB2	**Step down pre regulator feedback input plus input for linear post regulators and trackers, pin 2:** Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB1.
39	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
40	PG2	**Step down pre regulator power ground, pin 2:** Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PG1.
41	PG1	**Step down pre regulator power ground, pin 1:** Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PG2.
42	SW1	**Step down pre regulator power stage output:** Connect this pin straight (low ohmic and low inductive) to the pre regulator output filter.
43	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.

44	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
45	VS1	**Supply voltage step down pre regulator input:** Connect this input to the output of the step up pre regulator. If step up pre regulator option is not used, connect to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.

Pin	Symbol	Function
46	DRG	**Driver output for external step up regulator power stage, connect to gate:** Gate of low side switch of step up pre regulator: Connect to the gate of an external N-channel mosfet, line to be straight and as short as possible. If step up pre regulator option is not used, leave open.
47	RSH	**Sense resistor for external step up regulator power stage, high side:** Connect this pin to the high side of an external current sense resistor to determine the maximum current threshold through the external N-channel mosfet. If step up pre regulator option is not used, connect to ground.
48	RSL	**Sense resistor for external step up regulator power stage, low side:** Connect this pin to the low side of an external current sense resistor to determine the maximum current threshold through the external N-channel mosfet. If step up pre regulator option is not used, connect to ground.
	EP1	**Edge pin no 1:** Keep area below this pin free of ground or other signals, do not solder this pin to ground or any other signal. This pin must be kept free of soldering.
	EP2	**Edge pin no 2:** Keep area below this pin free of ground or other signals, do not solder this pin to ground or any other signal. This pin must be kept free of soldering.
	EP3	**Edge pin no 3:** Keep area below this pin free of ground or other signals, do not solder this pin to ground or any other signal. This pin must be kept free of soldering.
	EP4	**Edge pin no 4:** Keep area below this pin free of ground or other signals, do not solder this pin to ground or any other signal. This pin must be kept free of soldering.
Cooling Tab	GND	Cooling Tab. Connect externally to GND and heat sink area.

3.3 Pin Assignment - PG-LQFP-64

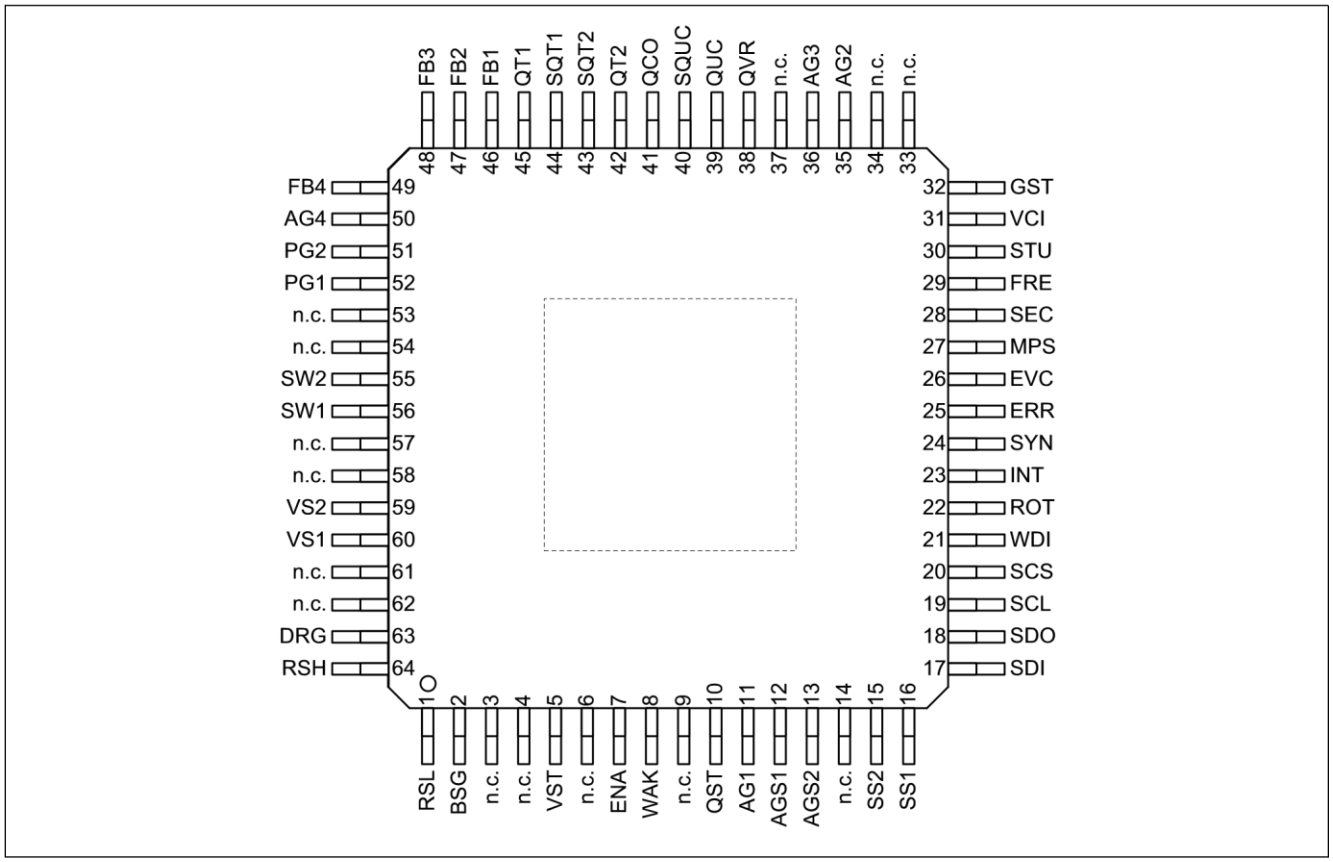


Figure 3 Pin Configuration - PG-LQFP-64

3.4 Pin Definitions and Functions - PG-LQFP-64

Pin	Symbol	Function
1	RSL	**Sense resistor for external step up regulator power stage, low side:** Connect this pin to the low side of an external current sense resistor to determine the maximum current threshold through the external N-channel mosfet. If step up pre regulator option is not used, connect to ground.
2	BSG	**Boost driver ground:** Connect this pin to ground at the low side of an external current sense resistor to decouple the driver noise from the sensitive ground. If step up pre regulator option is not used, connect to ground.
3	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
Pin	**Symbol**	**Function**

4	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
5	VST	**Supply voltage standby regulator, input:** Connect this input to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
6	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
7	ENA	**Enable Input:** A positive edge signal at this pin will wake the device. In case of not used, connect to ground.
8	WAK	**Wake/Inhibit Input:** A high level signal of defined length at this pin will wake the device. In case of not used, connect to ground.
9	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
10	QST	**Output standby LDO:** Connect a capacitor as close as possible to pin.
11	AG1	**Analogue ground, pin 1:** Connect this pin directly (low ohmic and low inductive) to ground.
12	AGS1	**Analogue ground, safety, pin 1:** Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
13	AGS2	**Analogue ground, safety, pin 2:** Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
14	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
15	SS2	**Safe state signal 2:** Safe state output signal 2, sets the application into a safe state. Signal is delayed against SS1, delay can be adjusted via SPI command.
16	SS1	**Safe state signal 1:** Safe state output signal 1, sets the application into a safe state.

17	SDI	**Serial peripheral interface, signal data input:** SPI signalling port, connect to SPI port “data output” of micro processor to receive commands during SPI communication.
18	SDO	**Serial peripheral interface, signal data output:** SPI signalling port, connect to SPI port “data input” of micro processor to send status information during SPI communication.

Pin	Symbol	Function
19	SCL	**Serial peripheral interface, signal clock:** SPI signalling port, connect to SPI port “clock” of micro processor to clock the device for SPI communication.
20	SCS	**Serial peripheral interface, signal chip select:** SPI signalling port, connect to SPI port “chip select” of micro processor to address the device for SPI communication.
21	WDI	**Watchdog input, trigger signal:** Input for trigger signal, connect the “trigger signal output” of the micro processor to this pin. In case of not used, leave open (internal pull-down).
22	ROT	**Reset output:** Open drain structure with internal pull-up current source. A low signal at this pin indicates a reset event.
23	INT	**Interrupt signal:** Push-pull-stage. A low pulse at this pin indicates an interrupt, the micro processor shall read out the SPI status registers. Connect to a non maskable interrupt port (NMI) of the micro processor core supply voltage.
24	SYN	**Synchronization output signal:** Connect this output to the optional external switch mode post regulator synchronization input. The signal delivers the step down regulator switching frequency either in phase or shifted by 180° (selectable via SPI command). The switch mode post regulator shall synchronize to the rising edge. If not used, leave open.
25	ERR	**Error signal input:** Input for error signal from micro processor safety managing unit (SMU, internal failure detection of the micro processor). Connect the “error signal output” of the micro processor to this pin.
26	EVC	**Enable external post regulator for core supply:** Connect this pin to the enable input of the external post regulator. If not used, leave open.
27	MPS	**Microcontroller programming support pin**: Pull down this pin to ground for operation. Optionally, this pin can be used for microcontroller debugging and programming purposes. For details please refer to **Chapter 11.7**.

28	SEC	**Configuration pin for external post regulator for core supply:** Connect this pin to ground if the option external post regulator is not used. If the option external post regulator is used, leave open.
29	FRE	**Frequency adjustment pin:** Connect pin to ground for low frequency range or leave open for high frequency range.
30	STU	**Configuration pin for step up converter:** Connect this pin to ground if the option step up pre regulator is not used. If the option step up pre regulator is used, leave open.
31	VCI	**Input for optional external post regulator output voltage (core supply):** Connect an external resistor divider to adjust the over and under voltage thresholds of reset output signal ROT. If the option external post regulator is not used, leave open.

Pin	Symbol	Function
32	GST	**Gate stress pin:** Not for customer use. Connect this pin directly (low ohmic and low inductive) to ground.
33	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
34	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
35	AG2	**Analogue ground, pin 2:** Connect this pin directly (low ohmic and low inductive) to ground.
36	AG3	**Analogue ground, pin 3:** Connect this pin directly (low ohmic and low inductive) to ground.
37	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
38	QVR	**Output voltage reference:** Connect a capacitor as close as possible to pin.
39	QUC	**Output LDO_uC supply (micro processor supply):** Connect a capacitor as close as possible to pin.
40	SQUC	**Sense connection for LDO_uC supply (micro processor supply):** Connect to QUC/LDO_uC externally.
41	QCO	**Output LDO_communication supply:** Connect a capacitor as close as possible to pin.

42	QT2	**Output tracker 2:** Connect a capacitor as close as possible to pin.
43	SQT2	**Sense connection tracker 2:** Connect to QT2/tracker 2 externally.
44	SQT1	**Sense connection tracker 1:** Connect to QT1/tracker 1 externally.
45	QT1	**Output tracker 1:** Connect a capacitor as close as possible to pin.
46	FB1	**Step down pre regulator feedback input plus input for linear post regulators and trackers, pin 1:** Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB1 - FB4.
47	FB2	**Step down pre regulator feedback input plus input for linear post regulators and trackers, pin 2:** Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB1 - FB4.

Pin	Symbol	Function
48	FB3	**Step down pre regulator feedback input plus input for linear post regulators and trackers, pin 3:** Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB1 - FB4.
49	FB4	**Step down pre regulator feedback input plus input for linear post regulators and trackers, pin 4:** Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB1 - FB4.
50	AG4	**Analogue ground, pin 4:** Connect this pin directly (low ohmic and low inductive) to ground.
51	PG2	**Step down pre regulator power ground, pin 2:** Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PG1.
52	PG1	**Step down pre regulator power ground, pin 1:** Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PG2.
53	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.

54	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
55	SW2	**Step down pre regulator power stage output, pin 2:** Connect this pin straight (low ohmic and low inductive) to the pre regulator output filter. Always connect in parallel with pin SW1.
56	SW1	**Step down pre regulator power stage output, pin 1:** Connect this pin straight (low ohmic and low inductive) to the pre regulator output filter. Always connect in parallel with pin SW2.
57	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
58	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
59	VS2	**Supply voltage step down pre regulator, pin 2, input:** Connect this input in parallel with VS1 to the output of the step up pre regulator. If step up pre regulator option is not used, connect in parallel with VS1 to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.

Pin	Symbol	Function
60	VS1	**Supply voltage step down pre regulator, pin 1, input:** Connect this input in parallel with VS2 to the output of the step up pre regulator. If step up pre regulator option is not used, connect in parallel with VS2 to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
61	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
62	N.C.	**Internally not connected:** This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
63	DRG	**Driver output for external step up regulator power stage, connect to gate:** Gate of low side switch of step up pre regulator: Connect to the gate of an external N-channel mosfet, line to be straight and as short as possible. If step up pre regulator option is not used, leave open.

64	RSH	**Sense resistor for external step up regulator power stage, high side:** Connect this pin to the high side of an external current sense resistor to determine the maximum current threshold through the external N-channel mosfet. If step up pre regulator option is not used, connect to ground.
Cooling Tab	GND	Cooling Tab. Connect externally to GND and heat sink area.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Boost driver ground	V_{BSG}	-0.3	–	0.3	V	–	P_4.1.1
Input standby LDO	V_{VST}	-0.3	–	40	V	2) 3)	P_4.1.2
Input voltage pin 1 (pre regulator)	V_{VS1}	-0.3	–	40	V	2) 3)	P_4.1.3
Input voltage pin 2 (pre regulator)	V_{VS2}	-0.3	–	40	V	2) 3) PG-LQFP-64 only	P_4.1.4
External step up power stage, gate	V_{DRG}	-0.3	–	40	V	2) 3)	P_4.1.5
External power stage, sense resistor high	V_{RSH}	-0.3	–	40	V	2) 3)	P_4.1.6
External power stage, sense resistor low	V_{RSL}	-0.3	–	6.0	V	–	P_4.1.7
Enable	V_{ENA}	-0.3	–	40	V	2) 3)	P_4.1.8
Enable	I_{ENA}	-5	–	–	mA	4)	P_4.1.9
Wake/Inhibit	V_{WAK}	-0.3	–	40	V	2) 3)	P_4.1.10
Wake/Inhibit	I_{WAK}	-5	–	–	mA	4)	P_4.1.11
Reset output	V_{ROT}	-0.3	–	6.0	V	–	P_4.1.12
SPI: Chip select CS	V_{SCS}	-0.3	–	6.0	V	–	P_4.1.13
SPI: Clock CLK	V_{SCL}	-0.3	–	6.0	V	–	P_4.1.14
SPI: Data_In DI	V_{SDI}	-0.3	–	6.0	V	–	P_4.1.15
SPI: Data_Out DO	V_{SDO}	-0.3	–	6.0	V	–	P_4.1.16
Interrupt	V_{INT}	-0.3	–	6.0	V	–	P_4.1.17
Window watchdog trigger	V_{WDI}	-0.3	–	6.0	V	–	P_4.1.18
Error pin	V_{ERR}	-0.3	–	6.0	V	–	P_4.1.19

Safe state 1	V_{SS1}	-0.3	–	6.0	V	–	P_4.1.20
Safe state 2	V_{SS2}	-0.3	–	6.0	V	–	P_4.1.21
Output voltage reference	V_{QVR}	-0.3	–	6.0	V	–	P_4.1.22
Output tracker 2	V_{QT2}	-0.3	–	40	V	–	P_4.1.23
Sense Pin for tracker 2	V_{SQT2}	-0.3	–	40	V	PG-LQFP-64 only	P_4.1.24
Output tracker 1	V_{QT1}	-0.3	–	40	V	–	P_4.1.25

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Sense Pin for tracker 1	V_{SQT1}	-0.3	–	40	V	PG-LQFP-64 only	P_4.1.26
Output LDO_Com	V_{QCO}	-0.3	–	6.0	V	–	P_4.1.27
Output LDO_µC	V_{QUC}	-0.3	–	6.0	V	–	P_4.1.28
Sense Pin for LDO_µC	V_{SQUC}	-0.3	–	6.0	V	PG-LQFP-64 only	P_4.1.29
V_Core_Mon ext core supply	V_{VCI}	-0.3	–	6.0	V	–	P_4.1.30
Select ext core supply	V_{SEC}	-0.3	–	6.0	V	–	P_4.1.31
Sync_Out ext core supply	V_{SYN}	-0.3	–	6.0	V	–	P_4.1.32
Enable ext core supply	V_{EVC}	-0.3	–	6.0	V	–	P_4.1.33
FB_BUCK4	V_{FB4}	-0.3	–	7.0	V	PG-LQFP-64 only	P_4.1.35
FB_BUCK3	V_{FB3}	-0.3	–	7.0	V	PG-LQFP-64 only	P_4.1.36
FB_BUCK2	V_{FB2}	-0.3	–	7.0	V	–	P_4.1.37
FB_BUCK1	V_{FB1}	-0.3	–	7.0	V	–	P_4.1.38
BU_GND2	V_{PG2}	-0.3	–	0.3	V	–	P_4.1.39
BU_GND1	V_{PG1}	-0.3	–	0.3	V	–	P_4.1.40
SW2	V_{SW2}	-0.3	–	40	V	PG-LQFP-64 only	P_4.1.41
SW1	V_{SW1}	-0.3	–	40	V	–	P_4.1.42
Select step up pre regulator	V_{STU}	-0.3	–	6.0	V	–	P_4.1.43
FRE	V_{FRE}	-0.3	–	6.0	V	–	P_4.1.44
Q_STBY	V_{QST}	-0.3	–	6.0	V	–	P_4.1.45
MPS	V_{MPS}	-0.3	–	6.0	V	–	P_4.1.46
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.47
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.48
ESD Susceptibility							

ESD Susceptibility to GND	V_{ESD}	-2	–	2	kV	HBM[5)]	P_4.1.49
ESD Susceptibility to GND	V_{ESD}	-500	–	500	V	CDM[6)]	P_4.1.50
ESD Susceptibility (corner pins) to GND	$V_{ESD,Corner}$	-750	–	750	V	CDM[6)]	P_4.1.51

1) Not subject to production test, specified by design.
2) Maximum rating is 60 V, if rise time from 0 to 60 V is longer than 10 ms
3) Maximum rating is 49 V, for an overall time of 10 s (in the range of 40 V to 49 V) during the lifetime of the product independent from the rise time.
4) Consider external series resistor for negative voltages < -0.3 V to ensure maximum rating of current
5) ESD susceptibility, HBM according to JEDEC HBM Human Body Model ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)
6) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Note:Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			

Supply Voltage Range for Normal Operation at input of the step-up converter	V_{Bat}	3	–	40	V	with step up pre regulator active in front of step down pre regulator[1)]	P_4.2.1
Supply Voltage Range for Normal Operation at pin VSx	V_{VS}	6	–	40	V	without step up pre regulator active in front of step down pre regulator	P_4.2.2
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.3

1) To start up the TLF35584 needs a minimum input voltage of 6.0V at the pin VSx.

Note:Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note:This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	12.2	K/W	–	P_4.3.1
Junction to Soldering Point (pin)	R_{thJSP}	20.1	–	22.1	K/W	JEDEC 2s2p, measured to pin: VQFN: 1, 6, 7, 28 ; LQFP: 2, 11, 35, 50	P_4.3.2
Junction to Soldering Point (pin)	R_{thJSP}	34.9	–	37.6	K/W	JEDEC 1s0p, measured to pin: VQFN: 1, 6, 7, 28 ; LQFP: 2, 11, 35, 50	P_4.3.3
Junction to Soldering Point (soldering pad)	R_{thJSP}	11.0	–	14.7	K/W	JEDEC 2s2p	P_4.3.4
Junction to Soldering Point (soldering pad)	R_{thJSP}	13.1	–	18.0	K/W	JEDEC 1s0p	P_4.3.5
Junction to Ambient	R_{thJA}	–	37	–	K/W	[2)]	P_4.3.6

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Quiescent Current Consumption

Table 4 Quiescent current consumption [1)]

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

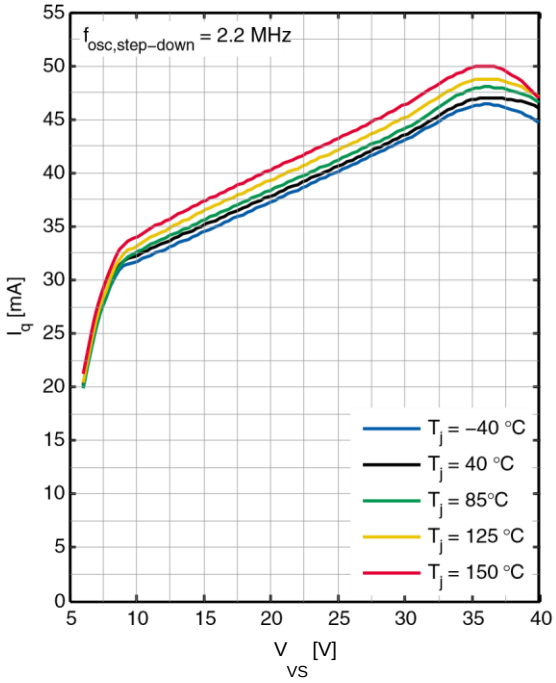
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
INIT state	I_q	–	–	45	mA	1) $T_j \leq 85°C$ Step-Up Converter is off, $f_{PREREG,BUCK}$ = 2.2 MHz	P_4.4.1
NORMAL state	I_q	–	–	45	mA	1) $T_j \leq 85°C$ Step-Up Converter is off, $f_{PREREG,BUCK}$ = 2.2 MHz	P_4.4.2
STANDBY state	I_q	–	–	70	µA	1) LDO_STBY is off V_{VS} = 14 V ; $T_j \leq 40°C$	P_4.4.3
STANDBY state	I_q	–	–	90	µA	LDO_STBY is off 1) $T_j \leq 85°C$	P_4.4.4
STANDBY state	I_q	–	–	120	µA	LDO_STBY is on 1) $T_j \leq 85°C$	P_4.4.5
SLEEP state	I_q	–	–	200	µA	1) $T_j \leq 85°C$	P_4.4.6
WAKE state	I_q	–	–	45	mA	1) $T_j \leq 85°C$ Step-Up Converter is off, $f_{PREREG,BUCK}$ = 2.2 MHz	P_4.4.7
FAILSAFE state	I_q	–	–	200	µA	1) $T_j \leq 85°C$; $t_{FAILSAFE}$ > $t_{FAILSAFE,min}$	P_4.4.8

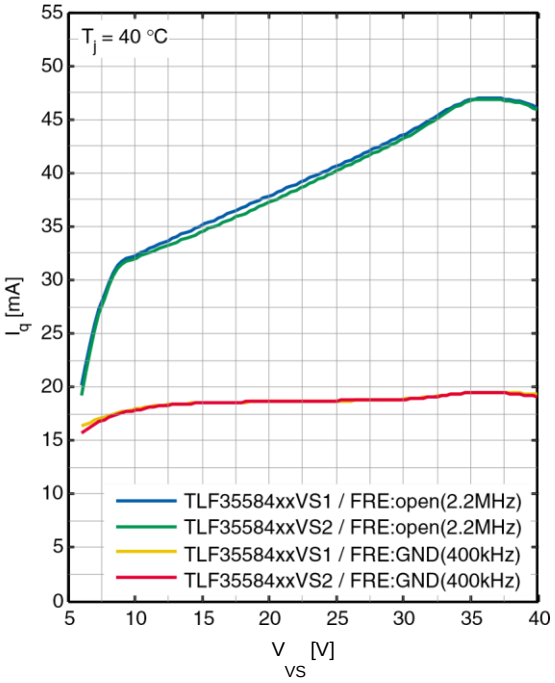
1) All quiescent current parameters are measured at $T_j \leq 85°C$ and 10 V ≤ V_{VS} ≤ 28 V with zero load and all selectable options (Outputs, Watchdog, Timers, Step-Up converter) switched off.

4.4.1 Typical Performance Characteristics

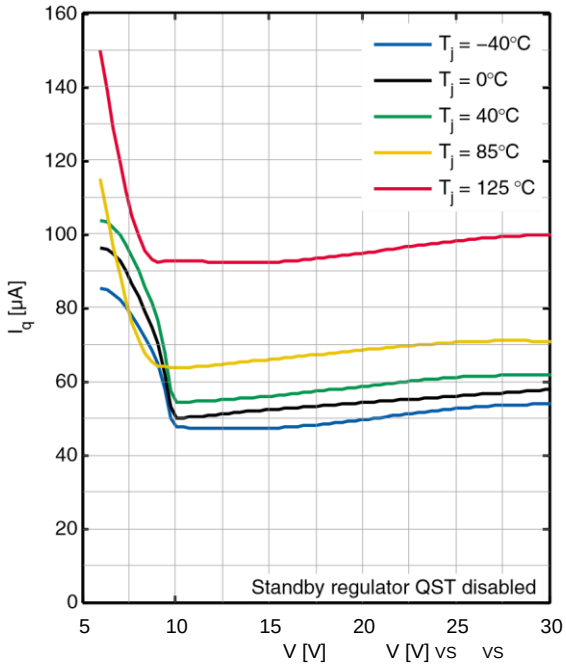
INIT, NORMAL and WAKE Current Consumption I_q versus Supply Voltage V_{VS} (FRE-Pin: open)

INIT, NORMAL and WAKE Current Consumption I_q versus Supply Voltage V_{VS} (various configuration)

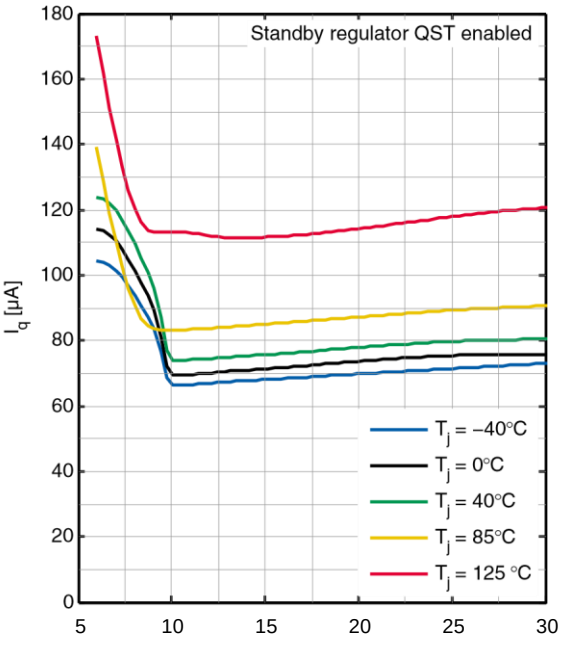




STANDBY Current Consumption I_q versus Supply Voltage V_{VS} (QST disabled)



STANDBY Current Consumption I_q versus Supply Voltage V_{VS} (QST enabled)



5 Wake Function

5.1 Introduction

The TLF35584 is automatically turned on when connected to a battery (Power-On-Reset POR) and moves into INIT-state, where the device will be configured. After successful configuration, the device will be sent to NORMAL state via SPI command. From NORMAL or WAKE state, the device can be sent to a low power state (SLEEP or STANDBY) via SPI commands. The WAK and ENA signal are external triggers to leave the low power states (or the FAILSAFE state).

Wake (pin WAK - level triggered) / Enable (pin ENA - edge triggered)

The WAK and ENA input pins are battery voltage level capable. A signal, with a voltage higher than $V_{WAK,hi}$ applied at pin WAK for $t_{WAK,min}$ represents a valid Wake-Signal. A positive going edge at pin ENA with a rise time $t_{ENA,rise}$ represents a valid Wake-Signal as well.

A valid Wake-Signal will bring the device from STANDBY to INIT state, from SLEEP to WAKE state or from FAILSAFE to INIT state.

A low signal $V_{WAK,lo}$ at pin WAK as well as a negative going edge at pin ENA will have no impact on the state machine and will not initiate a transition between states.

In case a valid Wake-Signal is detected during the transition phase from NORMAL to SLEEP state, the device will initiate a transition to WAKE state and generate an interrupt.

In case a valid Wake-Signal is detected during the transition phase from NORMAL to STANDBY state, the device will initiate a transition to INIT state and a Reset (ROT) will be generated.

Before sending a SPI transition command, pin ENA doesn't have to be brought below $V_{ENA,thrlo}$. Even if pin ENA is high (above $V_{ENA,thrhi}$), the SPI transition command will still send the device into SLEEP or STANDBY state.

For further details please refer to **Chapter 11 State Machine**.

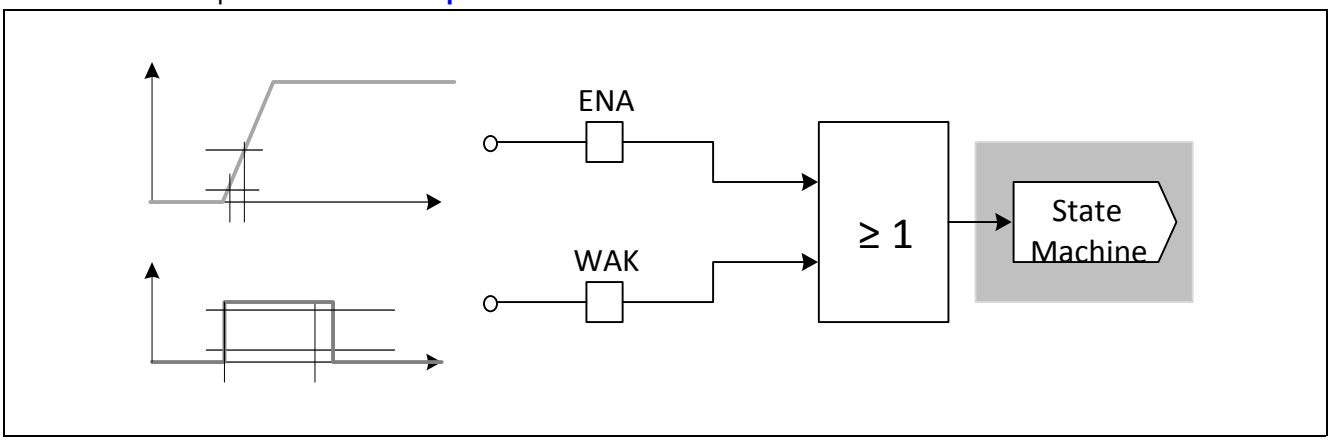


Figure 4 Principle of the enable function

5.2 Electrical Characteristics Enable Signal

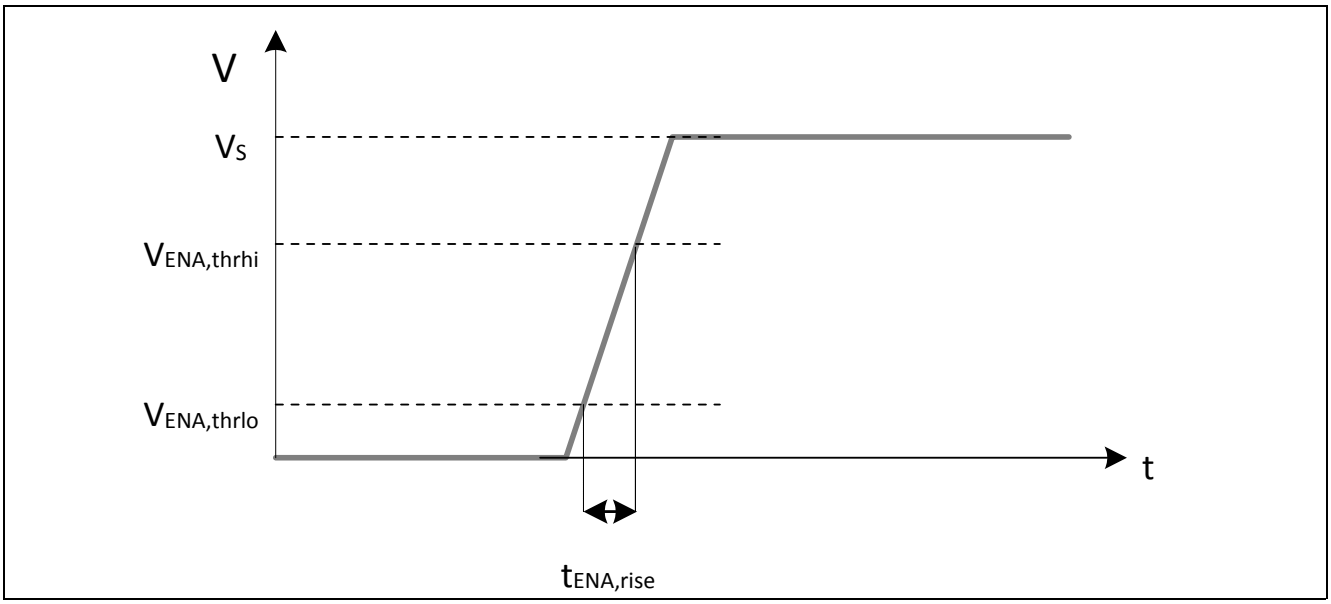


Figure 5 Valid enable signal

Table 5 Electrical Characteristics: Enable signal

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable EN							
Enable upper threshold	$V_{ENA,thrhi}$	–	–	2.00	V	V_{ENA}increasing	P_5.2.1
Enable lower threshold	$V_{ENA,thrlo}$	0.8	–	–	V	V_{ENA} decreasing	P_5.2.2
Enable threshold hysteresis	$V_{ENA,hyst}$	–	400	–	mV	-	P_5.2.3
Enable signal, rise time	$t_{ENA,rise}$	–	–	10	µs	–	P_5.2.4
Enable signal, minimum high time	$t_{ENA,high}$	20	–	–	µs	–	P_5.2.5
Enable high input current	$I_{ENA,hi}$	–	8	11	µA	V_{ENA} = 16 V	P_5.2.6
Enable low input current	$I_{ENA,lo}$	–	0.1	2	µA	V_{ENA} = 0.5 V	P_5.2.7

5.3 Electrical Characteristics Wake Signal

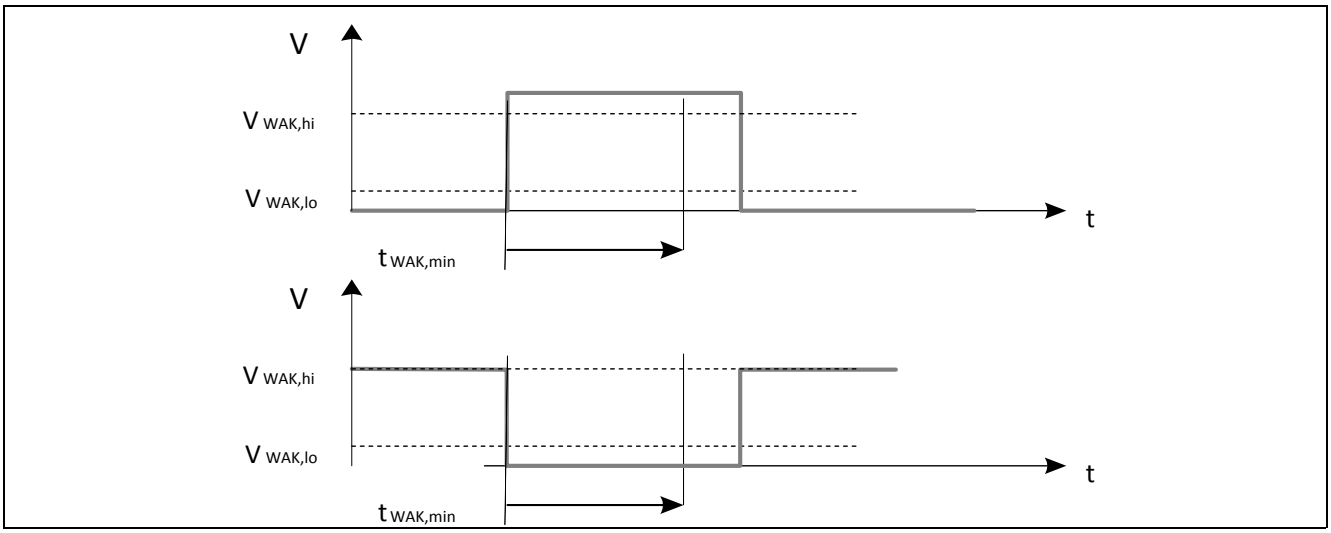


Figure 6 Valid wake signal

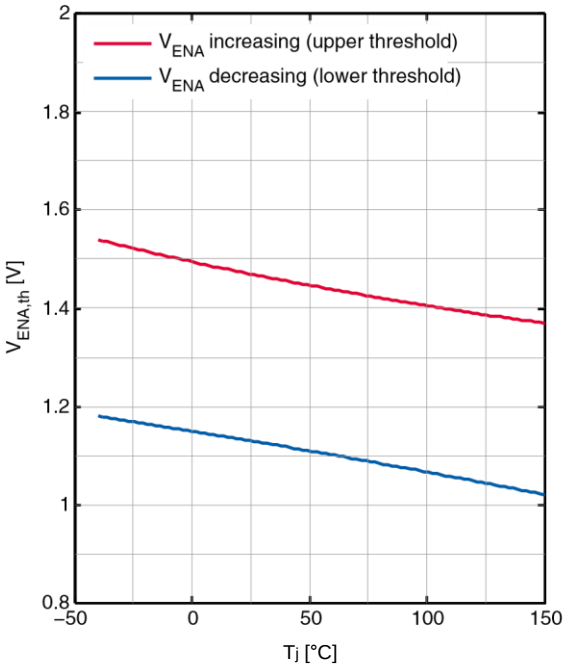
Table 6 Electrical Characteristics: Wake signal

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin

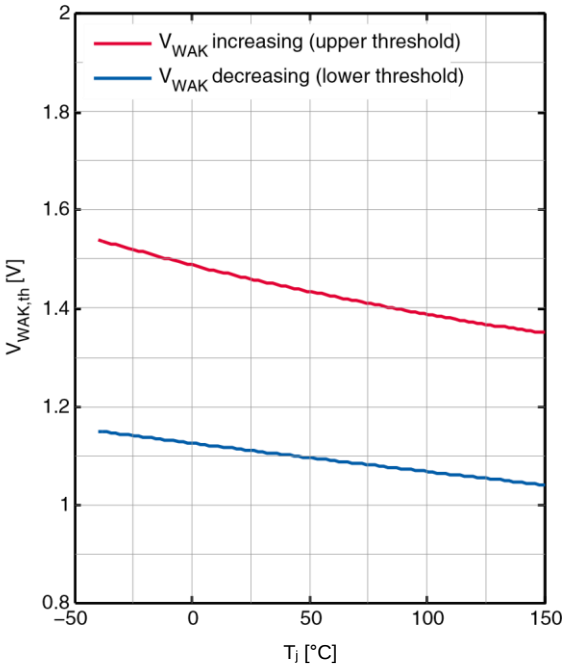
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
(unless otherwise specified)							
Wake/Inhibit							
Wake upper threshold	$V_{WAK,hi}$	–	–	2.00	V	V_{WAK} increasing	P_5.3.1
Wake lower threshold	$V_{WAK,lo}$	0.8	–	–	V	V_{WAK} decreasing	P_5.3.2
Wake signal hysteresis	$V_{WAK,hyst}$	–	400	–	mV	–	P_5.3.3
Wake signal, minimum length	$t_{WAK,min}$	40	–	–	µs	–	P_5.3.4
Wake high input current	$I_{WAK,hi}$	–	8	11	µA	V_{WAK} = 5.0V	P_5.3.5
Wake low input current	$I_{WAK,lo}$	–	0.1	2	µA	V_{WAK} = 0.5V	P_5.3.6

5.4 Typical Performance Characteristics

Enable Input Threshold Voltage $V_{ENA,th}$ versus Junction Temperature T_j



Wake Input Threshold Voltage $V_{WAK,th}$ versus Junction Temperature T_j



6 Pre Regulators

6.1 Introduction

The pre regulator is mandatory to maintain a stabilized and constant intermediate circuit voltage to supply the following post regulators. It consists of two independent regulators: A step up converter with an external power stage in front to maintain a minimum input voltage to the following step down converter.

The step up converter can be deactivated (if not needed) by connecting pin STU to ground. Leaving pin STU open activates the step up regulator.

The step down regulator frequency can be preset by leaving pin FRE open for the high switching frequency range or connecting to GND for the low switching frequency range.

The step down converter is constantly on, providing a stabilized intermediate circuit voltage V_{PREREG} to supply the following post regulators. The step up converter is connected directly to the input voltage V_{Bat}. It only operates during low input voltage condition (i.e. cranking) when the input voltage drops below the threshold $V_{PRE\_REG,boost,UV}$, to maintain an input voltage high enough for the following step down regulator. Low input voltage condition means, that the input voltage at pin VSx is too low to provide an intermediate circuit voltage V_{PREREG} within the specified limits. An internal comparator connected to the input voltage path detects the threshold when to turn on the step up converter. In case the input voltage is above the step up converter output voltage (threshold for switching on the step up converter), this regulator is deactivated by the internal comparator. An internal logic switches the step up converter on (and off again) whenever it is needed.

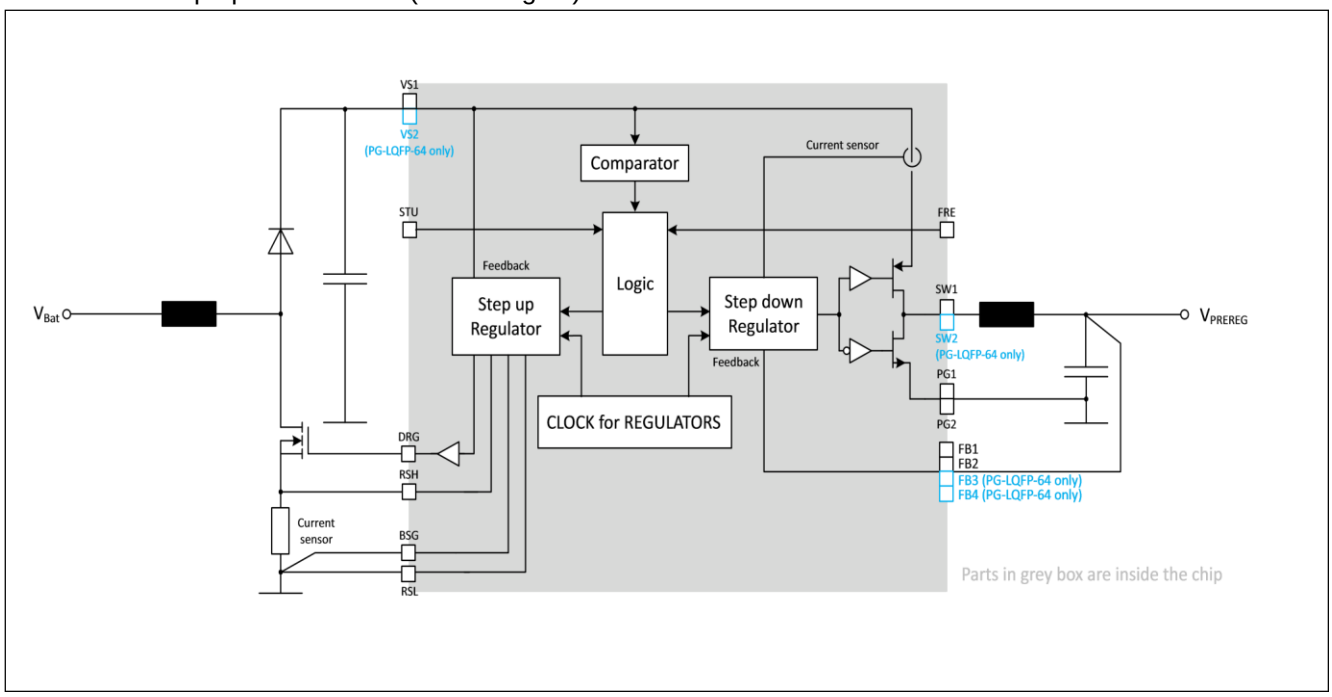


Figure 7 Principle pre regulator stage

6.2 Step Up Regulator

6.2.1 Functional description

The asynchronous step up pre regulator provides a higher output voltage than the input voltage when operating. This will be the case whenever the supply voltage should be too low to allow nominal values at the post regulator outputs. The boost pre regulator output voltage will be well below the nominal supply (battery) voltage to make sure, that he only operates during low input voltage conditions.

If the step up feature should not be necessary for the application, the external power elements (Mosfet, diode) could be skipped, the filter elements might be adjusted to the application requirements.

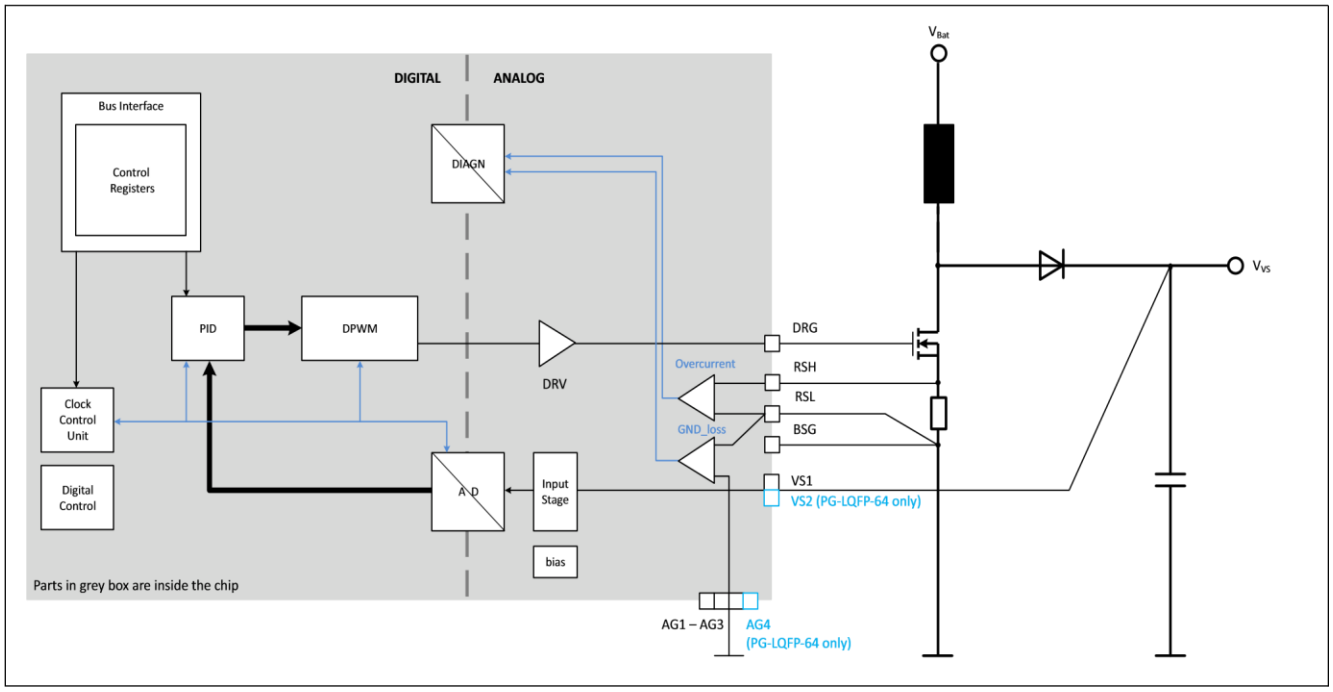


Figure 8 Step Up Regulator

6.2.2 Electrical characteristics

Table 7 Electrical Characteristics: Step up regulator

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Step up pre regulator							
Pre regulator boost output voltage	$V_{PRE\_REG,boost}$	7.00	7.5	8.00	V	–	P_6.2.2.1
Threshold external sense resistor for OC	$V_{RSH-RSL}$	190	210	230	mV	–	P_6.2.2.2

Low side sense input current	I_{RSL}	-120	-60	-30	µA	V_{RSL} = 0 V	P_6.2.2.3
High side sense input current	I_{RSH}	-45	-30	-15	µA	tested at V_{RSH} = 0 V	P_6.2.2.4
Input under voltage threshold	$V_{PRE\_REG,boost,UV}$	8	8.3	8.6	V	–	P_6.2.2.5
Input under voltage threshold hysteresis	$V_{PRE\_REG,boost,UV,hyst}$	80	–	200	mV	–	P_6.2.2.6
Gate driver peak sourcing current	$I_{DRG,SRC}$	–	130	–	mA	1)	P_6.2.2.7
Gate driver peak sinking current	$I_{DRG,SNK}$	–	100	–	mA	1)	P_6.2.2.8
Gate driver output rise time	$t_{R,DRG}$	12	–	150	ns	10% to 90% C_{DRG} = 470 pF	P_6.2.2.9
Gate driver output fall time	$t_{F,DRG}$	12	–	150	ns	90% to 10% C_{DRG} = 470 pF	P_6.2.2.10
Gate driver output voltage	V_{DRG}	4.5	5	5.5	V	–	P_6.2.2.11
Maximum Duty Cycle	D_{MAX}	75	95	–	%	–	P_6.2.2.12
Blanking time	t_{Blank}		240		ns	–	P_6.2.2.13

1) Specified by design, not subject to production test.

6.3 Step Down Regulator

6.3.1 Functional description

The synchronous step down pre regulator is continuously in operation providing a stable intermediate circuit voltage to supply the following post regulators. The internal power stage consists of synchronous P-channel (high side) and N-channel (low side) Mosfets. For startup a soft start function is implemented.

The regulation loop operates in voltage mode.

Under normal load conditions the regulator operates in Pulse Width Modulation (PWM). Under light load conditions it will operate in Pulse Frequency Modulation (PFM) to minimize the internal current consumption (only in SLEEP state, not in NORMAL, WAKE or INIT state).

The output filter of the step down regulator has to be sized to ensure a maximum output voltage ripple of 100 mV in order to be in line with the PSRR specified for the post regulators.

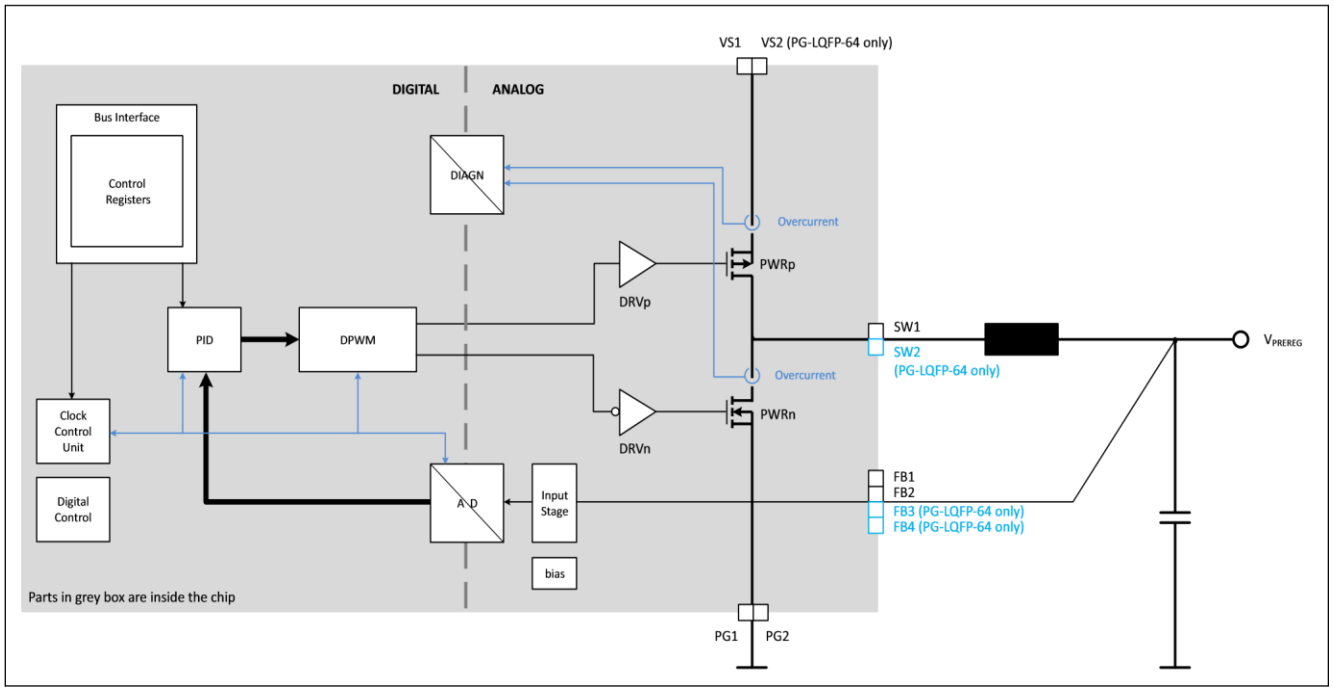


Figure 9 Step Down Regulator

6.3.2 Electrical characteristics

Table 8 Electrical Characteristics: Step down pre regulator

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Step Down Pre Regulator							
Output voltage	$V_{PREREG,BUCK}$	5.65	5.8	5.95	V	PWM-mode; V_{VS} ≥ 6.5 V	P_6.
Output voltage	$V_{PREREG,BUCK}$	5.6	5.8	6.00	V	PFM-mode; V_{VS} ≥ 6.5 V	P_6.
Power stage high side switch on resistance	$R_{ON, HS}$	150	360	630	mΩ	V_{VS} ≥ 6 V	P_6.
Power stage low side switch on resistance	$R_{ON, LS}$	50	200	300	mΩ	V_{VS} ≥ 6 V	P_6.

Buck peak over current limit	$I_{PREREG, max}$	1.578	1.857	2.135	A	–	P_6.
SW rise time	$t_{R, Buck}$	2	6	14	ns	1) 6.5V ≤ V_{VS} ≤ 18 V; I_{PREREG} ≥ 0.5 A	P_6.
SW fall time	$t_{F, Buck}$	2	9	18	ns	1) 6.5V ≤ V_{VS} ≤ 18 V; I_{PREREG} ≥ 0.5 A	P_6.
Soft start ramp	$t_{SS, BUCK}$	- 20 70	- P_6.3.2.8 I_{PREREG} 190	100 80 380	% ns µs	– ≥ 0.5 A 1) $V_{PRE\_REG,BUCK}$ rising from 5% to 95% of $V_{PREREG,nominal}$; 2.2 MHz switching frequency, no load	P_6. P_6.
Soft start ramp	$t_{SS, BUCK}$	0.7	2.0	3.5	ms	1) $V_{PRE\_REG,BUCK}$ rising from 5% to 95% of $V_{PRE\_REG,nominal}$; 400 kHz switching frequency, no load	P_6.
Current threshold for transition from PWM to PFM	$I_{PWM/PFM}$	26	57	90	mA	–	P_6.
Current threshold for	$I_{PFM/PWM}$	100	145	190	mA	–	P_6.

transition from PFM to PWM							
Over temperature warning threshold	$T_{j,OT,\ WRN}$	130	145	160	°C	T_j increasing 1)	P_6.

Table 8 Electrical Characteristics: Step down pre regulator (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

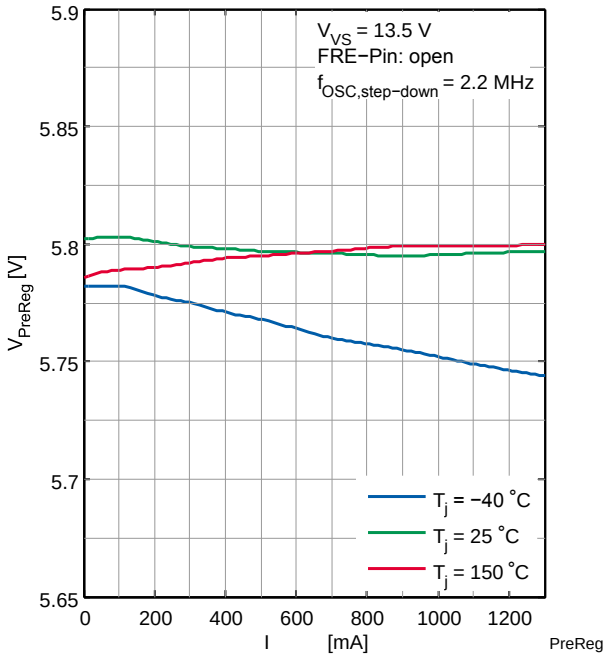
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over temperature shutdown threshold	$T_{j,OT,\ shutdown}$	175	190	205	°C	T_j increasing 1)	P_6.3.2.15
Over temperature sensor hysteresis	$T_{j,OT,\ hyst}$	–	10	–	°C	1)	P_6.3.2.16

1) Specified by design, not subject to production test

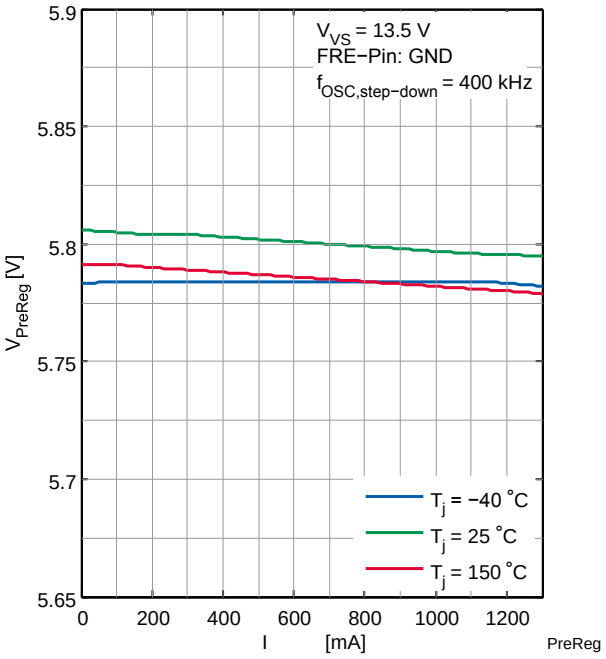
6.3.3 Typical Performance Characteristics

Pre Regulator Output Voltage V_{PreReg}
versus
Junction Temperature T_j (FRE-Pin: open)
Pre Regulator Output Voltage V_{PreReg}
versus

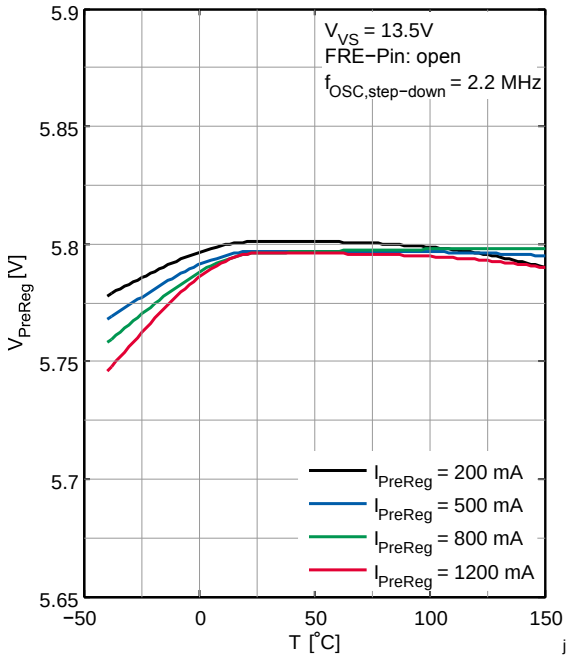
Junction Temperature T_j (FRE-Pin: GND)



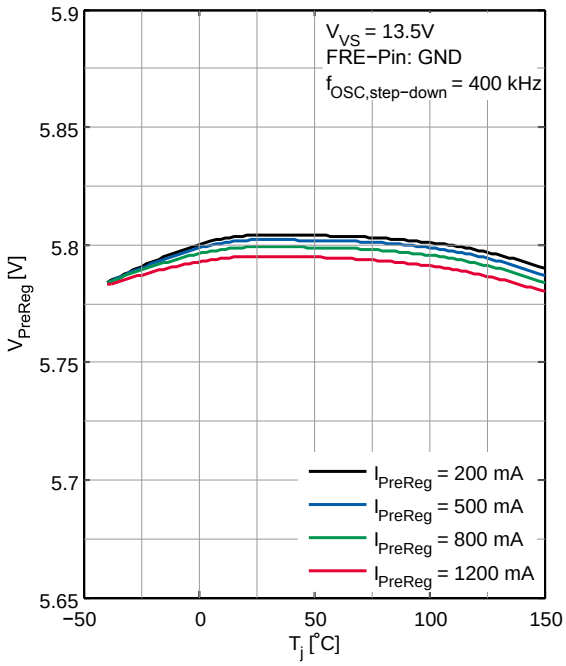
Pre Regulator Output Voltage V_{PreReg} versus Load Current I_{PreReg} (FRE-Pin: open)



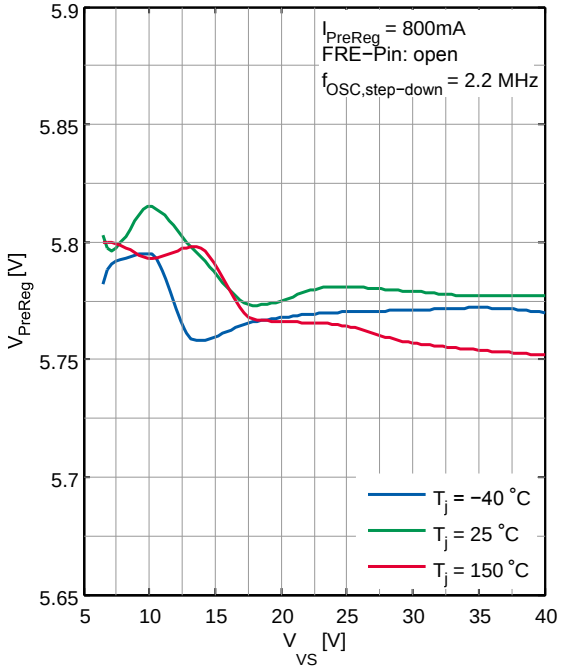
Pre Regulator Output Voltage V_{PreReg} versus Load Current I_{PreReg} (FRE-Pin: GND)



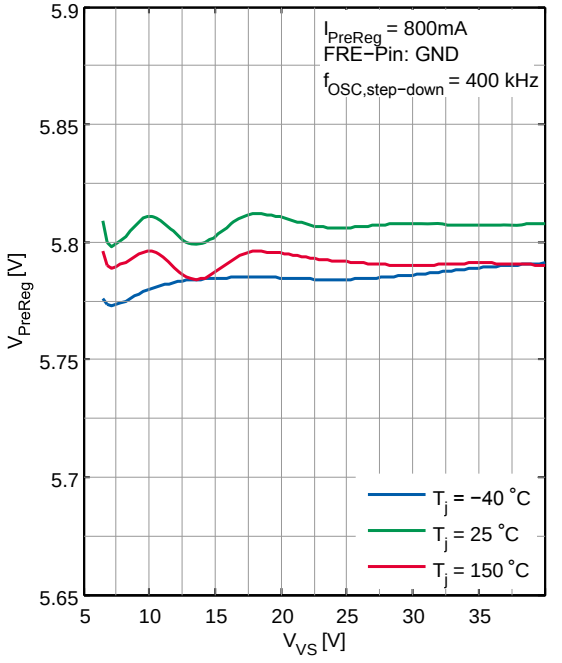
Pre Regulator Output Voltage V_{PreReg} versus Supply Voltage V_{VS} (FRE-Pin: open)



Pre Regulator Output Voltage V_{PreReg} versus Supply Voltage V_{VS} (FRE-Pin: GND)

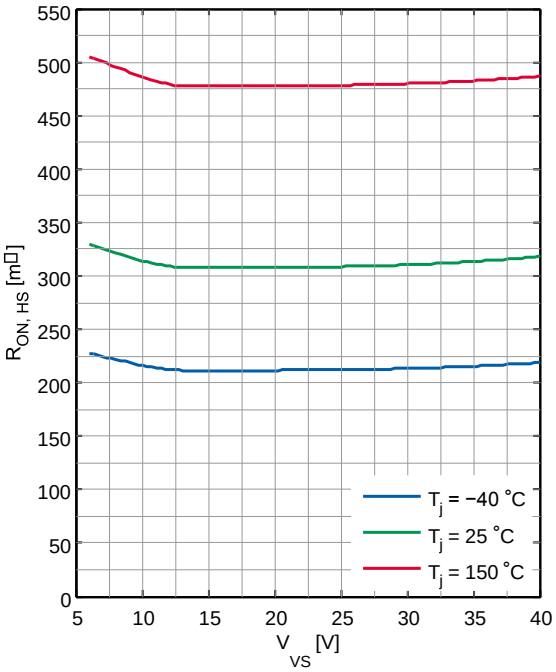


High-Side Switch ON resistance $R_{ON, HS}$ versus Supply Voltage V_{VS}

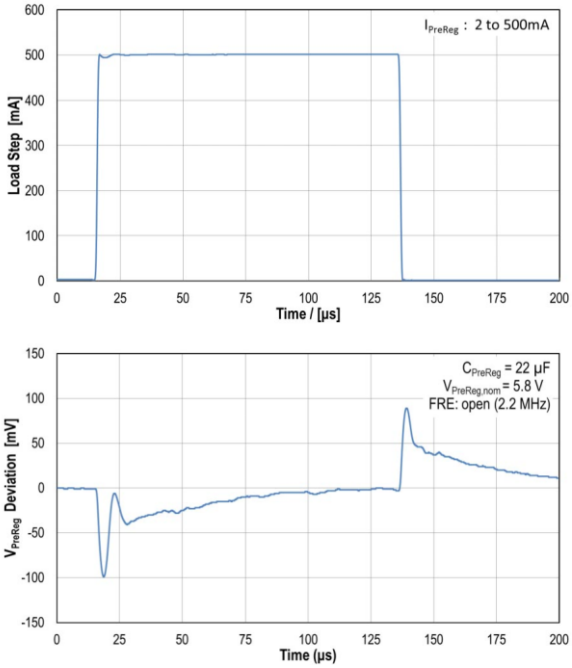


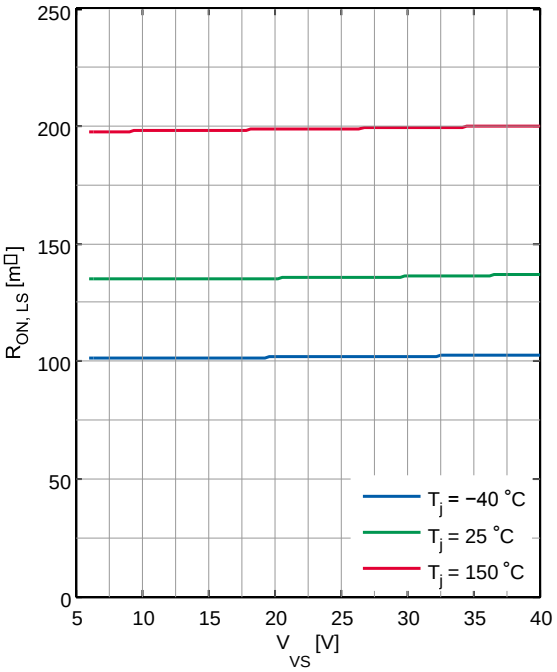
ON, LS versus
40

Low-Side Switch ON resistance R
Supply Voltage V_{VS}

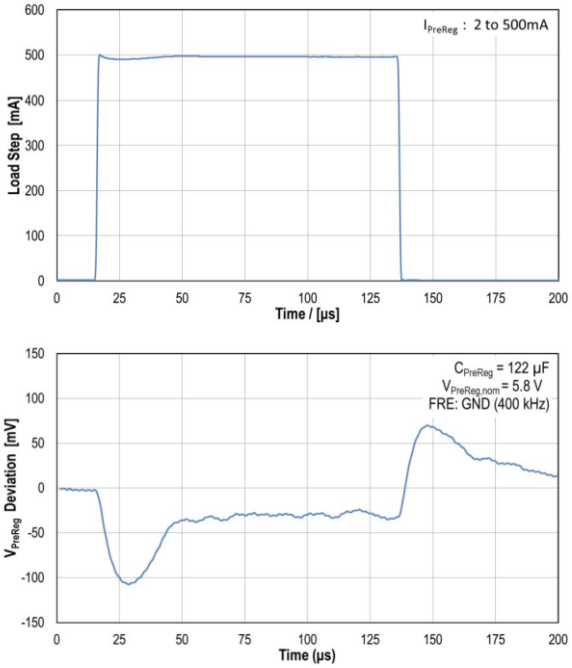


PreReg Dynamic Load Response (2mA to 500mA) (FRE-Pin: open ; $V_{PreReg,nom}$ = 5.8 V)





PreReg Dynamic Load Response (2mA to 500mA) (FRE-Pin: GND ; $V_{PreReg,nom}$ = 5.8 V)



6.4 Frequency setting

6.4.1 Introduction

The frequency source supplies the step up pre regulator and the step down pre regulator with a constant frequency. The synchronous power switches of the step down pre regulator will switch directly with the frequency f_{OSC}.

The frequency range of the step down pre regulator can be set to the high switching frequency range by leaving pin FRE open or to the low switching frequency range by connected the pin FRE to GND. The switching frequency will be set to the default value of the chosen frequency range. Optionally it can be fine tuned by SPI command (**BCK_FREQ_CHANGE**) or the spread-spectrum option can be activated (**BCK_FRE_SPREAD**).

The switching frequency range of the step up pre regulator is lower than the switching frequency range of the step down pre regulator.

The switching frequency of the step down pre regulator is offered at pin SYN for the optional external switch mode post regulator for the µC core supply, if the SEC pin is left open.

The synchronization function is not available in PFM mode.

The TLF35584 cannot be synchronized to an external frequency source.

6.4.2 Electrical characteristics frequency setting

Table 9 Electrical Characteristics: Oscillator

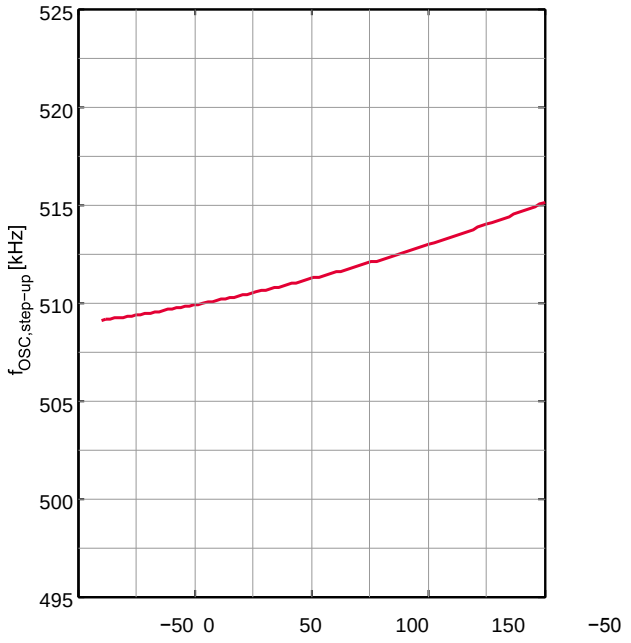
V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

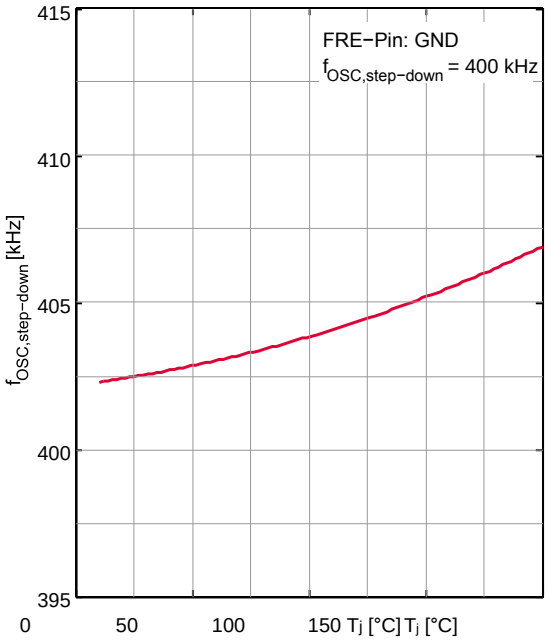
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Frequency Setting FREQ							
Step-up frequency range	$f_{OSC,step-up}$	400	500	600	kHz	–	P_6.4.2.1
Step-down low frequency range	$f_{OSC,step-down}$	300	400	500	kHz	FRE pin connected to GND	P_6.4.2.2
Step-down high frequency range	$f_{OSC,step-down}$	2000	2200	2500	kHz	FRE pin open	P_6.4.2.3

6.4.3 Typical Performance Characteristics

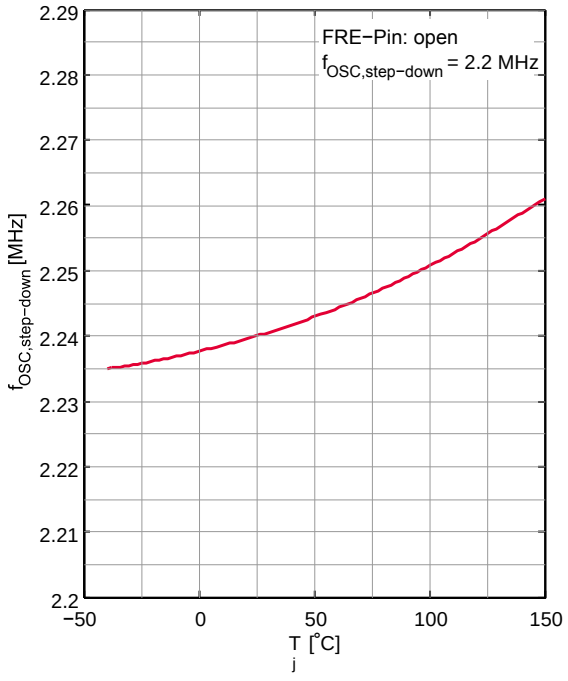
Step-up Switching Frequency $f_{OSC,step-up}$ versus Junction Temperature T_j (FRE-Pin: open)

Step-down Switching Frequency $f_{OSC,step-down}$ versus Junction Temperature T_j (FRE-Pin: GND)





Step-down Switching Frequency $f_{OSC,step-down}$ versus Junction Temperature T_j (FRE-Pin: open)



7 Post Regulators

7.1 Introduction

The TLF35584 includes a number of linear low drop post regulators and trackers and offers the possibility to connect an external post regulator for the µC core supply if needed.

The linear post regulators and trackers are supplied from pins FBx. The band gap 1 for regulator block provides the reference values for the error amplifiers of µC supply LDO (pin QUC), the communications supply LDO (pin QCO) and the reference voltage source (pin QVR). The trackers get their reference value from the reference voltage source (pin QVR). The output voltage of trackers 1 and 2 (present at pins QT1 and QT2) is following the reference voltage source Volt_Ref with a small drop.

An additional external post regulator can be added to deliver the core supply for the micro processor. If this option is used the configuration pin SEC must be left open. If the option is not used, pin SEC must be connected to ground.

The post regulator is to be connected external and uses its own reference voltage, the input is fed from the pre regulator output voltage V_{PREREG} (which is similar to the values at pins FBx). The post regulator is enabled by a high signal at pin EVC and switched off with a low signal at pin EVC. A synchronization signal (in phase or shifted by 180 degree with the step down pre regulator signal) is offered at pin SYN for usage of a switch mode post regulator.

All output voltages of the post regulators are connected to the voltage monitoring function (please refer to chapter **Monitoring Function**).

In case of an over voltage the related post regulator will be switched off, the shutdown signal is generated by the voltage monitoring function.

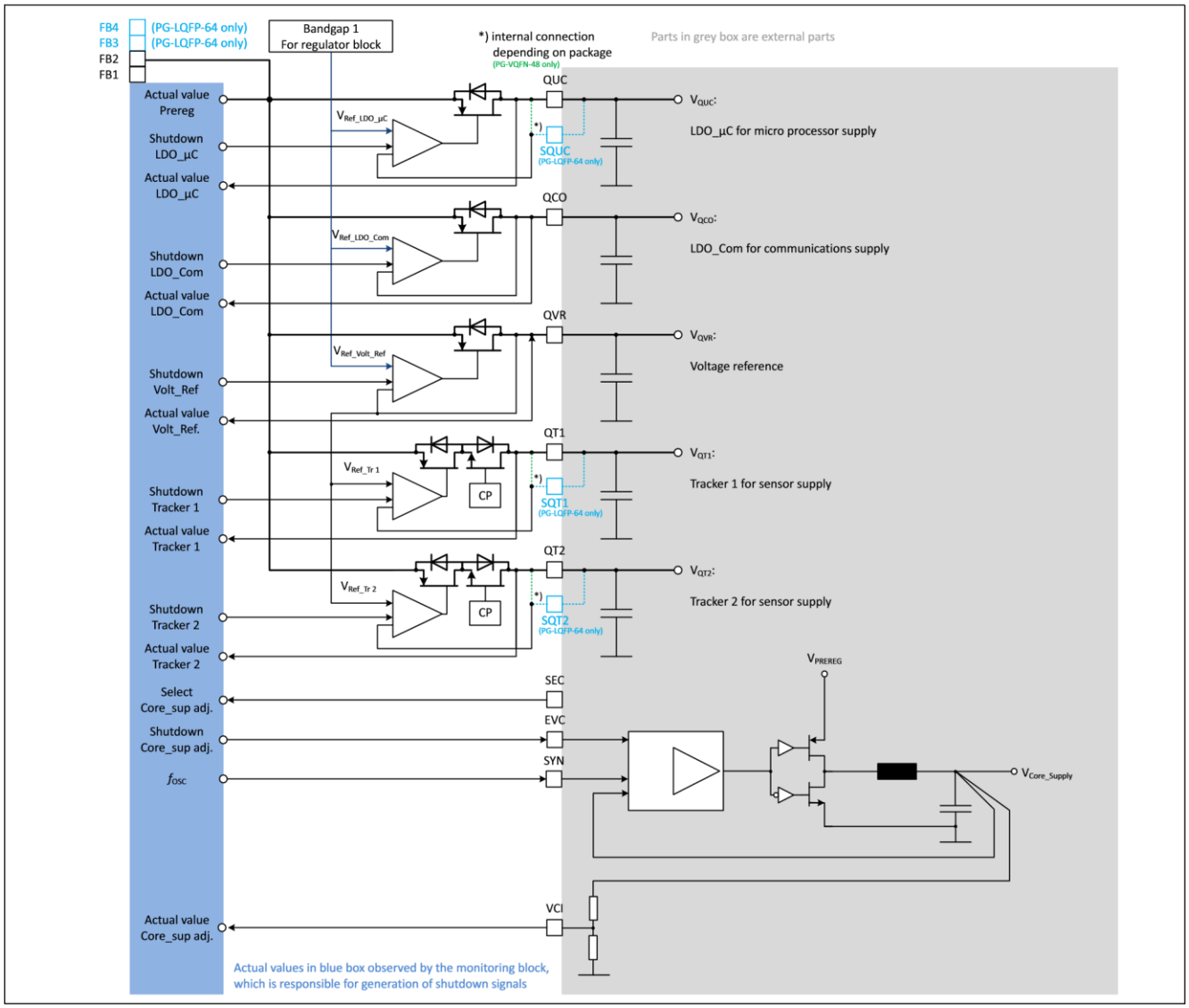


Figure 10 Principle post regulators

7.2 µ-Processor Supply

7.2.1 Functional description

The linear low drop regulator LDO_µC offers a precise 3.3 V or 5.0 V output voltage for micro processor supply.

The regulator is supplied from the intermediate circuit voltage V_{PREREG} which provides a stabilized voltage. The output voltage V_{QUC} (at pin QUC) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in **Table 10** “Electrical characteristics”. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element of the LDO_µC from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring. In case of over voltage at pin QUC, the LDO_µC will be switched off and the device will move into FAILSAFE state. The event will be stored in the SPI status register (**MONSF1**). In case of under voltage at pin QUC, the device will move into INIT state, pin ROT will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage should be present for more than t_{StG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).
- There is a dedicated temperature sensor for this regulator. In case the power stage temperature exceeds the pre warning threshold, an interrupt will indicate this event and it will be stored in an SPI status register (**OTWRNSF**). If the power stage temperature exceeds the temperature shutdown threshold, the device will move into FAILSAFE state, the regulator will be switched off and the event will be stored in an SPI status register (**OTFAIL**). The off time due to temperature shut down will be at least one second.

If the device enters FAILSAFE state the ROT is pulled low and all supplies are switched off.

If the device enters STANDBY state the LDO_µC is switched off For

further details please refer to **Chapter 11 State Machine**.

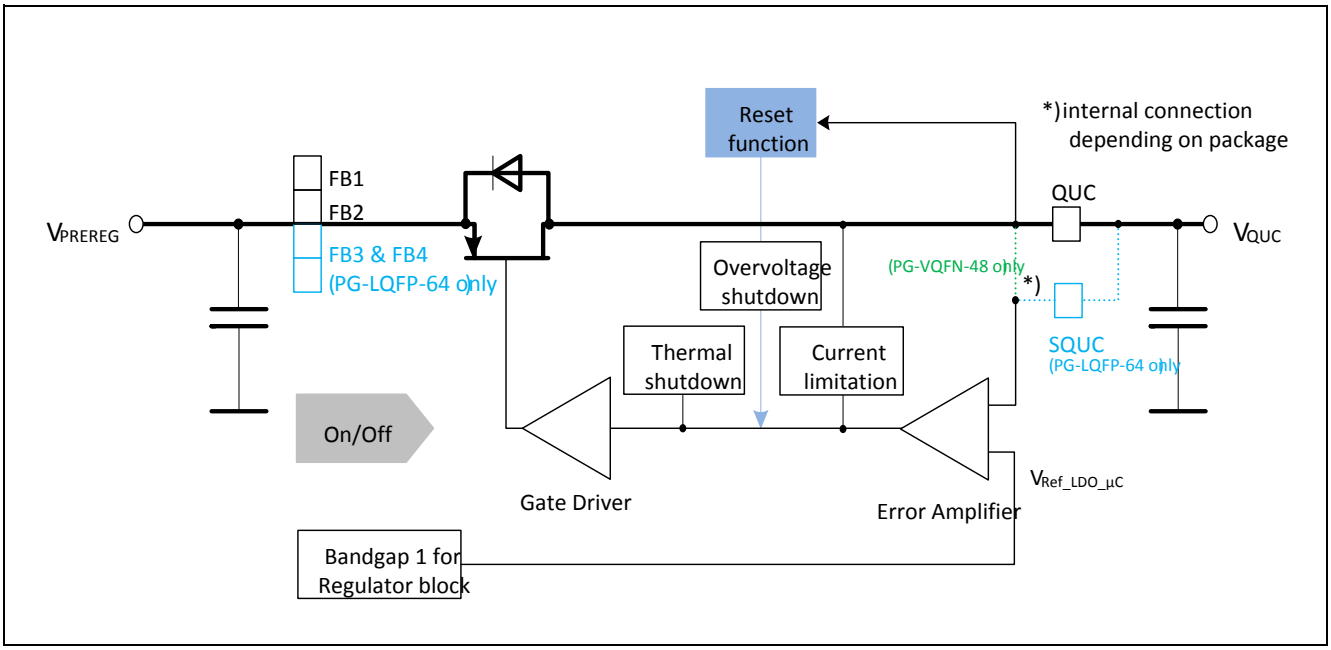


Figure 11 Low drop linear regulator for micro processor supply LDO_µC

7.2.2 Electrical characteristics

Table 10 Electrical characteristics: µProcessor supply

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
µ Processor supply							
Output voltage TLF35584xxVS1	V_{QUC}	4.9	5.0	5.1	V	0 mA ≤ I_{QUC}≤ 600 mA	P_7.2.2.1

Output voltage TLF35584xxVS2	V_{QUC}	3.23	3.3	3.37	V	0 mA ≤ I_{QUC}≤ 600 mA	P_7.2.2.2
Output current limitation	$I_{QUC, max}$	650	–	1100	mA	–	P_7.2.2.3
Drop voltage TLF35584xxVS1	$V_{dr, QUC}$	–	–	400	mV	1)	P_7.2.2.4
Drop voltage TLF35584xxVS2	$V_{dr, QUC}$	–	–	500	mV	1)	P_7.2.2.5
Load regulation TLF35584xxVS1	ΔV_{QUC}	–	45	81	mV	I_{QUC} = 100µA to 600 mA	P_7.2.2.6
Load regulation TLF35584xxVS2	ΔV_{QUC}	–	39	60	mV	I_{QUC} = 100µA to 600 mA	P_7.2.2.7
Power supply ripple rejection	$PSRR_{QUC}$	26	–	–	dB	2) V_{PREREG} = 5.8 V ; ESRC_{QUC} ≤ 100mΩ	P_7.2.2.8
Output capacitor	C_{QUC}	2.2	–	47	µF	2)	P_7.2.2.9
Output capacitor, ESR	$ESR\ C_{QUC}$	0	–	200	mΩ	2)	P_7.2.2.10
Over temperature warning threshold	$T_{j,OT, WRN}$	130	145	160	°C	T_j increasing 2)	P_7.2.2.11
Over temperature shutdown threshold	$T_{j,OT, shutdown}$	175	190	205	°C	T_j increasing 2)	P_7.2.2.12
Over temperature sensor hysteresis	$T_{j,OT, hyst}$	–	10	–	°C	2)	P_7.2.2.13

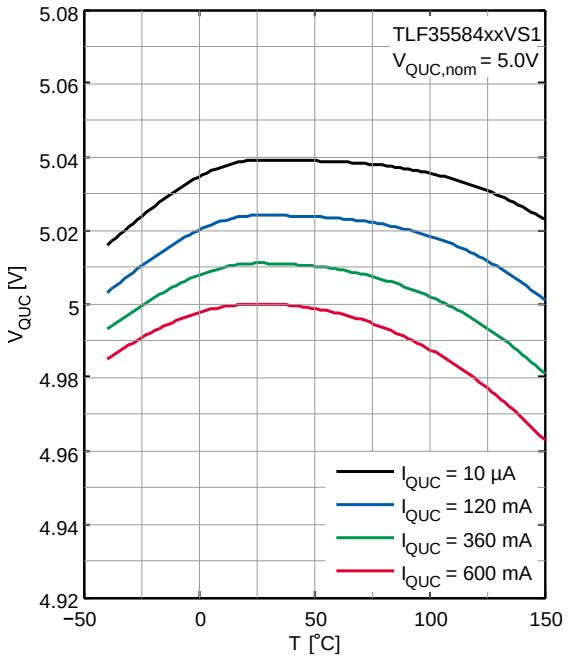
1) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

2) Specified by design, not subject to production test

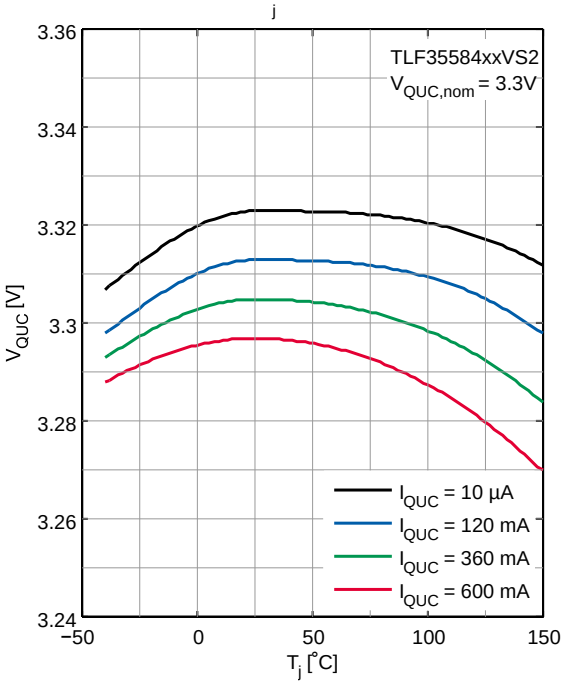
7.2.3 Typical Performance Characteristics

QUC Output Voltage V_{QUC} versus Junction Temperature T_j (TLF35584xxVS1)

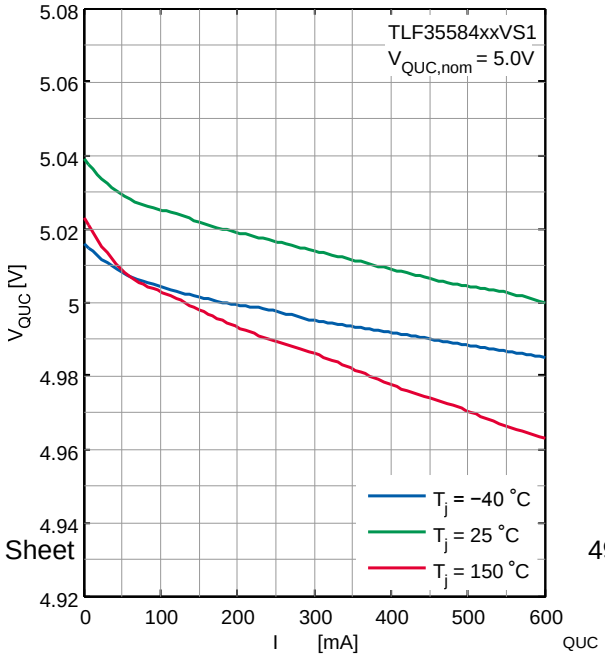
QUC Output Voltage V_{QUC} versus Junction Temperature T_j (TLF35584xxVS2)



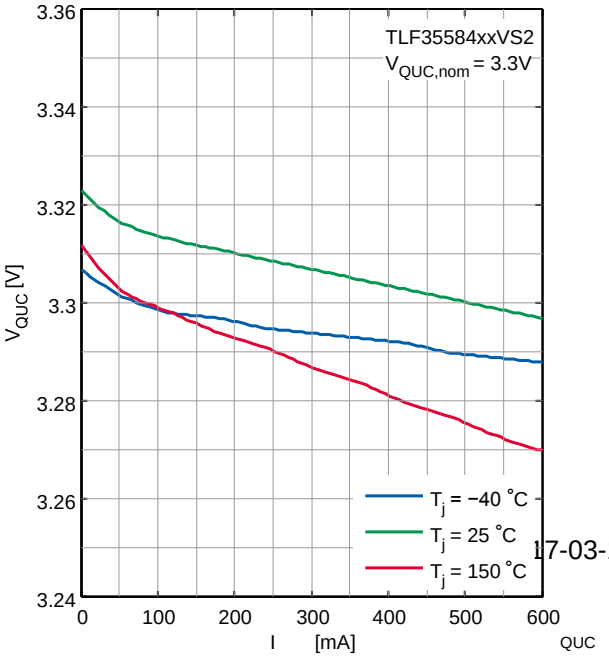
QUC Output Voltage V_{QUC} versus Load Current I_{QUC} (TLF35584xxVS1)



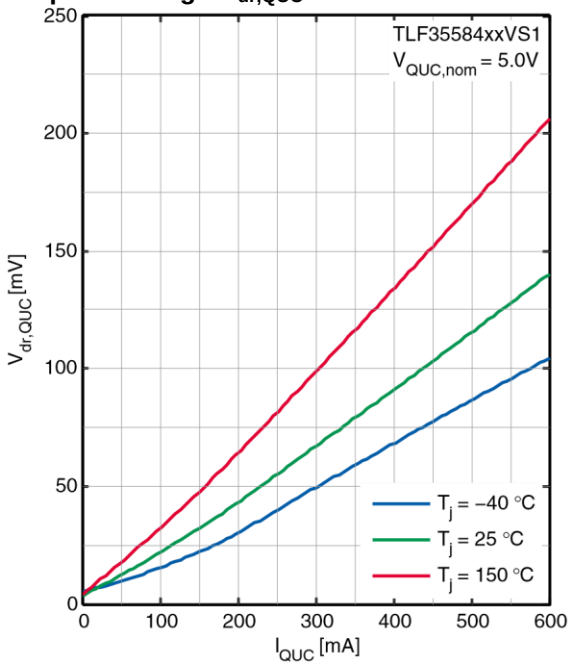
QUC Output Voltage V_{QUC} versus Load Current I_{QUC} (TLF35584xxVS2)



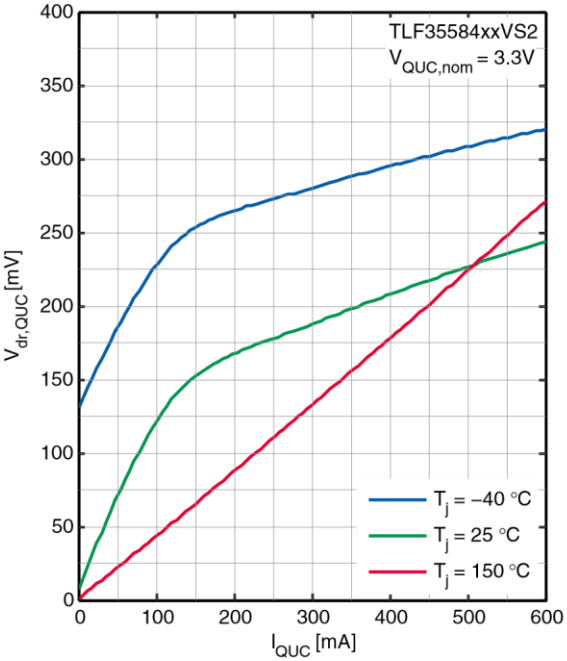
QUC Dropout Voltage $V_{dr,QUC}$ versus



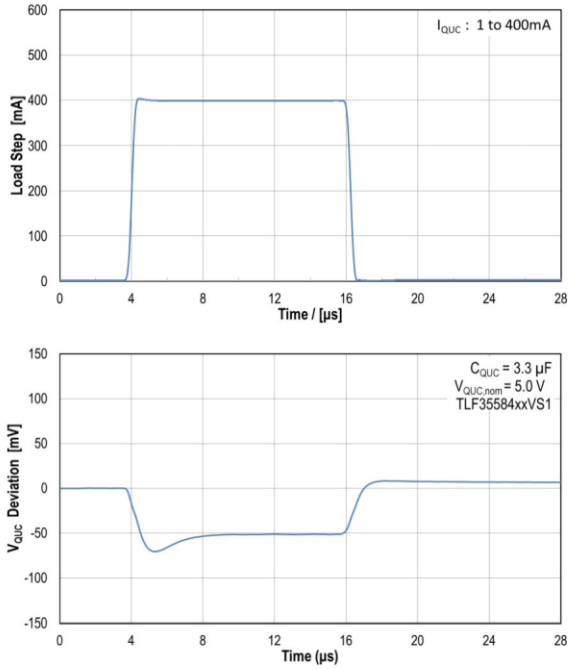
Load Current I_{QUC} (TLF35584xxVS1) QUC Dropout Voltage $V_{dr,QUC}$ versus



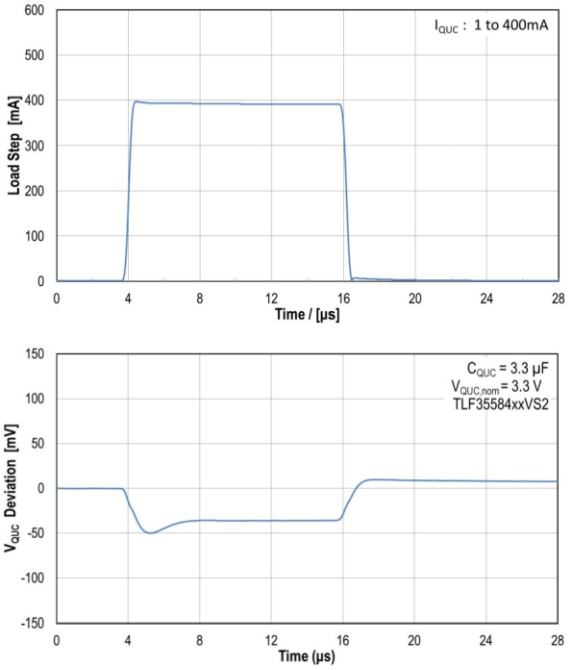
Load Current I_{QUC} (TLF35584xxVS2) QUC Dropout Voltage $V_{dr,QUC}$ versus



QUC Dynamic Load Response (1mA to 400mA) TLF35584xxVS1 ($V_{QUC,nom}$ = 5.0 V)

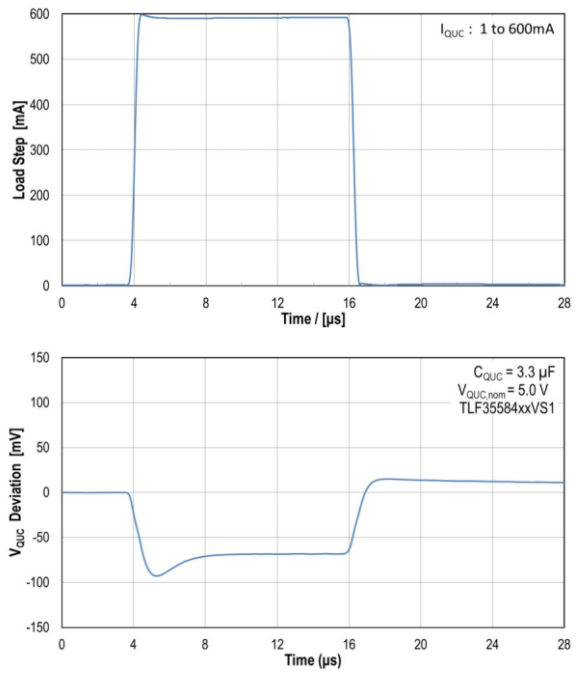


QUC Dynamic Load Response (1mA to 400mA) TLF35584xxVS2 ($V_{QUC,nom}$ = 3.3 V)

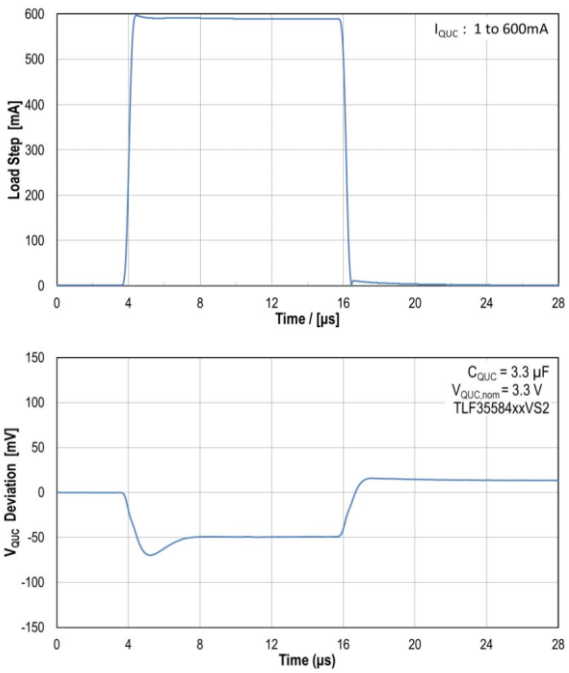


Load Current I_{QUC} (TLF35584xxVS2)

QUC Dynamic Load Response (1mA to 600mA)
TLF35584xxVS1 ($V_{QUC,nom}$ = 5.0 V)



QUC Dynamic Load Response (1mA to 600mA)
TLF35584xxVS2 ($V_{QUC,nom}$ = 3.3 V)



7.3 Communication Supply

7.3.1 Functional description

The linear low drop regulator LDO_Com offers a precise 5.0 V output voltage for communication supply.

The regulator is supplied from the intermediate circuit voltage V_{PREREG}, which provides a stabilized voltage. The output voltage V_{QCO} (at pin QCO) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor

should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in **Table 11** “Electrical characteristics”. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element of the LDO_Com from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring. In case of over voltage at pin QCO, the LDO_Com will be switched off, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF1**). In case of under voltage at pin QCO, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage should be present for more than t_{StG}, the regulator will be switched off. This event will be stored in the SPI status register (**MONSF0**) and an interrupt will be generated.
- There is a dedicated temperature sensor for this regulator. In case the power stage temperature exceeds the pre warning threshold, an interrupt will indicate this event and it will be stored in an SPI status register (**OTWRNSF**). If the power stage temperature exceeds the temperature shutdown threshold, this event will be stored in an SPI status register (**OTFAIL**), the regulator will be switched off and an interrupt will be generated. After a temperature shut down the LDO_Com can be re enabled via SPI command.

The regulator LDO_Com is switched off in STANDBY and FAILSAFE state. In INIT, SLEEP, NORMAL and WAKE state LDO_Com is ON or OFF depending on the SPI configuration.

For further details please refer to **Chapter 11 State Machine**.

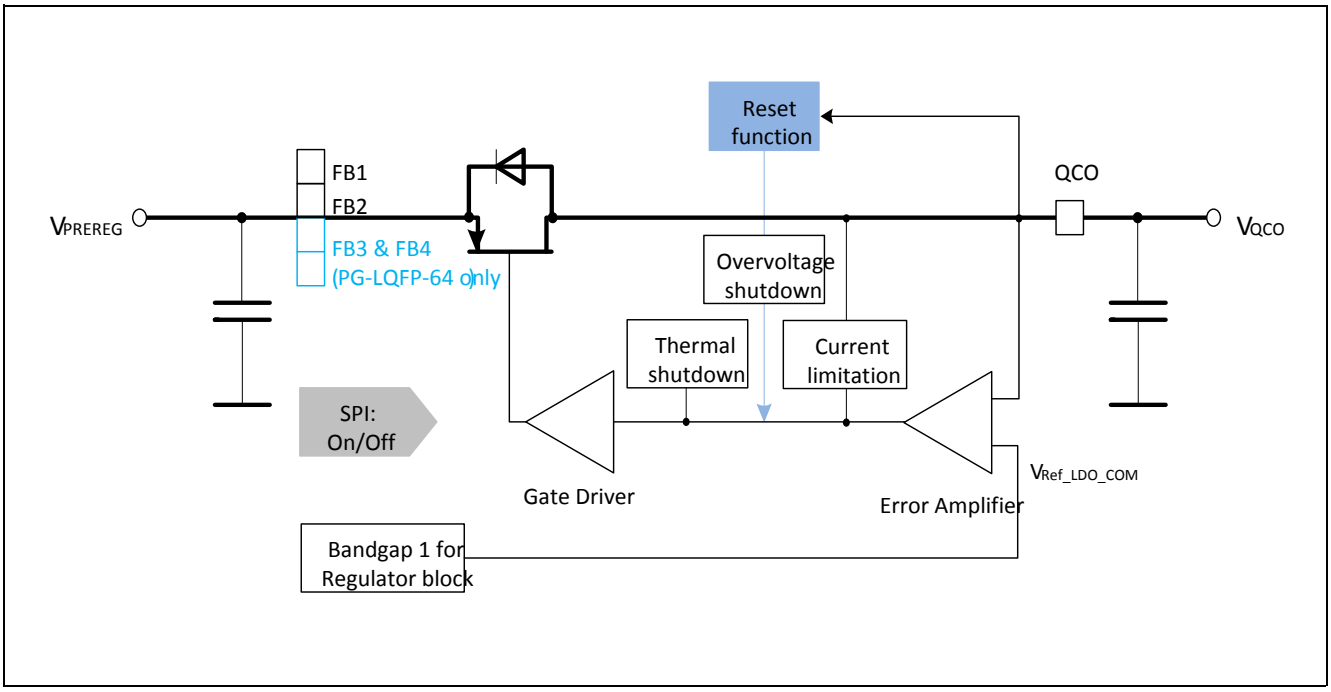


Figure 12 Low drop linear regulator for communications supply LDO_Com

7.3.2 Electrical characteristics

Table 11 Electrical characteristics: Communication supply

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			

Communication supply

Output voltage	V_{QCO}	4.90	5.00	5.10	V	0 mA ≤ I_{QCO}≤ 200 mA	P_7.3.2.1
Output current limitation	$I_{QCO, max}$	250	–	400	mA	–	P_7.3.2.2
Drop voltage	$V_{dr, QCO}$	–	–	400	mV	1)	P_7.3.2.3
Load regulation	ΔV_{QCO}	–	40	70	mV	I_{QCO} = 100µ to 200 mA	P_7.3.2.4
Power supply ripple rejection	$PSRR_{QCO}$	26	–	–	dB	2) V_{PREREG} = 5.8 V ; ESRC_{QCO} ≤ 100mΩ	P_7.3.2.5
Output capacitor	C_{QCO}	1	–	47	µF	2)	P_7.3.2.6
Output capacitor, ESR	$ESR\ C_{QCO}$	0	–	200	mΩ	2)	P_7.3.2.7
Over temperature warning threshold	$T_{j,OT, WRN}$	130	145	160	°C	T_j increasing 2)	P_7.3.2.8
Over temperature shutdown threshold	$T_{j,OT, shutdown}$	175	190	205	°C	T_j increasing 2)	P_7.3.2.9
Over temperature sensor hysteresis	$T_{j,OT, hyst}$	–	10	–	°C	2)	P_7.3.2.10

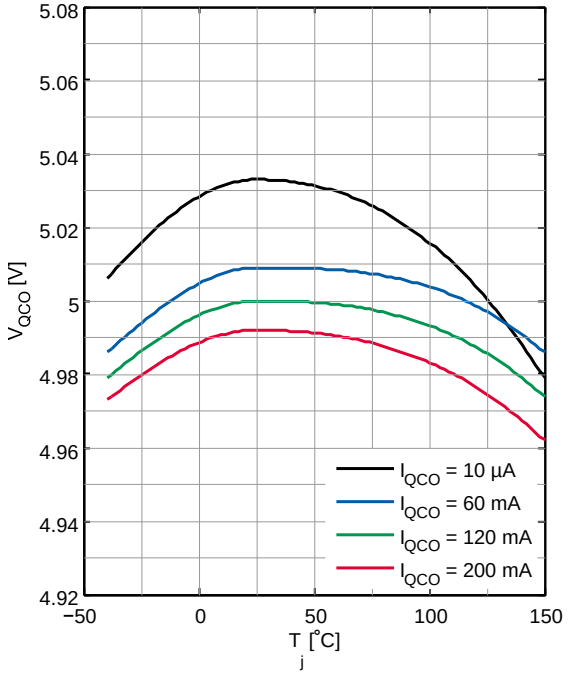
1) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

2) Specified by design, not subject to production test

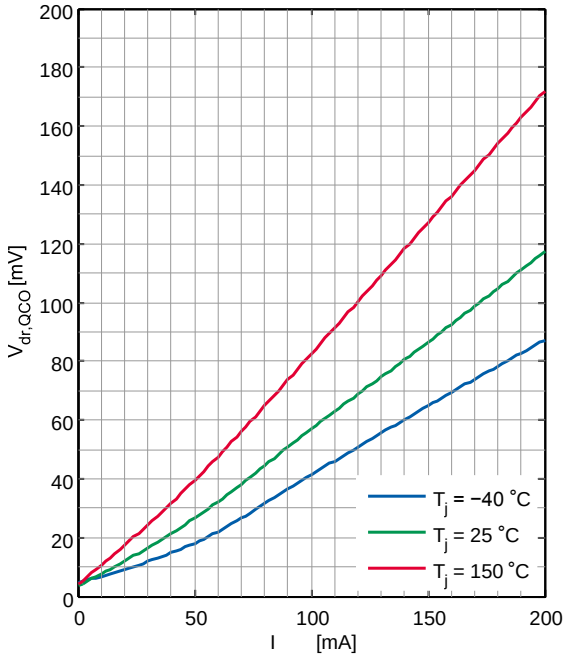
7.3.3 Typical Performance Characteristics

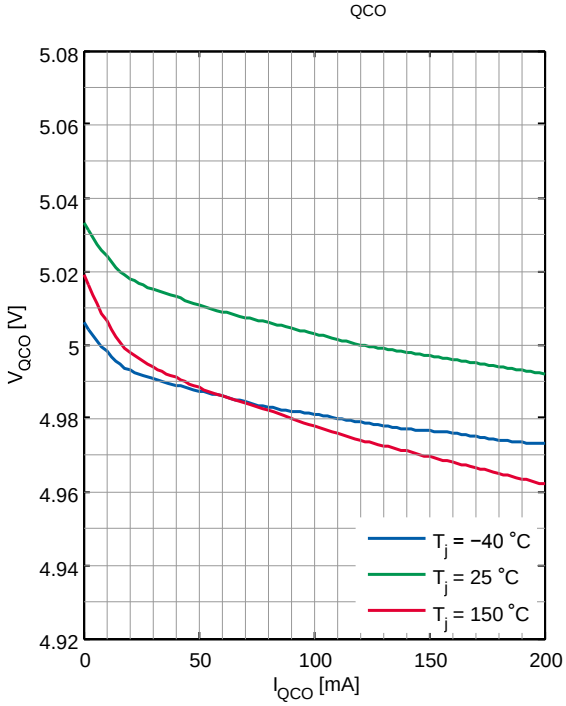
QCO Output Voltage V_{QCO} versus Junction Temperature T_j

QCO Output Voltage V_{QCO} versus Load Current I_{QCO}

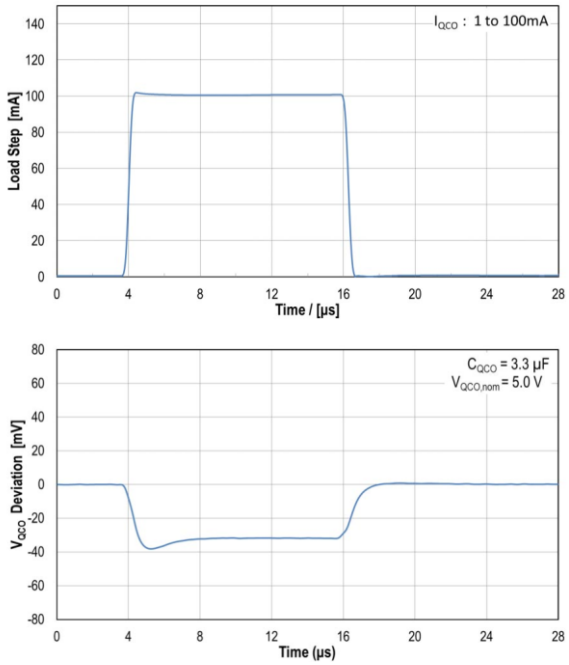


QCO Dropout Voltage $V_{dr,QCO}$ versus Load Current I_{QCO}





QCO Dynamic Load Response (1mA to 100mA) ($V_{QCO,nom}$ = 5.0 V)



7.4 Voltage Reference

7.4.1 Functional description

The linear low drop regulator Volt_Ref offers a highly precise 5.0 V output voltage as a voltage reference.

The regulator is supplied from the intermediate circuit voltage V_{PREREG}, which provides a stabilized voltage. The output voltage V_{QVR} at pin QVR is controlled by the error amplifier. The actual value is compared to a reference

voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in **Table 12** “Electrical characteristics”. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element of the Volt_Ref from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring. In case of over voltage at pin QVR, the LDO Volt_Ref will be switched off and the device will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin QVR, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage should be present for more than t_{StG}, the regulator will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.
- There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at LDO_µC and step down pre regulator. In case of the chip temperature will exceed the pre warning threshold, an interrupt will indicate this event and it will be stored in a SPI status register (**OTWRNSF**). If the chip temperature will exceed the temperature shutdown threshold, the regulator will be switched off. The temperature switch off time will be at least one second. An overload at LDO Volt_Ref (over current detected for more than 1ms) will be indicated by an interrupt and it will be stored in a SPI status register (**OTWRNSF**).

If the device enters FAILSAFE state the ROT is pulled low and all supplies are switched off.

The regulator Volt_Ref is switched off in STANDBY and FAILSAFE state. In INIT, SLEEP, NORMAL and WAKE state Volt_Ref is ON or OFF depending on the SPI configuration.

For further details please refer to **Chapter 11 State Machine**.

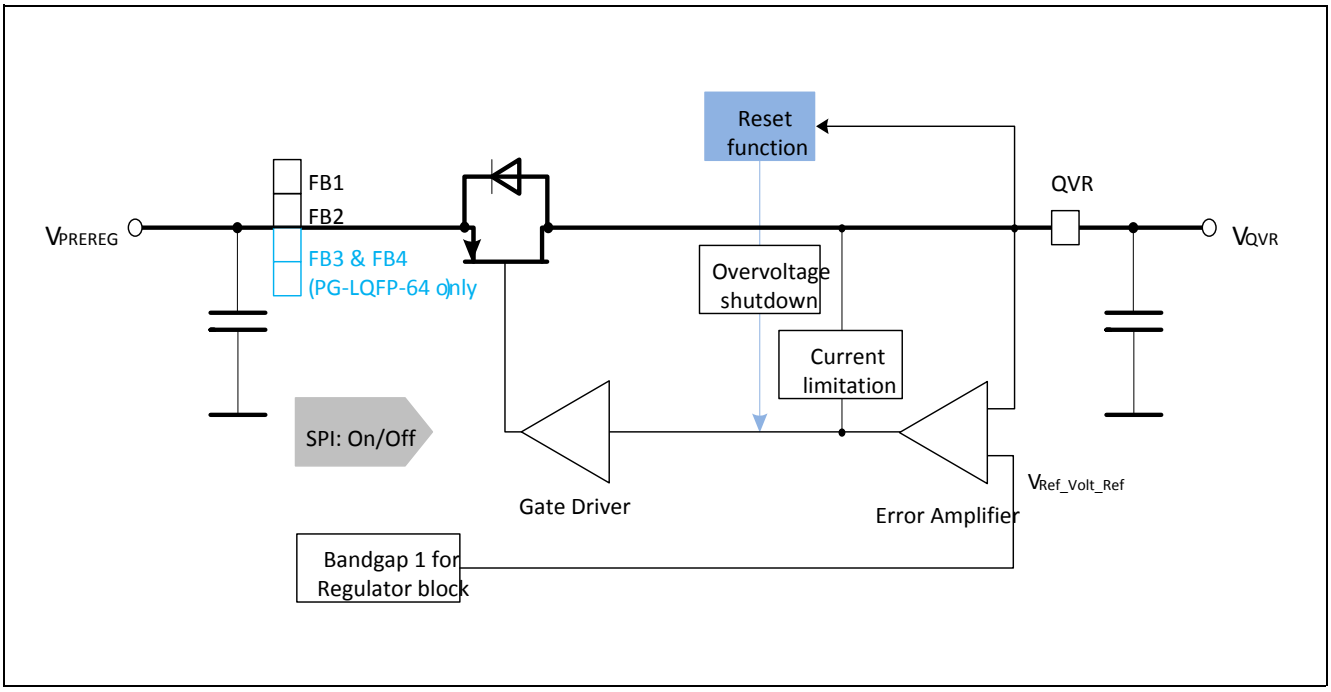


Figure 13 Precise low drop linear regulator as a voltage reference Volt_Ref

7.4.2 Electrical characteristics

Table 12 Electrical characteristics: Voltage reference

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage reference							
Output voltage	V_{QVR}	4.95	5.00	5.05	V	0 mA ≤ I_{QVR}≤ 150 mA	P_7.4.2.1
Output current limitation	$I_{QVR, max}$	170	–	345	mA	–	P_7.4.2.2
Drop voltage	$V_{dr, QVR}$	–	–	400	mV	1)	P_7.4.2.3
Load regulation	ΔV_{QVR}	–	4.5	9	mV	I_{QVR} = 100µ to 150 mA	P_7.4.2.4
Power supply ripple rejection	$PSRR_{QVR}$	26	–	–	dB	2) V_{PREREG} = 5.8 V ; ESRC_{QVR} ≤ 100mΩ	P_7.4.2.5
Output capacitor	C_{QVR}	1	–	10	µF	2)	P_7.4.2.6

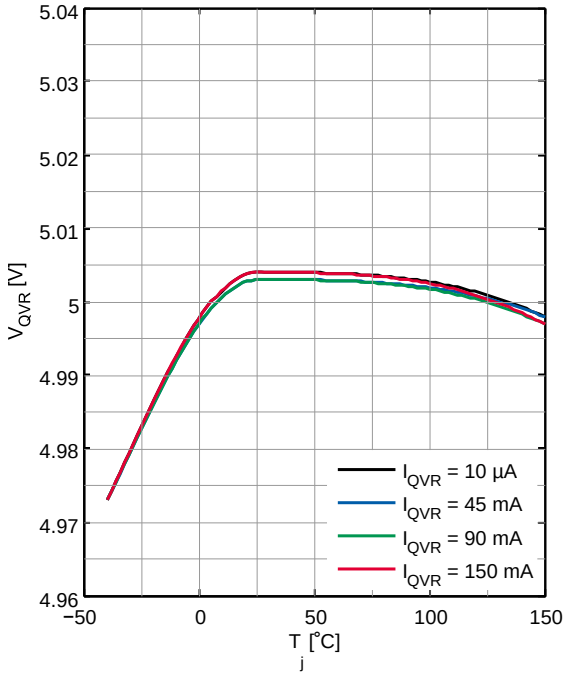
Output capacitor, ESR	$ESR\ C_{QVR}$	0	–	200	mΩ	2)	P_7.4.2.7

1) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max} + 100$ mV.

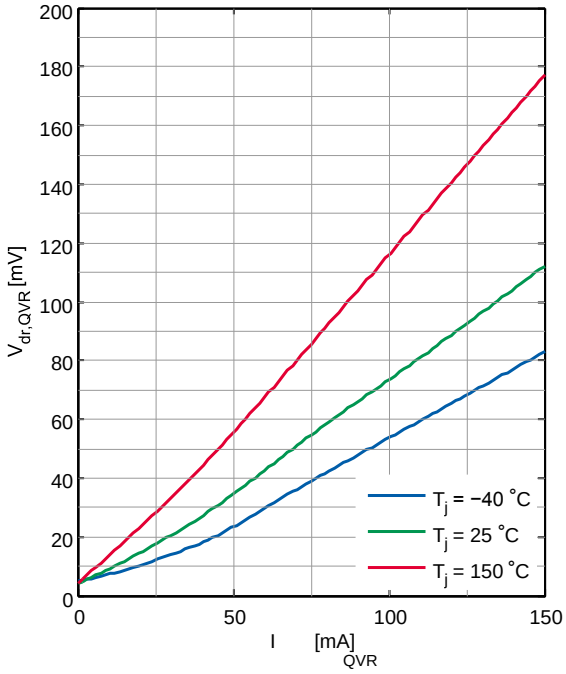
2) Specified by design, not subject to production test

7.4.3 Typical Performance Characteristics

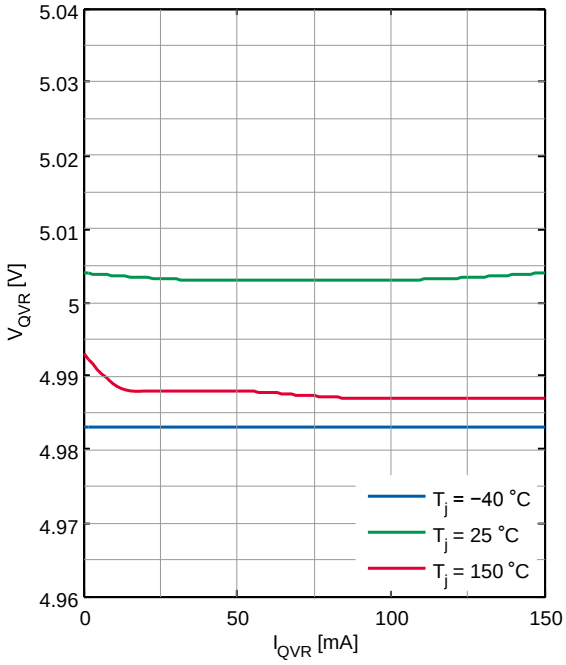
QVR Output Voltage V_{QVR} versus Junction Temperature T_j



QVR Output Voltage V_{QVR} versus Load Current I_{QVR}

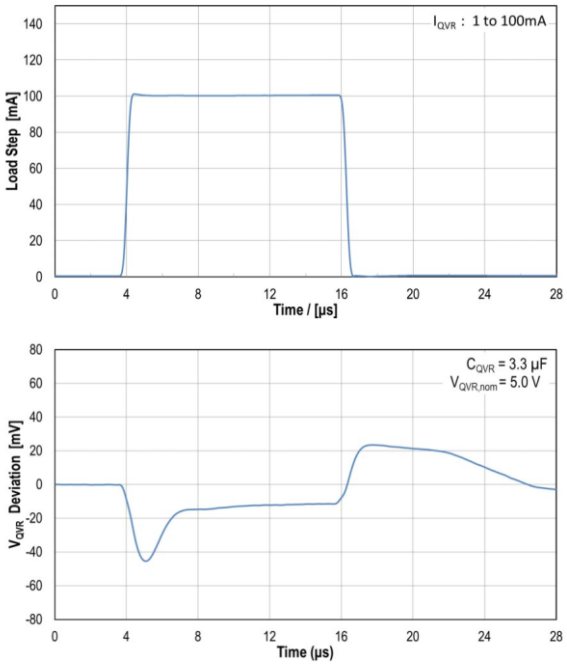


QVR Dropout Voltage $V_{dr,QVR}$ versus Load Current I_{QVR}



QVR Dynamic Load Response (1mA to 100mA)

($V_{QVR,nom}$ = 5.0 V)



7.5 Tracker 1 & 2

7.5.1 Functional description

The linear trackers 1 and 2 offer a sensor supply with a very high accuracy referred to voltage reference output (pin QVR).

Both trackers are supplied by the intermediate circuit voltage V_{PREREG}, which provides a stabilized voltage. The output voltage V_{QTx} at pin QTx is controlled by the error amplifier. The actual value is compared to a reference voltage provided by the reference voltage V_{QVR} at pin QVR. The tracker output voltages follow the Volt_Ref output with a very small drop. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for each tracker should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in **Table 13** “Electrical characteristics”. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent damage to both trackers and the application:

- To protect the pass element of a tracker from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited and in consequence the output voltage will decrease. A tracker is protected against short circuit to ground and short circuit to battery voltage.
- The output voltage is monitored by the voltage monitoring. In case of over voltage at pin QTx, the corresponding tracker will be switched off, the event will be stored in an SPI status register (**MONSF1**) and an interrupt will be generated. In case of under voltage at pin QTx, the event will be stored in an SPI status register (**MONSF2**) and an interrupt will be generated. The tracker will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage should be present for more than t_{StG}, the tracker will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.
- The tracker is capable to withstand a short circuit either to ground or to battery voltage without receiving a damage. In case of a short circuit to battery voltage and if the battery voltage is above the tracker over voltage threshold, the tracker will be switched off, the event will be stored in the SPI status register (**MONSF1**).

- There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at LDO_µC and step down pre regulator. In case of the chip temperature will exceed the pre warning threshold, the event will be stored in an SPI status register (**OTWRNSF**) and an interrupt will be generated. If the chip temperature exceeds the temperature shutdown threshold, the tracker will be switched off. The temperature switch off time is at least one second.

Both trackers are switched off in STANDBY and FAILSAFE. In INIT, NORMAL, SLEEP and WAKE state each tracker is ON or OFF depending on the SPI configuration.

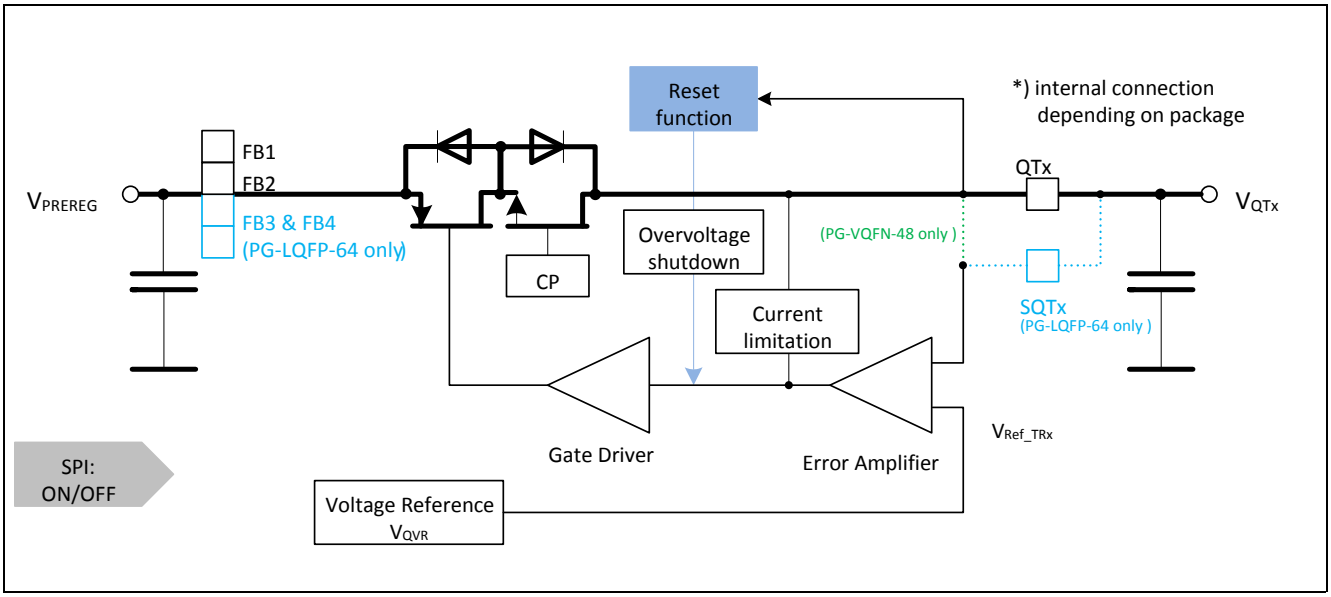


Figure 14 Tracker 1 & 2 for sensor supply

7.5.2 Electrical characteristics

Table 13 Electrical characteristics: Tracker 1 & 2

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Sensor supply, Tracker 1 & 2							
Output voltage tracking accuracy to voltage reference 1)	ΔV_{QTx}	– 10	–	10	mV	0 mA ≤ I_{QT1}≤ 150 mA	P_7.5.2.1
Output current limitation	$I_{QTx, max}$	170	–	320	mA	–	P_7.5.2.2
Drop voltage	$V_{dr, QTx}$	–	–	400	mV	2)	P_7.5.2.3

Power supply ripple rejection	$PSRR_{QTx}$	26	–	–	dB	3) V_{PREREG} = 5.8 V ; ESRC_{QTx} ≤ 100 mΩ	P_7.5.2.4
Output capacitor	C_{QTx}	1	–	10	µF	3)	P_7.5.2.5
Output capacitor, ESR	$ESR\ C_{QTx}$	0	–	200	mΩ	3)	P_7.5.2.6

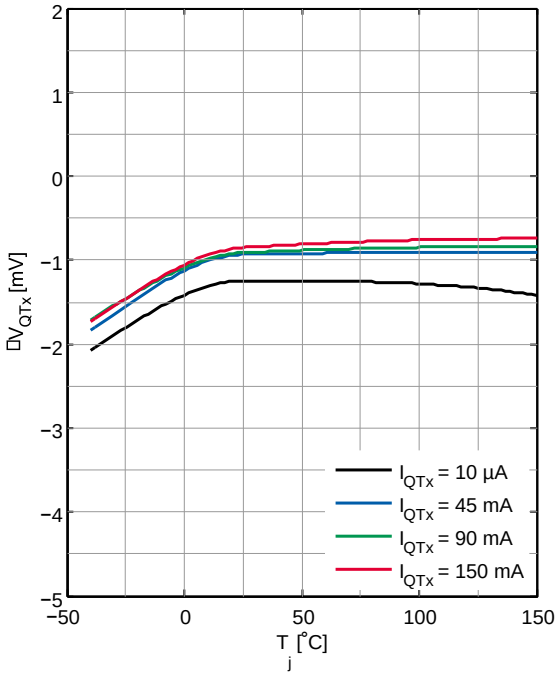
1) The output voltage of the tracker (pin QTx) is derived from the output voltage of the voltage reference (pin QVR). If the voltage reference is switched off (voltage at pin QVR = 0V), than the output voltage at pin QTx will also be 0V, if the tracker should be switched on, as the tracker output voltage is derived from pin QVR. But if the tracker is switched on and its output voltage is 0V (because voltage at pin QVR is 0V), an under voltage at pin QTx will be detected and an interrupt will be issued.

2) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

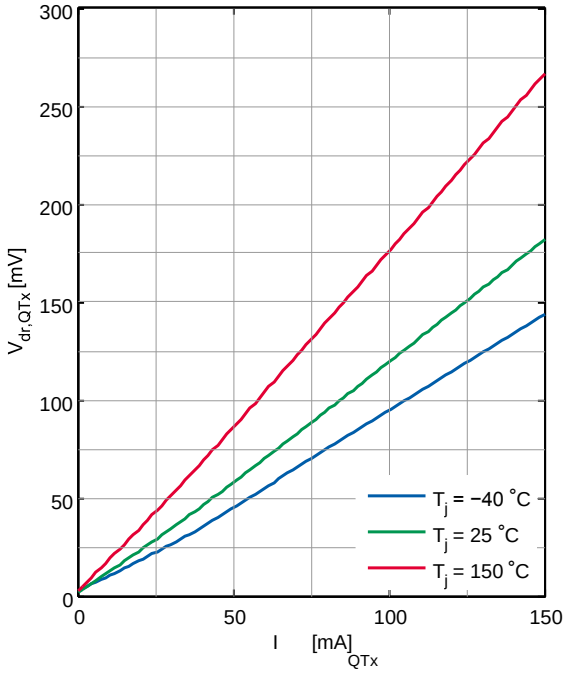
3) Specified by design, not subject to production test

7.5.3 Typical Performance Characteristics

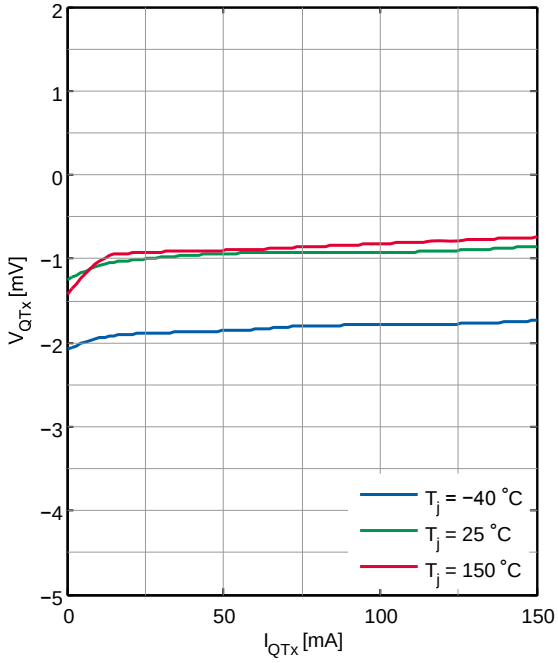
QTx Output Voltage V_{QTx} versus Junction Temperature T_j



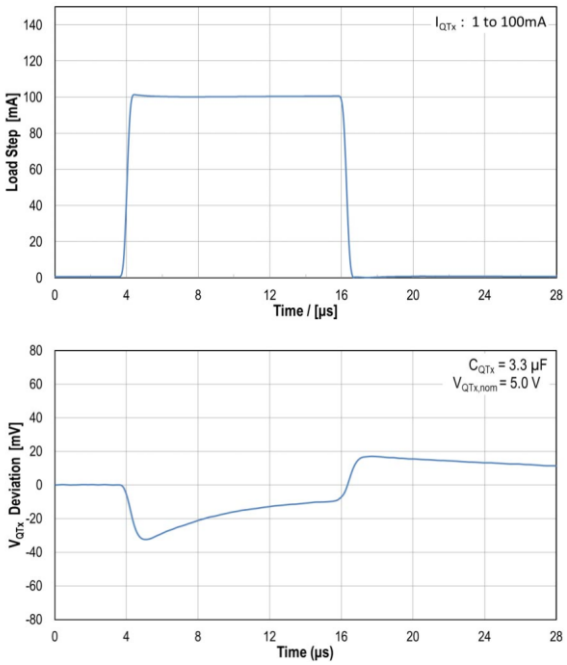
QTx Output Voltage V_{QTx} versus Load Current I_{QTx}



QTx Dropout Voltage $V_{dr,QTx}$ versus Load Current I_{QTx}



($V_{QTx,nom}$ = 5.0 V)



QTx Dynamic Load Response (1mA to 100mA)

7.6 External Post Regulator for Core Supply (optional)

An additional external post regulator may be added to the TLF35584 to provide the core supply voltage V_{Core_Supply} for the µC if needed.

In this case the configuration pin SEC has to be left open to indicate that the external core voltage supply option is active. The configuration of the SEC pin will only be read during the power sequencing at the point the core supply would be started (Movements to INIT, please refer to **Figure 16** and **Figure 17**).

The regulator is fed from the intermediate circuit voltage V_{PREREG}. The post regulator is enabled by a high signal at pin EVC and switched off by a low signal at pin EVC. The EVC signal is controlled by the state machine. For example a detection of over voltage at pin VCI will create a low signal at pin EVC and shut down the post regulator to protect the µC core.

The device offers a synchronization signal of 50% duty cycle at pin SYN equal in phase (only with a very small delay) and frequency or shifted by 180 degree to the internal step down pre regulator (the selection is done via SPI command). It is highly recommended to synchronize the external switch mode post regulator to this signal to avoid interferences. The external post regulator will be enabled as soon as the pre regulator output voltage V_{PREREG} is present and the LDO_µC output voltage V_{QUC} is above the lower reset threshold.

The output voltage of the post regulator V_{Core_Supply} will be monitored by the reset function of the device. To obtain a proper monitoring the output voltage of the post regulator has to be connected to the voltage monitoring input at pin VCI via a resistor divider. The resistor divider should be dimensioned to adjust the post regulator output voltage V_{Core_Supply} to the internal reset reference voltage V_{VCI}.

The synchronization signal at pin SYN can be switched on via SPI command, default configuration is off.

Protection circuitry should be installed to prevent the external regulator and the application from damage:

- To protect the pass device(s) of the external post regulator from overstress a current limitation function should limit the output current to the maximum specified limit. Current sensing should be done via a current mirror, no sense resistor should be used. In case the maximum current should occur, it will be limited, thus the output voltage will decrease. The regulator should be protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring of the TLF35584, no further reset function is required on the external post regulator. In case such a reset function should be present, it will not be used or supported

by the reset function of the TLF35584. In case of over voltage at pin, VCI the external post regulator will be switched off by pulling pin EVC to low and the TLF35584 will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VCI, the device will move into INIT state, pin ROT will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The external post regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage is present for more than t_{StG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).

- There should be a temperature shutdown function at the external post regulator. If the power stage temperature should exceed the temperature shutdown threshold, the post regulator should be switched off by its own temperature shutdown. The TLF35584 will recognize this as an under voltage and react as described above.

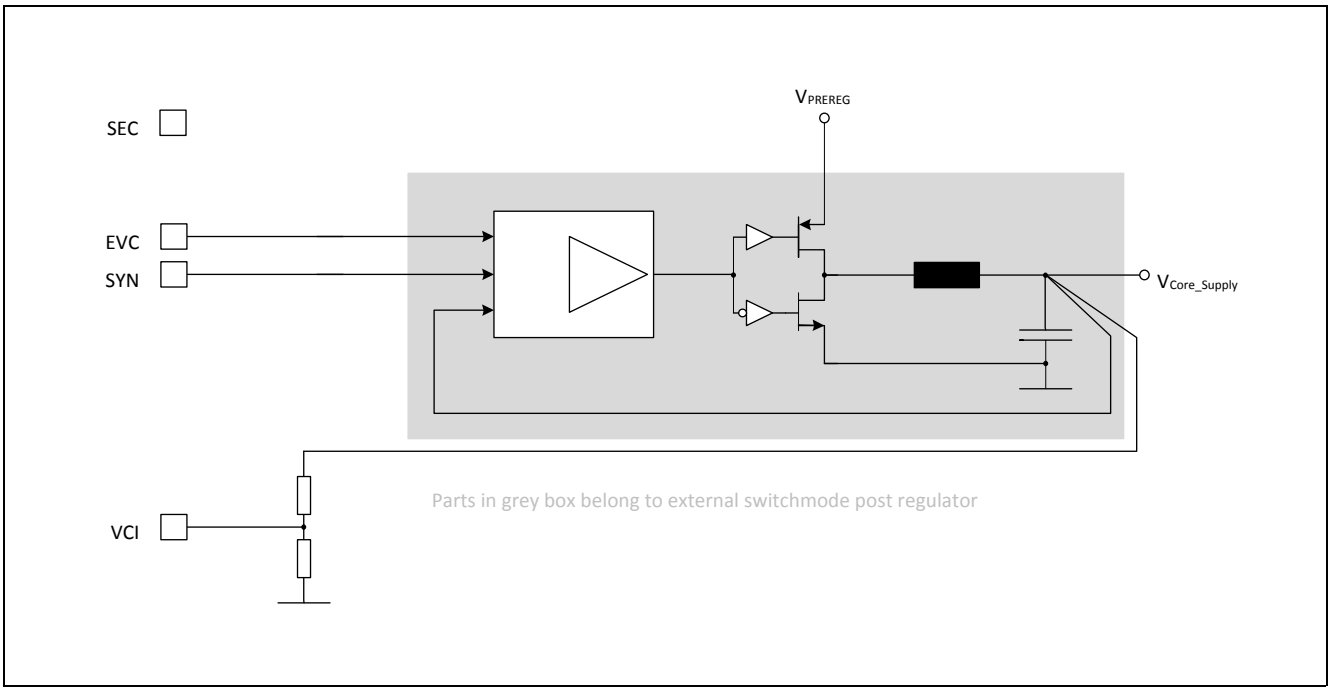


Figure 15 External switch mode post regulator for core supply

Table 14 Electrical characteristics: External post regulator

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable signal, pin EVC							
Enable high level TLF35584xxVS1	$V_{EVC, high}$	4.0	–	–	V	V_{QUC} = 5.0 V, I_{EVC} = -9 mA	P_7.6.0.1
Enable high level TLF35584xxVS1	$V_{EVC, high}$	4.6	–	–	V	V_{QUC} ≥ 4.7 V, I_{EVC} = -0.5 mA	P_7.6.0.2

Enable low level TLF35584xxVS1	$V_{EVC, low}$	–	–	0.7	V	V_{QUC} = 5.0 V I_{EVC} = 7 mA	P_7.6.0.3
Enable high level TLF35584xxVS2	$V_{EVC, high}$	2.3	–	–	V	V_{QUC} = 3.3 V I_{EVC} = -7 mA	P_7.6.0.4
Enable high level TLF35584xxVS2	$V_{EVC, high}$	3.0	–	–	V	V_{QUC} ≥ 3.1 V, I_{EVC} = -0.5 mA	P_7.6.0.5
Enable low level TLF35584xxVS2	$V_{EVC, low}$	–	–	0.7	V	V_{QUC} = 3.3 V I_{EVC} = 5.5 mA	P_7.6.0.6
Enable rise time	$t_{EVC, rise}$	–	–	25	ns	$C_{EVC, load}$ = 50 pF 1)	P_7.6.0.7
Enable fall time	$t_{EVC, fall}$	–	–	25	ns	$C_{EVC, load}$ = 50 pF 1)	P_7.6.0.8
Synchronisation signal source							
TLF35584xxVS1	$V_{SYN, high}$	4.0	–	–	V	V_{QUC} = 5.0 V, I_{SYN} = -9 mA	P_7.6.0.9

Sync out high level **Table 14 Electrical characteristics: External post regulator** (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
Sync out high level TLF35584xxVS1	$V_{SYN, high}$	4.6	–	–	V	V_{QUC} ≥ 4.7 V, I_{SYN} = -0.5 mA	P_7.6.0.10
Sync out low level TLF35584xxVS1	$V_{SYN, low}$	–	–	0.7	V	V_{QUC} = 5.0 V I_{SYN} = 7 mA	P_7.6.0.11
Sync out high level TLF35584xxVS2	$V_{SYN, high}$	2.3	–	–	V	V_{QUC} = 3.3 V I_{SYN} = -7 mA	P_7.6.0.12
Sync out high level TLF35584xxVS2	$V_{SYN, high}$	3.0	–	–	V	V_{QUC} ≥ 3.1 V, I_{SYN} = -0.5 mA	P_7.6.0.13
Sync out low level TLF35584xxVS2	$V_{SYN, low}$	–	–	0.7	V	V_{QUC} = 3.3 V I_{SYN} = 5.5 mA	P_7.6.0.14
Sync out signal duty cycle	D_{SYN}	–	50	–	%	–	P_7.6.0.15
Synch out signal rise time	$t_{SYN, rise}$	–	–	25	ns	$C_{SYN, load}$ = 50 pF 1)	P_7.6.0.16
Synch out signal fall time	$t_{SYN, fall}$	–	–	25	ns	$C_{SYN, load}$ = 50 pF 1)	P_7.6.0.17

Core voltage supply monitoring input							
pull-up current	I_{VCI}	–	100	130	nA	V_{VCI} = 0.8 V	P_7.6.0.18

1) specified by design, not subject to production test

Core voltage monitoring input I

7.7 Power Sequencing

The TLF35584 includes a power sequencing function to ensure a proper ramping up of all output voltages. After the internal Power-On-Reset (POR) is released the standby regulator and the pre regulator start to operate.

In case of one of the non microcontroller related voltages (Volt_Ref, LDO_Com, Tracker1 or Tracker2) cannot be ramped up (e.g. short to GND), the power sequence is stopped, but the reset output is still released after the power on reset delay time t_{rd}. The microcontroller should check the status of the outputs by reading the SPI status register
(**VMONSTAT**).

In case the microcontroller is sending a SPI request to enable or disable any non microcontroller related LDO (Volt_Ref, LDO_Com, Tracker1 or Tracker2) during the power sequencing, the sequence will be stopped and the requested configuration will be executed.

7.7.1 Power sequencing from POR to INIT state

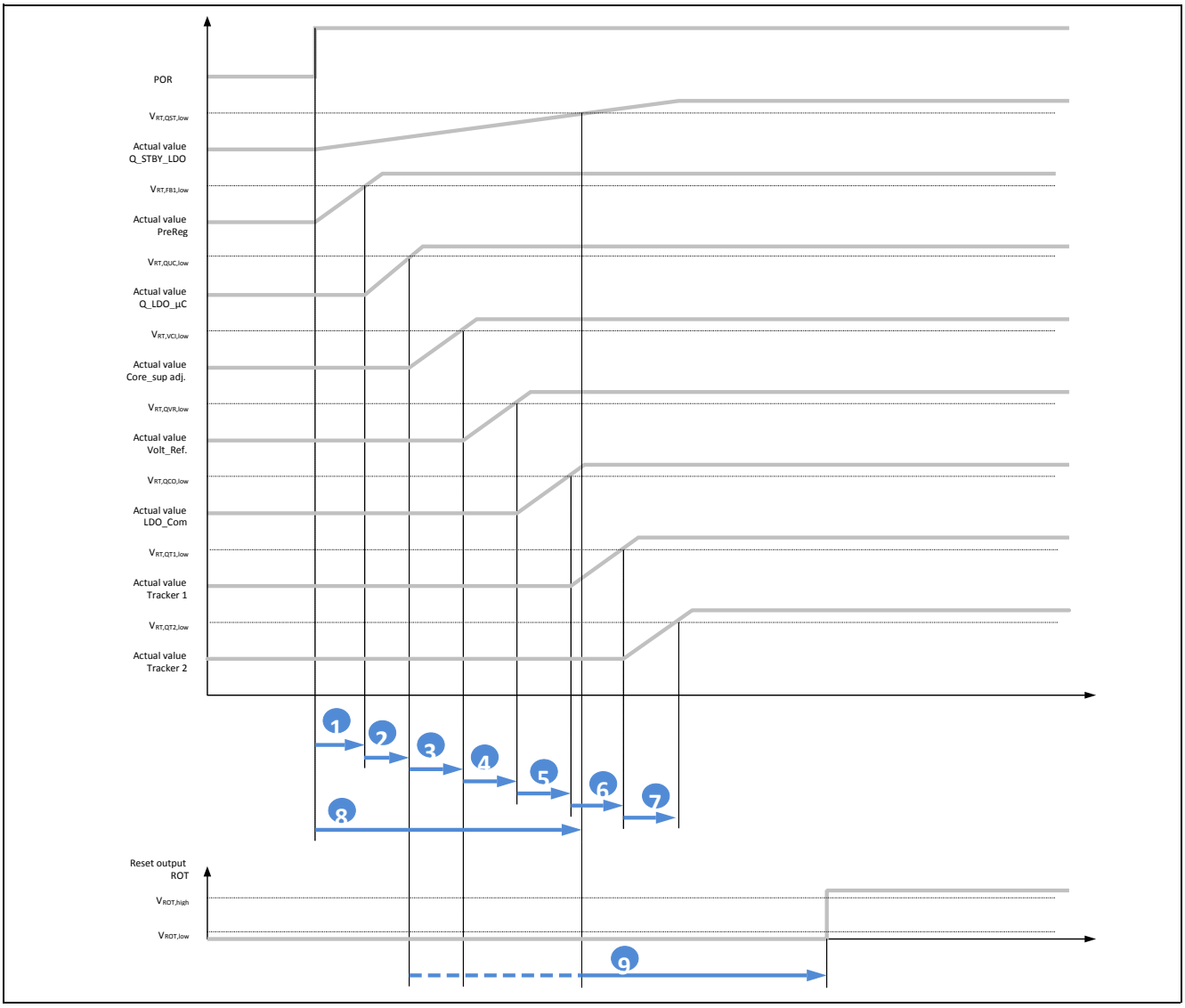


Figure 16 Power sequencing POR to INIT state

Description:

1. After POR is released the standby regulator and the pre regulator start to operate.
2. When V_{FB} is above the lower reset threshold $V_{RT,FB,low}$, the LDO_µC starts to operate.
3. When V_{QUC} is above the lower reset threshold $V_{RT,QUC,low}$, the external core supply will be enabled, when selected. If the external core supply is not selected, the voltage reference LDO starts to operate.
4. If the external core supply is selected and V_{VCI} is above the lower reset threshold $V_{RT,VCI,low}$, the voltage reference LDO starts to operate.
5. When V_{QVR} is above the lower reset threshold $V_{RT,QVR,low}$, the LDO_Com starts to operate.
6. When V_{QCO} is above the lower reset threshold $V_{RT,QCO,low}$, the Tracker 1 starts to operate.
7. When V_{QT1} is above the lower reset threshold $V_{RT,QTx,low}$, the Tracker 2 starts to operate.

8. This is the time from the enabling of the standby regulator until its output V_{QST} is above the lower reset threshold $V_{RT,QST,low}$.
9. The reset delay time t_{RD} starts after LDO_STBY, LDO_µC and the external core supply (if selected) have reached their lower reset threshold $V_{RT,x,low}$. The reset delay time is programmable via SPI. After the rest delay time is expired, the ROT pin is pulled to high. The figure shows the possibilities of the t_{RD} starting time.

Once the ROT is high, the microcontroller can change the configuration of the selectable LDOs which might change the power sequencing accordingly.

7.7.2 Power sequencing STANDBY to INIT state

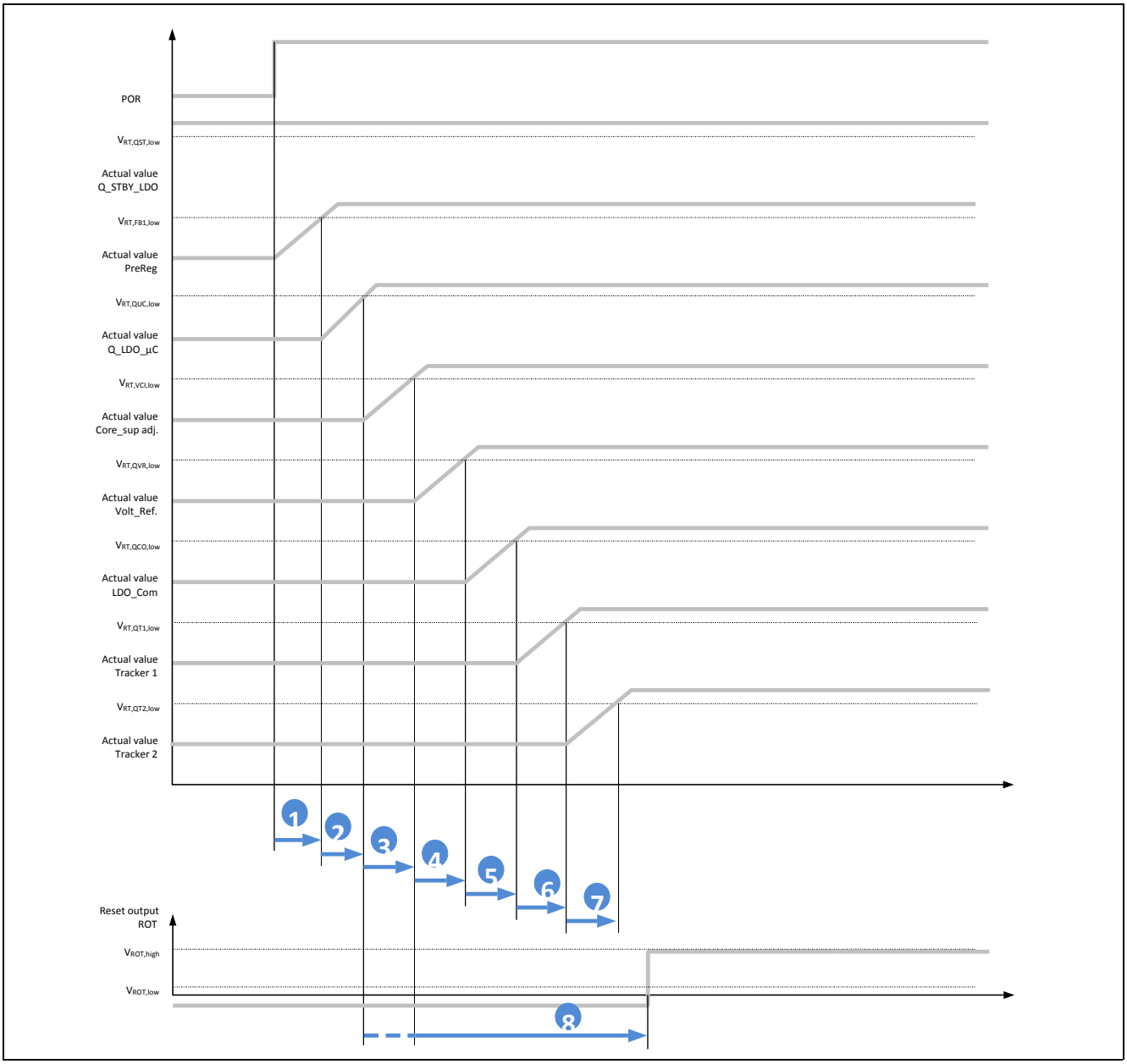


Figure 17 Power sequencing STANDBY to INIT state

Description: Input voltage is present, device is in STANDBY state, LDO_STBY is active.

1. After a valid Wake-Signal or an expired wake-up timer the pre regulator starts to operate.
2. When V_{FB} is above the lower reset threshold $V_{RT,FB,low}$, the LDO_µC starts to operate.
3. When V_{QUC} is above the lower reset threshold $V_{RT,QUC,low}$, the external core supply will be enabled, when selected. If the external core supply is not selected, the voltage reference LDO starts to operate.
4. If the external core supply is selected and V_{VCI} is above the lower reset threshold $V_{RT,VCI,low}$, the voltage reference LDO starts to operate.

5. When V_{QVR} is above the lower reset threshold $V_{RT,QVR,low}$, the LDO_Com starts to operate.
6. When V_{QCO} is above the lower reset threshold $V_{RT,QCO,low}$, the Tracker 1 starts to operate.
7. When V_{QT1} is above the lower reset threshold $V_{RT,QTx,low}$, the Tracker 2 starts to operate.
8. The reset delay time t_{RD} starts after LDO_µC and the external core supply (if selected) have reached their lower reset threshold $V_{RT,x,low}$. The reset delay time is programmable via SPI. After the rest delay time is expired the ROT pin is pulled to high. The figure shows the possibilities of the t_{RD} starting time.

7.7.3 Power sequencing SLEEP to WAKE state

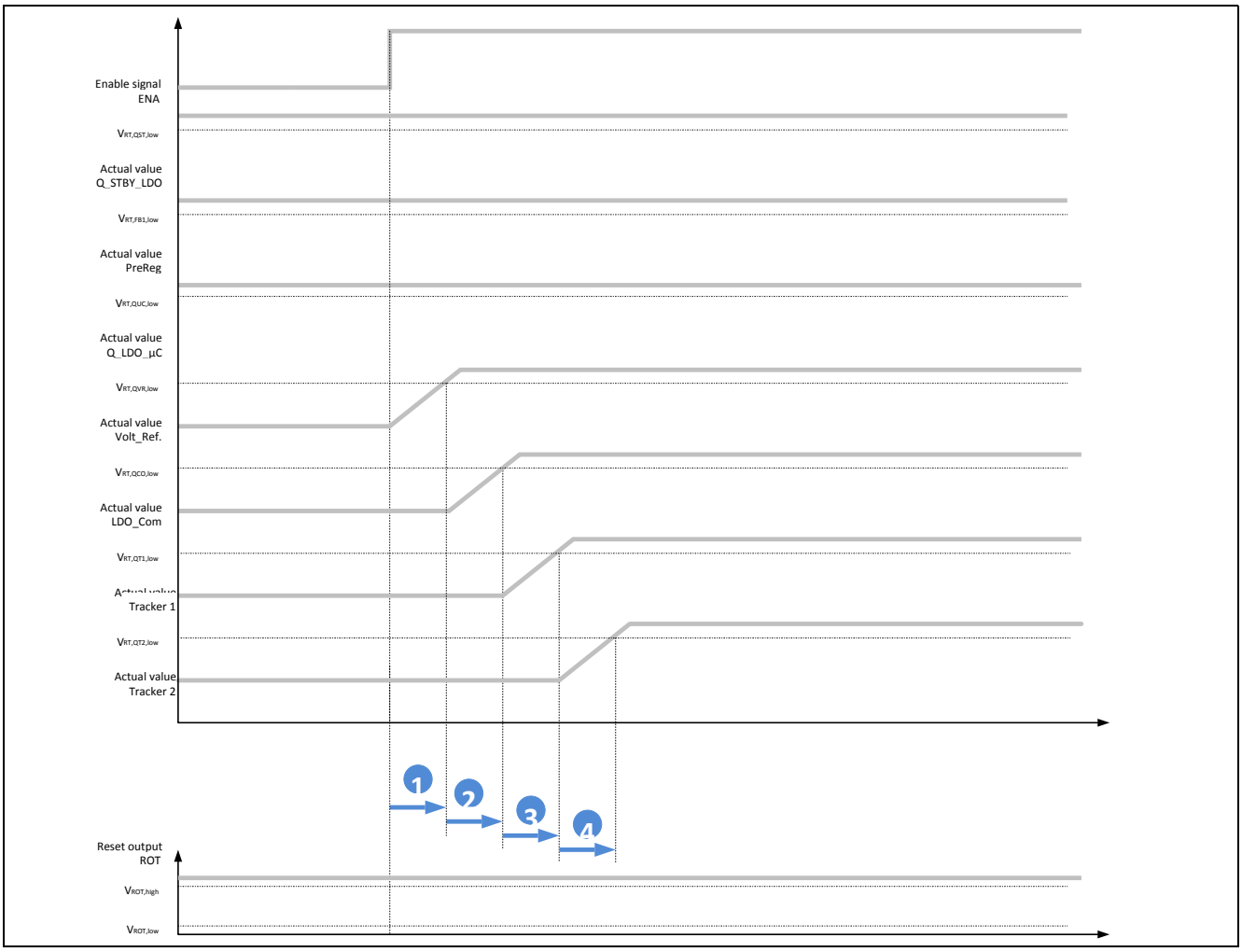


Figure 18 Power sequencing SLEEP to WAKE state

Description: Input voltage is present, device is in SLEEP state, all selectable LDOs switched off in SLEEP state, all selectable LDOs were switched on in previous NORMAL state:

1. After a valid Wake-Signal or an expired wake-up timer the voltage reference starts to operate.
2. When V_{QVR} is above the lower reset threshold $V_{RT,QVR,low}$, the LDO_Com starts to operate.
3. When V_{QCO} is above the lower reset threshold $V_{RT,QCO,low}$, the Tracker 1 starts to operate.
4. When V_{QT1} is above the lower reset threshold $V_{RT,QTx,low}$, the Tracker 2 starts to operate.

The reset output ROT is high in SLEEP state and will be kept high for WAKE state.

In case a selectable LDO was switched off in the previous NORMAL state, it will not be enabled during the transition from SLEEP to WAKE, the power sequencing will follow up with the next LDO. In case a LDO was enabled during SLEEP state and was enabled in the previous NORMAL state, it will be kept enabled.

8 Monitoring Function

8.1 Introduction

The TLF35584 includes an independent voltage monitoring function of all output voltages, including the optional external post regulator for µC core supply, if in use.

The monitoring function consists of two comparators for each output voltage. One is for detecting over voltage, the other is for detecting under voltage. Both comparators get their reference value from an independent bandgap only used for the voltage monitoring block. This bandgap is independent from the voltage regulator bandgap. The bandgap provides the reference value for over voltage detection (highvoltage reset threshold $V_{RT,xxx,high}$) and for under voltage detection (low voltage reset threshold $V_{RT,xxx,low}$). Under normal operation conditions the output voltage of the related regulator has to stay within the voltage window defined by the upper limit $V_{RT,xxx,high}$ and the lower limit $V_{RT,xxx,low}$.

There is a dedicated temperature sensor for the monitoring block. If the power stage temperature exceeds the temperature shutdown threshold, the device will move into FAILSAFE state, the regulator will be switched off and the event will be stored in an SPI status register (**OTFAIL**). The off time due to temperature shut down will be at least one second.

Characteristics:

The behavior of the over and under voltage comparators is as following:

- The upper limits $V_{RT,xxx,high}$ and the lower limits $V_{RT,xxx,low}$ are fixed for every regulator and cannot be programmed or varied by SPI command.
- An over voltage will be detected if the regulator output voltage is higher than the related over voltage reset threshold $V_{RT,xxx,high}$ for more than the reset reaction time t_{RR}. An over voltage higher than the related over voltage reset threshold $V_{RT,xxx,high}$ which is present for shorter than the reset reaction time t_{RR} will be regarded as a spike and will not be detected.
  An under voltage will be detected if the regulator output voltage is lower than the related under voltage reset threshold $V_{RT,xxx,low}$ for more than the reset reaction time t_{RR}. An under voltage lower than the related under voltage reset threshold $V_{RT,xxx,low}$ which is present for shorter than the reset reaction time t_{RR} will be regarded as a spike and will not be detected.
- The reset reaction time t_{RR} is not valid for the internal voltage supplies in case of under and over voltage.
- The detection of an over voltage will shut down the related regulator immediately to protect the loads from harm or destruction. This shut down may lead (depending on the affected regulator) to further action, please refer to chapter **State Machine** for details.
- The detection of an under voltage will not shut down the related regulator.
- The post regulators (including the optional external post regulator for µC core supply) have a short to ground detection. If the detected under voltage is present for more than the short to ground detection time t_{StG}, the related regulator will shut down to protect himself and the chip from over heating. This shut down may lead (depending on the affected regulator) to further action, please refer to chapter **State Machine** for details. (It is mandatory that the external post regulator for µC core supply has an enable or inhibit function).
- The over and under voltage detection is active only if the related regulator is in use (including the external post regulator for µC core supply) and switched on.

Indication of over and under voltage:

Depending on the related regulator the indication of over and under voltage will be different, either by reset signal or by interrupt indication:

- Every over and under voltage detection will be stored in the SPI status register (**MONSF0**, **MONSF1**, **MONSF2**).
- For µC related output voltages (V_{QST} , V_{QUC} , V_{VCI}), over and under voltage are indicated by the hardware reset pin ROT. In case of an over or under voltage, pin ROT is pulled to low.
- In case of over voltage or a detection of a short to ground at the external post regulator for µC core supply, the pin EVC will be pulled to low to shut down the regulator.
- For the pre regulator output (V_{FB}) and the voltage reference output (V_{QVR}) only over voltage is indicated by the hardware reset pin ROT. In case of an over voltage, pin ROT is pulled to low.
- For the pre regulator output and the voltage reference output, only under voltage is indicated by an interrupt.
- For all not µC related output voltages (V_{QCO} , V_{QT1} , V_{QT2}), over and under voltage are indicated by an interrupt.
- For the internal supply voltages, over and under voltage are indicated by the hardware reset pin ROT. In case of an over or under voltage, pin ROT is pulled to low.

This introduction is an overview, for details please refer to the following sub chapters.

8.2 Shutdown Function

A short to ground detection time t_{StG} at the pre regulator output is only active during the power sequence in INIT state. If the output voltage of the pre regulator should not be within the specified limits within a certain time frame, the device will move into FAILSAFE state. There will be no reaction on a detected short to ground once the $V_{PREREG,BUCK}$ is in a valid range after crossing the first time its UV threshold (step 1 completed according to the power sequencing described in **Chapter 7.7**). If the output voltage of the pre regulator should be too low in other cases, the behavior of the device will depend on the voltage monitoring of the post regulators.

The detection of an over voltage at output voltages V_{QUC}, V_{VCI}, V_{QST}, V_{QVR} or V_{FB} will shut down all regulators to protect the loads from harm or destruction and moves the device to FAILSAFE.

The detection of an over voltage at output voltages V_{QCO}, V_{QT1} and V_{QT2} will shut down the related regulator to protect the loads from harm or destruction and generate an interrupt event.

If the detected under voltage at output voltages V_{QUC}, V_{VCI} or V_{QST} should be present for more than the short to ground detection time t_{StG}, all regulators will shut down to protect themselves and the chip from over heating and move the device to FAILSAFE.

If the detected under voltage at output voltages V_{QVR}, V_{QCO}, V_{QT1} or V_{QT2} should be present for more than the short to ground detection time tStG, the related regulator will shut down to protect himself and the chip from over heating and generate an interrupt event.

8.3 Reset Function

The reset generator starts to operate as soon as the internal POR is released.

Distinguish between “Soft Reset” and “Hard Reset”

It is called a “Soft Reset” if pin ROT goes below $V_{ROT,low}$, but the pre and post regulator output voltages are not switched off.

It is called a “Hard Reset” if pin ROT goes below $V_{ROT,low}$ and the post regulator output voltages are switched off. The power sequencing will be restarted after a delay of t_{SDT}.(Applicable to the second initialization timeout in a row)

Safe State Control trigger event

The safe state control function is connected to the monitoring block. In case of a safe state control trigger event is detected, pins Safe State Control Outputs (SS1 and SS2) and ROT will be pulled to ground. The safe state control trigger event will be stored in a SPI register (respective bits in **SYSFAIL**, **INITERR**, **MONSF1**, **MONSF2**, **MONSF3** or **OTFAIL**). For trigger conditions of safe state signal SS1 please refer to chapter **Safe State Control Function**.

Reset output pin

The reset output pin ROT is an open drain structure. As soon as a reset condition occurs, the ROT pin is pulled below $V_{ROT,low}$. An internal pull up current is pulling the output towards V_{QUC}.

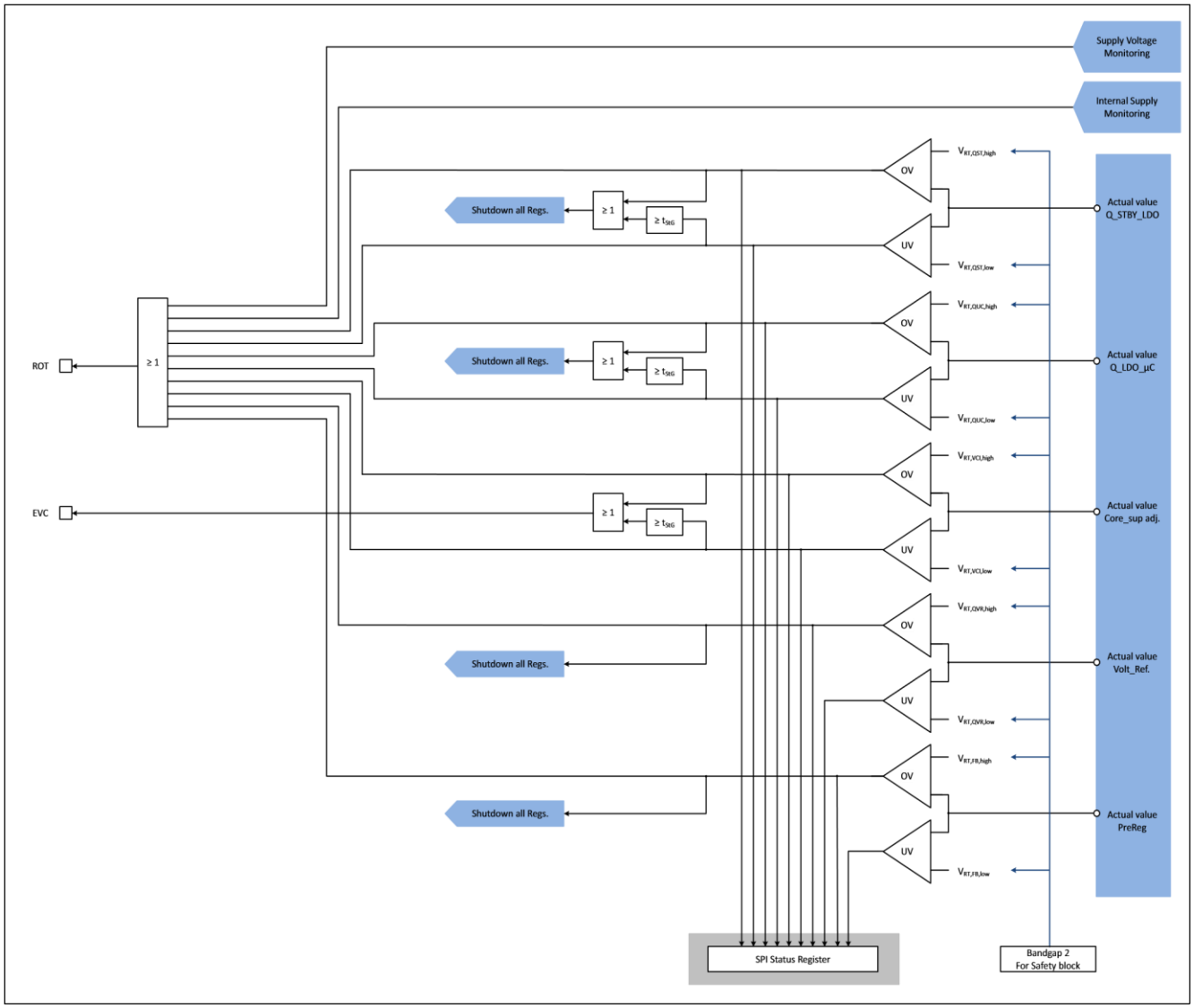


Figure 19 Principle reset function

Detailed description of the reset function (Figure 19):

The following regulators contribute to the reset function:

- Internal supply monitoring (not visible externally)
- The standby regulator (Q_STBY_LDO): V_{QST}
- The LDO for supplying the µC (Q_LDO_µC): V_{QUC}
- The external post regulator for µC core supply (Core_sup adj.): V_{VCI}
- The voltage reference (Volt_Ref.): V_{QVR} - only over voltage, not under voltage, not short to ground
- The pre regulator (PreReg.): V_{FB} - only over voltage, not under voltage

The actual values of these outputs are taken directly at the output pins and are monitored by two comparators for each regulator, one for over voltage (named OV), the other for under voltage (named UV). The reference values $V_{RT,XXX,high}$ and $V_{RT,XXX,low}$ are provided by an independent band gap 2 only related to the monitoring functions.

The “Internal supply voltage regulator monitoring” of over and under voltage events and IBIAS monitoring are contributing to trigger a reset. If one or both of the internal supply voltages should be out of their specified windows, the proper function of the device cannot be guaranteed any more. The IBIAS monitor fault is stored in a status bit (**BIASHI** or **BIASLOW**). The fault of the internal supplies will trigger a “Move to Powerdown” event (please refer to chapter **State Machine** for details).

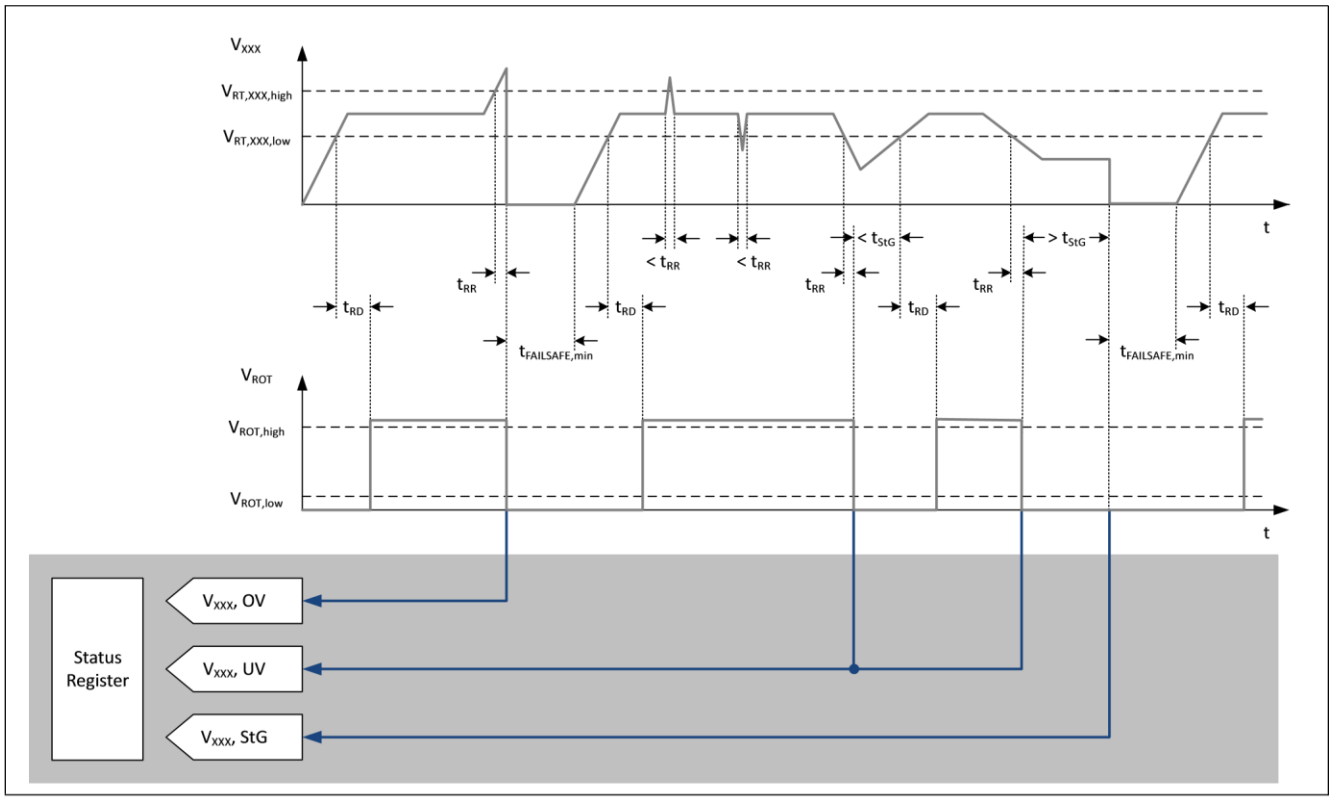


Figure 20 Timing diagram hardware reset signal ROT for output voltages

Description:

- V_{XXX} = Output voltage monitored by reset generator: V_{QUC} , V_{VCI}, V_{QST}, V_{QVR} or V_{FB}
- $V_{RT,XXX,high}$= Over voltage reset threshold: $V_{RT,QUC,high}$, $V_{RT,VCI,high}$, $V_{RT,QST,high}$, $V_{RT,QVR,high}$ or $V_{RT,FB,high}$
- $V_{RT,XXX,low}$= Under voltage reset threshold: $V_{RT,VCI,low}$, $V_{RT,QUC,low}$ or $V_{RT,QST,low}$
- t_{RD} = Reset delay time, adjustable by SPI command
- t_{RR} = Reset reaction time, time between detecting over voltage and pulling ROT to low
- < t_{RR} = Not detectable, because shorter than reset reaction time
- > t_{StG} = Short to ground detection time, time after an under voltage is considered as a short to ground
- $t_{FAILSAFE,min}$ = System shutdown time (FAILSAFE), time between pulling ROT to low and restart of the device, for details please refer to chapter **State Machine**
- V_{ROT} = Hardware reset signal, ROT
- $V_{ROT,high}$ = Hardware reset signal, high level

- $V_{ROT,low}$ = Hardware reset signal, low level
- $V_{XXX,OV}$ = Over voltage detected for V_{XXX} and stored in SPI register (**MONSF1**)
- $V_{XXX,UV}$ = Under voltage detected for V_{XXX} and stored in SPI register (**MONSF2**)
- $V_{XXX,StG}$ = Short to ground detected for V_{XXX} and stored in SPI register (**MONSF0**)
- Applies as well to bias current violations, supply overvoltage (**MONSF3**), temperature shutdown (**OTFAIL**) contributing to the reset function. Please refer to **Figure 43** and **Figure 50**

8.4 Interrupt Function

The interrupt generator starts to operate as soon as the internal POR is released.

The voltage monitoring function supervises the values of the non µC related post regulator output voltages V_{QCO}, V_{QT1} and V_{QT2}, the pre regulator output voltage V_{FB} (under voltage only) and the voltage reference output V_{QVR} (under voltage and short to ground only). The result is written in a SPI status register (**IF** and **MONSF0**, **MONSF1** or **MONSF2**) and indicated via interrupt (pin INT). The connection of all these monitoring signals is a logic OR.

The interrupt pin INT does not only indicate the result of the voltage monitoring, but also interrupts due to other events in the device.

Interrupt output pin

The interrupt output pin INT is a push pull structure. An interrupt is indicated by pulling the INT pin to ground.

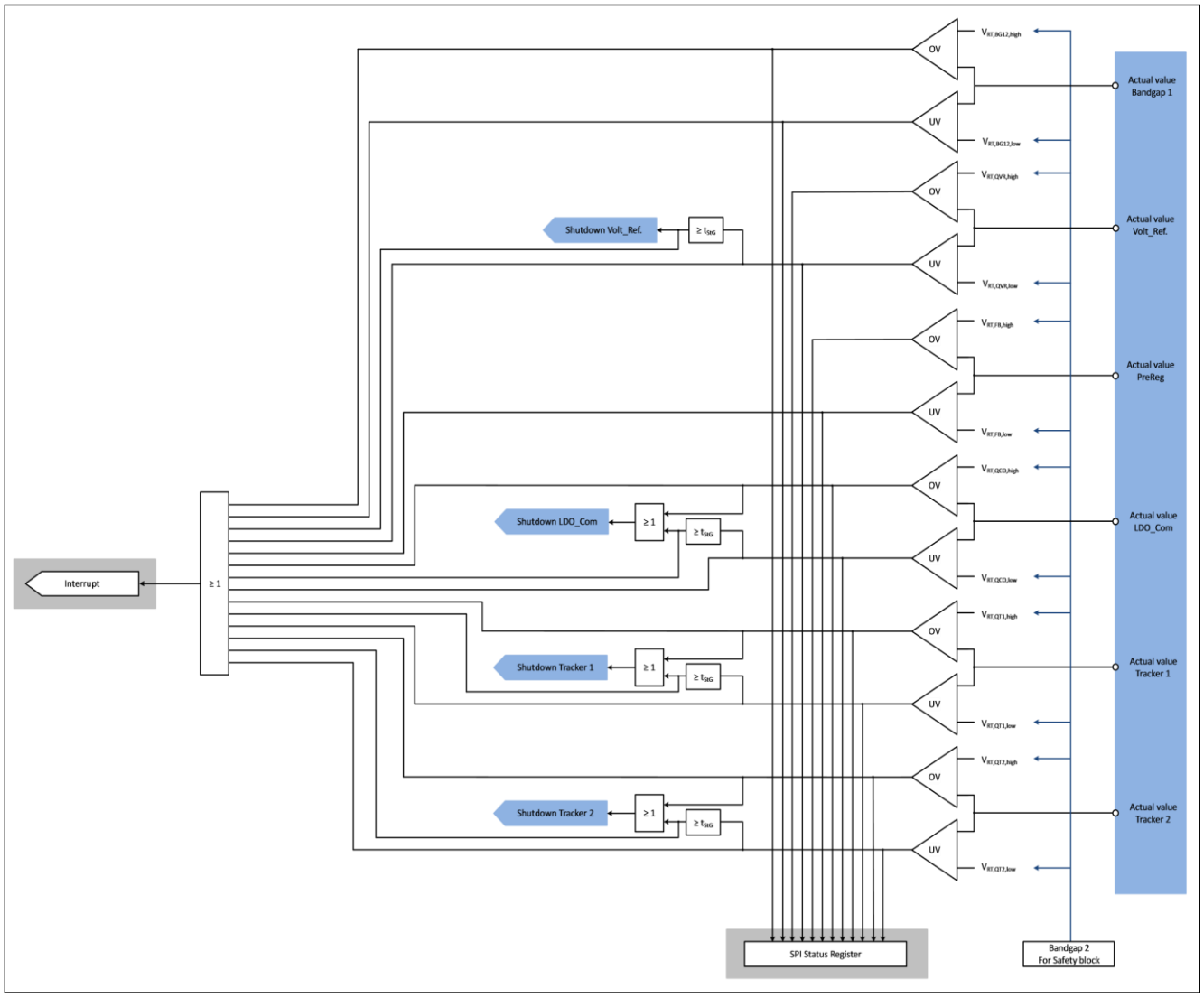


Figure 21 Principle indication of voltage monitoring via interrupt

Detailed description of the voltage monitoring via interrupt function (Figure 21):

The following regulators contribute to the voltage monitoring via interrupt function:

- The pre regulator (PreReg.): V_{FB} , just under voltage
- The voltage reference (Volt_Ref.): V_{QVR} , just under voltage and short to GND
- The LDO for supplying the communication (LDO_Com): V_{QCO}
- The sensor supply 1 (Tracker 1): V_{QT1}
- The sensor supply 2 (Tracker 2): V_{QT2}

The actual values of these outputs are taken directly at the output pins and monitored by two comparators for each regulator, one for over voltage (named OV), the other for under voltage (named UV). The reference values $V_{RT,XXX,high}$ and $V_{RT,XXX,low}$ are provided by an independent band gap 2 only related to the monitoring functions.

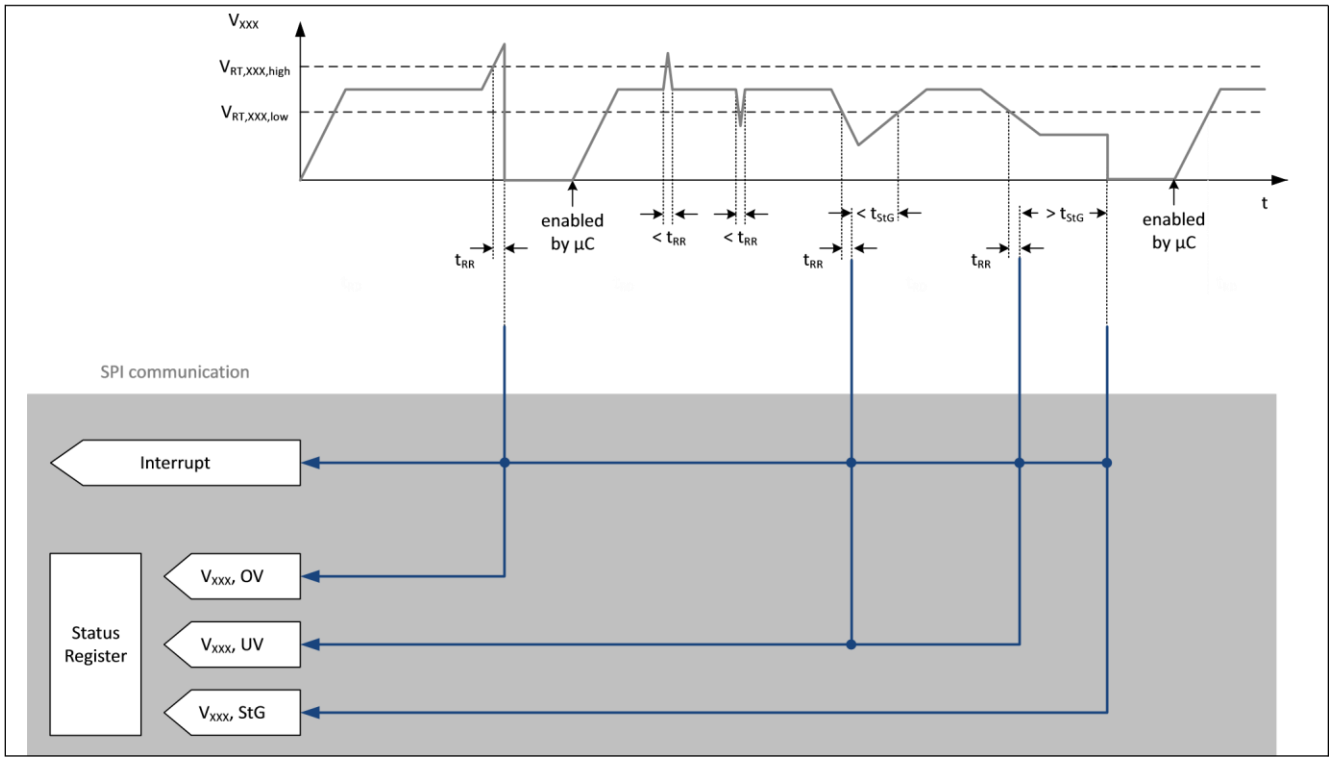


Figure 22 Timing diagram interrupt indication for output voltages

Description:

- V_{XXX} = Output voltage monitored by interrupt indication: V_{FB} , V_{QVR}, V_{QCO} , V_{QT1} or V_{QT2}
- $V_{RT,XXX,high}$= Over voltage interrupt indication: $V_{RT,QCO,high}$, $V_{RT,QT1,high}$ or $V_{RT,QT2,high}$
- $V_{RT,XXX,low}$= Under voltage interrupt indication: $V_{RT,FB,low}$, $V_{RT,QVR,low}$, $V_{RT,QCO,low}$, $V_{RT,QT1,low}$ or $V_{RT,QT2,low}$
- t_{RR} = Reset reaction time, time between detecting overvoltage and an interrupt is generated
- < t_{RR} = Not detectable, because shorter than reset reaction time
- > t_{StG} = Short to ground detection time, time after an under voltage is considered as a short to ground
- $V_{XXX,OV}$ = Over voltage detected for V_{XXX} and stored in SPI register (**MONSF1**)
- $V_{XXX,UV}$ = Under voltage detected for V_{XXX} and stored in SPI register (**MONSF2**)
- $V_{XXX,StG}$ = Short to ground detected for V_{XXX} and stored in SPI register (**MONSF0**)
- Applies as well to detection of bandgap 1 to 2 variations (**MONSF3**), over load and temperature events (**OTWRNSF**, **OTFAIL**) contributing to the interrupt function. Please refer to **Figure 42**

8.5 Electrical Characteristics Voltage Monitoring and Reset Function

Table 15 Electrical Characteristics: Hardware reset signals

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values	Unit	Note /	Number

		Min.	Typ.	Max.		Test Condition	
Timing							
Reset cycle time	t_{CYCLE}	9.4	10	10.65	µs	–	P_8.5.1
Reset delay time, default value	t_{RD}	–	1000	–	t_{CYCLE}	–	P_8.5.2
Reset delay time, adjustable range by SPI command	t_{RD}	20	–	1500	t_{CYCLE}	1)	P_8.5.3
Reset reaction time	t_{RR}	8	–	20	µs	–	P_8.5.4
Reset reaction time, standby regulator	$t_{RR, STBY}$	8	–	40	µs	–	P_8.5.5
Short to ground detection time	t_{StG}	2.7	3	3.3	ms		P_8.5.6
Step-down regulator short to ground detection time	$t_{StG,HF}$	2.7	3	3.3	ms	step down pre regulator 2.2 MHz switching frequency	P_8.5.7
Step-down regulator short to ground detection time	$t_{StG,LF}$	5.4	6	6.6	ms	step down pre regulator 400 kHz switching frequency	P_8.5.8
System shutdown time	t_{SDT}	9	–	20	ms	–	P_8.5.9
Reset thresholds standby regulator, pin QST							
Over voltage reset threshold TLF35584xxVS1	$V_{RT,QST,high}$	5.25	5.35	5.45	V	V_{QST} increasing	P_8.5.10
Over voltage reset hysteresis TLF35584xxVS2	$V_{RT,QST,OV\ hyst}$	30	–	90	mV	–	P_8.5.11
Under voltage reset threshold TLF35584xxVS1	$V_{RT,QST,low}$	4.2	4.3	4.4	V	V_{QST} decreasing	P_8.5.12
Under voltage reset hysteresis TLF35584xxVS1	$V_{RT,QST,UV\ hyst}$	30	–	70	mV	–	P_8.5.13
Over voltage reset threshold TLF35584xxVS2	$V_{RT,QST,high}$	3.46	3.53	3.6	V	V_{QST} increasing	P_8.5.14
Over voltage reset hysteresis TLF35584xxVS2	$V_{RT,QST,OV\ hyst}$	20	–	55	mV	–	P_8.5.15
Under voltage reset threshold TLF35584xxVS2	$V_{RT,QST,low}$	2.9	2.97	3.05	V	V_{QST} decreasing	P_8.5.16
Under voltage reset hysteresis TLF35584xxVS2	$V_{RT,QST,UV\ hyst}$	20	–	50	mV	–	P_8.5.17
Reset thresholds LDO_µC, pin QUC							

Table 15 Electrical Characteristics: Hardware reset signals (cont'd)

V_{VS} = 6.0 V to 40 V; T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin, unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Monitoring Function Number
		Min.	Typ.	Max.			
Over voltage reset threshold (TLF35584xxVS1)	$V_{RT,QUC,high}$	5.25	5.35	5.45	V	$V_{LDO\_\mu C}$ increasing	P_8.5.18
Over voltage reset hysteresis TLF35584xxVS1	$V_{RT,QUC,OV\ hyst}$	30	–	90	mV	2)	P_8.5.19
Under voltage reset threshold TLF35584xxVS1	$V_{RT,QUC,low}$	4.2	4.3	4.4	V	$V_{LDO\_\mu C}$ decreasing	P_8.5.20
Under voltage reset hysteresis TLF35584xxVS1	$V_{RT,QUC,UV\ hyst}$	30	–	70	mV	2)	P_8.5.21
Over voltage reset threshold TLF35584xxVS2	$V_{RT,QUC,high}$	3.46	3.53	3.6	V	V_{QUC} increasing	P_8.5.22
Over voltage reset hysteresis TLF35584xxVS2	$V_{RT,QUC,OV\ hyst}$	20	–	55	mV	2)	P_8.5.23
Under voltage reset threshold TLF35584xxVS2	$V_{RT,QUC,low}$	2.9	2.97	3.05	V	V_{QUC} decreasing	P_8.5.24
Under voltage reset hysteresis TLF35584xxVS2	$V_{RT,QUC,UV\ hyst}$	20	–	50	mV	2)	P_8.5.25
Reset thresholds external core supply, pin VCI							
Over voltage reset threshold	$V_{RT,VCI,high}$	860	872	884	mV	V_{VCI} increasing	P_8.5.26
Over voltage reset hysteresis	$V_{RT,VCI,OV\ hyst}$	5	–	15	mV	2)	P_8.5.27
Under voltage reset threshold	$V_{RT,VCI,low}$	716	728	740	mV	V_{VCI} decreasing	P_8.5.28
Under voltage reset hysteresis	$V_{RT,VCI,UV\ hyst}$	5	–	15	mV	2)	P_8.5.29
Reset thresholds V_PreReg, pins FBx							
Over voltage reset threshold	$V_{RT,FB,high}$	6.46	6.58	6.7	V	V_{FB} increasing	P_8.5.30
Over voltage reset hysteresis	$V_{RT,FB,OV\ hyst}$	40	–	120	mV	–	P_8.5.31
Under voltage reset threshold	$V_{RT,FB,low}$	5.0	5.1	5.2	V	V_{FB} decreasing	P_8.5.32
Under voltage reset hysteresis	$V_{RT,FB,UV\ hyst}$	30	–	90	mV	–	P_8.5.33
Reset thresholds LDO_Com, pin QCO							
Over voltage reset threshold	$V_{RT,QCO,high}$	5.4	5.5	5.6	V	V_{QCO} increasing	P_8.5.34
Over voltage reset hysteresis	$V_{RT,QCO,OV\ hyst}$	30	–	90	mV	–	P_8.5.35
Under voltage reset threshold	$V_{RT,QCO,low}$	4.4	4.5	4.6	V	V_{QCO} decreasing	P_8.5.36
Under voltage reset hysteresis	$V_{RT,QCO,UV\ hyst}$	20	–	80	mV	–	P_8.5.37
Reset thresholds voltage reference, pin QVR							

Table 15 Electrical Characteristics: Hardware reset signals (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Over voltage reset threshold	$V_{RT,QVR,high}$	5.25	5.35	5.45	V	V_{QVR} increasing	P_8.5.38

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over voltage reset hysteresis	$V_{RT,QVR,OV\ hyst}$	30	–	80	mV	–	P_8.5.39
Under voltage reset threshold	$V_{RT,QVR,low}$	4.2	4.3	4.4	V	V_{QVR} decreasing	P_8.5.40
Under voltage reset hysteresis	$V_{RT,QVR,UV\ hyst}$	30	–	70	mV	–	P_8.5.41
Reset thresholds tracker 1, pin QT1							
Over voltage reset threshold	$V_{RT,QT1,high}$	5.4	5.5	5.6	V	V_{QT1} increasing	P_8.5.42
Over voltage reset hysteresis	$V_{RT,QT1,OV\ hyst}$	30	–	90	mV	–	P_8.5.43
Under voltage reset threshold	$V_{RT,QT1,low}$	4.4	4.5	4.6	V	V_{QT1} decreasing	P_8.5.44
Under voltage reset hysteresis	$V_{RT,QT1,UV\ hyst}$	20	–	80	mV	–	P_8.5.45
Reset thresholds tracker 2, pin QT2							
Over voltage reset threshold	$V_{RT,QT2,high}$	5.4	5.5	5.6	V	V_{QT2} increasing	P_8.5.46
Over voltage reset hysteresis	$V_{RT,QT2,OV\ hyst}$	30	–	90	mV	–	P_8.5.47
Under voltage reset threshold	$V_{RT,QT2,low}$	4.4	4.5	4.6	V	V_{QT2} decreasing	P_8.5.48
Under voltage reset hysteresis	$V_{RT,QT2,UV\ hyst}$	20	–	80	mV	–	P_8.5.49
Input Voltage VSx Monitoring, pin VSx							
Input over voltage reset threshold	$V_{VS,OV}$	45	47	49	V		P_8.5.50
Overtemperature Protection of Monitoring							
Over temperature shutdown threshold	$T_{j,OT,\ shutdown}$	175	190	205	°C	T_j increasing 2)	P_8.5.51
Over temperature shutdown hysteresis	$T_{j,OT,\ hyst}$	–	10	–	°C	2)	P_8.5.52
Reset output ROT							
Reset output, pull-up current	$I_{ROT,\ pu}$	-175	-110	-15	µA	V_{ROT} <= 2.0 V	P_8.5.53

Table 15 Electrical Characteristics: Hardware reset signals (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reset output, low level TLF35584xxVS1	$V_{ROT, low}$	–	–	0.7	V	V_{QUC} = 5.0 V, I_{ROT} = 7 mA	P_8.5.54
Reset output, low level TLF35584xxVS1	$V_{ROT, low}$	–	–	0.4	V	V_{QUC} = 5.0 V, I_{ROT} = 3.5 mA	P_8.5.55
Reset output, low level TLF35584xxVS2	$V_{ROT, low}$	–	–	0.7	V	V_{QUC} = 3.3 V, I_{ROT} = 5.5 mA	P_8.5.56
Reset output, low level TLF35584xxVS2	$V_{ROT, low}$	–	–	0.4	V	V_{QUC} = 3.3 V, I_{ROT} = 3 mA	P_8.5.57
Reset output fall time [2]	$t_{ROT, fall}$	–	–	25	ns	$C_{ROT,load}$ = 50 pF	P_8.5.58
Interrupt output INT							
Interrupt output, high level TLF35584xxVS1	$V_{INT, high}$	4.0	–	–	V	V_{QUC} = 5.0 V, I_{INT} = -9 mA	P_8.5.59
Interrupt output, low level TLF35584xxVS1	$V_{INT, low}$	–	–	0.7	V	V_{QUC} = 5.0 V I_{INT} = 7 mA	P_8.5.60
Interrupt output, high level TLF35584xxVS2	$V_{INT, high}$	2.3	–	–	V	V_{QUC} = 3.3 V I_{INT} = -7 mA	P_8.5.61
Interrupt output, low level TLF35584xxVS2	$V_{INT, low}$	–	–	0.7	V	V_{QUC} = 3.3 V I_{INT} = 5.5 mA	P_8.5.62
Interrupt output rise time [2]	$t_{INT, rise}$	–	–	25	ns	$C_{INT,load}$ = 50 pF	P_8.5.63
Interrupt output fall time [2]	$t_{INT, fall}$	–	–	25	ns	$C_{INT,load}$ = 50 pF	P_8.5.64

1) Due to internal delays the reset delay time can be enlarged by max 50µs. Please consider the transition time into INIT state $t_{r,INIT}$ specified in **Table 11-8** prior to the power sequencing started by entering INIT state.

2) Specified by design, not subject to production test

9 Standby LDO and Internal Supplies

9.1 Standby LDO:

9.1.1 Functional description

The standby regulator LDO_STBY is independent from the pre regulator stage and the other post regulators. It might be switched ON or OFF in all states (for details please refer to chapter **State Machine**). The linear low drop regulator LDO_STBY offers a precise 3.3 V (or 5.0 V, equal to LDO_µC) output voltage for standby supply.

The LDO_STBY will keep its state by leaving the STANDBY state according to its previous configuration. For STANDBY state, the status of LDO_STBY (ON or OFF) has to be defined in previous states.

The regulator is supplied from pin VST. Depending on the needs of the application pin VST might be connected directly to battery voltage (protected by reverse polarity diode) or to the output of the step up pre regulator (pin VSx). The output voltage V_{QST} (at pin QST) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop is depending on the load current, the characteristics of the output capacitor and the chip temperature. To ensure stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in table “Electrical characteristics”.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current should occur, it will be limited., thus the output voltage will decrease. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring. In case of over voltage at pin QST, the LDO_STBY will be switched off and the device will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin QST, the device will move into INIT state, pin ROT will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage should be present for more than t_{StG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).
- There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at LDO_µC and step down pre regulator. In case of the chip temperature will exceed the pre warning threshold, an interrupt will indicate this event and it will be stored in an SPI status register (**OTFAIL**). If the chip temperature will exceed the temperature shutdown threshold, the post regulator will be switched off. The temperature switch off time will be at least one second. An overload at LDO STBY (over current detected for more than 1ms) will be indicated by interrupt, except if the device is in STANDBYstate and the event will be stored in SPI status register (**OTWRNSF**).

The regulator LDO_STBY may be configured to be ON or OFF in every state, except FAILSAFE. The selection for STANDBY state shall be done by SPI command before entering this state.

For further details please refer to **Chapter 11 State Machine**.

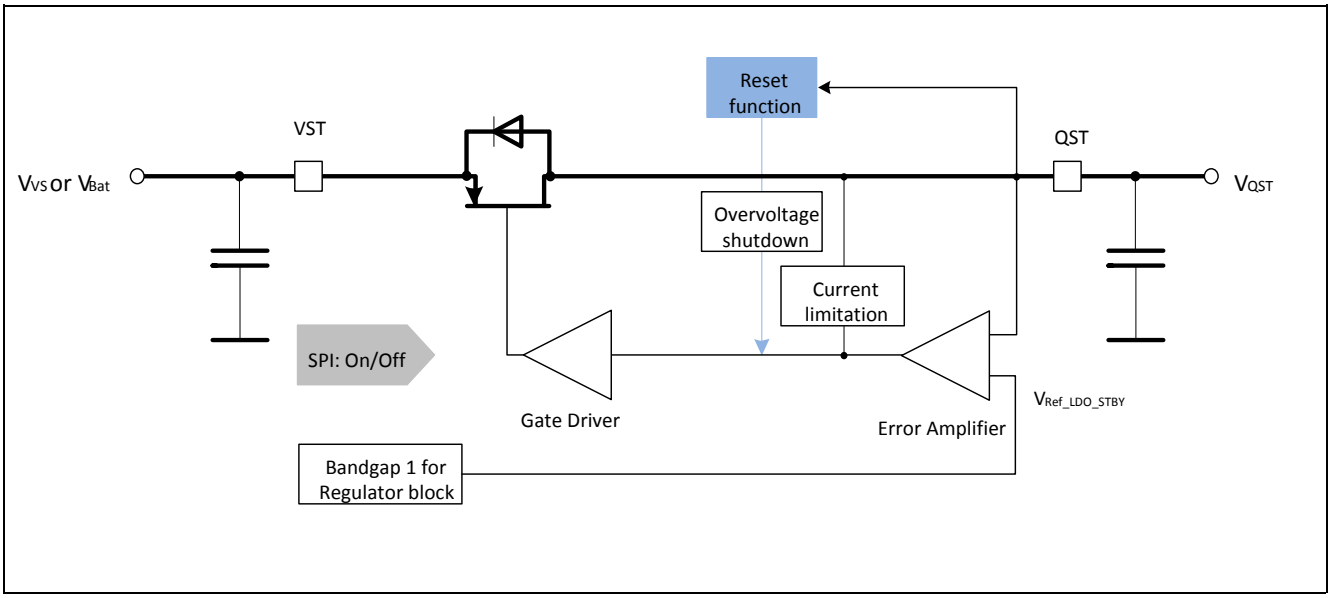


Figure 23 Low drop linear regulator for standby supply

9.1.2 Electrical characteristics

Table 16 Electrical characteristics: Standby LDO

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Standby LDO							
Output voltage TLF35584xxVS1	V_{QST}	4.8	5.0	5.2	V	0 mA ≤ I_{QST}≤ 10 mA	P_9.1.1
Output voltage TLF35584xxVS2	V_{QST}	3.17	3.3	3.43	V	0 mA < I_{QST}< 10 mA	P_9.1.2
Output current limitation	$I_{QST, max}$	15	–	40	mA	–	P_9.1.3
Drop voltage	$V_{dr, QST}$	–	–	400	mV	–	P_9.1.4
Load regulation TLF35584xxVS1	$\Delta V_{QST, load}$	–	25	40	mV	I_{QST} = 100 µA to 10 mA	P_9.1.5
Load regulation TLF35584xxVS2	$\Delta V_{QST, load}$	–	20	40	mV	I_{QST} = 100 µA to 10 mA	P_9.1.6

Line regulation TLF35584xxVS1	$\Delta V_{QST,\ line}$	–	0.1	0.5	mV/V	–	P_9.1.7
Line regulation TLF35584xxVS2	$\Delta V_{QST,\ line}$	–	0.1	0.5	mV/V	–	P_9.1.8

Table 16 Electrical characteristics: Standby LDO (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power supply ripple rejection	$PSRR_{QST}$	40	–	–	dB	f_{ripple} = 100 kHz 1) ESRC_{QST} ≤ 100mΩ	P_9.1.9
Output capacitor	C_{QST}	0.47	–	10	µF	1)	P_9.1.10
Output capacitor, ESR	$ESR\ C_{QST}$	0	–	200	mΩ	1)	P_9.1.11

1) Specified by design, not subject to production test

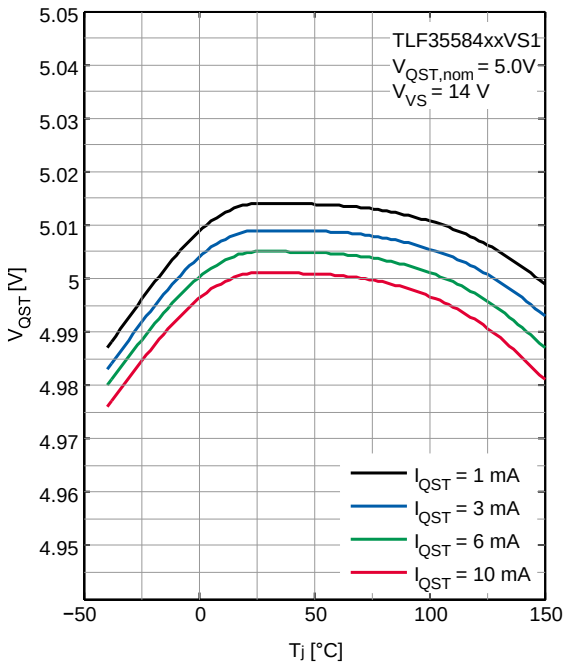
9.1.3 Typical Performance Characteristics

QST Output Voltage V_{QST} versus Junction Temperature T_j (TLF35584xxVS1)

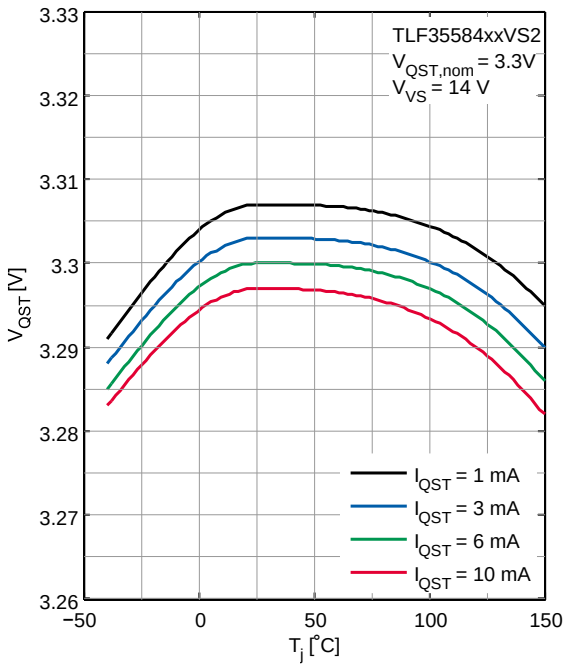
QST Output Voltage V_{QST} versus

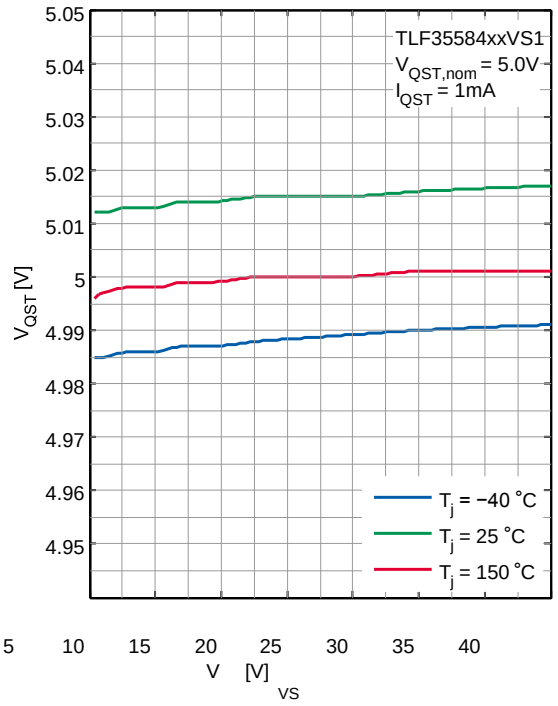
Junction Temperature T_j (TLF35584xxVS2)

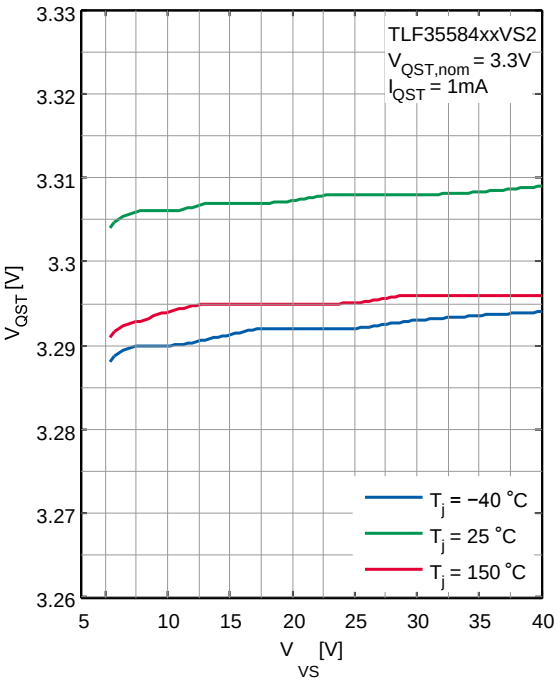
QST Output Voltage V_{QST} versus Supply Voltage V_{VS} (TLF35584xxVS1)



QST Output Voltage V_{QST} versus Supply Voltage V_{VS} (TLF35584xxVS2)

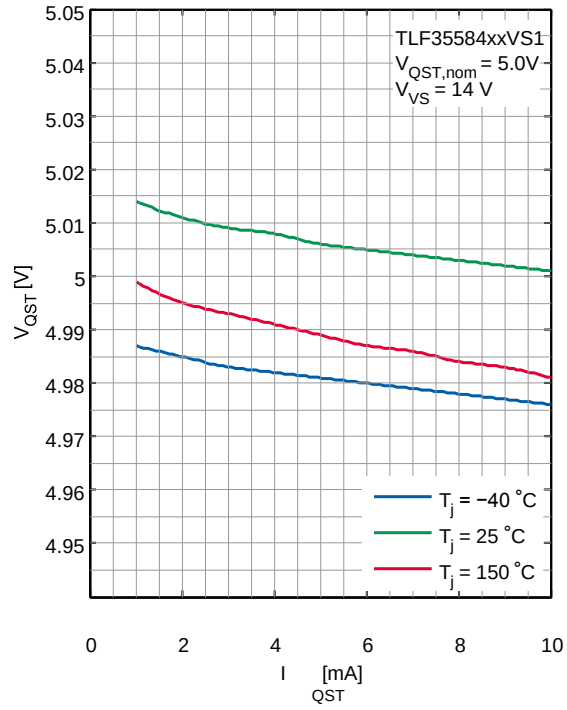


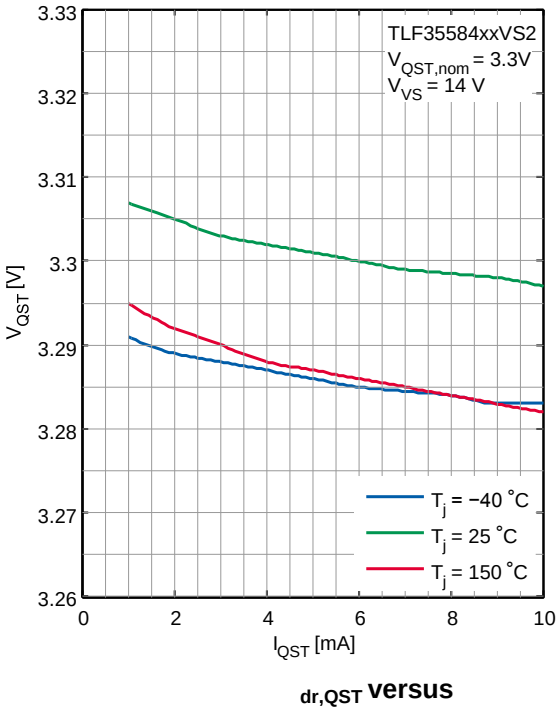




QST Output Voltage V_{QST} versus Load Current I_{QST} (TLF35584xxVS1)

QST Output Voltage V_{QST} versus Load Current I_{QST} (TLF35584xxVS2)



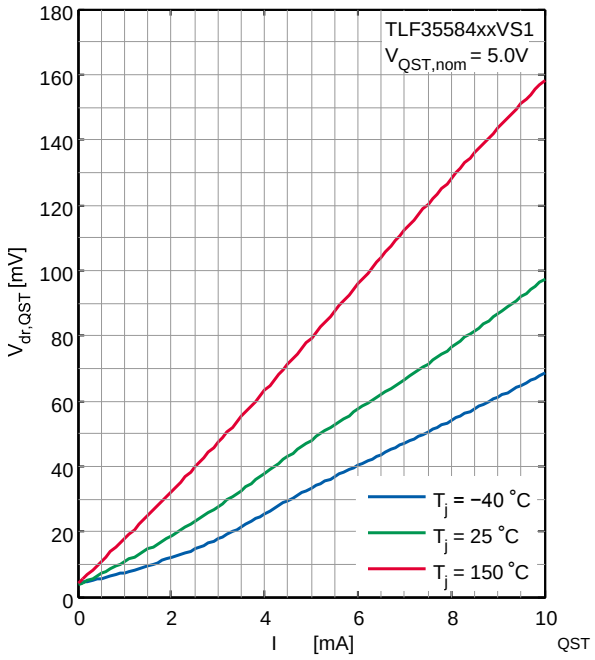


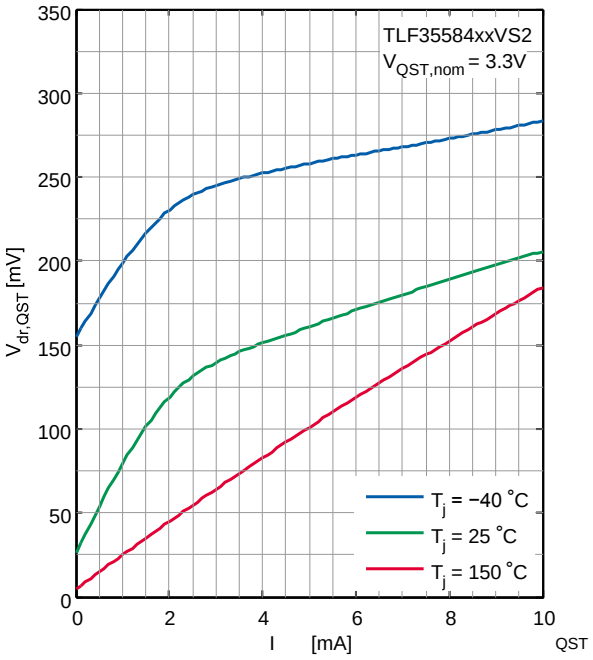
QST Dropout Voltage $V_{dr,QST}$ versus Load Current I_{QST} (TLF35584xxVS1)

QST Dropout Voltage $V_{dr,QST}$ versus

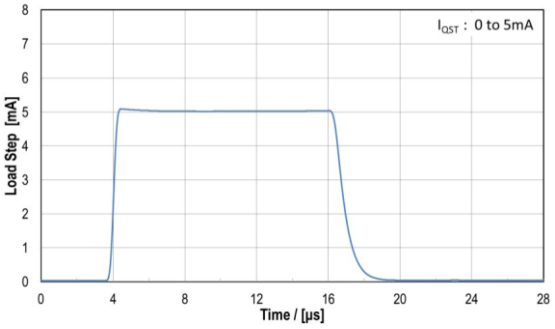
Load Current I_{QST} (TLF35584xxVS2) QST Dynamic Load Response (0mA to 5mA)

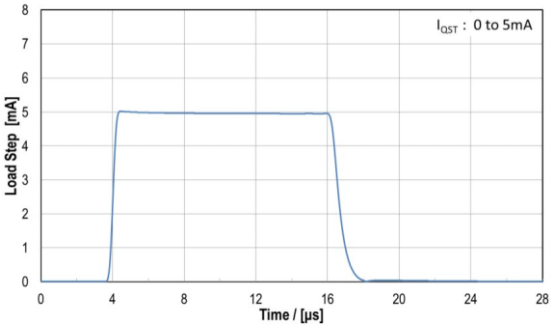
TLF35584xxVS1 ($V_{QST,nom}$ = 5.0 V) QST Dynamic Load Response (0mA to 5mA)

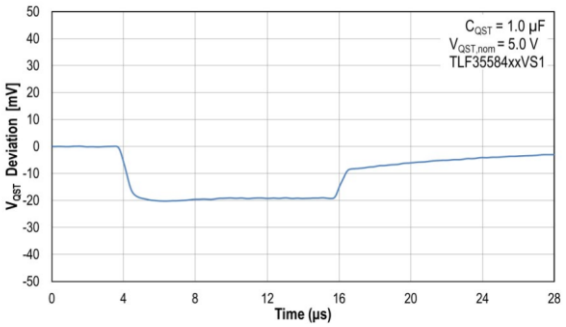


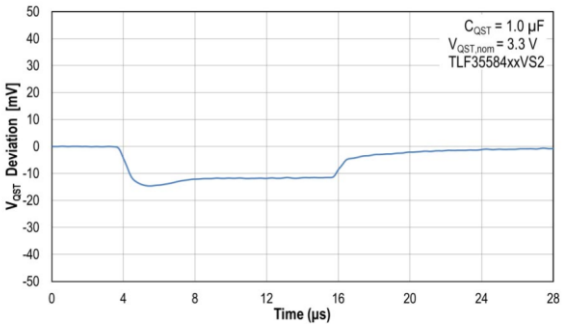


TLF35584xxVS2 ($V_{QST,nom}$ = 3.3 V)









9.2 Internal Supplies

The TLF35584 includes internal voltage supplies and bias currents to operate all regulators, monitoring and logic functions. These internal supplies are monitored internally to ensure proper functionality of the functional blocks the TLF35584 provides. The device will react on internal failure conditions as described in the **State Machine**, **Monitoring Function**, **Interrupt Generation** and **Safe State Control Function**.

The internal regulators do not require external components (i.e capacitors). The internal voltages are not visible at any pin.

10 Wake Up Timer

10.1 Description

The wake up timer is a function to wake up the TLF35584.

The wake up timer value may be set by SPI in INIT, NORMAL and WAKE state. The value is stored in the 24 bit wide wake up timer register (**WKTIMCFG0**, **WKTIMCFG1**, **WKTIMCFG2**).

The wake up timer is implemented as a 24 bit counter which is clocked by a 100 kHz or 100 Hz clock (time-base). The time-base may be selected via SPI.

For the chosen time-base of 100 kHz the timer resolution is 10 µs and a wake up time between 10 µs to 168 s can be configured via SPI.[1)]

For the chosen time-base of 100 Hz the timer resolution is 10 ms and a wake up time between 10 ms to 1.9 days can be configured via SPI.

When entering STANDBY or SLEEP state, the counter is loaded with the value of the wake up timer register and starts decrementing. At underflow, the timer will wake up the device from either SLEEP or STANDBY state. When leaving SLEEP state, an interrupt will be generated.

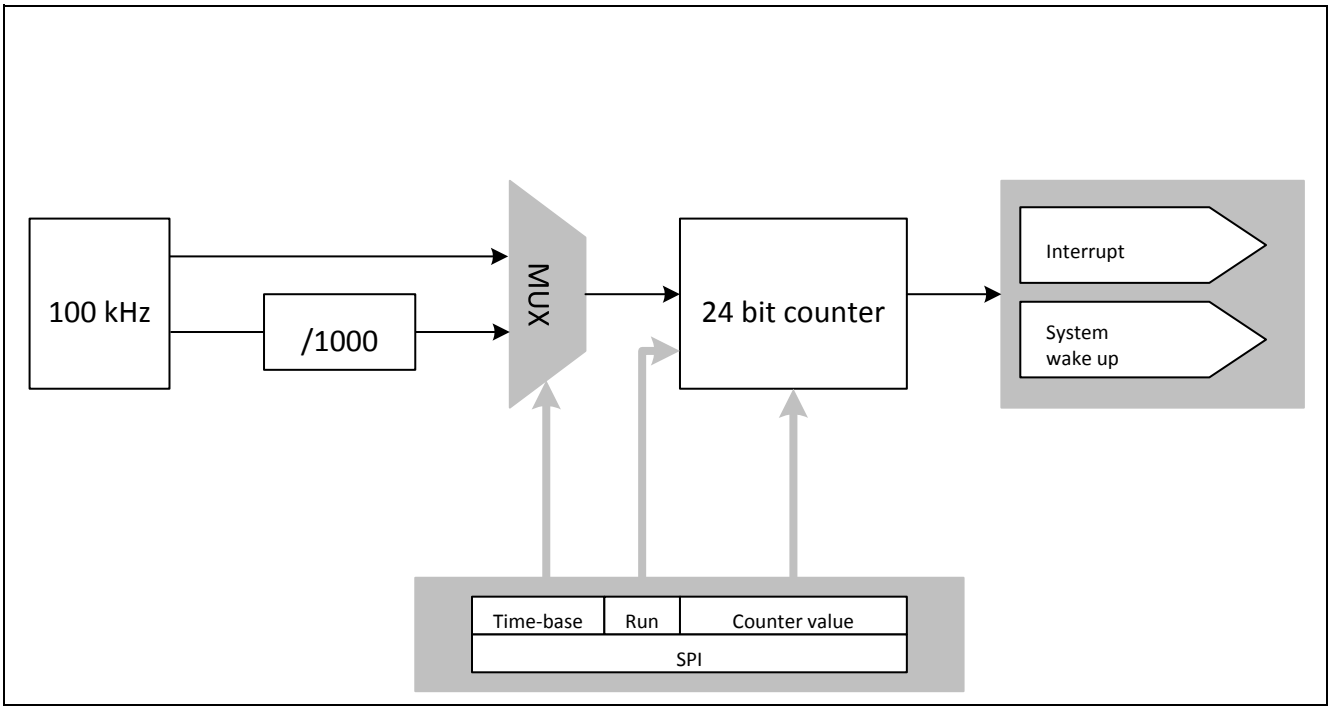


Figure 24 Wake up timer principle

[1)] An additional activation delay time for the start of the wake up timer of max. 40 µs has to be considered after entering SLEEP or STANDBY state.

10.2 Electrical Characteristics

Table 17 Electrical Characteristics: Wake up timer

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Wake up timer							
Time base, resolution	$t_{WakeUpTimer}$	9.5	10	10.5	µs	1)	P_10.2.1
Time base, resolution	$t_{WakeUpTimer}$	9.5	10	10.5	ms	–	P_10.2.2
Counter	C	-	24	-	bit	2)	P_10.2.3

1) Due to internal delays the wake-up time can be enlarged by max 50µs.

2) Specified by design, not subject to production test

11 State Machine

11.1 Introduction

The state machine describes the different states of operation, the device may get into. The following figure shows the state machine flow diagram, for detailed information please refer to following pages.

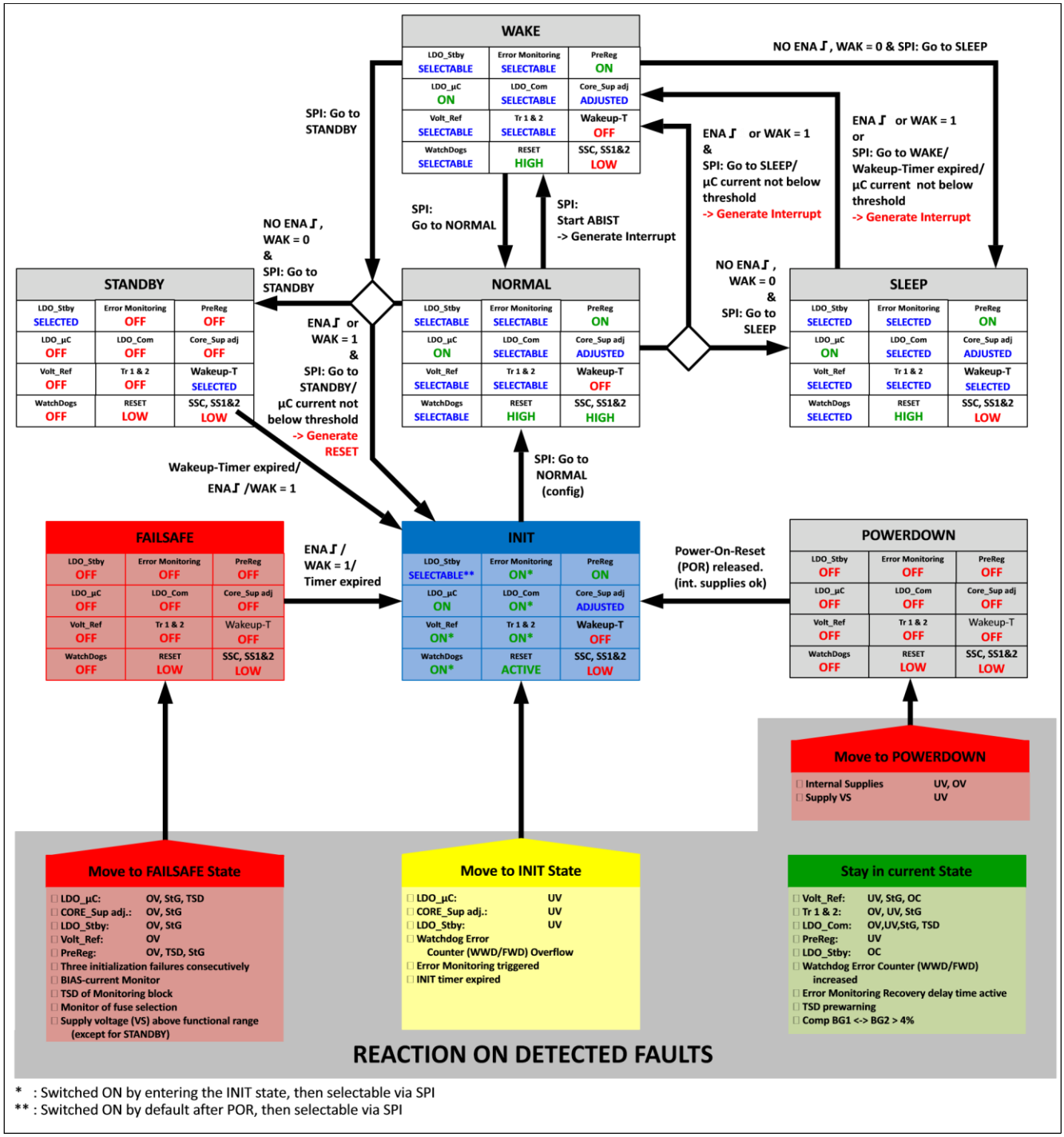


Figure 25 Flow Diagram State Machine

Description:

- ON /OFF:= Switched ON or OFF, not configurable by SPI command
- ON*:= Switched ON by entering the INIT state, then selectable via SPI
- SELECTED:= May be configured (switched ON or OFF) by SPI command in previous state or is selected by the state transition request (DEVCTRL) in case of LDO configuration for SLEEP state.
- SELECTABLE:= May be switched ON or OFF by SPI command in this state
- SELECTABLE**:= Switched ON by default after POR, then selectable via SPI
- ADJUSTED:= Defined present or not present by configuration pin, not configurable by SPI command
- ACTIVE:= as described in INIT-State
- SSC, SS1&2:= Safe State Control signals 1 and 2
- LOW:= Signal is low
- HIGH:= Signal is high
- OV:= Over voltage
- UV:= Under voltage
- StG:= Short to ground
- TSD:= Thermal shut down
- OC:= Over current
- ABIST:= Analog built in self test
- Comp BG1 <-> BG2 > 4%: The difference between both band gaps 1 and 2 is more than 4%

11.2 Description of States

11.2.1 POWERDOWN-state

The device is in POWERDOWN-state as long the Power-on-Reset (POR) is not released.

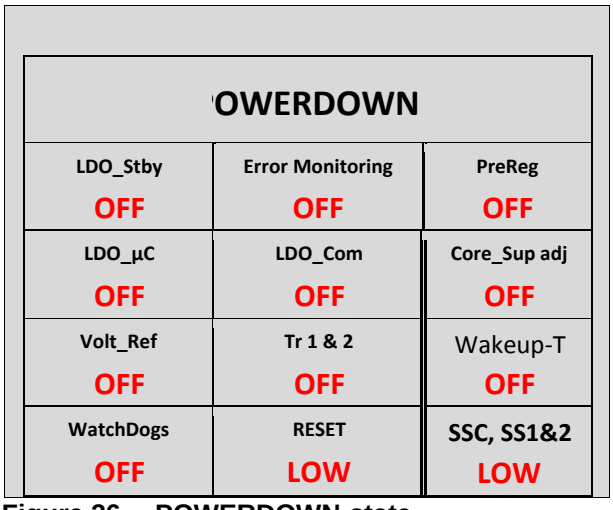


Figure 26 POWERDOWN-state

Table 11-1 POWERDOWN-state Settings

Part/Function	Value	Description

LDO_Stby	OFF	• The LDO_Stby is off
PreReg	OFF	• The pre regulators are off
LDO_µC	OFF	• The LDO_µC is off
LDO_Com	OFF	• The LDO_Com is off
Core_Sup adj.	OFF	• The function Core_Sup adj. is off
Volt_Ref	OFF	• The voltage reference is off
Tr.1 & 2	OFF	• Both trackers 1 & 2 are off
Wake-up-T.	OFF	• The wake-up timer is off
Watchdogs	OFF	• The watchdogs are off
Error monitoring	OFF	• The Error monitoring is off
RESET	LOW	• The reset output is low
SSC, SS1&2	LOW	• Both safe state signals are LOW and the application is in safe state

11.2.2 INIT-state

During INIT-state the device expects valid communication with the µC within the INIT timer. Otherwise an initialization timeout will occur. The INIT timer starts with the rising edge of ROT. The INIT timer is stopped as soon as three boundary conditions are fulfilled:

- Valid SPI communication received from µC
- Watchdog(s) serviced once according to default configuration or according to reconfiguration
- ERR monitoring serviced properly (minimum 3 periods provided) or configured to be OFF

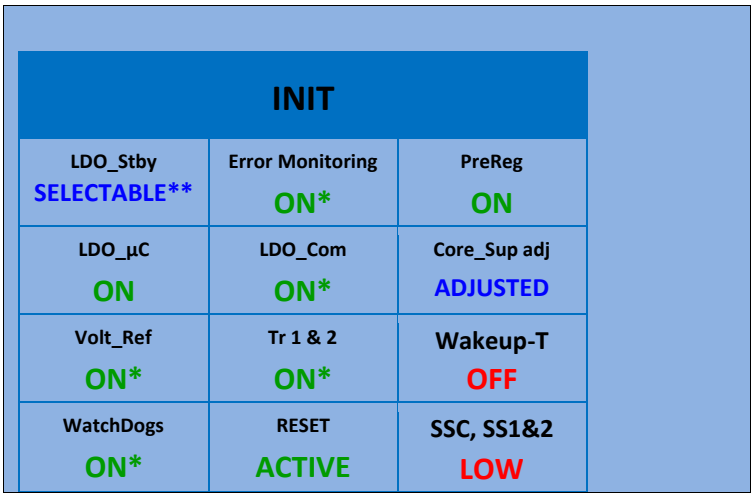


Figure 27 INIT-state

Part/Function	Value	Description
LDO_Stby	SELECTABLE**	• The LDO_Stby is switched on when entering from POWERDOWN-state • It may be switched on or off by SPI command. This configuration is kept through all states, except POWERDOWN-state
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU.

LDO_µC	ON	• The LDO_µC is on
LDO_Com	ON*	• The LDO_Com is switched on per default • The LDO_Com may be switched off and on by SPI
Core_Sup adj.	ADJUSTED	• The Core_Sup adj. is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
Volt_Ref	ON*	• The Volt_Ref is switched on per default • The Volt_Ref may be switched off and on by SPI
Tr.1 & 2	ON*	• Both trackers 1 & 2 are switched on per default • Both trackers 1 & 2 may be switched off and on by SPI independently
Wake-up-T.	OFF	• The wake-up timer is off
Watchdogs	ON*	• The window watchdog is switched on per default in SPI triggered mode • The functional watchdog is switched off per default • The watchdogs may be configured and switched ON or OFF by SPI
Error monitoring	ON	• The Error monitoring is switched on per default • The Error monitoring may be configured and switched ON or OFF by SPI

Table 11-2 INIT-state Settings

Table 11-2 INIT-state Settings (cont'd)

Part/Function	Value	Description
RESET	ACTIVE	• The reset output goes HIGH as soon as all µC related output voltages V_{QST}, V_{QUC} and V_{VCI} are above their under voltage reset threshold,$V_{RT,XXX,low}$ delayed by the reset delay time t_{RD}.
SSC, SS1&2	LOW	• Both safe state signals are LOW and the application is in safe state

11.2.3 NORMAL -state

In NORMAL-state the device is supplying the µC and the applications. Safety and monitoring functions (like resetblock and safe state control) are active. The µC may configure several post regulators of the device and the wakeup-timer via SPI command for this state.

NORMAL		
LDO_Stby SELECTABLE	Error Monitoring SELECTABLE	PreReg ON
LDO_µC ON	LDO_Com SELECTABLE	Core_Sup adj ADJUSTED
Volt_Ref SELECTABLE	Tr 1 & 2 SELECTABLE	Wakeup-T OFF
WatchDogs SELECTABLE	RESET HIGH	SSC, SS1&2 HIGH

Figure 28 NORMAL-state

Table 11-3 NORMAL-state Settings

Part/Function	Value	Description
LDO_Stby	SELECTABLE	• The LDO_Stby may be switched on or off by SPI command.
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU.
LDO_µC	ON	• The LDO_µC is on
LDO_Com	SELECTABLE	• The LDO_Com may be switched on of off by SPI command
Core_Sup adj.	ADJUSTED	• The Core_Sup adj. is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
Volt_Ref	SELECTABLE	• The Volt_Ref may be switched on of off by SPI command
Tr.1 & 2	SELECTABLE	• Both trackers 1 & 2 may be switched off and on by SPI independently
Wake-up-T.	OFF	• The wake-up timer is switched off
Watchdogs	SELECTABLE	• The watchdogs may be configured and switched ON or OFF by SPI
Error monitoring	SELECTABLE	• The Error monitoring may be configured and switched ON or OFF by SPI
RESET	HIGH	• The reset output is HIGH
SSC, SS1&2	HIGH	• Both safe state signals are HIGH

11.2.4 STANDBY-state

The STANDBY-state is a low power state which the µC may enter to reduce the current consumption to a minimum when the application is not used for a long time. The application is in a safe state.

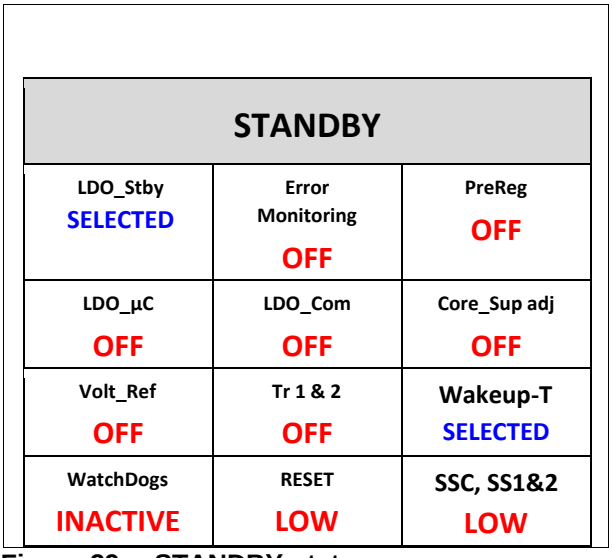


Figure 29 STANDBY-state

Table 11-4 STANDBY-state Settings

Part/Function	Value	Description
LDO_Stby	SELECTED	• The LDO_Stby is ON or OFF depending on its configuration
PreReg	OFF	• The pre regulator are off
LDO_µC	OFF	• The LDO_µC is off
LDO_Com	OFF	• The LDO_Com is off
Core_Sup adj.	OFF	• The function Core_Sup adj. is off
Volt_Ref	OFF	• The voltage reference is off
Tr.1 & 2	OFF	• Both trackers 1 & 2 are off
Wake-up-T.	SELECTED	• The wake-up timer is ON or OFF depending on its configuration
Watchdogs	OFF	• The watchdogs are off
Error monitoring	OFF	• The Error monitoring is off
RESET	LOW	• The reset output is low
SSC, SS1&2	LOW	• Safe state signals 1 and 2 are low • The application is in a safe state

11.2.5 SLEEP-state

The SLEEP-state is a low power state which the µC may enter to reduce the current consumption when the application is not used (e.g. micro controller is in STOP mode). The µC may configure the status of regulators and the safety functions via SPI command in the previous state. The application is in a safe state

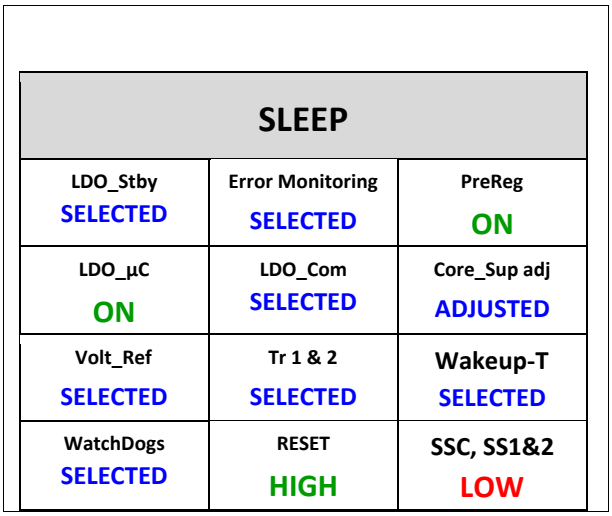


Figure 30 SLEEP-state

Table 11-5 SLEEP-state Settings

Part/Function	Value	Description
LDO_Stby	SELECTED	• The LDO_Stby is switched ON or OFF according to previous configuration.
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU
LDO_µC	ON	• The LDO_µC is switched on • In SLEEP-state the device is monitoring the output current of LDO_µC: If the LDO_µC current exceeds a certain threshold $I_{LDO\_\mu C,att}$, an interrupt will be generated and the device will move to WAKE state

LDO_Com	SELECTED	• The LDO_Com is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
Core_Sup adj.	ADJUSTED	• The Core_Sup adj. is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
Volt_Ref	SELECTED	• The Volt_Ref is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
Tr.1 & 2	SELECTED	• The trackers are switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP-state
Wake-up-T.	SELECTED	• The wake-up timer is ON or OFF depending on its configuration
Watchdogs	SELECTED	• The watchdogs are ON or OFF depending on their configuration for SLEEP
Error monitoring	SELECTED	• The Error monitoring is ON or OFF depending on its configuration for SLEEP
RESET	HIGH	• The reset output is HIGH
SSC, SS1&2	LOW	• Both safe state signals are LOW and the application is in safe state

11.2.6 WAKE-state

The WAKE-state is an intermediate state between NORMAL and the low power states SLEEP and STANDBY. This state provides the same functionality as the NORMAL state, but shall ensure the application being in safe state by keeping low the safe state outputs. It should be used to prepare the system for a correct and safe reentry to the NORMAL state by servicing the watchdogs and the error monitoring (minimum 3 periods) according to the selected configuration. Furthermore it provides the possibility to move the device into the low power states SLEEP and STANDBY.

The TLF35584 moves from SLEEP or from the transition to SLEEP into WAKE state, if the output current from LDO_µC exceeds a certain threshold $I_{LDO\_\mu C,att}$, an valid ENA or WAK signal is recognized or the SPI command GoToWake is sent. Another transition into WAKE state is initiated by the usage of the ABIST in NORMAL state.

By entering the state an interrupt is generated and the supervision functions (watchdogs and ERR monitoring) will become active according to their previous configuration in NORMAL state. Upon entering the WAKE-state the configuration of the LDOs resumes to the one of the previous NORMAL state. The application is in a safe state

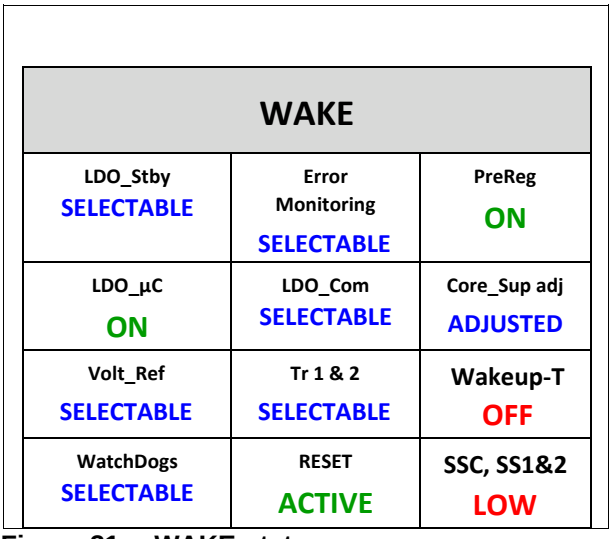


Figure 31 WAKE-state

Table 11-6 WAKE-state Settings

Part/Function	Value	Description
LDO_Stby	SELECTABLE	• The LDO_Stby may be switched ON or OFF by SPI command.
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU.
LDO_µC	ON	• The LDO_µC is on
LDO_Com	SELECTABLE	• The LDO_Com will be switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
Core_Sup adj.	ADJUSTED	• The Core_Sup adj. is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
Volt_Ref	SELECTABLE	• The voltage reference will be switched ON or OFF depending on its configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command

Table 11-6 WAKE-state Settings (cont'd)

Part/Function	Value	Description
Tr.1 & 2	SELECTABLE	• Both trackers 1 & 2 will be switched ON or OFF depending on their configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
Wake-up-T.	OFF	• The wake-up timer is switched off
Watchdogs	SELECTABLE	• The watchdogs will be switched ON or OFF depending on their configuration in NORMAL-State prior to SLEEP-state when entering WAKE-State • The watchdogs may be configured and switched ON or OFF by SPI
Error monitoring	SELECTABLE	• The Error monitoring will be switched ON or OFF depending on the configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • The Error monitoring may be configured and switched ON or OFF by SPI
RESET	HIGH	• The reset output is HIGH
SSC, SS1&2	LOW	• Both safe state signals are LOW and the application is in safe state

11.2.7 FAILSAFE-state

FAILSAFE-state occurs after the detection of a severe failure. In FAILSAFE-state all regulators are switched off. The application is in a safe state.

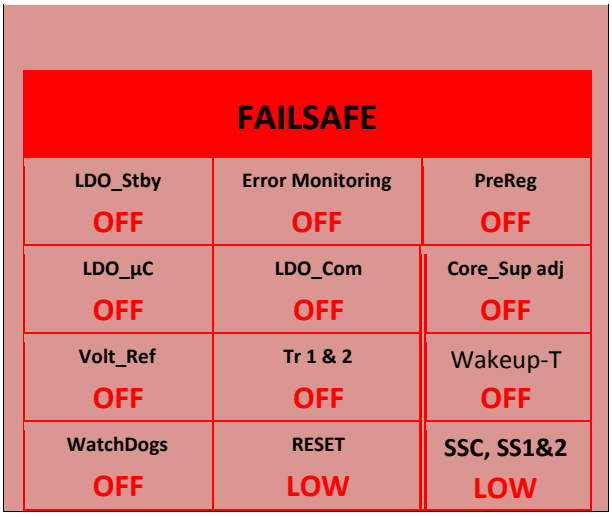


Figure 32 Fail safe-state

Table 11-7 FAILSAFE-state Settings

Part/Function	Value	Description
LDO_Stby	OFF	• The LDO_Stby is off
PreReg	OFF	• The pre regulators are off
LDO_µC	OFF	• The LDO_µC is off
LDO_Com	OFF	• The LDO_Com is off
Core_Sup adj.	OFF	• The function Core_Sup adj. is off
Volt_Ref	OFF	• The voltage reference is off
Tr.1 & 2	OFF	• Both trackers 1 & 2 are off
Wake-up-T.	OFF	• The wake-up timer is off
Watchdogs	OFF	• The watchdogs are off
Error monitoring	OFF	• The Error monitoring is off
RESET	LOW	• The reset output is low
SSC, SS1&2	LOW	• Both safe state signals are LOW and the application is in safe state

11.3 Transition Between States

State transitions requested via SPI command are initiated with a valid positive going edge of the chip select (SCS).

11.3.1 POWERDOWN -> INIT-state

The device moves from POWERDOWN to INIT-state when the Power-on-Reset (POR) is released. The POR is only released when all of the following conditions are met:

- V_{VS} above $V_{PD,hi}$ when increasing
- no under or over voltage on internal supplies

11.3.2 INIT -> NORMAL-state

Prerequisites:

- Watchdog(s) need to be serviced once according to default configuration or according to reconfiguration within the INIT timer
- ERR monitor needs to be serviced with a valid signal (minimum 3 periods) or disabled within the INIT timer.
- If functional watchdog is activated, a valid FWD triggering needs to be provided.
- A delay of 60µs after the provided services has to be considered to ensure proper release of internal validation signals.

Triggering Events:

- State transition is only initiated by the SPI command “Go to NORMAL”.

Exceptions:

- none

Timing Description:

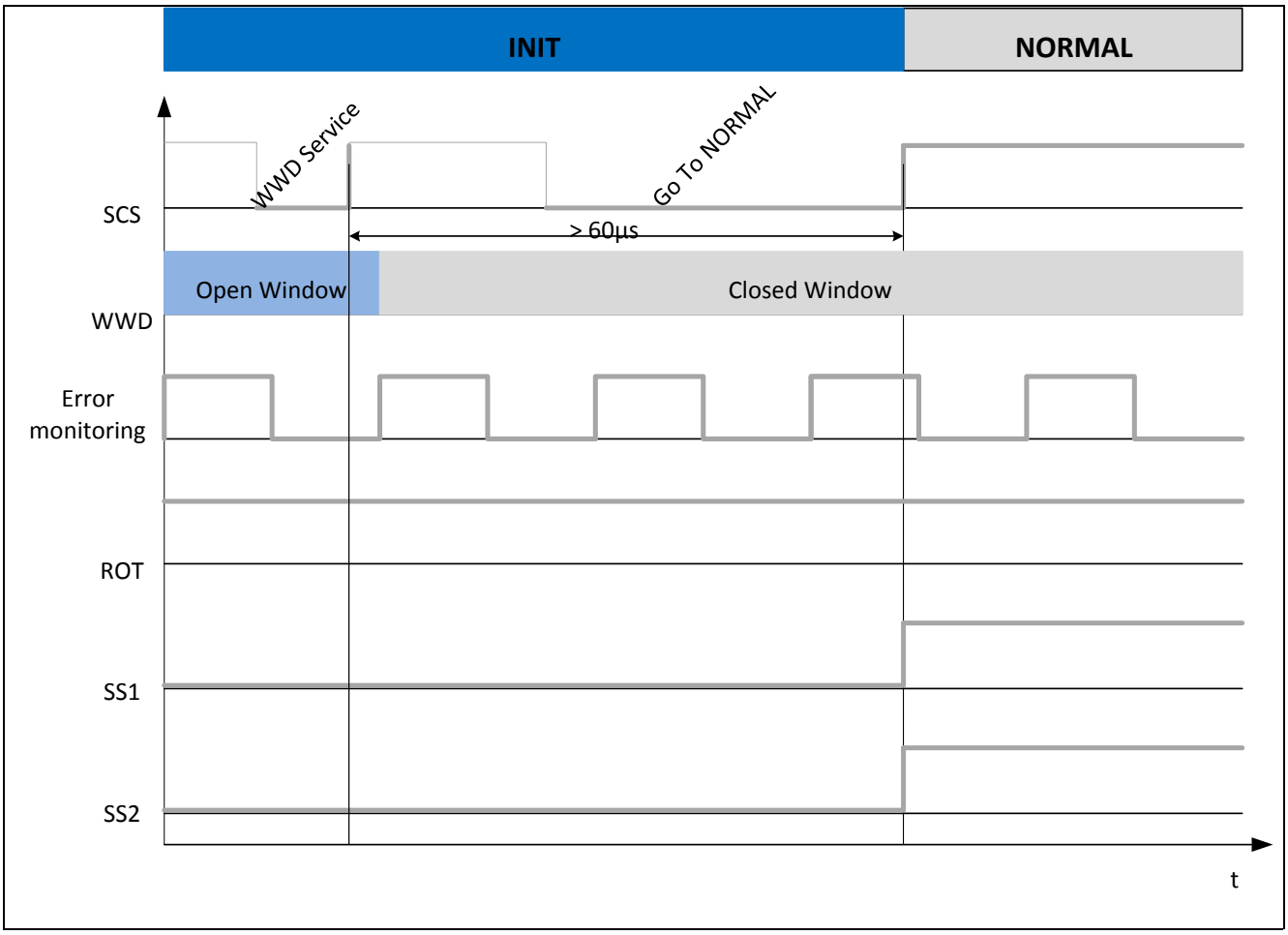


Figure 33 Transition from INIT to NORMAL state

- A valid SPI command “Go to NORMAL” (valid with chip select high at pin SCS) will move the device from INIT state to NORMAL state.
- Reset pin ROT stays HIGH as the post regulators are already active in INIT state.
- With the positive edge of chip select high (at pin SCS) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs according to **Table 18** has to be considered)

11.3.3 Movements between NORMAL and SLEEP state

11.3.3.1 NORMAL -> SLEEP-state

Prerequisites:

- Selection of LDO_µC current monitor or absolute transition timer.
- Transition delay timer $t_{tr,del}$ needs to be configured or default is used.
- Optionally LDO_µC current threshold needs to be defined or default is used.

Triggering Events:

- State transition is only initiated by the SPI command “Go to SLEEP”.

Exceptions:

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to SLEEP state, the device will move to the WAKE state and send an interrupt (at pin INT)
- If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected LDO_µC current threshold before the transition delay timer $t_{tr,del}$ has expired, the device will move to the WAKE state and send an interrupt (at pin INT)

Timing Diagram

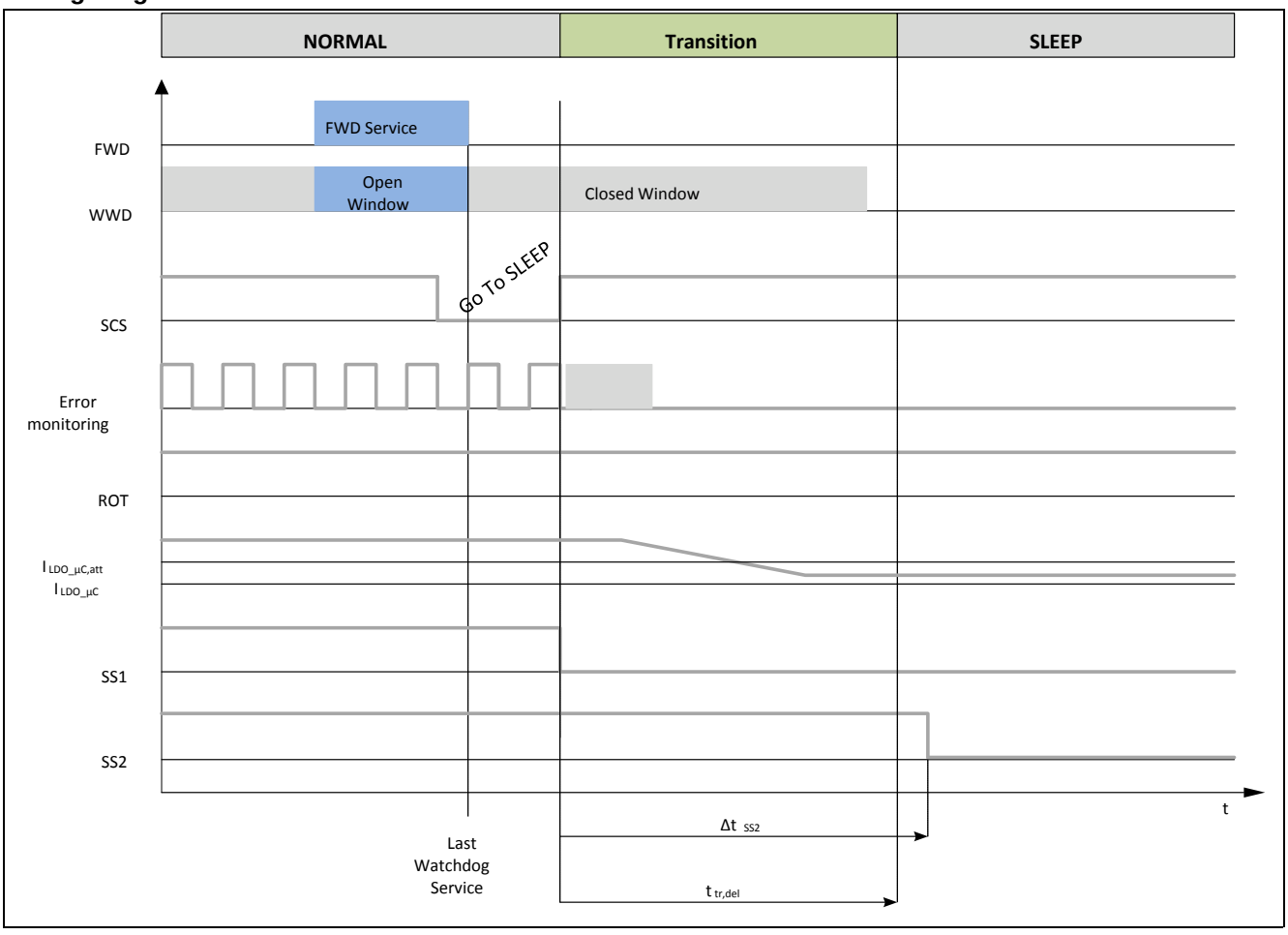


Figure 34 Transition from NORMAL to SLEEP state

- Before the SPI command “Go to SLEEP” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to SLEEP”
- The positive edge of chip select (pin SCS) after the SPI command “Go to SLEEP” initiates the transition. With chip select high the safe state signal SS1 is pulled to zero and the device leaves NORMAL state and enters the transition state (to SLEEP state). (Internal reaction time for the safe state outputs according to **Table 18** has to be considered)

- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS. If the error monitoring should be selected to be active in SLEEP state continuos toggling is mandatory.
- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS. If one or both watchdogs should be selected to be active in SLEEP state continuos watchdog service is mandatory.
- Reset pin ROT stays HIGH as the post regulators are not switched off.
- In case the absolute transition timer is selected, the device moves from transition state to SLEEP state after the transition delay time $t_{tr,del}$. The transition time $t_{tr,del}$ can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs. After this transition time it should be ensured that the µC current consumption has fallen below the LDO_µC monitoring threshold $I_{LDO\_\mu C,att}$ to keep the device in SLEEP state.
- If the LDO_µC current monitor is enabled the µC current out of pin QUC must fall below the LDO_µC monitoring threshold $I_{LDO\_\mu C,att}$ within the configured maximum transition time $t_{tr,del}$ in **DEVCFG0.TRDEL**. The time for the transition is depending, how long it takes that the µC current falls below the LDO_µC monitoring threshold $I_{LDO\_\mu C,att}$, if it is below the transition is done.
- After delay time Δt_{SS2} the safe state signal SS2 goes to zero. The adjusted delay time Δt_{SS2} is independent from the transition delay time $t_{tr,del}$.

11.3.3.2 SLEEP -> WAKE-state

Prerequisites:

- none

Triggering Events:

- SPI command “Go to WAKE”.
- Valid Wake-Signal (ENA or WAK).
- Current of LDO_µC exceeding the configured threshold.
- Wake-up timer expired, if enabled

Exceptions:

- none

Timing Diagram

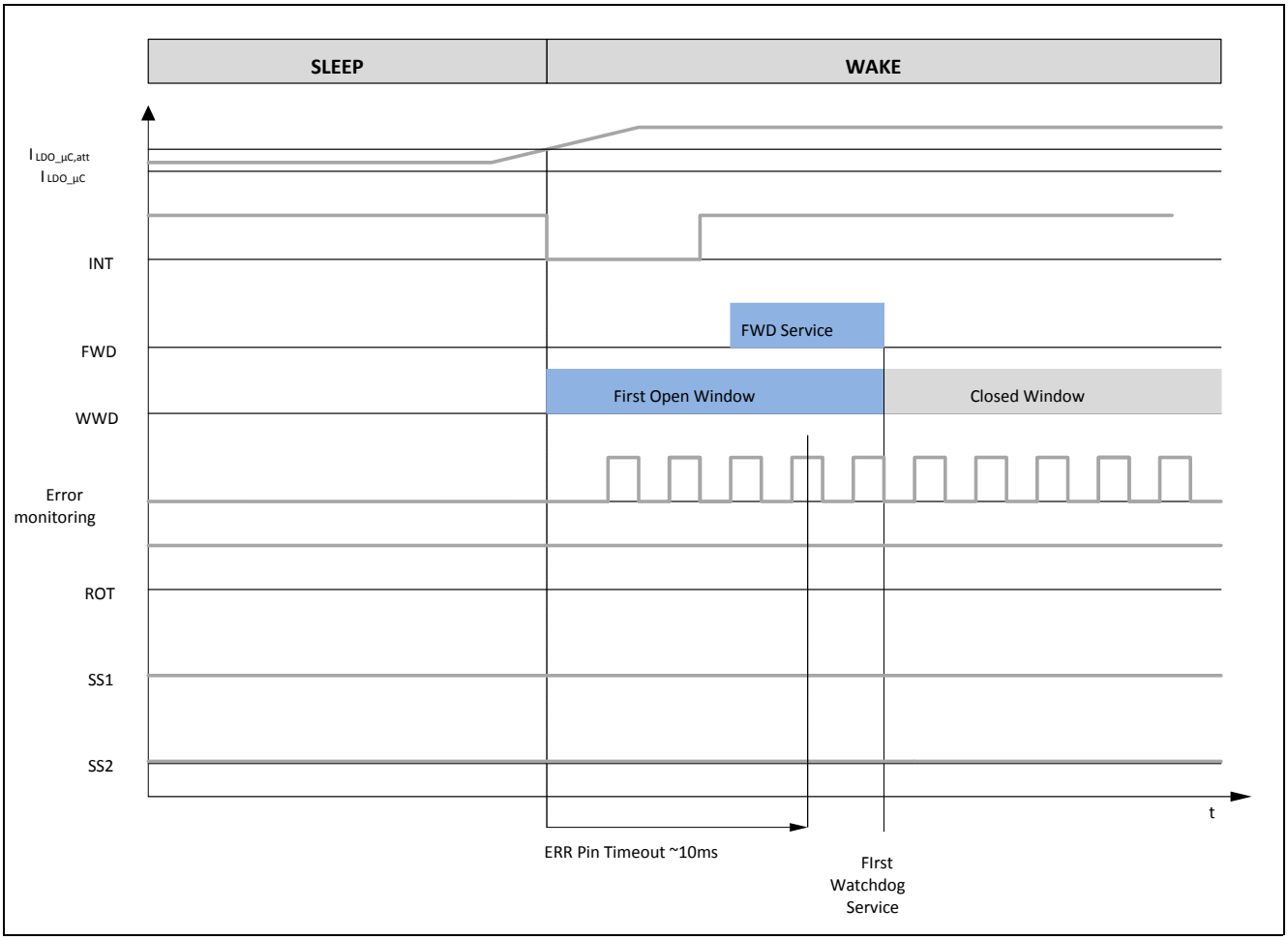


Figure 35 Transition from SLEEP to WAKE state

- The state transition is completed without a transition time and is indicated by an interrupt at pin INT. The triggering event for the transition from SLEEP can be read from the status register **WKSF**.
- All three monitoring functions (window watchdog, functional watchdog and error monitoring) will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
- The configuration of the LDOs will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
- In case the window watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INT) the window watchdog will open the first Open Window, the time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60 ms (**WDCYC** = 0) (if the window watchdog has not been active in SLEEP state) and requires service. If the window watchdog has been active in SLEEP state continuos service is mandatory.
- In case the functional watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INT) the functional watchdog will start the heartbeat timer and require service. If the functional watchdog has been active in SLEEP state continuos service is mandatory.

- In case the ERR pin monitoring was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INT) the error monitoring will become active again. Latest 10 ms after the activation a toggling signal (with at least three periods past) at pin ERR is required. If the error monitoring has been active in SLEEP state continuos toggling is mandatory.
- Reset pin ROT stays HIGH as the post regulators are active in SLEEP state and in WAKE state.
- The safe signals SS1 and SS2 will stay LOW in SLEEP and in WAKE state.
- If all active monitoring functions (window watchdog, functional watchdog and error monitoring) are serviced properly in WAKE state, you may stay in WAKE state as long as you want.
- If all three monitoring functions (window watchdog, functional watchdog and error monitoring) are inactive (switched off) in WAKE state, you may stay in WAKE state as long as you want.

11.3.3.3 WAKE -> SLEEP state

Prerequisites:

- Selection of LDO_µC current monitor or absolute transition timer.
- Transition delay timer $t_{tr,del}$ needs to be configured or default is used.
- Optionally LDO_µC current threshold needs to be defined or default is used.

Triggering Events:

- State transition is only initiated by the SPI command “Go to SLEEP”.

Exceptions:

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to SLEEP state, the device will move back to the WAKE state and send an interrupt (at pin INT)
- If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected LDO_µC current threshold before the transition delay timer $t_{tr,del}$ has expired, the device will move back to the WAKE state and send an interrupt (at pin INT)

Timing Diagram

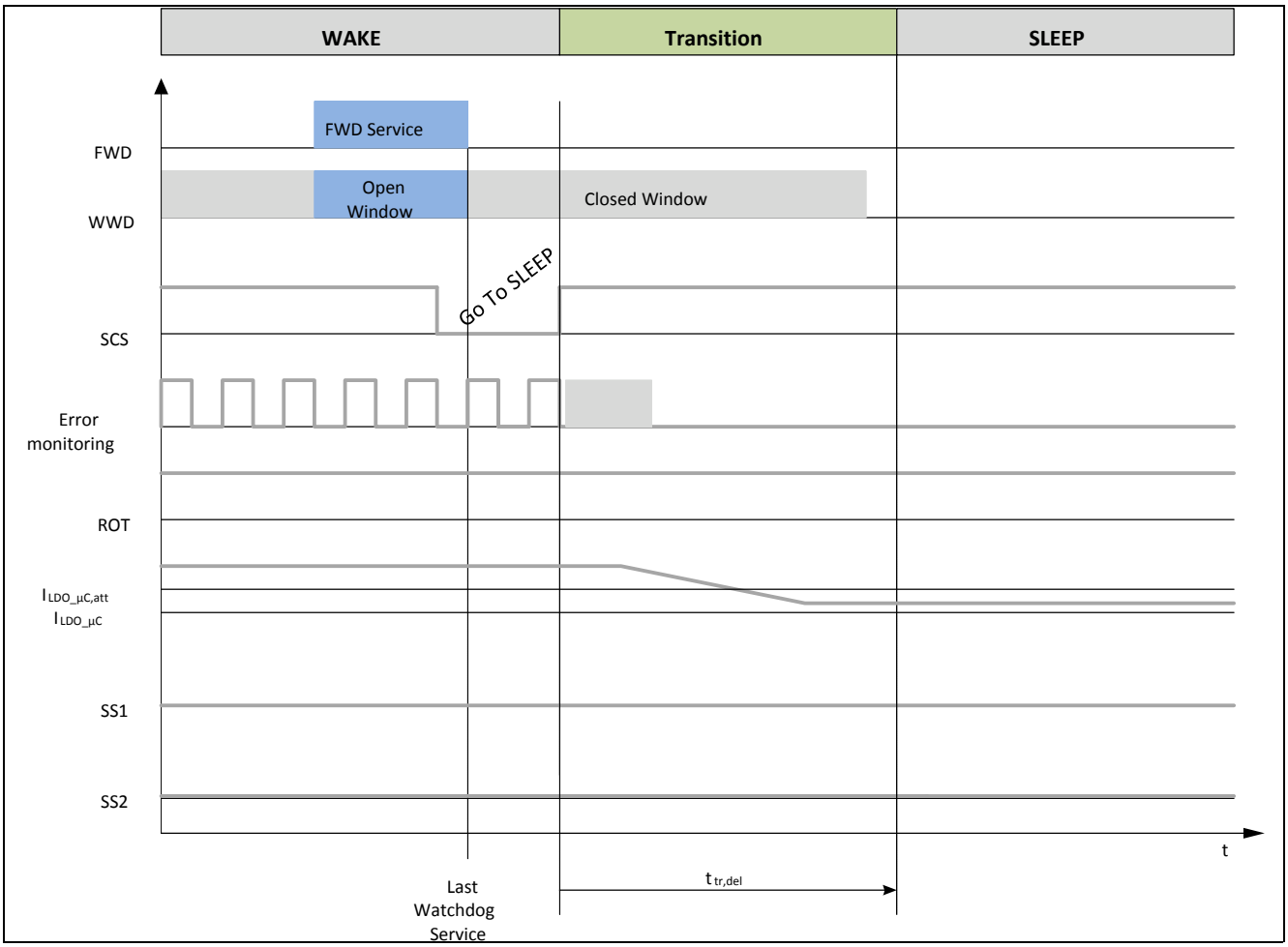


Figure 36 Transition from WAKE to SLEEP state

- Before the SPI command “Go to SLEEP” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to SLEEP”
- The positive edge of chip select (pin SCS) after the SPI command “Go to SLEEP” initiates the transition. With chip select high the device leaves WAKE state and enters the transition state (to SLEEP state).
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS. If the error monitoring should be selected to be active in SLEEP state continuos toggling is mandatory.
- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS. If one or both watchdogs should be selected to be active in SLEEP state continuos watchdog service is mandatory.
- Reset pin ROT stays HIGH as the post regulators are not switched off.
- If the LDO_µC current monitor is enabled the µC current out of pin QUC must fall below the LDO_µC monitoring threshold $I_{LDO\_\mu C,att}$ within the configured maximum transition delay time $t_{tr,del}$. The time for the transition is depending, how long it takes that the µC current falls below the LDO_µC monitoring threshold $I_{LDO\_\mu C,att}$, if it is below the transition is done.
- Safe state signals SS1 and SS2 stay LOW all the time.

11.3.4 Movements between NORMAL and STANDBY state

11.3.4.1 NORMAL -> STANDBY-state

Prerequisites:

- Selection of LDO_µC current monitor or absolute transition timer.
- Transition timer needs to be configured or default is used.
- Optionally LDO_µC current threshold needs to be defined or default is used.

Triggering Events:

- State transition is only initiated by the SPI command “Go to STANDBY”.

Exceptions:

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to STANDBY state, the device will move to the INIT state and a reset (ROT) is generated.
- If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected LDO_µC current threshold before the transition delay timer $t_{tr,del}$ has expired, the device will move to the INIT state and a reset (ROT) is generated.

Timing Diagram:

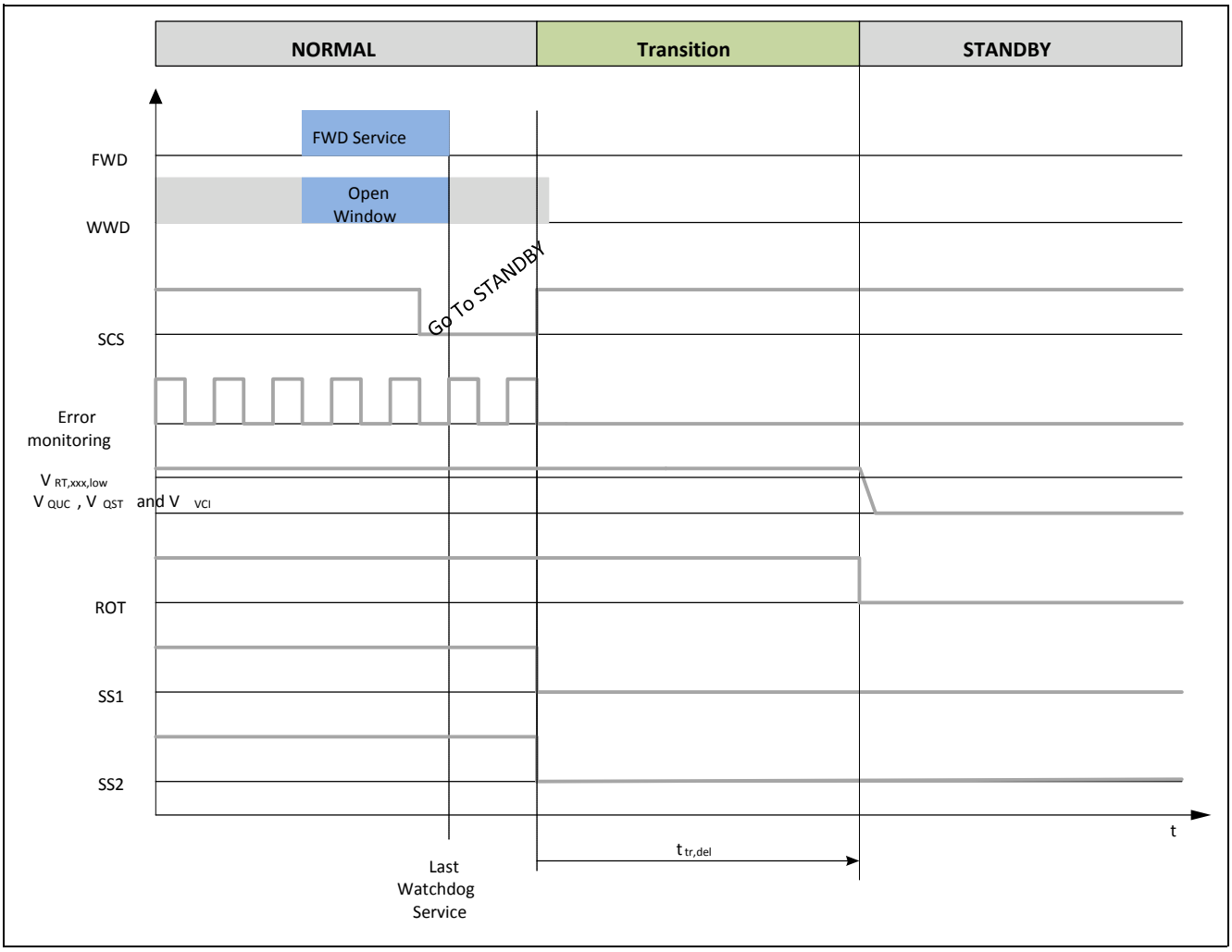


Figure 37 Transition from NORMAL to STANDBY state

- Before the SPI command “Go to STANDBY” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”
- The positive edge of chip select (pin SCS) after the SPI command “Go to STANDBY” initiates the transition. With chip select high the safe state signals SS1 and SS2 are pulled to zero without delay between SS1 and SS2. The device leaves NORMAL state and enters the transition state (to STANDBY state).
  (Internal reaction time for the safe state outputs according to **Table 18** has to be considered)
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS.
- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS.
- With a successful transition from NORMAL to STANDBY state the reset (ROT) is pulled to LOW after the transition time after chip select (pin SCS) going high.
- All pre regulators and all post regulators (with the exception of the standby LDO - it may be ON or OFF in STANDBY state) are switched off at the point when the transition is completed after the reset (ROT) is pulled low.

- In case the absolute transition timer is selected, the device moves from transition state to STANDBY state after the transition delay time $t_{tr,del}$. The transition time $t_{tr,del}$ can be determined by SPI command between 100 µs to
  1.6 ms, the default setting is 900 µs.
- In case the LDO_µC current monitor is selected for the transition, the device moves from transition state to STANDBY state at the point the current consumption measured at the LDO_µC drops below the selected threshold before the transition delay timer $t_{tr,del}$ has expired.

11.3.4.2 STANDBY -> INIT state

Prerequisites:

- none

Triggering Events:

- Valid ENA (edge) or WAK (level) signal.
- Wake-up timer expired, if enabled

Exceptions:

- none

Timing Diagram

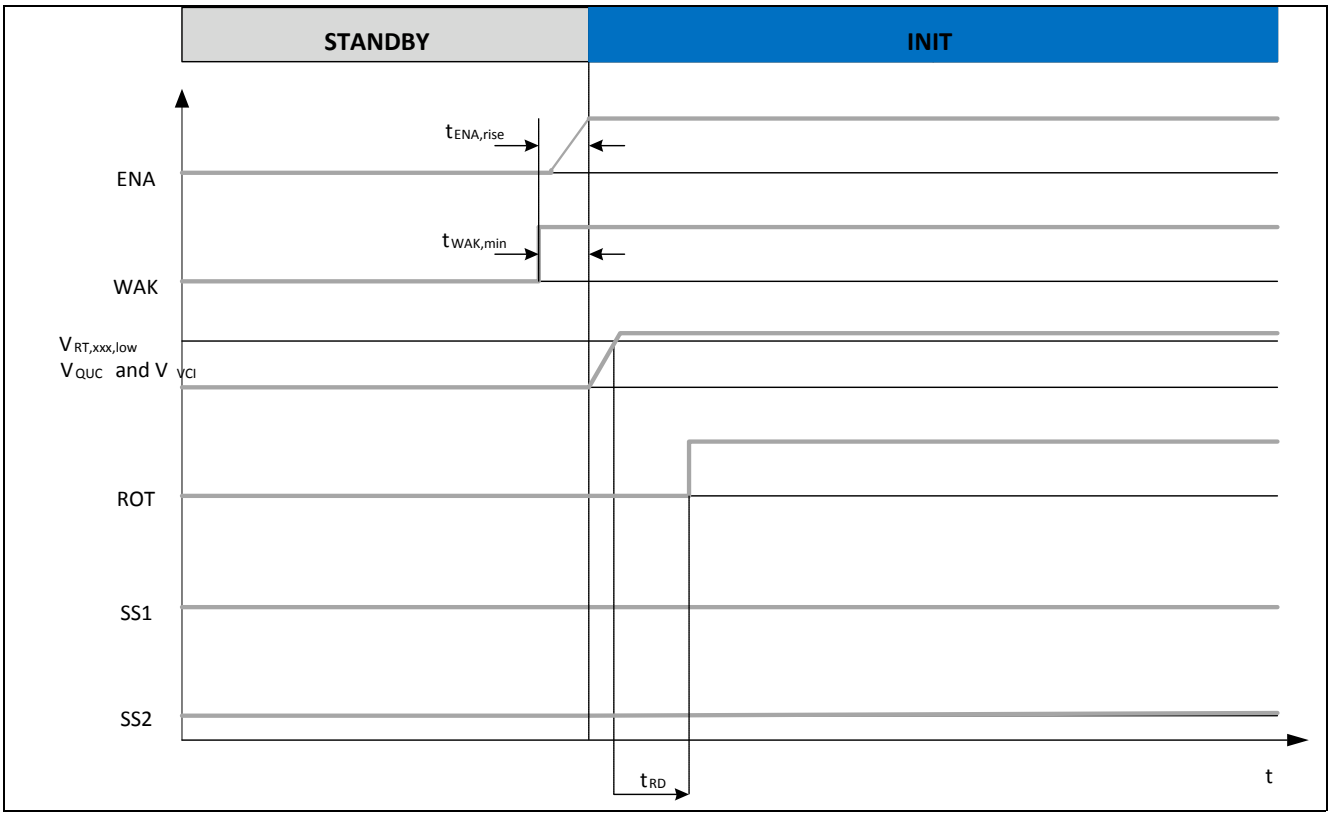


Figure 38 Transition from STANDBY to INIT state

- All pre regulators and all post regulators are switched on according to the power sequencing, except the LDO_Stby is kept ON or OFF according to its configuration (simplified in figure above).
- The power on reset delay time is started as soon as the latest of the µC related regulators V_{QUC} or V_{VCI} (if enabled) crosses the related under voltage reset threshold $V_{RT,xxx,low}$ on the way up.
- After the power on reset delay time has expired the reset (ROT) is set to HIGH.
- The safe signals SS1 and SS2 will stay LOW in STANDBY state and in INIT state.

11.3.4.3 INIT -> NORMAL state

For this state transition please refer to the **Chapter 11.3.2**.

11.3.5 NORMAL -> WAKE state

For this state transition please refer to the description of ABIST in **Chapter 11.6.1**.

11.3.6 WAKE -> NORMAL-state

Prerequisites:

- The activated supervision functions (e.g. window watchdog, functional watchdog, ERR pin monitoring) need to be serviced at least once (minimum 3 periods for ERR monitoring) in the active WAKE state, if they are restarted/reinitialized in WAKE state (e.g. watchdog being inactive in previous SLEEP state)

Triggering Events:

- State transition is only initiated by the SPI command “Go to NORMAL”.

Exceptions:

- none

Timing Diagram

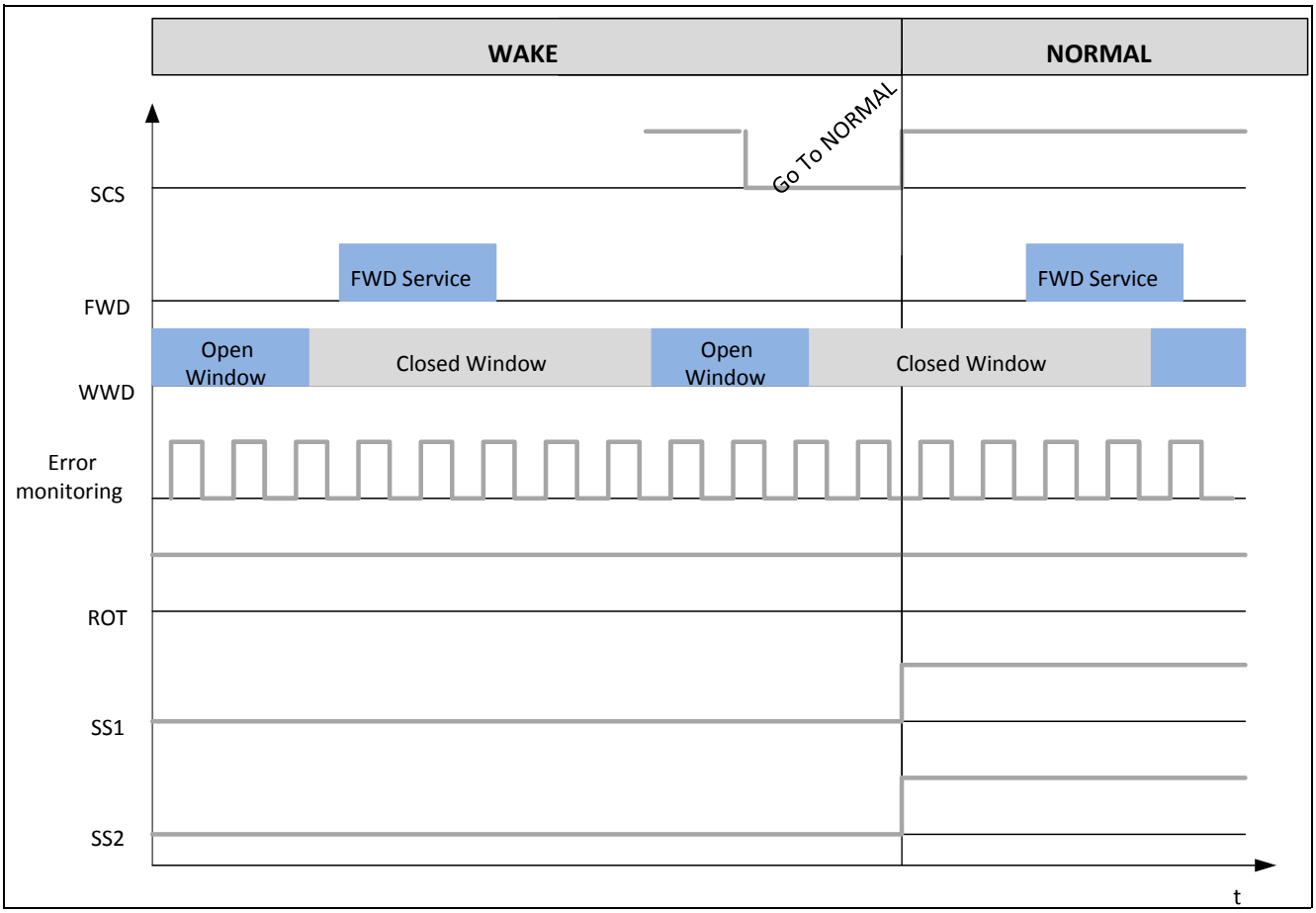


Figure 39 Transition from WAKE to NORMAL state

- The enable signal will be disregarded. A valid enable (edge) signal will not move the device from WAKE to NORMAL state.
- The state of wake signal will be disregarded. A valid wake (level) signal will not move the device from WAKE to NORMAL state.
- The window watchdog (if active in WAKE state) will require continuos service - not synchronized to the transition from WAKE state to NORMAL state.
- The functional watchdog (if active in WAKE state) will require continuos service - not synchronized to the transition from WAKE state to NORMAL state.
- The error monitoring (at pin ERR) (if active in WAKE state) will require a continuos toggling signal - not synchronized to the transition from WAKE state to NORMAL state - but minimum 3 periods detected to enter accept the movement into NORMAL state.
- Reset pin ROT stays HIGH as the post regulators are active in WAKE state and in NORMAL state.
- With the positive edge of chip select high (at pin SCS) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs according to **Table 18** has to be considered)

11.3.7 WAKE -> STANDBY state

Prerequisites:

- Selection of LDO_µC current monitor or absolute transition timer.
- Transition timer needs to be configured or default is used.

- Optionally LDO_µC current threshold needs to be defined or default is used.

Triggering Events:

- State transition is only initiated by the SPI command “Go to STANDBY”.

Exceptions:

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to STANDBY state, the device will move to the INIT state and a reset (ROT) is generated.
- If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected current threshold before the transition timer has expired, the device will move to the INIT state and a reset (ROT) is generated.

Timing Diagram:

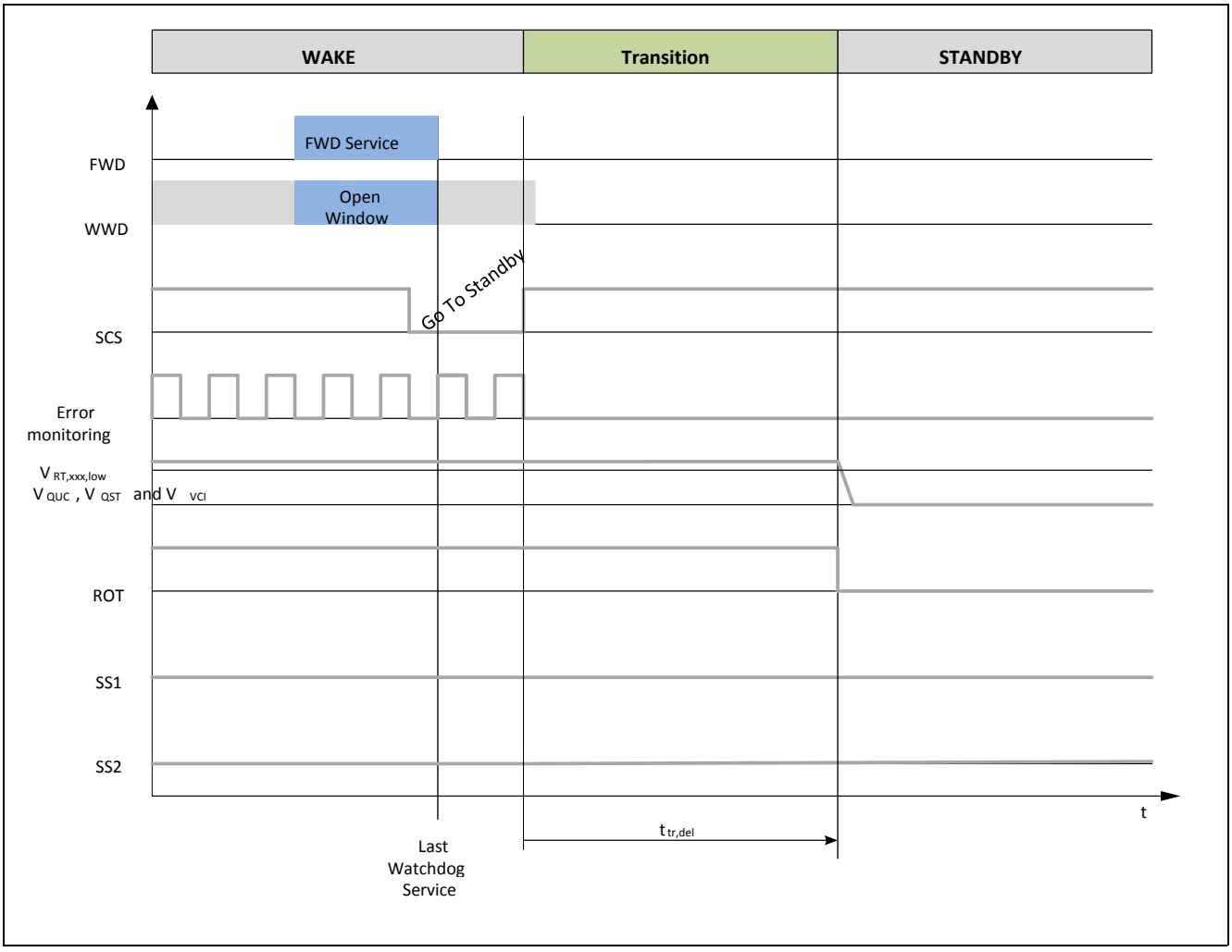


Figure 40 Transition from WAKE to STANDBY state

- Before the SPI command “Go to STANDBY” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”
- The positive edge of chip select (pin SCS) after the SPI command “Go to STANDBY” initiates the transition. In the WAKE state the safe state signals SS1 and SS2 are LOW and will be kept LOW for the transition to STANDBY. The device leaves WAKE state and enters the transition state (to STANDBY state).
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS.
- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS.
- With a successful transition from WAKE to STANDBY state the reset (ROT) is pulled to LOW after the transition time after chip select (pin SCS) going high.
- All pre regulators and all post regulators (with the exception of the standby LDO - it may be ON or OFF in STANDBY state) are switched off at the point when the transition is completed after the reset (ROT) is pulled low.
- In case the absolute transition timer is selected, the device moves from transition state to STANDBY state after the transition time $t_{tr,del}$. The transition time $t_{tr,del}$ can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs.
- In case the LDO_µC current monitor is selected for the transition, the device moves from transition state to STANDBY state at the point the current consumption measured at the LDO_µC drops below the selected threshold before the transition delay timer $t_{tr,del}$ has expired.

11.3.8 FAILSAFE -> INIT state

Prerequisites:

- FAILSAFE timer has expired.

Triggering Events:

- Self triggered transition after the prerequisite is fulfilled.

- Valid ENA (edge) or WAK (level) signal (only needed if exception true)

Exceptions:

- In case the FAILSAFE is entered three times in a row with the same failure the self-triggered transition is blocked.

Timing Diagram

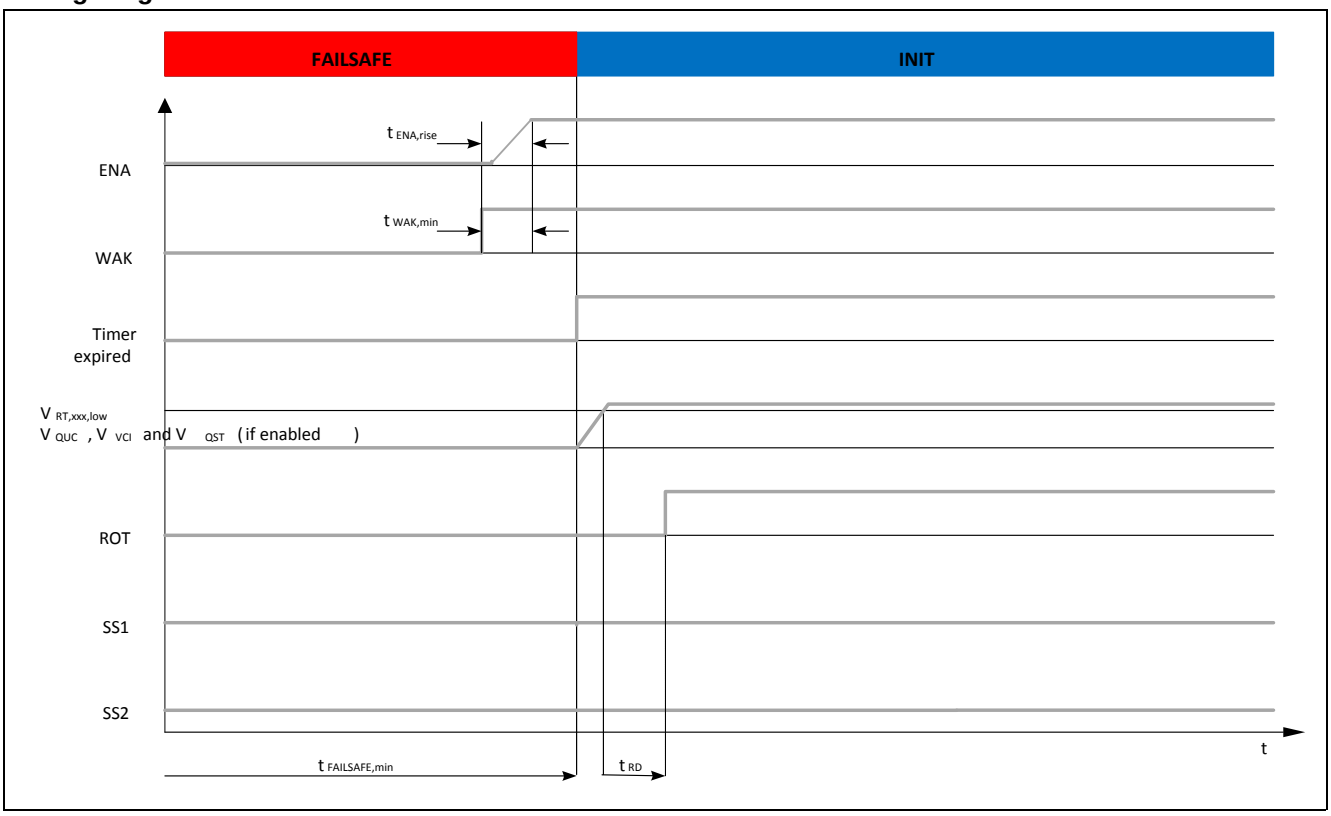


Figure 41 Transition from FAILSAFE to INIT state

- The device transition from FAILSAFE state to INIT state happens earliest after the minimum FAILSAFE time $t_{FAILSAFE,min}$, which is 20 ms for all failures except a thermal shutdown. In case of a thermal shutdown the minimum FAILSAFE time $t_{FAILSAFE,min}$ is 1s. A command to transition before the minimum FAILSAFE time $t_{FAILSAFE,min}$ has expired, will not be executed.
- After entering INIT state the voltage regulators will ramp up according to the power sequencing.
- The power on reset delay time is started as soon as the latest of the µC related regulators V_{QUC}, V_{VCI} or V_{QST} (according to the previous configuration) crosses the related under voltage reset threshold $V_{RT,xxx,low}$ on the way up.
- After the power on reset delay time has expired the reset (ROT) is set to HIGH.
- The device needs to be configured and initiated. All settings done in the configuration registers before the device went into FAILSAFE state are lost, except the configuration of the LDO_Stby (**RSYSPCFG0**) and the reset delay time (**DEVCFG1**).
- The safe state signal SS1 and SS2 are LOW in FAILSAFE state and will be LOW in INIT state

11.4 Reaction on detected faults

Errors are classified according to their severity into 4 different error classes:

- Stay in Current State - Failures affecting peripherals without direct risk for the microcontroller, that are indicated by an interrupt to allow analysis by the microcontroller without changing the state.
- Move to INIT - Medium severity errors that brings the device back to INIT state and generate a reset for the microcontroller.
- Move to FAILSAFE - Critical error with high risk of damaging the microcontroller.
- Move to POWERDOWN - Most critical error with high risk of damaging ourself plus the microcontroller

The error classes are overruled according to their severity, e.g. movement to POWERDOWN takes precedence over movement to FAILSAFE which takes precedence over movement to INIT.

The move to INIT, FAILSAFE and POWERDOWN errors are named “error triggered state transitions” in this document.

11.4.1 Stay in current State

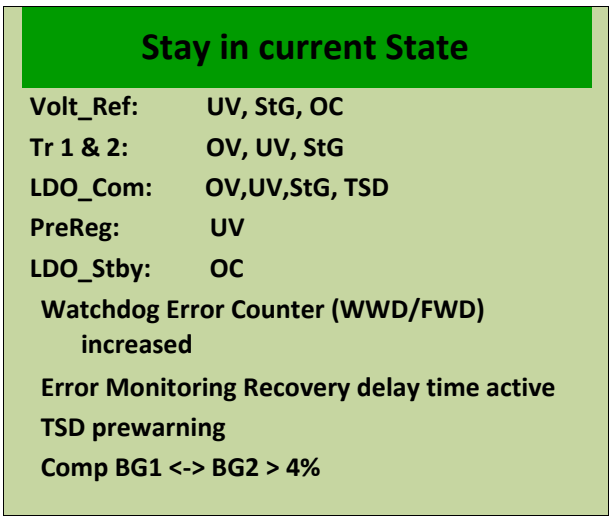


Figure 42 Stay in current State

The following failures will not trigger a movement of the device to another state by themselves, but will indicate the failure by an interrupt event:

- Detection of under voltage or a short to ground or overload detection at voltage reference
- Detection of over voltage, under voltage or a short to ground at trackers 1 or 2
- Detection of over voltage, under voltage, a short to ground or thermal shutdown at LDO_Com
- Detection of under voltage at pre regulator.
- Detection of overload at standby regulator
- Increase of window/functional watchdog status counter, but actual value still stays below the threshold
- Error monitoring recovery delay time is active and ERR signal stops toggling.
- Thermal shutdown pre warning (Step down pre regulator or/and LDO_µC or/and LDO_Com)
- Bandgap monitoring: If the deviation between both bandgaps is larger than 4%

The interrupt may not be visible on the INT pin in STANDBY and FAILSAFE state due to microcontroller supplies being switched off. The event is stored in the status flags (**IF**, **SYSSF**, **MONSF0**, **MONSF1**, **MONSF2**, **OTWRNSF**, **OTFAIL**).

11.4.2 Transition into INIT State

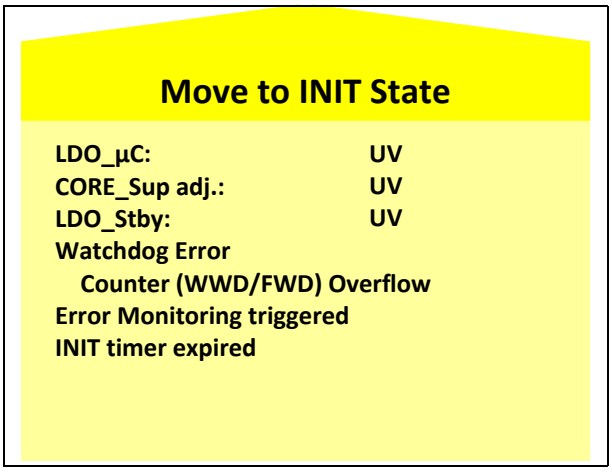


Figure 43 Move to INIT State

The following failures will bring the device from any state to INIT-state:

- Detection of under voltage at LDO_µC, Core_Sup adj. or LDO_Stby
- Detection of window/functional watchdog status counter overflow
- Stop of error signal detected (immediate reaction mode) or stop or error signal detected for more than recovery delay time (recovery mode)
- One or two consecutive expires of the INIT timer (configuration in INIT state failed)

11.4.2.1 INIT -> INIT state due to detected fault

11.4.2.1.1 INIT -> INIT-state due to INIT timer expired for the first time

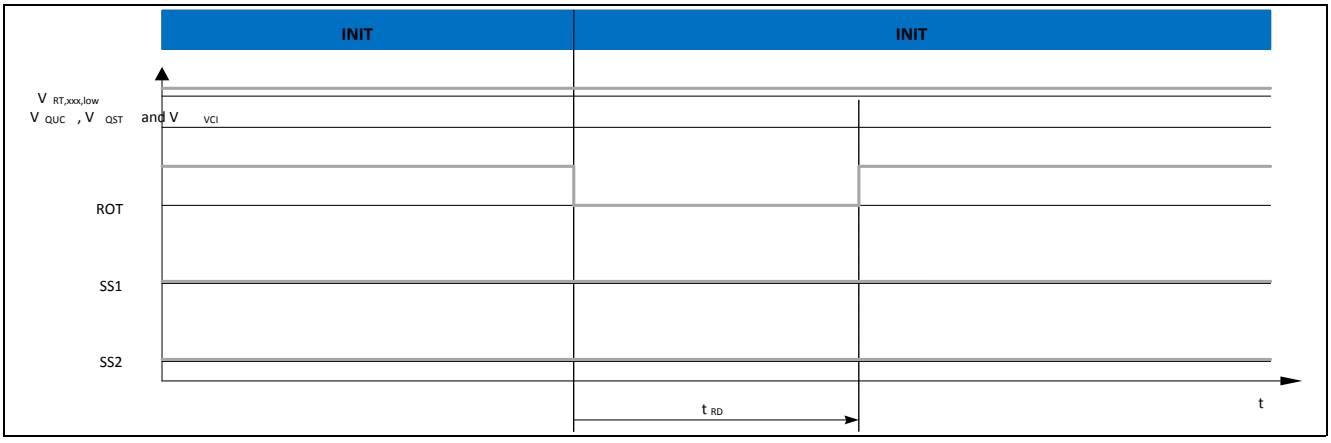


Figure 44 Transition from INIT to INIT state - first movement

Description:

- The device transition from INIT to INIT state (or stays in INIT state) for the first time is issuing a “soft reset”. Pin ROT is pulled to LOW for the reset delay time t_{RD} in case all µC related voltages are in valid range. The power sequence is started after entering the INIT state: the disabled outputs are re-activated, the other ones are kept enabled, except the LDO_Stby will keep its configuration being ON or OFF.

11.4.2.1.2 INIT -> INIT-state due to INIT timer expired for the second time

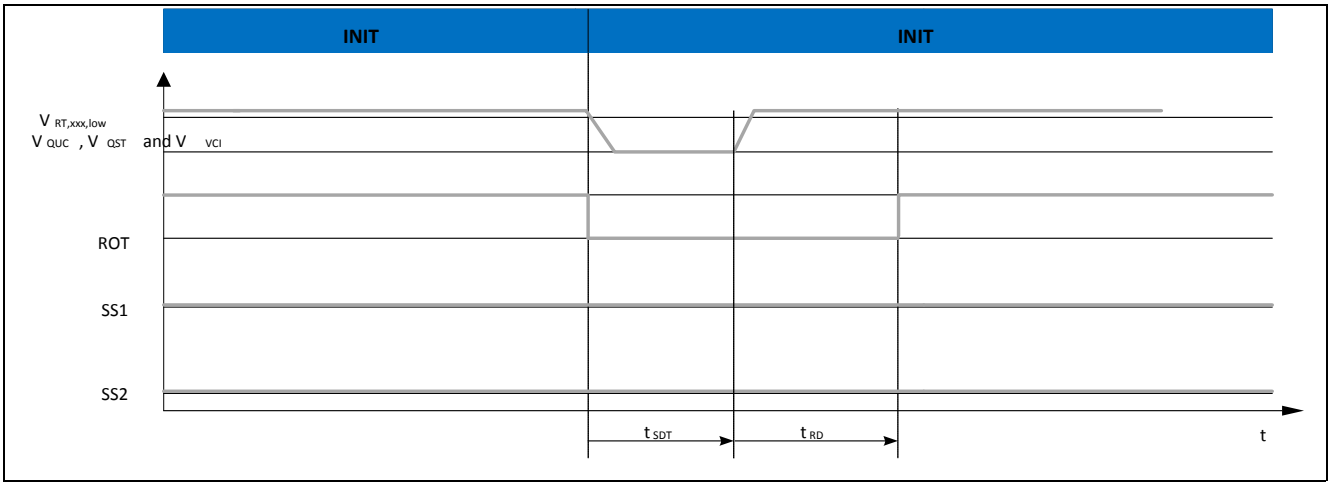


Figure 45 Transition from INIT to INIT state - second movement

Description:

- The device transition from INIT to INIT state (or stays in INIT state) for the second time is issuing a “hard reset” - pin ROT is pulled to LOW and all outputs are disabled for the time *t* and restarted according to the power sequencing (Please refer to **Chapter 8.3**), except the LDO_Stby will restore its configuration being ON or OFF.
- The ROT pin will be released according to the power sequencing using the reset delay time t_{rd}.

Note:Please refer also to the transition INIT to FAILSAFE

11.4.2.2 NORMAL -> INIT state due to detected fault

Timing Diagram

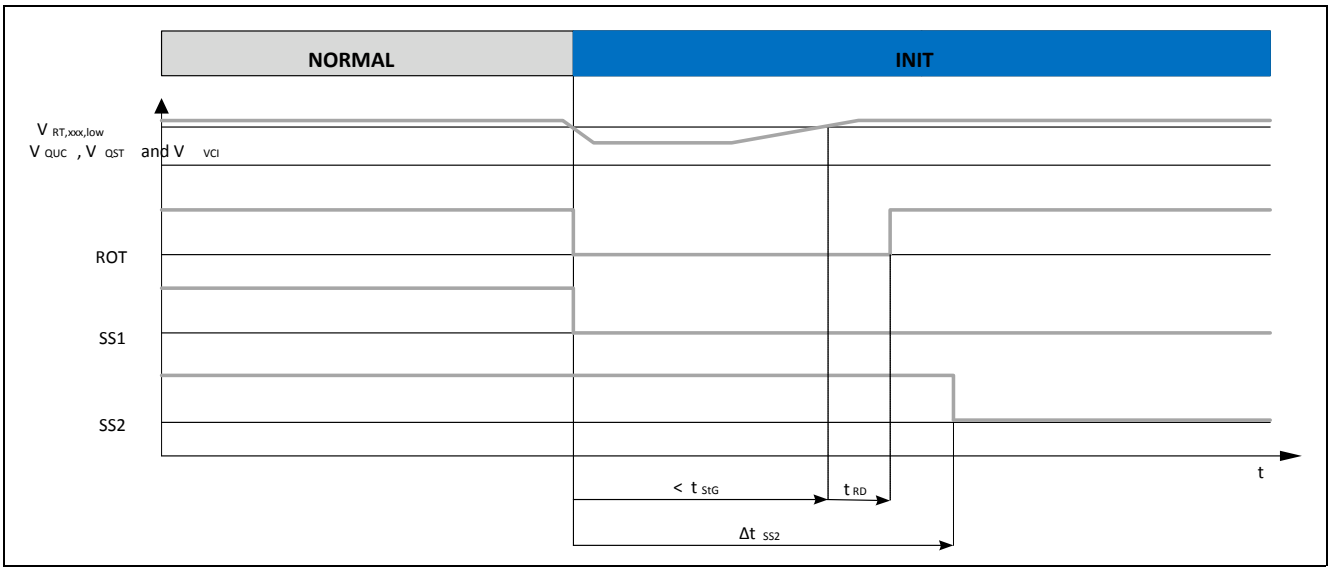


Figure46 Transition from NORMAL to INIT state

Description:

- The device transitions from NORMAL into INIT state issuing a “soft reset” - pin ROT is pulled to LOW and all the outputs are enabled, except the LDO_Stby will keep its configuration being ON or OFF. Outputs that where disabled in NORMAL state will get switched on again.
- This might be issued by an undervoltage of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure. The under voltage is shorter than the short to ground detection time t_{StG}. The reset delay time t_{RD} is started as soon as all µC related voltages V_{QUC}, V_{QST} or V_{VCI} are back in the valid range. The ROT pin is released accordingly. An under voltage longer than the short to ground detection time t_{StG} would first lead to a transition from NORMAL to INIT state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE state.
- The “soft reset” can also be initiated by a window watchdog error counter overflow (> Σ WWD), a functional watchdog error counter overflow (> Σ FWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} will be started falling edge of the ROT pin. Please consider the state transition time to INIT state in **Table 11-8**.
- SS1 will be pulled to LOW immediately with pin ROT, SS2 will be pulled to LOW after the selected Δt_{SS2}.
- Please mind that in case of an UV event on QUC, a delayed SS2 signal will follow V_{QUC} as it is supplied from QUC.

Note:In case the device is sent back to NORMAL state before the configured Δt_{SS2} has expired the SS2 will be kept HIGH without being set to LOW.

11.4.2.3 STANDBY -> INIT state due to detected fault

Timing Diagram

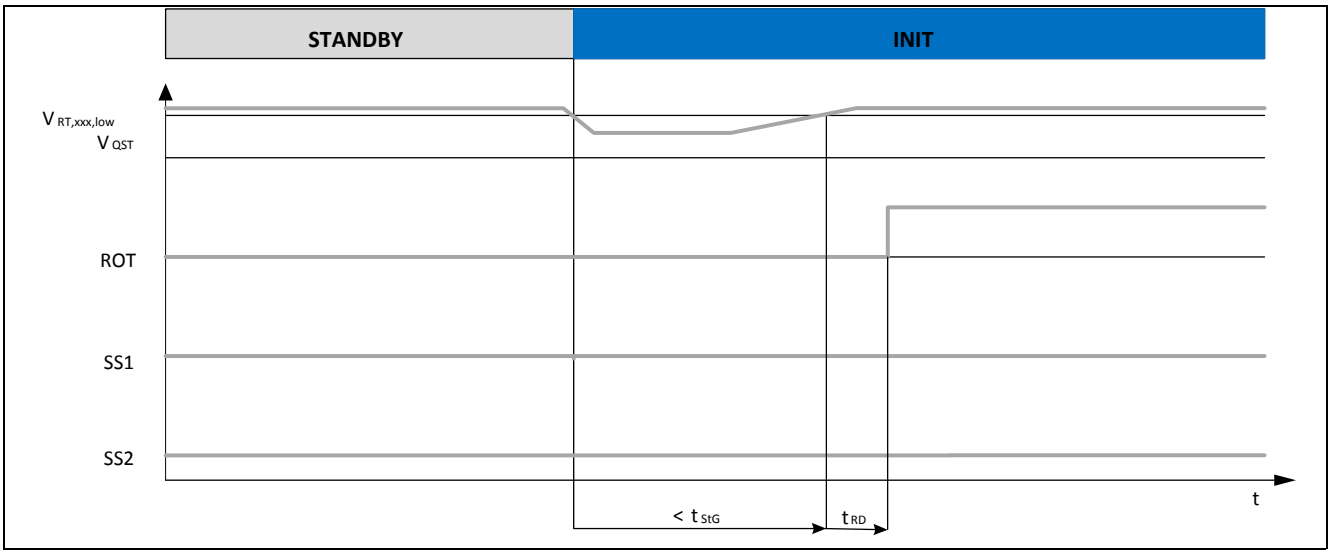


Figure47 Transition from STANDBY to INIT state

Description:

- The device transitions from STANDBY into INIT because of an under voltage of the µC related voltage V_{QST} as shown in the figure. The under voltage is shorter than the short to ground detection time t_{StG}. An under voltage longer than the short to ground detection time t_{StG} would first lead to a transition from STANDBY to INIT state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE state.
- The power sequence is started after entering the INIT state: the disabled outputs are re-activated, except the LDO_Stby will keep its configuration being ON or OFF.
- The power on reset delay time is started according to the power sequencing and releases the ROT accordingly.
  • The safe state signals SS1 and SS2 are LOW in STANDBY state and will be LOW in INIT state Exception:
- Exception: In case of an over or undervoltage of the internal supply voltages a “hard reset” is always initiated. Please refer to **Chapter 8.3**.

11.4.2.4 SLEEP -> INIT state due to detected fault

Description:
Timing Diagram

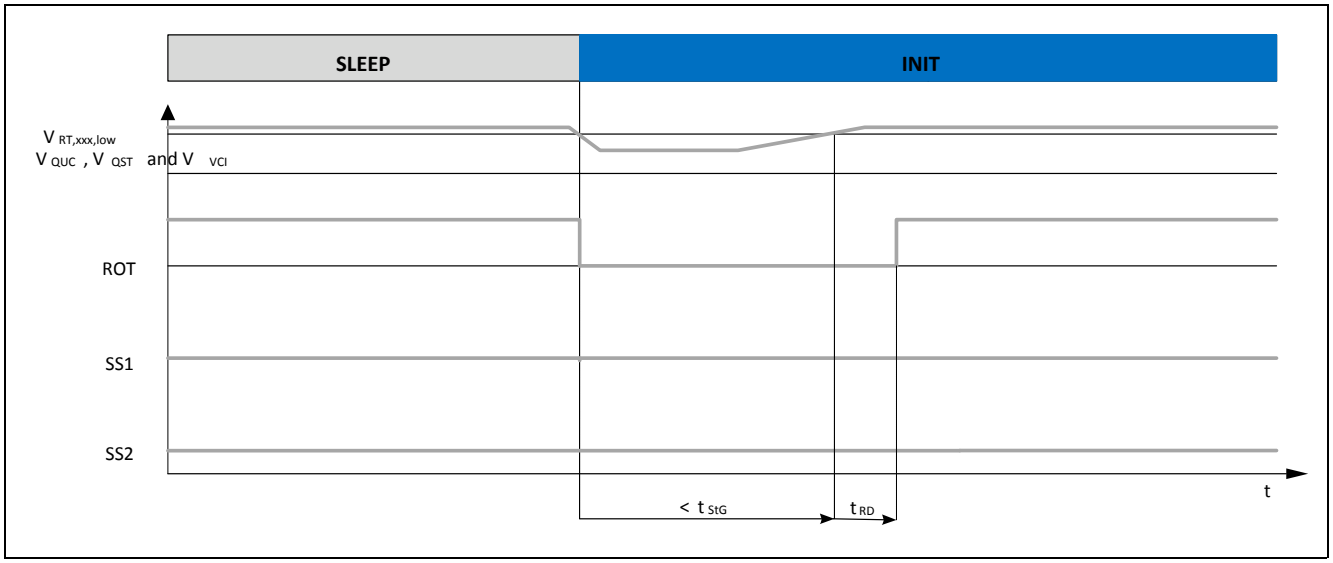


Figure48 Transition from SLEEP to INIT state

- The device transitions from SLEEP into INIT state issuing a “soft reset” - pin ROT is pulled to LOW for a certain time t_{RD} and all the outputs are kept enabled. Outputs that where disabled in SLEEP state will get switched on again, except the LDO_Stby will keep its configuration being ON or OFF.
- This might be issued by an undervoltage of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure. The under voltage is shorter than the short to ground detection time t_{StG}. The reset delay time t_{RD} is started as soon as all µC related voltages V_{QUC}, V_{QST} or V_{VCI} are back in the valid range. The ROT pin is released accordingly. An under voltage longer than the short to ground detection time t_{StG} would first lead to a transition from SLEEP to INIT state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE state
- The “soft reset” can also be initiated by a window watchdog error counter overflow (> Σ WWO), a functional watchdog error counter overflow (> Σ FWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} will be started falling edge of the ROT pin. Please consider the state transition time to INIT state in **Table 11-8**.
- The safe state signals SS1 and SS2 are LOW in SLEEP state and will be LOW in INIT state Exception:
- Exception: In case of an over or undervoltage of the internal supply voltages a “hard reset” is always initiated. Please refer to **Chapter 8.3**.

11.4.2.5 WAKE -> INIT state due to detected fault

Timing Diagram

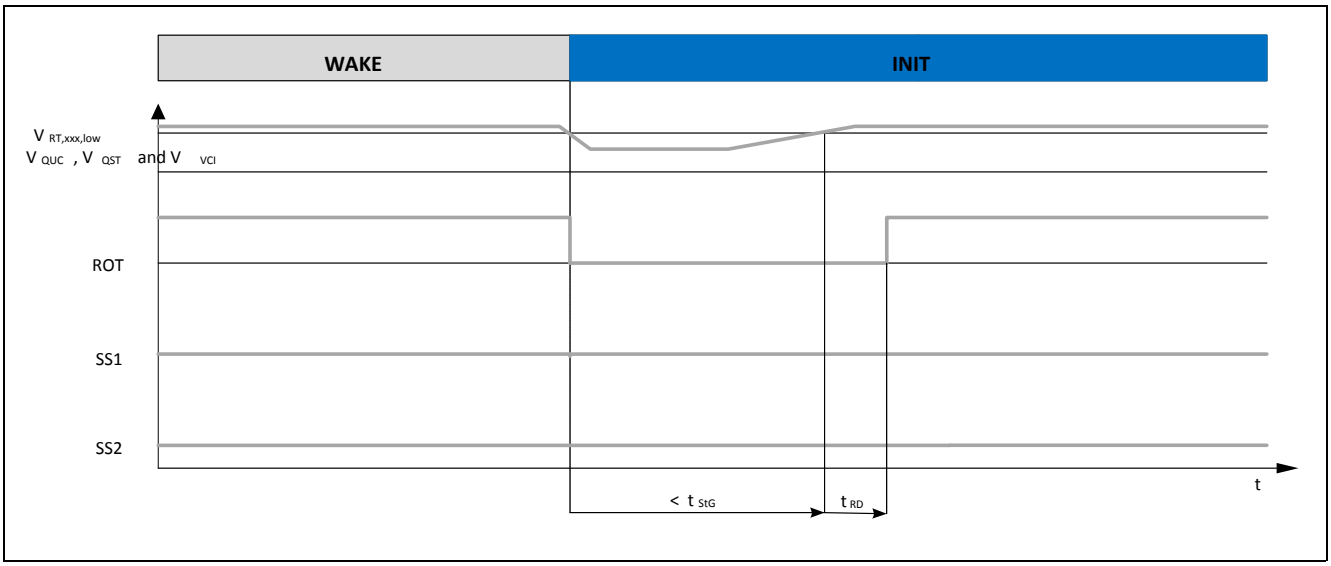


Figure49 Transition from WAKE to INIT state

Description:

- The device transitions from WAKE into INIT state issuing a “soft reset” - pin ROT is pulled to LOW for a certain time t_{RD} and all the outputs are kept enabled. Outputs that where disabled in WAKE state will get switched on again, except the LDO_Stby will keep its configuration being ON or OFF.
- This might be issued by an undervoltage of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure. The under voltage is shorter than the short to ground detection time t_{StG}. The reset delay time t_{RD} is started as soon as all µC related voltages V_{QUC}, V_{QST} or V_{VCI} are back in the valid range. The ROT pin is released accordingly. An under voltage longer than the short to ground detection time t_{StG} would first lead to a transition from WAKE to INIT state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE state.
- The “soft reset” can also be initiated by a window watchdog error counter overflow (> Σ WWO), a functional watchdog error counter overflow (> Σ FWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} will be started falling edge of the ROT pin. Please consider the state transition time to INIT state in **Table 11-8**.
- The safe state signals SS1 and SS2 are LOW in WAKE state and will be LOW in INIT state.

Exception:

- Exception: In case of an over or undervoltage of the internal supply voltages a “hard reset” is always initiated. Please refer to **Chapter 8.3**.

11.4.3 Transition into FAILSAFE State

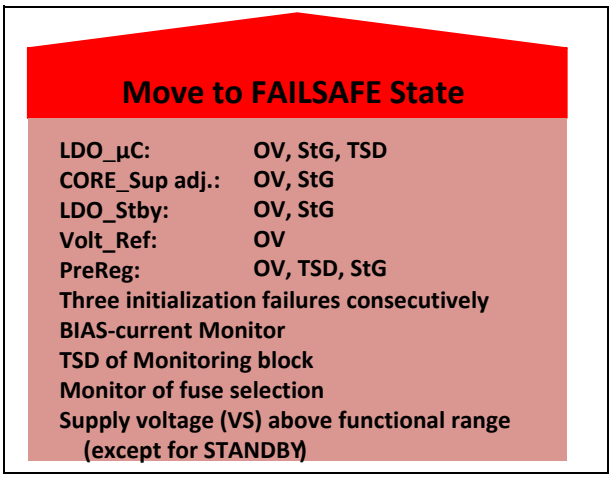


Figure 50 Move to FAILSAFE State

The following failures will bring the device from any state to FAILSAFE-state:

- Detection of over voltage, a short to ground or thermal shutdown at LDO_µC
- Detection of over voltage or a short to ground at Core_Sup adj. or LDO_Stby
- Detection of over voltage at voltage reference
- Detection of over voltage, short to ground[1)] (only during startup phase in INIT state) or thermal shutdown at pre regulator
- Three consecutive initialization failures(e.g. configuration in INIT state failed)
- A BIAS current monitor failure
- A over temperature shutdown due to exceeded temperature in the monitoring block.
- A fuse selection monitor failure
- An over voltage at the supply pins (VS) will trigger the overvoltage protection and move the device into FAILSAFE-state (except for STANDBY state)

11.4.3.1 INIT -> FAILSAFE state due to detected fault

Timing Diagram

[1]) A detected short to GND of the pre regulator after the power sequencing in INIT state (once above the UV threshold) will not be considered as a Move to FAILSAFE event, but the event will be stored in **MONSF0.PREGSG** without an interrupt.

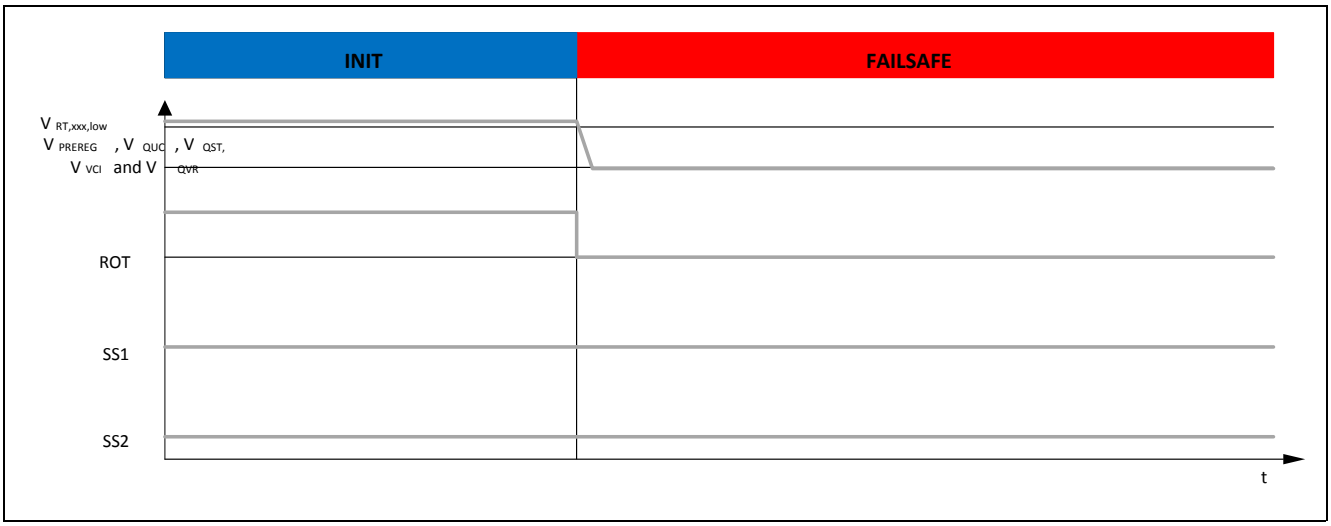


Figure 51 Transition from INIT to FAILSAFE state

Description:

- The transition from INIT state into FAILSAFE state will be initiated by any failure (external or internal) case mentioned in **Chapter 11.4.3**.
- Pin ROT will be pulled to LOW as soon as one of the MoveToFailsafe failures is detected, if is not already LOW due to an undervoltage on a µC related regulator.
- All regulators will be switched off, when the device turns from INIT into FAILSAFE state, regardless if they are in over voltage condition or not.
- The safe state signals SS1 and SS2 are LOW in INIT state and will be LOW in FAILSAFE state.

11.4.3.2 XXXX -> INIT -> FAILSAFE state due to detected fault

Timing Diagram

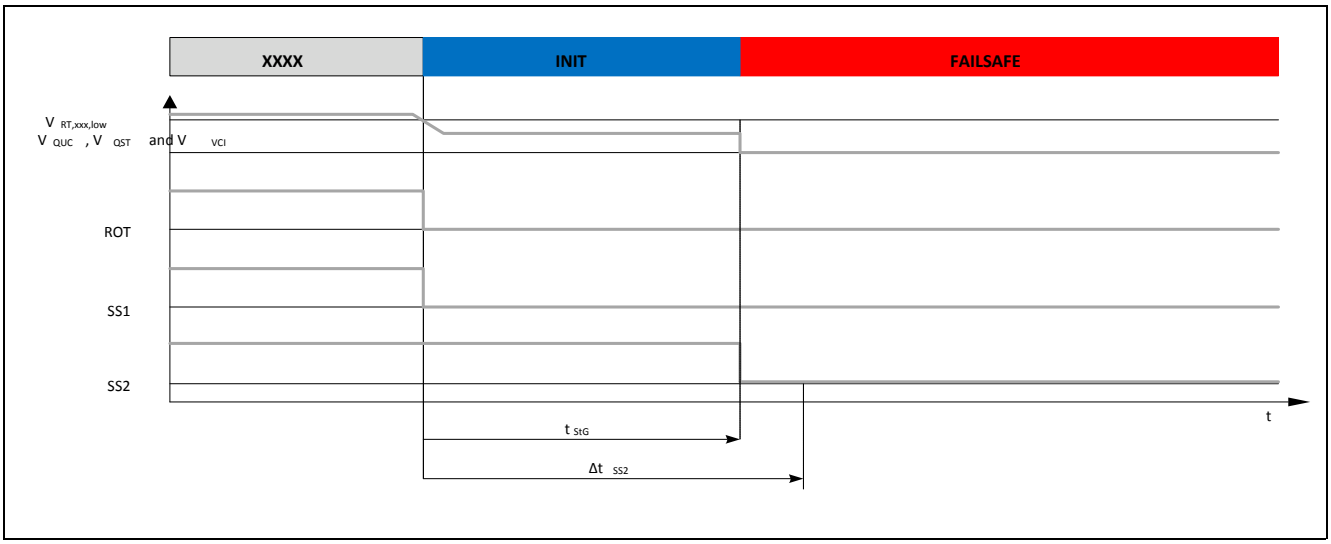


Figure52 Transition from XXXX to INIT to FAILSAFE state after detection of short to ground

Description:

- The detection of an under voltage of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure will initiate the transition into INIT state. (please refer to previous chapter Transition into INIT state)
- Pin ROT will be pulled to LOW as soon as the under voltage is detected (at one or more of the regulators mentioned above - whichever is the first)
- The safe state signal SS1 will be pulled to LOW together with pin ROT going to low
- If the short to ground maintains for longer than the short to ground detection time t_{StG} a short to ground event is detected.
- All regulators will be switched off as soon as the short to GND is detected, regardless if they are in under voltage condition or not.
- The device moves from INIT state to FAILSAFE state
- The safe state signal SS2 will be pulled to LOW together with the transition from INIT to FAILSAFE state, even if the delay time Δt_{SS2} has not expired yet, because LDO_µC is switched off (LDO_µC is switched on in INIT state, but switched off in FAILSAFE state).

11.4.3.3 NORMAL -> FAILSAFE state due to detected fault

Timing Diagram

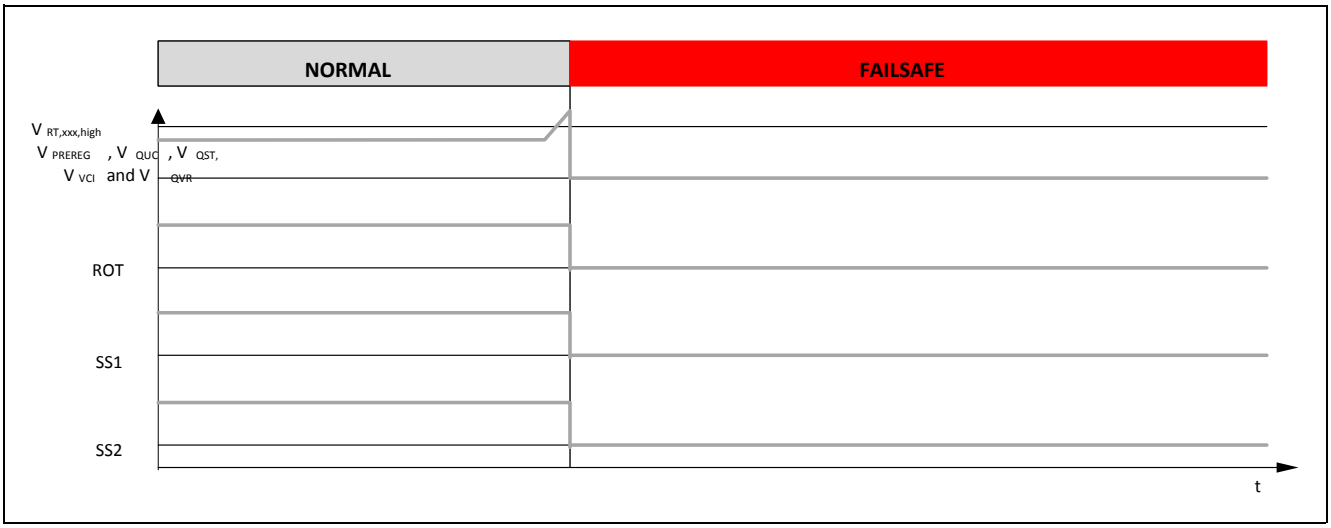


Figure 53 Transition from NORMAL to FAILSAFE state

Description:

- The detection of an over voltage of the preregulator voltage V_{PREREG} or the µC related voltages V_{QUC}, V_{QST}, V_{VCI} or V_{QVR} as shown in the figure will initiate the transition from NORMAL state to FAILSAFE state.
- Pin ROT will be pulled to LOW as soon as the over voltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
- All regulators will be switched off, when the device turns from NORMAL into FAILSAFE state, regardless if they are in over voltage condition or not.
- The safe state signals will be pulled to LOW immediately with pin ROT going to low, because the LDO_µC is switched off.
- The transition from NORMAL state into FAILSAFE state will be initiated by any failure (external or internal) case mentioned in **Chapter 11.4.3**.
- The detection of a short to ground of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the **Figure 52** will first be detected as an under voltage event and move the device from NORMAL state to INIT state. After the short to ground detection time t_{StG} the device will then move from INIT state to FAILSAFE state (please refer to transition from INIT state to FAILSAFE state).

11.4.3.4 STANDBY -> FAILSAFE state due to detected fault

Timing Diagram

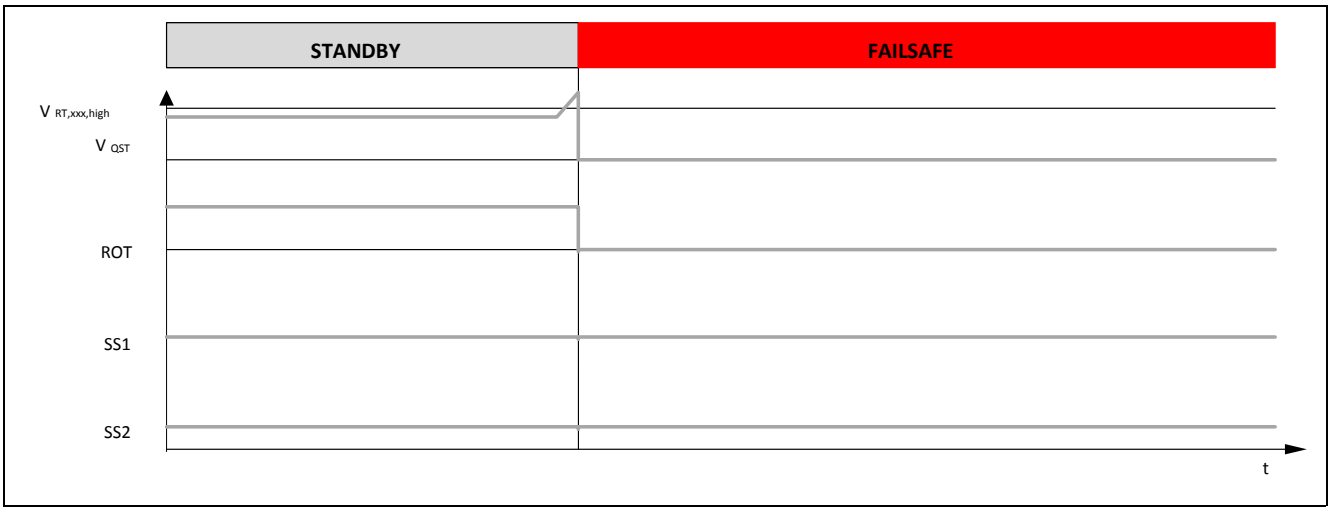


Figure 54 Transition from STANDBY to FAILSAFE state

Description:

- The detection of an over voltage of the µC related voltage V_{QST} as shown in the figure will initiate the transition from STANDBY state to FAILSAFE state.
- Pin ROT is LOW in STANDBY state and will stay LOW in FAILSAFE state.
- The safe state signals SS1 and SS2 are LOW in STANDBY state and will be LOW in FAILSAFE state.
- Beside the example above the transition from STANDBY state into FAILSAFE is initiated by an internal BIAS current monitor failure.
- The detection of a short to ground of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the **Figure 52** will first be detected as an under voltage event and move the device from STANDBY state to INIT state. After the short to ground detection time t_{StG} the device will then move from INIT state to FAILSAFE state (please refer to transition from INIT state to FAILSAFE state).

11.4.3.5 SLEEP -> FAILSAFE state due to Fault

Timing Diagram

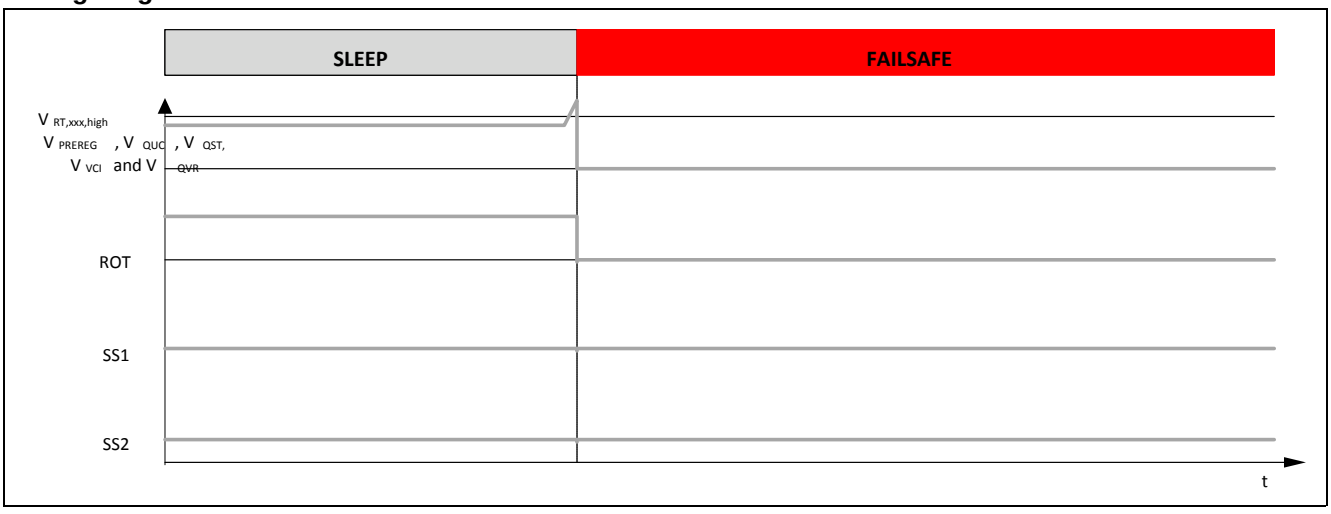


Figure 55 Transition from SLEEP to FAILSAFE state

Description:

- The detection of an over voltage of the preregulator voltage V_{PREREG} or the µC related voltages V_{QUC}, V_{QST}, V_{VCI} or V_{QVR} as shown in the figure will initiate the transition from SLEEP state to FAILSAFE state.
- Pin ROT will be pulled to LOW as soon as the over voltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
- All regulators will be switched off, when the device turns from SLEEP into FAILSAFE state., regardless if they are in over voltage condition or not.
- The safe state signals will stay at LOW as in the SLEEP state.
- The transition from SLEEP state into FAILSAFE state will be initiated by any failure (external or internal) case mentioned in **Chapter 11.4.3**.
- The detection of a short to ground of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the **Figure 52** will first be detected as an under voltage event and move the device from SLEEP state to INIT state. After the short to ground detection time t_{StG} the device will then move from INIT state to FAILSAFE state (please refer to transition from INIT state to FAILSAFE state).

11.4.3.6 WAKE -> FAILSAFE state due to detected fault

Timing Diagram

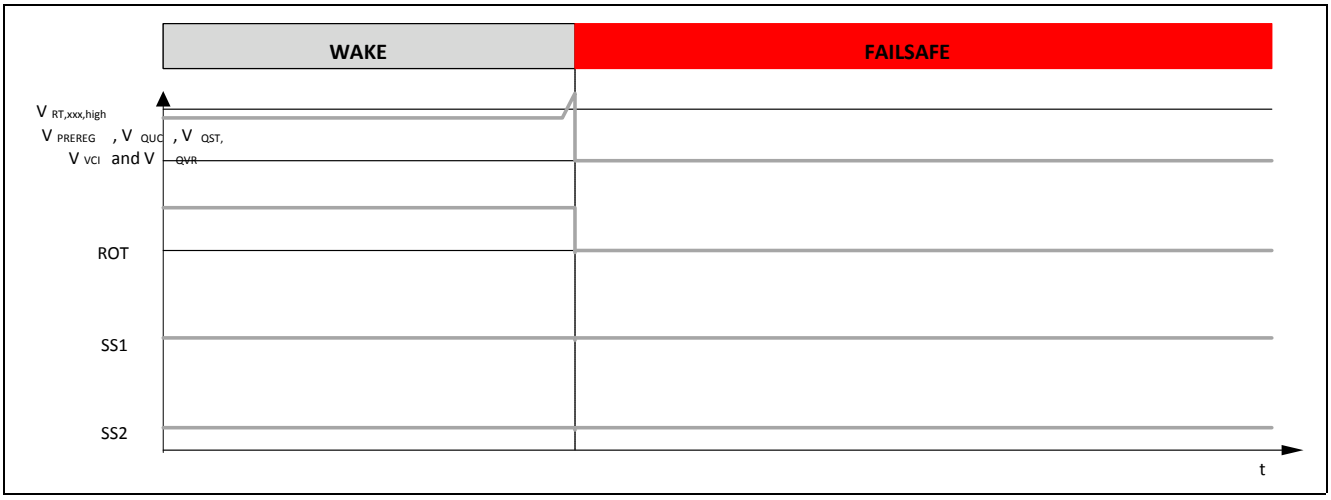


Figure 56 Transition from WAKE to FAILSAFE state

Description:

- The detection of an over voltage of the preregulator voltage V_{PREREG} or the µC related voltages V_{QUC}, V_{QST}, V_{VCI} or V_{QVR} as shown in the figure will initiate the transition from WAKE state to FAILSAFE state.
- Pin ROT will be pulled to LOW as soon as the over voltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
- All regulators will be switched off, when the device turns from WAKE into FAILSAFE state., regardless if they are in over voltage condition or not.
- The safe state signals will stay at LOW as in the WAKE state.
- The transition from WAKE state into FAILSAFE state will be initiated by any failure (external or internal) case mentioned in **Chapter 11.4.3**.

- The detection of a short to ground of the µC related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the **Figure 52** will first be detected as an under voltage event and move the device from WAKE state to INIT state. After the short to ground detection time t_{StG} the device will then move from INIT state to FAILSAFE state (please refer to transition from INIT state to FAILSAFE state).

11.4.3.7 Transition into FAILSAFE state due to thermal shutdown

Timing Diagram

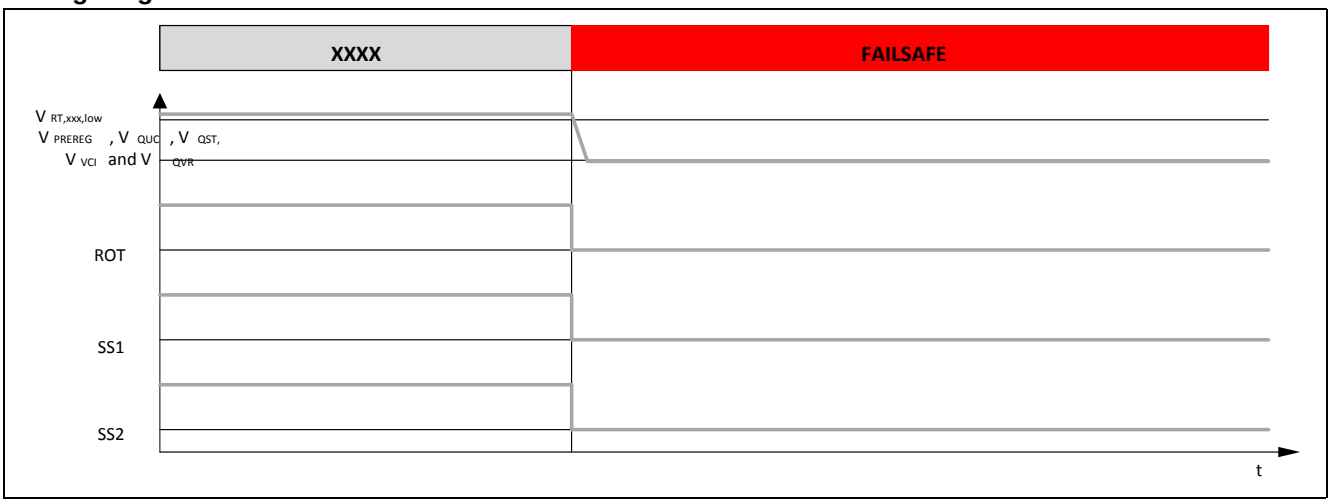


Figure 57 Transition into to FAILSAFE state due to thermal shutdown

Description:

- The transition from any state into FAILSAFE state will be initiated by a thermal shutdown (TSD).
- Pin ROT will be pulled to LOW as soon as the thermal shutdown will be detected.
- All regulators will be switched off, when the device turns from xxx into FAILSAFE state. regardless if they are in over temperature condition or not
- Out of NORMAL state the safe state signals SS1 and SS2 will be pulled to LOW immediately with pin ROT going to low, because the LDO_µC is switched off. Out of any other state the safe state signals SS1 and SS2 are LOW and will stay low.
- The device will stay in FAILSAFE state after a thermal shutdown (TSD) at least for 1 s.

11.4.4 Transition into POWERDOWN-state

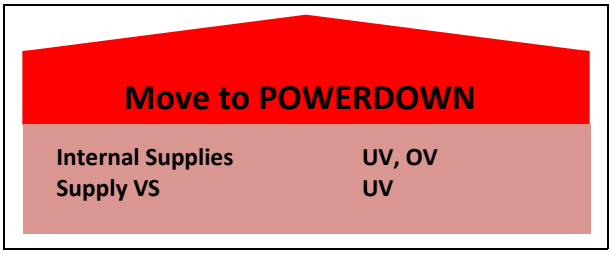


Figure 58 Move to POWERDOWN-state

The following failures/event will bring the device always with highest priority to POWERDOWN-state:

- V_{VS} below $V_{PD,lo,min}$ when decreasing

- Detection of over- or under voltage on internal supplies

11.5 Electrical Characteristics

Table 11-8 Electrical characteristics: State machine

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
INIT timer / Initialization time-out	t_{INIT}	550	600	650	ms	–	P_11.5.1
FAILSAFE time	$t_{FAILSAFE,min}$	18	20	22	ms	–	P_11.5.2
FAILSAFE time TSD	$t_{FAILSAFE,min}$	0.9	1	1.1	s	for thermal shutdown TSD	P_11.5.3
Transition delay timer accuracy	$t_{tr,del}$	-20	–	+20	%	1) Configurable value DEVCFG0.TRDEL	P_11.5.4
LDO_µC current monitoring for low power states	$I_{LDO\_µC,att}$	-30	–	+30	%	Configurable value DEVCFG2.CTHR ; $V_{PREREG} > V_{QUC} + V_{dr,QUC}$	P_11.5.5
State transition time	t_{tr}	–	–	100	µs	except transitions to SLEEP, to STANDBY2) or from STANDBY	P_11.5.6
State transition time to INIT	$t_{tr,INIT}$	–	–	150	µs	valid for “Move to INIT” events excluding transitions from STANDBY, FAILSAFE and POWERDOWN	P_11.5.7

State transition time to INIT	$t_{tr,INIT}$	–	–	250	µs	valid for transitions from STANDBY, FAILSAFE and interrupted transition to STANDBY	P_11.5.8
Internal start-up time from POWERDOWN	$t_{tr,pwrd}$	–	0.4	2	ms	from first VS connection to INIT/ power sequence	P_11.5.9
PowerDown threshold high (Power-On-Reset POR)	$V_{PD,hi}$	–	–	6	V	V_{VS} increasing	P_11.5.10
PowerDown threshold low (Power-On-Reset POR)	$V_{PD,lo}$	2	–	3.5	V	V_{VS} decreasing	P_11.5.11

1) Due to internal delays the transition delay time can be enlarged by max 30 µs.

2) For transition times into SLEEP or STANDBY please refer to the transition delay timer configurable by register DEVCFG0.TRDEL and its accuracy specified in **Table 11-8**.

11.6 Built In Self Test (BIST) Features

TLF35584 provides the option to test certain observation functions with the assistance of the external µC via built in self-test features. These features are described in the following chapters.

11.6.1 Analog Built In Self Test (ABIST)

TLF35584 provides the option to test the comparator and evaluation logic related to the monitoring functions contributing to the activation of the secondary safety shutdown path and the generation of an interrupt. Further on additional comparators and evaluation logic related to the safe state control itself can be tested (SSC overvoltage watchdog and toggling monitor). This is accomplished via an internal ABIST controller which performs tests on each comparator generating artificial undervoltage and overvoltage (or current) conditions, is checking the result

and generates the information which needs to be evaluated by the µC to judge, if the ABIST operation has been performed successfully or not.

The following status information on ABIST operation is generated by the system:

- In case an ABIST operation has been requested by the µC, a status is provided after the ABIST has been performed (**ABIST_CTRL0.STATUS**). This status needs to be evaluated by the µC. The provided status is just a GO-NOGO information, which means information about a particularly tested path is provided. The basic comparator function is tested, but not the respective threshold values.

The test of the monitoring and safety relevant output functions is run on three different areas in the system:

- The functionality of a comparator and its corresponding deglitching logic can be tested by a “comparator only” test. This test is performed by generating the failure condition for a time shorter than the deglitching time, accordingly the secondary safety shutdown path nor the interrupt is triggered due to the detected failure. During this test only the selected comparator(s) are tested. In case more than one comparator is selected, the test is performed with a fixed sequence of comparators to be tested. The completion of the test is indicated by an interrupt.
- The functionality of a comparator including its corresponding deglitching logic and the contribution to the respective safety measure can be tested. The safety measure is either the activation of the secondary safety shutdown path or the generation of an interrupt. This test is performed in a time longer than the deglitching time.
- While the device provides information about the status for the first and the second ABIST, further microcontroller cooperation is required for the third area. The µC is responsible to check if the secondary safety shutdown path has been activated successfully (SS1/SS2 are set low) or an interrupt event has been detected by the µC.

11.6.1.1 How to run the ABIST

During ABIST, servicing of the watchdog(s) and error monitoring is required to be performed according to the configuration by the microcontroller. Error in not doing so will lead to failure events in these functions and will lead to the assertion of interrupt, reset or safe state output events accordingly, which is disturbing the proper analysis of the ABIST results. Optionally watchdog functionality and/or error monitoring can be disabled during ABIST operation via a protected register access. In this case, no servicing is required.

During a performed ABIST including the deglitching logic the FLAG registers (**SYSFAIL**, **INITERR**, **IF**) as well as the status information (**MONSF1**, **MONSF2**, **MONSF3**) are triggered and updated by out of range conditions caused by the ABIST functionality, which has to be considered beside the results provided in the ABIST related registers (**ABIST_CTRL0** to **ABIST_SELECT2**).

During the time, when the ABIST is performed by internal hardware, the assertion of ROT due to the occurrence of any event which is supposed to trigger the respective action and is part of the logic which is affected by the ABIST control is blocked. In addition, the state machine will not change its state according to the reaction on detected faults described in **Chapter 11.4**. In case an ABIST contributing to the secondary safety shutdown path is started and the device is in NORMAL state, the state machine will move from NORMAL to WAKE state. Furthermore, all voltages will be kept enabled regardless of any out of range detection caused by ABIST itself.

The test of a single functionality is basically always performed in the same way:

- All comparators are assumed to be enabled in case they are selected to be tested, while this is true for any µC related voltage it might not be the case for non µC related voltages. Accordingly, configurable LDO’s have to be enabled before they can be tested. On the other hand the ABIST test on a comparator which is not used by the system is not required to be performed.
- The comparators to be tested shall be selected by setting the individual bit(s) in the respective register(s) (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**). For this selection it is necessary to

differentiate by the contribution to the different safety measure. The differentiation can be derived from **Table 11-9**.

- The microcontroller shall configure the register **ABIST_CTRL0** according to the functionality to be tested. The configuration consist of the tested safety measure (**ABIST_CTRL0.INT**), the tested area/coverage by the ABIST (**ABIST_CTRL0.PATH**) and the configuration whether a sequence or a single comparator shall be tested (**ABIST_CTRL0.SINGLE**).
- The microcontroller shall set the global ABIST start bit (**ABIST_CTRL0.START**) to start the ABIST.
- The global ABIST start bit shall be read by the µC. If this bit is still set, ongoing ABIST functionality is performed. Upon completion of the selected ABIST operation(s) the start bit is cleared and an interrupt event is generated.
- Each bit which has been set to select the test of a dedicated comparator (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**) is cleared once a successful ABIST operation has been performed on the particular comparator. Each bit which has been set to select the test of a dedicated comparator is kept unchanged if the ABIST operation on this particular comparator has not been performed successfully.

In this way the µC can determine which comparator failed in case the ABIST status information shows a failing ABIST operation.

Table 11-9 Contribution of comparators to safety measures

Comparator	Secondary Safety Shutdown Path	Interrupt	ABIST_Select register bit
LDO_µC Overvoltage	X		**ABIST_SELECT0.UCOV**
Core_Sup Overvoltage	X		**ABIST_SELECT0.VCOREOV**
LDO_Stby Overvoltage	X		**ABIST_SELECT0.STBYOV**

Table 11-9 Contribution of comparators to safety measures (cont'd)

Comparator	Secondary Safety Shutdown Path	Interrupt	ABIST_Select register bit
Volt_Ref Overvoltage	X		**ABIST_SELECT0.VREFUV**
PreReg Overvoltage	X		**ABIST_SELECT0.PREGOV**
LDO_µC Undervoltage	X		**ABIST_SELECT1.UCUV**
Core_Sup Undervoltage	X		**ABIST_SELECT1.VCOREUV**
LDO_Stby Undervoltage	X		**ABIST_SELECT1.STBYUV**
BIAS current low	X		**ABIST_SELECT2.BIASLOW**
BIAS current high	X		**ABIST_SELECT2.BIASHI**
Supply VS Overvoltage	X		**ABIST_SELECT2.VBATOV**
Internal Supply Overvoltage	X 1)		**ABIST_SELECT2.INTOV**
Tracker 1 Overvoltage		X	**ABIST_SELECT0.TRK1OV**
Tracker 2 Overvoltage		X	**ABIST_SELECT0.TRK2OV**
LDO_Com Overvoltage		X	**ABIST_SELECT0.COMOV**

Volt_Ref Undervoltage		X	**ABIST_SELECT1.VREFUV**
Tracker 1 Undervoltage		X	**ABIST_SELECT1.TRK1UV**
Tracker 2 Undervoltage		X	**ABIST_SELECT1.TRK2UV**
LDO_Com Undervoltage		X	**ABIST_SELECT1.COMUV**
Pre_Reg Undervoltage		X	**ABIST_SELECT1.PREGUV**
V_{BG1} - 4% ≤ V_{BG2}		X	**ABIST_SELECT2.BG12UV**
V_{BG1} + 4% ≥ V_{BG2}		X	**ABIST_SELECT2.BG12OV**

1) This comparator must be tested only by “comparator only” test

11.6.1.2 Testing the comparator logic only

During the ABIST operation the comparators are triggered by the ABIST controller for a time shorter than the internal deglitching time t_{rr} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied.

The provided information of each comparator is checked against the expected value. If the comparator output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the **STATUS** in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass. A bit which is still set, would indicated the failing comparator(s), that makes the overall **STATUS** to be failed.

Accordingly the maximum selection[1)] (including possible ones) for the comparator test would be the following:

Secondary safety shutdown path (SS1/2) related:

- **ABIST_SELECT0** : 00101111_B ($2F_H$)
- **ABIST_SELECT1** : 00001110_B ($0E_H$)
- **ABIST_SELECT2** : 11001001_B ($C9_H$)
- Start of the test by **ABIST_CTRL0** : 00000001_B (01_H) Interrupt (INT) related:
- **ABIST_SELECT0** : 11010000_B ($D0_H$)
- **ABIST_SELECT1** : 11110001_B ($F1_H$)

- **ABIST_SELECT2** : 00110000_B (30_H)
- Start of the test by **ABIST_CTRL0** : 00001001_B (09_H)

This type of ABIST can be performed in the following states of the **State Machine**: INIT, NORMAL, WAKE. In case of an successful ABIST there shall be no reaction of secondary safety shutdown path SS1/2 and only an interrupt generated due to the finished ABIST (**IF.ABIST** set and **IF.MON** not set, considering cleared interrupt flags prior to the ABIST and no real failure events during the ABIST).

11.6.1.3 Testing the comparator logic and the corresponding deglitching logic

During the ABIST operation the comparators are triggered by the the ABIST controller for a time longer than the internal deglitching time t_{rr} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied. The deglitching logic will forward the failure trigger after t_{rr} and makes the device react on the recognized failure event. This reaction consists the storage of the respective monitoring failure flags and as well the triggering of the respective output function, which is either the interrupt INT

[1]) Please mind that for a test of a comparators the corresponding output has to be enabled.

or the secondary safety shutdown path SS1/2. The reaction of the safe state outputs SS1/2 can only be observed in case the test is started in NORMAL state.

Furthermore the provided information of each deglitching logic output is checked against the expected value. If the deglitching logic output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the **STATUS** in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass recognized by the ABIST controller. A bit which is still set, would indicated the failing comparator(s), that makes the overall **STATUS** to be failed.

Beside the results read from the ABIST controller related registers, the result provided in the failure/interrupt flags (**SYSFAIL**, **INITERR** and **IF**) and monitoring status flags (**MONSF1**, **MONSF2** or **MONSF3**) have to be read and checked by the microcontroller against the expected result considering the configuration set before the start of the ABIST.

INTOV located in register **ABIST_SELECT2** cannot be tested in this way, testing of the comparator logic only is required according to **Chapter 11.6.1.2**.

The maximum selection[1)] for the comparator and deglitching logic test would be the following:

Secondary safety shutdown path (SS1/2) related:

- **ABIST_SELECT0** : 00101111_B ($2F_H$)
- **ABIST_SELECT1** : 00001110_B ($0E_H$)
- **ABIST_SELECT2** : 11000001_B ($C1_H$)
- Start of the test by **ABIST_CTRL0** : 00000011_B (03_H) Interrupt (INT) related:
- **ABIST_SELECT0** : 11010000_B ($D0_H$)
- **ABIST_SELECT1** : 11110001_B ($F1_H$)
- **ABIST_SELECT2** : 00110000_B (30_H)
- Start of the test by **ABIST_CTRL0** : 00001011_B ($0B_H$)

The analysis based on the maximum possible selection would consist the following:

Secondary safety shutdown path (SS1/2) related:

- **IF** : 01000000_B (40_H)
- **INITERR** : 00000100_B (04_H)
- **SYSFAIL** : 00000100_B (04_H)
- **MONSF1** : 00101111_B ($2F_H$)
- **MONSF2** : 00001110_B ($0E_H$)
- **MONSF3** : 11000001_B ($C1_H$)
- Start of the test by **ABIST_CTRL0** : 00000011_B (03_H) Interrupt (INT) related:
- **IF** : 01001000_B (48_H)
- **INITERR** : 00000000_B (00_H)

[1]) Please mind that for a test of a comparators the corresponding output has to be enabled.

- **SYSFAIL** : 00000000_B (00_H)
- **MONSF1** : 11010000_B ($D0_H$)
- **MONSF2** : 11110001_B ($F1_H$)
- **MONSF3** : 00110000_B (30_H)
- Start of the test by **ABIST_CTRL0** : 00001011_B ($0B_H$)

This type of ABIST can be performed in the following states of the **State Machine**: INIT, WAKE, NORMAL. If this test is run in NORMAL state on comparators contributing to the secondary safety shutdown path the device will switch low the safe state outputs SS1/2 and the **State Machine** will move to WAKE state, without triggering a reset ROT.
It has to be considered that testing the complete monitoring chain till the respective output (SS1/2 or INT) in this way will cover only the first comparator in the sequence, as this one will trigger the output reaction. For further details, please refer to **Chapter 11.6.1.4**.
If this test is run in INIT or WAKE state, contribution to activation of the secondary safety shutdown path cannot be tested. The system is in a safe state already and the secondary safety shutdown path is already activated. In any way the proper behavior of the secondary shutdown p3ath as well as the interrupt signal needs to be checked by the microcontroller.

11.6.1.4 Testing the complete monitoring chain (comparators, deglitching and output)

The testing of the complete monitoring chain from the comparator till the respective output function has to be divided into the two functions available in TLF35584. First the secondary safety shutdown path called SS1/2 for severe microcontroller related failure events and secondly the interrupt function INT for peripheral related failure events in terms of voltage and current monitoring.

11.6.1.4.1 Testing the activation of the secondary safety shutdown path

To test the activation of the secondary safety shutdown path, the device has to be brought into NORMAL state. The µC shall check if the secondary safety shutdown path has been de-activated successfully (SS1/2 high).

Once in NORMAL state a single comparator contributing to the secondary safety shutdown path shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** ($00x0xxxx_B$), **ABIST_SELECT1** ($0000xxx0_B$) or **ABIST_SELECT2** ($xx00000x_B$). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the secondary safety shutdown path. Then a single comparator ABIST operation on the full path of the secondary safety shutdown path needs to be started (register **ABIST_CTRL0**: 00000111_B (07_H)). Upon completion of the requested ABIST operation the device will autonomously move into WAKE state and an interrupt event is generated. The interrupt event will indicate the completion of the ABIST (**IF.ABIST**). Furthermore the respective monitoring failure flag for the selected comparator will be set (either **INITERR.VMONF** for "**Move to INIT State**" failures or **SYSFAIL.VMONF** for "**Move to FAILSAFE State**" failures) which has to be checked and cleared by the microcontroller.

The secondary safety shutdown path shall be activated (SS1/2 low), it is the responsibility of the µC to check the activation of the secondary safety shutdown path. If SS2 delay is enabled, this delay will be applied when the ABIST operation is performed, i.e. the activation of the shutdown path connected to SS2 will be delayed according to the programmed value for failure cases not leading to FAILSAFE.
The µC needs to read and check the status of the requested ABIST operation (**ABIST_CTRL0.STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Furthermore, the microcontroller has to proceed with the following steps to check the safe state control and the safe state outputs:

- Check that the secondary safety shutdown path has been activated successfully (SS1/2 low)

- Enable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
- Select generation of valid toggling signal for the safe state control (set **ABIST_CTRL1**.**ABIST_CLK_EN**)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
- De-select generation of toggling signal for the safe state control (reset **ABIST_CTRL1**.**ABIST_CLK_EN**)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
- Disable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)

Afterwards a test of all comparators which contribute to the activation of the secondary safety shutdown path shall be configured and started according to **Chapter 11.6.1.3**.

11.6.1.4.2 Testing the generation of an interrupt event

The test of the generation of an interrupt event can be done in the states INIT, NORMAL and WAKE state. Even though it is recommended to have the application in safe state (INIT or WAKE state).

For this test first a single comparator contributing to the interrupt function shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** ($xx0x0000_B$), **ABIST_SELECT1** ($xxxx000x_B$) or **ABIST_SELECT2** ($00xx0000_B$). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the interrupt function. Then a single comparator ABIST operation on the full path of the interrupt needs to be started (register **ABIST_CTRL0**: 00001111_B ($0F_H$)). The artificial failure, triggered by the ABIST controller, on the selected comparator will generate an interrupt (INT) event. It is the responsibility of the µC to check the generation of this interrupt event on the triggered failure. As this is a test of the generation of an interrupt based on a failure event, there is no dedicated ABIST completion event, nor the **ABIST** bit in the interrupt flags will be set. Accordingly it is recommended to store the information about the started ABIST in the firmware. After the interrupt has been generated the interrupt flag register shall be checked for the monitoring bit (**IF**.**MON**) set and the ABIST completion bit (**IF**.**ABIST**) not set.

The µC needs to read and check the status of the requested ABIST operation (**ABIST_CTRL0**.**STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Afterwards a test of all comparators which contribute to the interrupt generation shall be configured and started according to **Chapter 11.6.1.3**.

11.6.1.5 Abort conditions for ABIST operation

In case of an severe monitoring failure event (contribution to the secondary safety shutdown path) detected on a not selected comparator[1)] or a severe failure event not related to the voltage or bias current monitoring function during the proceeding of an ABIST operation on the comparators only (**ABIST_CTRL0**.**PATH** not set), the device will react as it is supposed to do in normal operation. Accordingly the monitoring, reset and safe state control are reacting. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.

In case of an ABIST operation on the full path (**ABIST_CTRL0**.**PATH** set) the comparators for voltage and bias current monitoring are blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL state (e.g. test of activation of secondary safety shutdown path described in **Chapter 11.6.1.4.1**). Severe failure events not related to the voltage and bias current

[1]) Please mind that selected comparators might be blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL state (e.g. test of activation of secondary safety shutdown path described in **Chapter 11.6.1.4.1**).

monitoring will trigger the same device reaction as in usual condtion. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.

This ABIST abort will be shown by the TLF35584 in the register **SYSFAIL.ABISTERR**. The artificial failure events, that have been generated until the abort of the ABIST due to the detected real failure, will be stored as well in the monitoring registers.

11.6.2 Logic Built In Self Test

No dedicated Built In Self Test for the digital logic exists in the device. It is therefore assumed that any test which is related to the digital logic is performed by the µC.

The following blocks inside the digital logic can be tested by the µC:

- FWD/WWD
- Error monitoring

In order to verify correct functionality of these blocks and to check their contribution to ROT/INT and finally SS1/2 the µC shall generate an error condition on the particular block and check for the occurrence of the expected system behavior.

- For the watchdog functionality this basically means either stop triggering the WD(s) and/or generate false trigger events. This will either generate and interrupt or even assert the reset. Finally the secondary safety shutdown path will be activated, the µC will be reset and the device will move into INIT state. In order to verify the activation of the secondary shutdown path, this kind of test shall only be executed after the device has been moved into NORMAL state.
- For the error monitoring block, this means that the toggling at the ERR pin needs to be stopped in order to observe the required system behavior. It is up to the µC to make use of the error recovery mechanism or not.

11.7 Microcontroller Programming Support

The TLF35584 offers a microcontroller programming support feature, that can be used to avoid periodic reset triggering due to missing triggering of the window watchdog and error monitoring within the INIT timer. The activation of the microcontroller programming support feature shall be done by pulling the MPS pin to 5 V. The voltage shall be provided earliest with the enabling of the voltage reference. Therefore it would be one option to connect the MPS pin to the output QVR during microcontroller programming.

The active microcontroller programming support feature includes the following changes to the normal operation of the device:

- The INIT timer will be stopped.
- The contribution of the window watchdog failure counter overflow to the reset ROT will be blocked.
- The contribution of the functional watchdog failure counter overflow to the reset ROT will be blocked.
- The contribution of the error monitoring to the reset ROT will be blocked.

As only the contribution of the watchdogs and the error monitoring to the reset function is blocked/disconnected, the state machine and safe state control function are not affected. Accordingly an overflow of the window or functional watchdog failure counter will trigger a “Move to INIT” event, but without issuing a reset of the microcontroller.

The microcontroller programming support feature offers as well the possibility to move the TLF35584 to any other state according to the state machine. E.g. in case MPS pin is high in NORMAL and there is a watchdog error counter overflow the device would move into INIT without issuing a reset.

12 Safe State Control Function

12.1 Introduction

The safe state control monitors safety related signals and controls the safe state signals SS1 and SS2.

The following description summarizes the contributors to the safe state control function and the possibilities to adjust them.

Principle of operation:

The safe state control function monitors the following inputs:

- Result of the Error Monitoring. “Error”-signal at pin ERR is expected to be a toggling signal. A permanent low or high signal will be detected as an error.
- Over and under voltage of the micro processor related regulators (for details please refer to chapter **Monitoring Function**)
- Result of Window Watchdog Failure Counter Threshold Comparator. Whether threshold Σ WWO for “Invalid window watchdog triggering” has been exceeded.
- Result of Functional Watchdog Failure Counter Threshold Comparator: Whether threshold Σ FWO for “Invalid functional watchdog triggering” has been exceeded.
- Thermal shutdown signal (TSD) for relevant events moving the device into FAILSAFE state.
- Internal clock
- SPI state transition request. A valid GoToNORMAL command triggers the signals SS1/2 to switch high in case the other boundary conditions are fulfilled. Moving the device out of NORMAL state by SPI command will switch the signals SS1 and 2 (optionally delayed by t_{SS2}) to low.

The following parameters of the safe state control function are programmable via SPI, this settings can be done during INIT, NORMAL, SLEEP and WAKE state, WWD and FWD configuration and error pin configuration including disabling of individual functionality via protected register (for description of states please refer to chapter **State Machine**):

- Number of invalid watchdog triggers, that lead to activating SS1 and SS2: There are two watchdog trigger failure counters implemented, one for the window watchdog the other for the functional watchdog. Every counter increments by two at every invalid watchdog triggering and decrements by one at every valid watchdog triggering. (valid and invalid triggering is described in chapter functional and window watchdog). An incrementing change is indicated by an interrupt. A decrementing change is not indicated by an interrupt. The thresholds can be programmed by SPI command for each counter individually. This function might be used to test the watchdog function.
- Immediate reaction or recovery delay reaction, only related to input signal ERR: This parameter determines whether the safe state control will immediately react to an error indicated by SMU or react after a certain delay, if the error indication is still present. In recovery delay reaction the safe state control will generate an interrupt and start the programmed recovery delay time. If within this time the error should disappear (means the error signal should toggle again, before the recovery delay time has ended), the safe state control will keep the safe state output SS1/2 high. If within this time the error signal should not disappear and maintain the error indication (means the error signal should not toggle again, before the recovery delay time has ended), the safe state control will activate the safe state signals SS1 and SS2 after the recovery delay time has ended. Immediate reaction means reaction after signal detection delay time.

- Recovery delay time Δt_{REC}, only related to input signal ERR: An error (violation of valid ERR signal) has to be longer than this delay time to lead to activating the safe state signals SS1 and SS2. This delay time is only active if recovery delay time mode was selected.
- Delay time Δt_{SS2} between safe state signal 1 and safe state signal 2

The safe state function offers two output signals, both of them as output stages to drive external switches (additional driver stage is necessary):

- Safe state signal 1 (present at pin SS1)
- Safe state signal 2 (present at pin SS2), it may be delayed to safe state signal 1 by an adjustable delay time Δt_{SS2} (via SPI)

Error signal from microcontroller safety management unit (SMU) at pin ERR:

The error monitoring function requires a toggling signal at pin ERR with a determined timing in case of fault-free operation of the microcontroller by its SMU. This toggling signal is considered as a “being alive” indication. An error should be indicated by a constant low signal. A constant high signal will also be regarded as a failure indication, probably caused by a short circuit. The result is given to the safe state control.

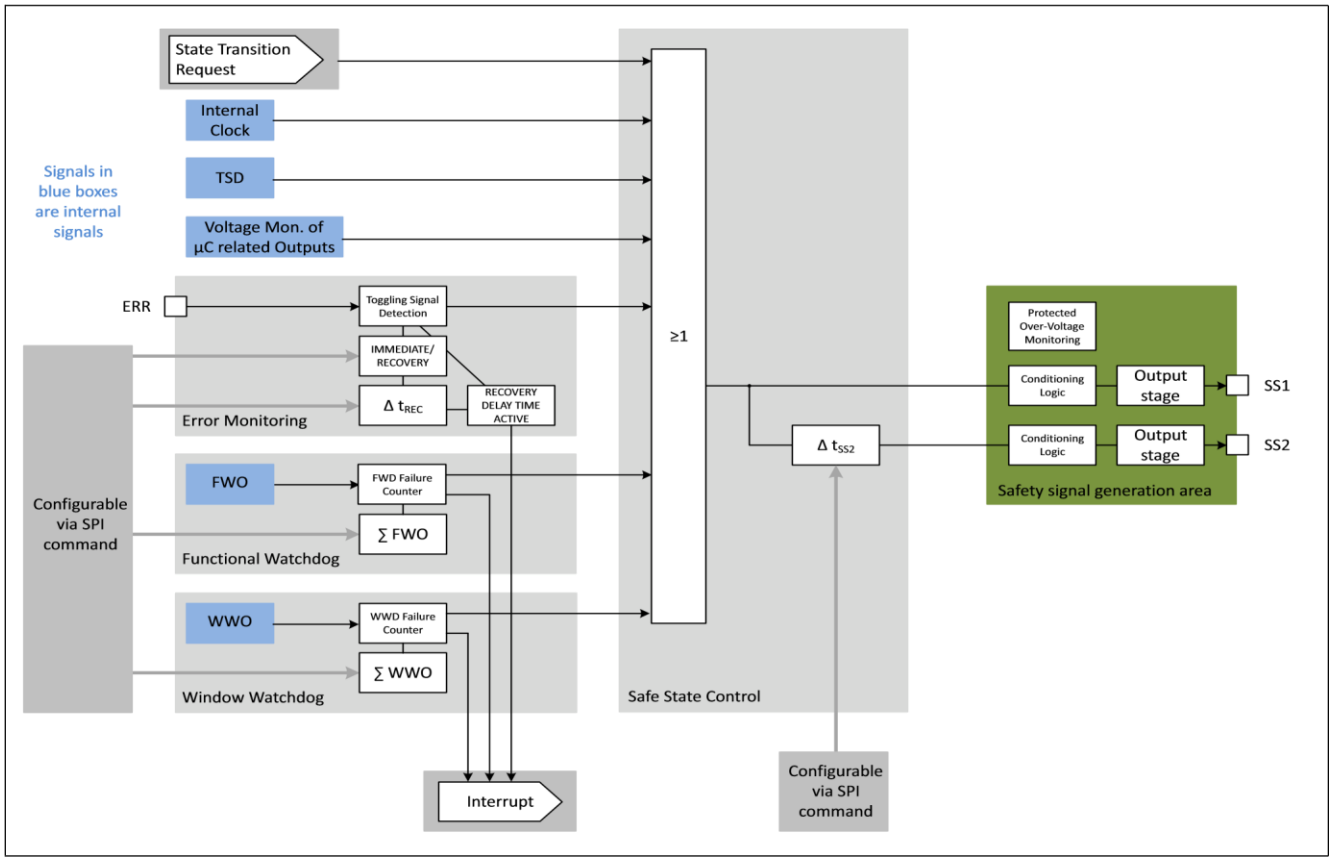


Figure 59 Principle safe state control function

Description:

- State Transition Request= Micro processor can request a de-activation of the Secondary Safety Shutdown path (SS1/2 high) via SPI. Being in NORMAL state the micro processor can activate the Secondary Safety Shutdown path (SS1/2 low) by moving the device out of NORMAL state by SPI.
- ERR = Error pin connected to safety management unit (SMU) of micro processor
- TSD = Thermal shutdown
- ROT = Reset output

- Σ WWO = Number of “Invalid WWD triggering”, after safe state control shall activate the safe state signal SS1 and SS2, located in window watchdog block
- Σ FWO = Number of “Invalid FWD triggering”, after safe state control shall activate the safe state signal SS1 and SS2, locked in functional watchdog block
- IMMEDIATE/RECOVERY = Distinguish between immediate reaction to SMU signal or recovery delay time, located in error monitoring block
- Δt_{REC} = Recovery delay time for SMU signal at pin ERR, located in error monitoring block
- Δt_{SS2} = Delay time between safe state signal 1 and safe state signal 2
- SS1 = Safe state signal 1
- SS2 = Safe state signal 2

12.2 Electrical Characteristics

Table 18 Electrical Characteristics: Safe State Control

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ERR pin							
ERR valid high level	$V_{ERR,hi}$	3.6	–	–	V	V_{ERR} increasing, V_{QUC} = 5.0 V	P_12.2.1
ERR valid low level	$V_{ERR,lo}$	–	–	0.8	V	V_{ERR} decreasing, V_{QUC} = 5.0 V	P_12.2.2
ERR hysteresis	$V_{ERR,hyst}$	–	350	–	mV	V_{QUC} = 5.0 V	P_12.2.3
ERR valid high level	$V_{ERR,hi}$	2.0	–	–	V	V_{ERR} increasing, V_{QUC} = 3.3 V	P_12.2.4
ERR valid low level	$V_{ERR,lo}$	–	–	0.8	V	V_{ERR} decreasing, V_{QUC} = 3.3 V	P_12.2.5
ERR hysteresis	$V_{ERR,hyst}$	–	160	–	mV	V_{QUC} = 3.3 V	P_12.2.6

ERR pull-down current	I_{ERR}	–	150	330	µA	$V_{ERR} = V_{QUC}$	P_12.2.7
ERR input capacitance	C_{ERR}	–	4	15	pF	1)	P_12.2.8
Valid ERR input signal frequency	$f_{ERR,valid}$	10	–	45	kHz	considering a duty cycle of 50%	P_12.2.9
Invalid ERR input signal frequency (low frequency)	$f_{ERR,invalid,LF}$	0	–	5	kHz	considering a duty cycle of 50%	P_12.2.10
Invalid ERR input signal frequency (high frequency)	$f_{ERR,invalid,HF}$	96.2	–	500	kHz	considering a duty cycle of 50%	P_12.2.11
Invalid ERR input signal detection time (low frequency)	$\Delta t_{DET,LF}$	50.1	–	99.9	µs	derived from $f_{ERR,valid}$ and $f_{ERR,invalid,LF}$	P_12.2.12
Invalid ERR input signal detection time (high frequency)	$\Delta t_{DET,HF}$	5.2	–	11.1	µs	derived from $f_{ERR,valid}$ and $f_{ERR,invalid,HF}$	P_12.2.13
ERR reactivation time-out	$t_{ERR,TO}$	9	10	11	ms	after SLEEP	P_12.2.14
ERR reactivation time-out (first edge expected)	$t_{ERR,ren}$	50.1	–	110	µs	after reenabling via SPI 2)	P_12.2.15
Safe state signal 1 pin SS1							
SS1 output, high level TLF35584xxVS1	$V_{SS1,hi}$	3.6	4.8	V_{QUC}	V	$I_{SS1} \geq$ -1 mA; V_{QUC} = 5.0 V	P_12.2.16
SS1 output, high level TLF35584xxVS1	$V_{SS1,hi}$	3.0	4.3	V_{QUC}	V	$I_{SS1} \geq$ -5 mA; V_{QUC} = 5.0 V	P_12.2.17
SS1 output, high level TLF35584xxVS2	$V_{SS1,hi}$	2.9	3.2	V_{QUC}	V	$I_{SS1} \geq$ -1 mA; V_{QUC} = 3.3 V	P_12.2.18

Table 18 Electrical Characteristics: Safe State Control (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SS1 output, high level TLF35584xxVS2	$V_{SS1,hi}$	2.0	2.8	V_{QUC}	V	$I_{SS1} \geq$ -5 mA; V_{QUC} = 3.3 V	P_12.2.19
SS1 pull-down resistor	$R_{SS1,pd}$	70	100	130	kΩ		P_12.2.20
SS1 output, low level	$V_{SS1,lo}$	–	0	0.8	V	3) 4) $R_{SS1,pd} \leq$ 100 kΩ ; $C_{SS1} \geq$ 50 pF ; LDO_µC active ; $V_{QUC} \geq$ 2 V	P_12.2.21
SS1 internal reaction time	$t_{SS1,act}$	–	12	30	µs		P_12.2.22
Safe state signal 2 pin SS2							

SS2 output, high level TLF35584xxVS1	$V_{SS2,hi}$	3.6	4.8	V_{QUC}	V	I_{SS2} ≥ -1 mA; V_{QUC} = 5.0 V	P_12.2.23
SS2 output, high level TLF35584xxVS1	$V_{SS2,hi}$	3.0	4.3	V_{QUC}	V	I_{SS2} ≥ -5 mA; V_{QUC} = 5.0 V	P_12.2.24
SS2 output, high level TLF35584xxVS2	$V_{SS2,hi}$	2.9	3.2	V_{QUC}	V	I_{SS2} ≥ -1 mA; V_{QUC} = 3.3 V	P_12.2.25
SS2 output, high level TLF35584xxVS2	$V_{SS2,hi}$	2.0	2.8	V_{QUC}	V	I_{SS2} ≥ -5 mA; V_{QUC} = 3.3 V	P_12.2.26
SS2 pull-down resistor	$R_{SS2,pd}$	70	100	130	kΩ		P_12.2.27
SS2 output, low level	$V_{SS2,lo}$	–	0	0.8	V	3) 4) $R_{SS2,pd}$ ≤ 100 kΩ ; C_{SS2} ≥ 50 pF ; LDO_µC active ; V_{QUC} ≥ 2 V	P_12.2.28
SS2 internal reaction time	$t_{SS2,act}$	–	12	30	µs		P_12.2.29
Adjustable parameters							
SSC time base accuracy	t_{SSC}	-10	–	10	%	timebase for Δt_{REC} and Δt_{SS2}	P_12.2.30
adjustable recovery delay time	Δt_{REC}	0	–	10	ms	selectable 0, 1.0, 2.5, 5.0 and 10 ms; t_{SSC} to be considered	P_12.2.31
adjustable delay time between SS1 and SS2	Δt_{SS2}	0	–	250	ms	selectable 0, 10,50, 100 and 250 ms; t_{SSC} to be considered	P_12.2.32

1) Specified by design, not subject to production test

2) It is recommended to provide the ERR signal to the ERR pin before activating the function again via SPI.

3) Internal and external pull-down resistors have to be considered for failure cases with QUC being off.

4) Considering loss of analog safety ground (AGS1 and AGS2).

12.3 Reaction On Microprocessor Safety Management Unit (SMU - Pin ERR):

12.3.1 Immediate reaction on ERR monitoring failure

The micro processor safety management unit (SMU) indicates a serious error by stopping the toggling signal at pin ERR, immediate reaction to error signal is set:

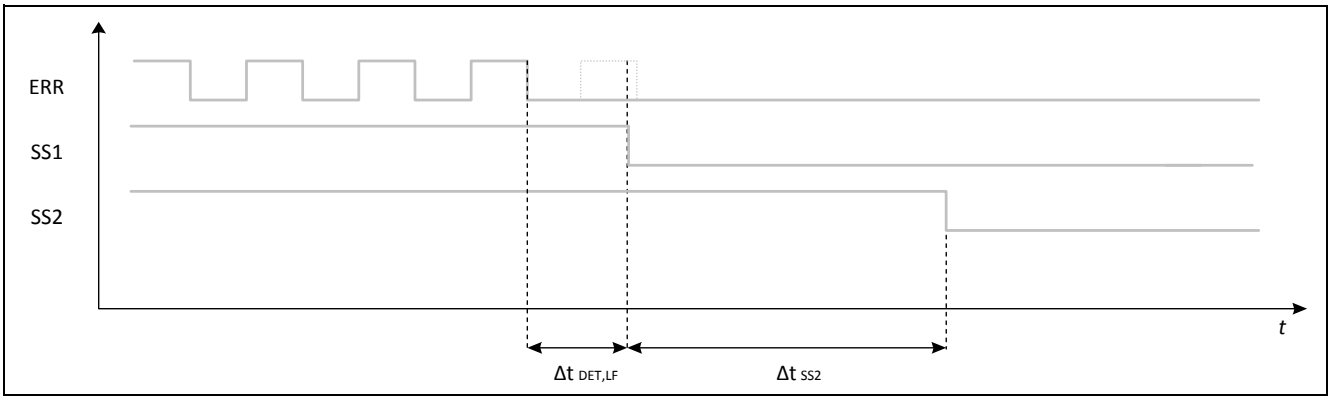


Figure 60 Flow diagram reaction on SMU signal (ERR signal remains low)

Description:

- The ERR signal stops toggling and remains low.
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized falling edge.
- The safe state signal 1 (at pin SS1) is pulled to low
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

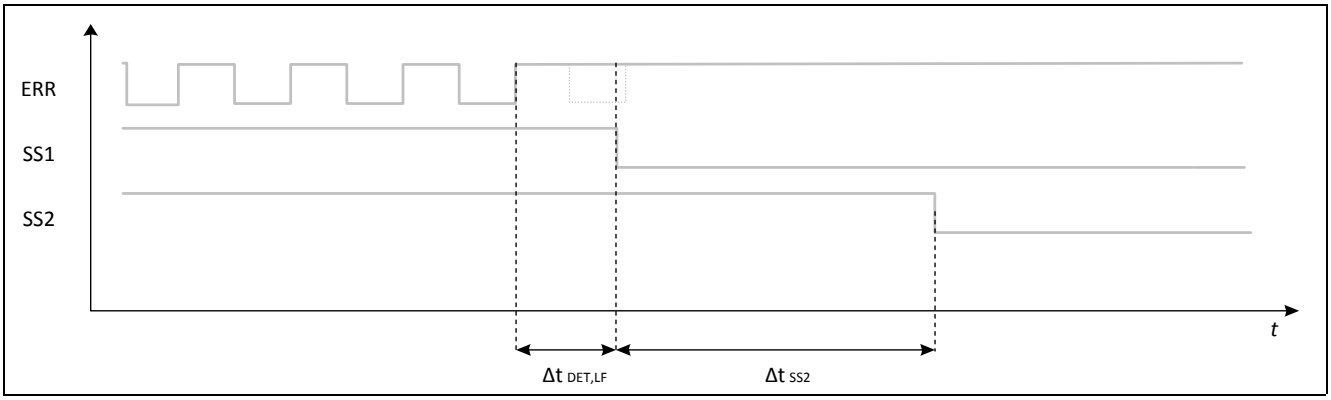


Figure 61 Flow diagram reaction on SMU signal (ERR signal remains high)

Description:

- The ERR signal stops toggling and remains high.
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized rising edge.
- The safe state signal 1 (at pin SS1) is pulled to low
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

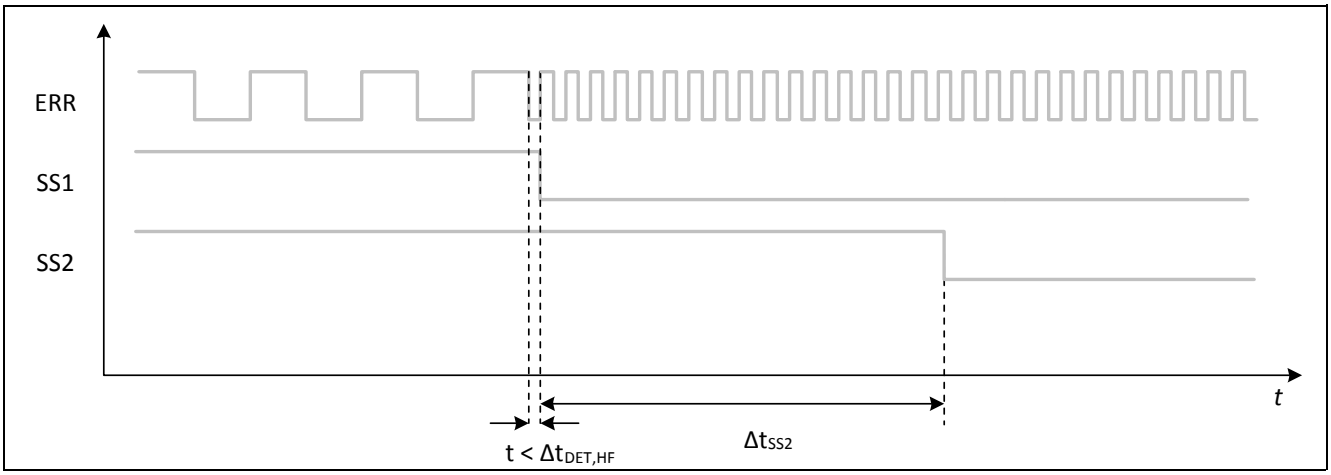


Figure 62 Flow diagram reaction on SMU signal (ERR signal frequency too high)

Description:

- The ERR signal starts toggling with a frequency of $f_{ERR,invalid,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- The safe state signal 1 (at pin SS1) is pulled to low.
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}.

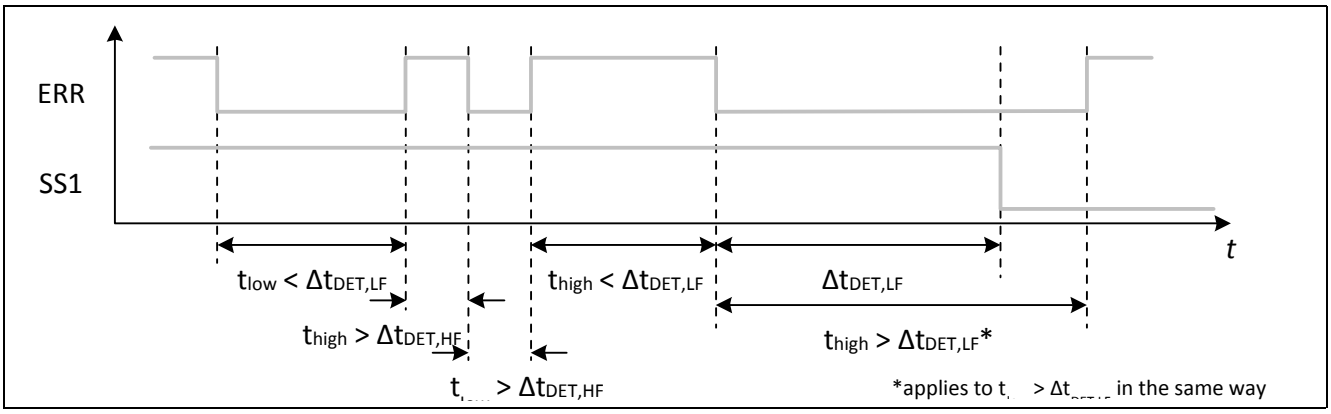


Figure 63 Flow diagram reaction on SMU signal (duty-cycle different than 50%, t_{low} or t_{high} too long)

Description:

- The ERR signal toggles with changing high and low times (duty cycle can vary as well), but t_{low} and t_{high} are in the valid range between $t_{DET,HF}$ and $t_{DET,LF}$ first.
- Then a low pulse of ERR shown in the figure is longer than the detection time $t_{DET,LF}$.
- This is detected as an error as soon as the edge-to-edge time is longer than the detection time $\Delta t_{DET,LF}$.
- The safe state signal 1 (at pin SS1) is pulled to low.
- The safe state signal 2 (at pin SS2) is pulled to low accordingly after an optional delay time Δt_{SS2}.(not in figure)
- The condition can be applied to the high pulse being longer than the detection time $t_{DET,LF}$ in the same way.

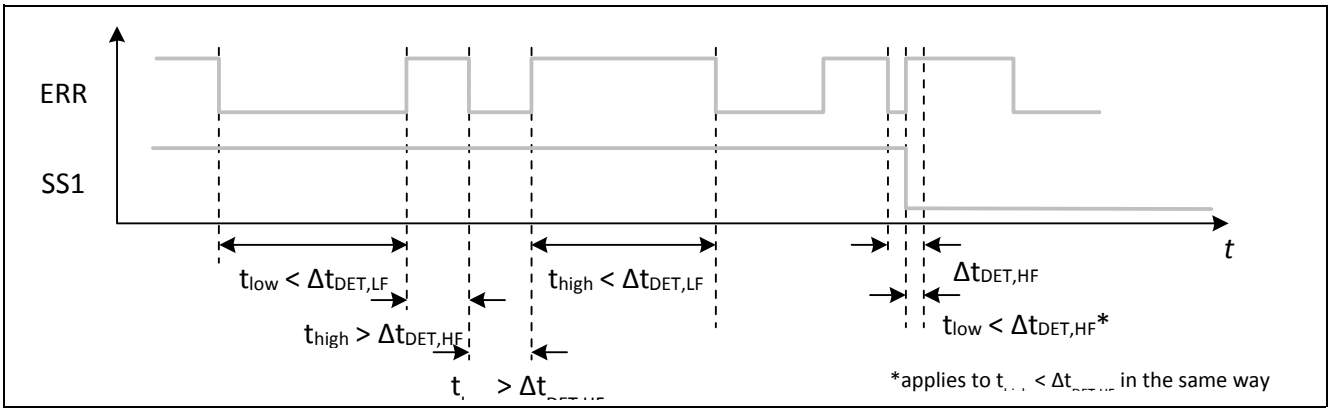


Figure 64 Flow diagram reaction on SMU signal (duty-cycle different than 50%, t_{low} or t_{high} too short)

Description:

- The ERR signal toggles with changing high and low times (duty cycle can vary as well), but t_{low} and t_{high} are in the valid range between $t_{DET,HF}$ and $t_{DET,LF}$ first.
- Then a low pulse of ERR shown in the figure is shorter than the detection time $t_{DET,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- The safe state signal 1 (at pin SS1) is pulled to low.
- The safe state signal 2 (at pin SS2) is pulled to low accordingly after an optional delay time Δt_{SS2}.(not in figure)
- The condition can be applied to the high pulse being shorter than the detection time $t_{DET,HF}$ in the same way.

12.3.2 Recovery delay reaction on ERR monitoring failure

The micro processor safety management unit (SMU) indicates a serious error by stopping the toggling signal at pin ERR, recovery delay time reaction to error signal is set - the SMU is given time to recover:

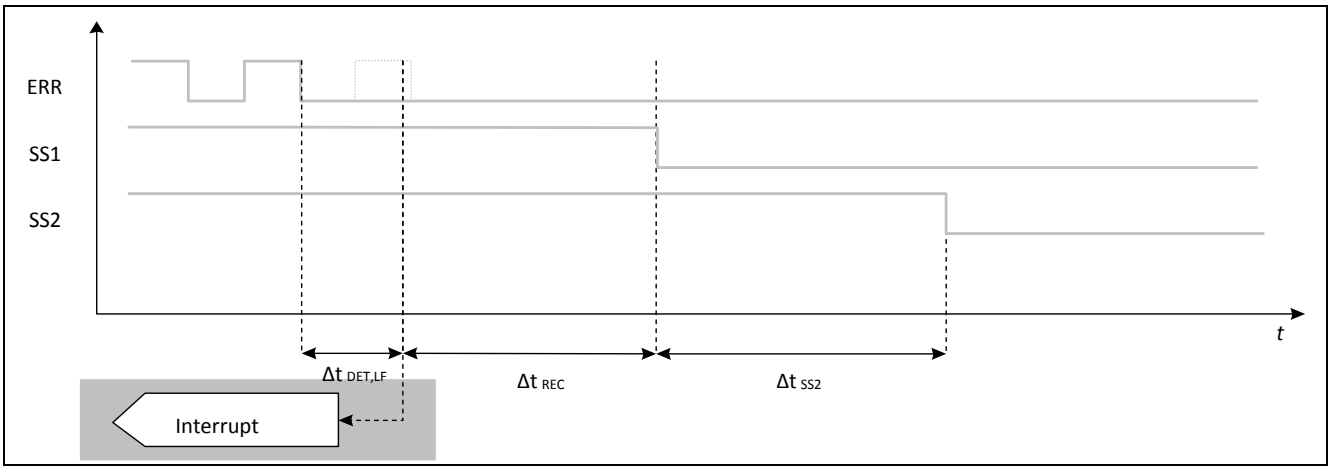


Figure 65 Flow diagram reaction on SMU signal, error longer than recovery delay time

Description:

- The ERR signal stops toggling and remains low (or high).
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized edge.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}

- The safe state signal 1 (at pin SS1) is pulled to low after Δt_{REC} has expired
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

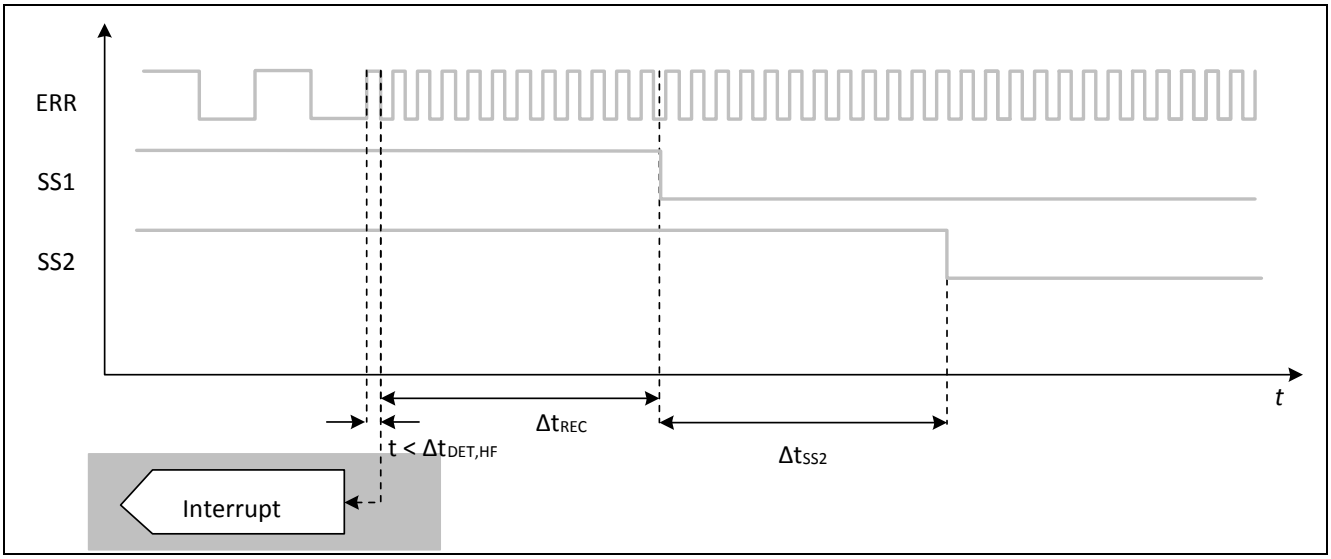


Figure 66 Flow diagram reaction on SMU signal, error longer than recovery delay time (ERR signal frequency too high)

Description:

- The ERR signal starts toggling with a frequency of $f_{ERR,invalid,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}
- The safe state signal 1 (at pin SS1) is pulled to low after Δt_{REC} has expired
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

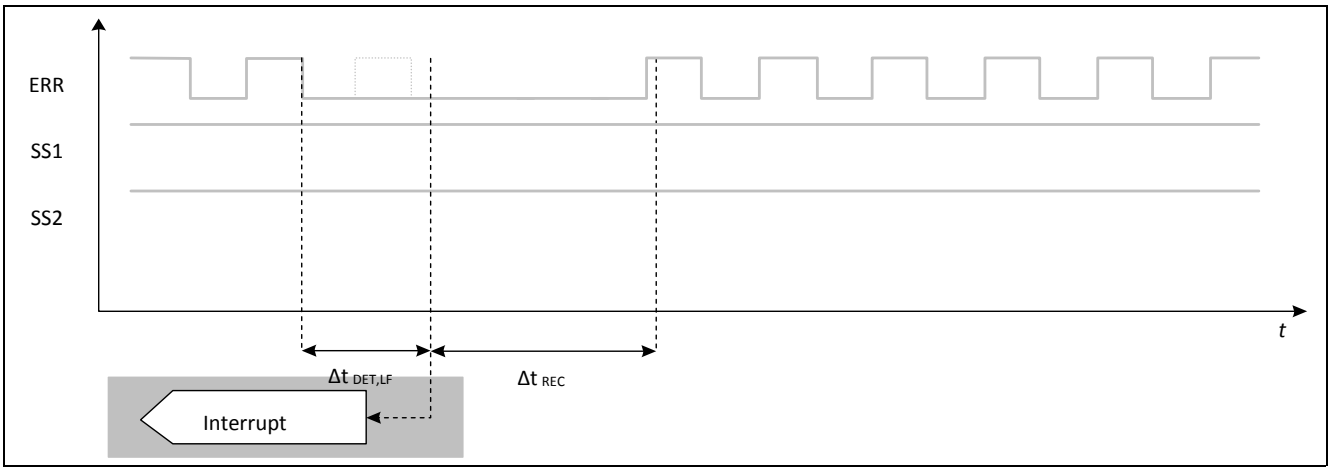


Figure 67 Flow diagram reaction on SMU signal, error shorter than recovery delay time

Description:

- The ERR signal stops toggling and remains low (or high).
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized edge.

- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}
- Before Δt_{REC} has expired the ERR signal resumes toggling.
- The safe state signals 1 (at pin SS1) and 2 (at pin SS2) are kept high all the time.

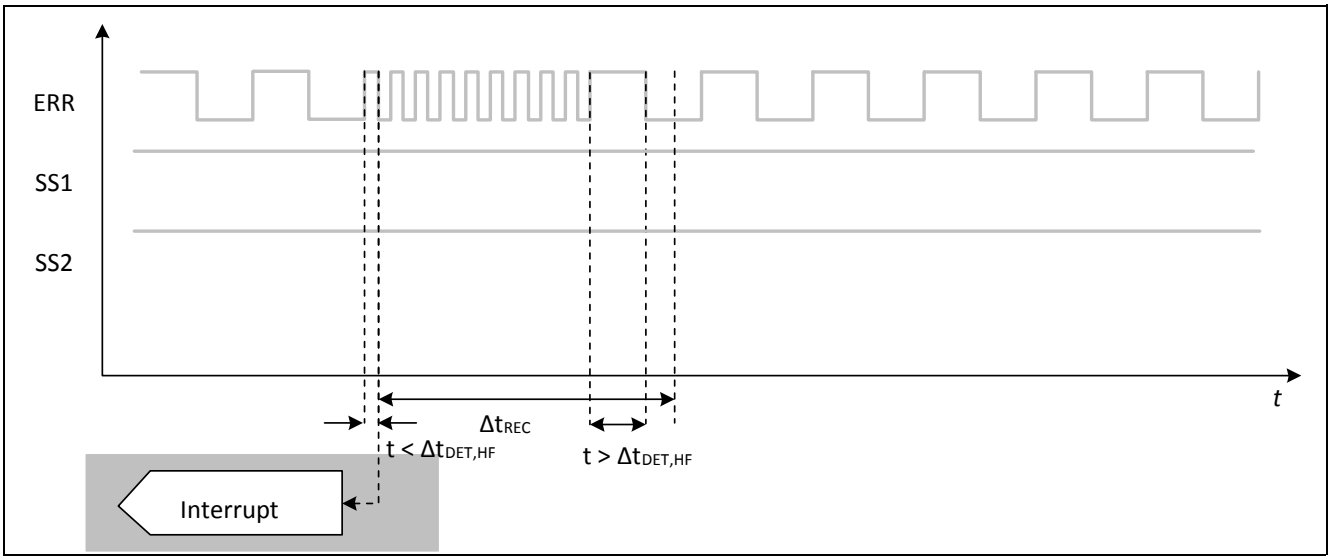


Figure 68 Flow diagram reaction on SMU signal, error shorter than recovery delay time (ERR signal frequency too high)

Description:

- The ERR signal starts toggling with a frequency of $f_{ERR,invalid,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}
- Before Δt_{REC} has expired the ERR signal resumes toggling with a valid frequency.
- The safe state signals 1 (at pin SS1) and 2 (at pin SS2) are kept high all the time.

12.4 Reaction On Error Triggered State Transitions

The reset output (ROT) indicates the behavior of the microcontroller related regulators (for details please refer to chapter voltage monitoring and reset function).

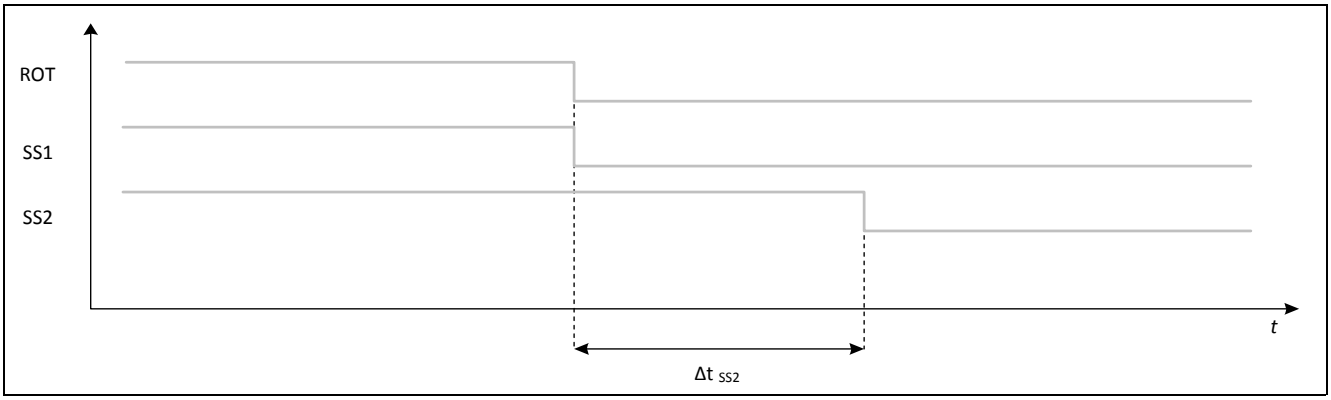


Figure 69 Flow diagram reaction on an error triggered state transition- soft reset

Description:

- The falling edge of ROT signal indicates an error

- Safe state signal 1 (at pin SS1) goes to low immediately with the occurrence of the error
- Safe state signal 2 (at pin SS2) goes to low after a delay time Δt_{SS2} which was set by SPI command
- Please mind that in case of an UV event on QUC, a delayed SS2 signal will follow V_{QUC} as it is supplied from QUC.

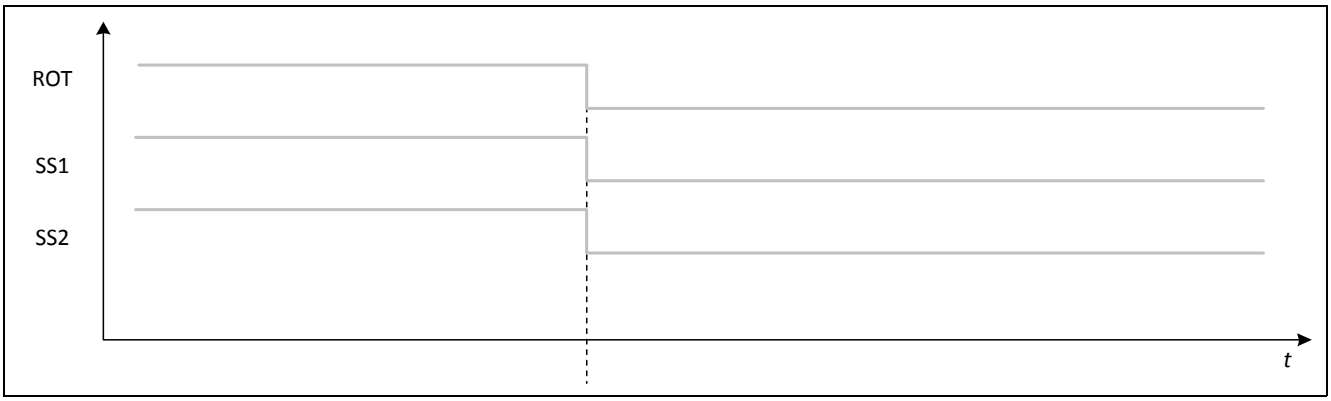


Figure 70 Flow diagram reaction on an error triggered state transitions - hard reset

Description:

- The falling edge of ROT signal indicates an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the occurrence of the error
- Safe state signal 2 (at pin SS2) goes to low together with SS1 as the supplying post regulator LDO_µC is switched off when pin ROT goes to low

12.5 Reaction On Window Watchdog Output (WWO)

The TLF35584 has an implemented window watchdog failure counter (**WWDSTAT.WWDECNT**). The counter increments by two at every invalid window watchdog triggering and decrements by one at every valid window watchdog triggering. (For specification of valid and invalid triggering please refer to chapter functional and window watchdog).

The status of the window watchdog failure counter is written in the so called window watchdog status counter. Any incrementation of the window watchdog status counter is indicated by an interrupt. Any decrementation of the window watchdog status counter is not indicated by an interrupt. The content of the window watchdog status counter cannot be less than zero.

The threshold for activating the safe state signals SS1 and SS2 Σ WWO can be changed in INIT, NORMAL and WAKE state. (**WDCFG0.WWDETHR**)

The content of the status counter will be compared to the programmed threshold Σ WWO (**RWDCFG0.WWDETHR**). If the content of the status counter is equal or higher than Σ WWO, the safe state signals SS1 and SS2 will be activated (low).

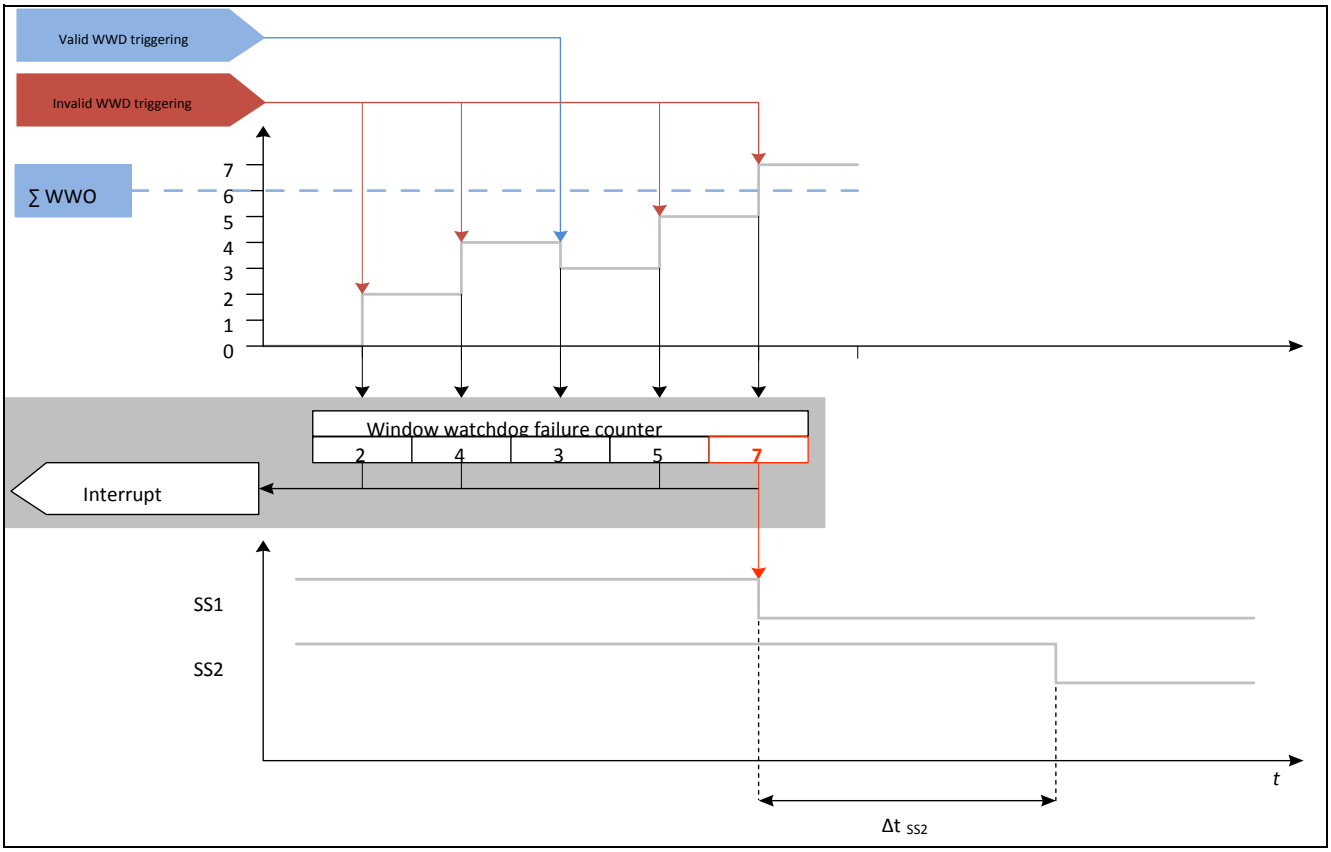


Figure 71 Flow diagram reaction on WWO

Description:

- The threshold Σ WWO is set to 6 (example)
- An invalid watchdog triggering increments the window watchdog status counter by two, this is indicated by an interrupt
- A valid watchdog triggering decrements the window watchdog status counter by one, this is not indicated by an interrupt
- The status counter value 7 is recognized as an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the counter status change
- Safe state signal 2 (at pin SS2) goes to low after a delay time Δt_{SS2} which was set by SPI command

12.6 Reaction On Functional Watchdog Output (FWO)

The TLF35584 has an implemented functional watchdog failure counter (**FWDSTAT1.FWDECNT**). The counter increments by two at every invalid functional watchdog triggering and decrements by one at every valid functional watchdog triggering. (For specification of valid and invalid triggering please refer to chapter functional and window watchdog).

The status of the functional watchdog failure counter is written in the so called functional watchdog status counter. Any incrementation of the functional watchdog status counter is indicated by an interrupt. Any decrementation of the functional watchdog status counter is not indicated by an interrupt. The content of the functional watchdog status counter cannot be less than zero.

The threshold for activating the safe state signals SS1 and SS2 Σ FWO can be changed in INIT, NORMAL and WAKE state. (**WDCFG1.FWDETHR**)

The content of the status counter will be compared to the programmed threshold Σ FWO (**RWDCFG1.FWDETHR**). If the content of the status counter is equal or higher than Σ FWO, the safe state signals SS1 and SS2will be activated (low).

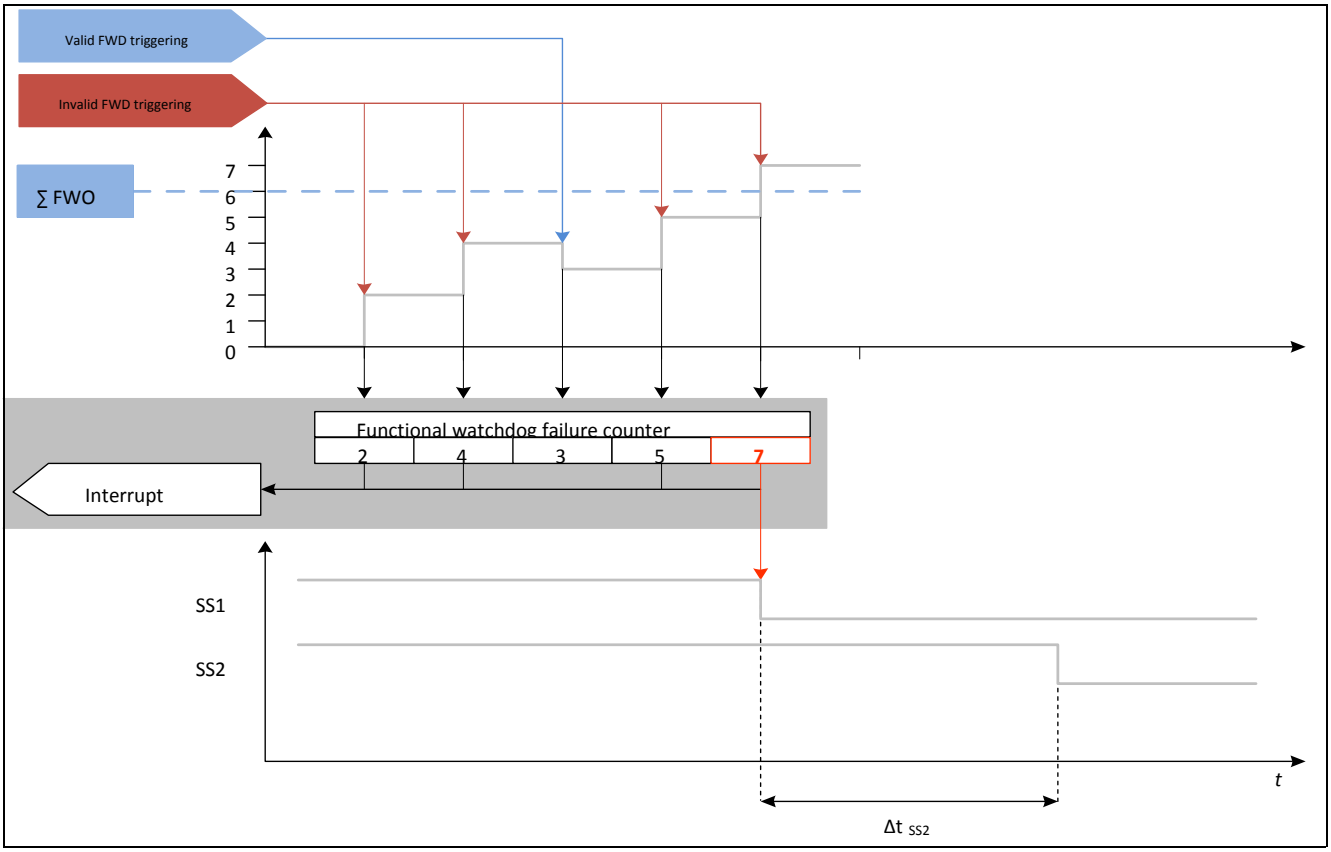


Figure 72 Flow diagram reaction on FWO

Description:

- The threshold Σ FWO is set to 6 (example)
- An invalid watchdog triggering increments the functional watchdog status counter by two, this is indicated by an interrupt
- A valid watchdog triggering decrements the functional watchdog status counter by one, this is not indicated by an interrupt
- The status counter value 7 is recognized as an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the counter status change
- Safe state signal 2 (at pin SS2) goes to low after a delay time Δt_{SS2} which was set by SPI command

12.7 Reaction On Thermal Shutdown (TSD)

The thermal shutdown (TSD) indicates temperature overstress: on the chip: As a consequence all pre and post regulators will be shut down immediately.

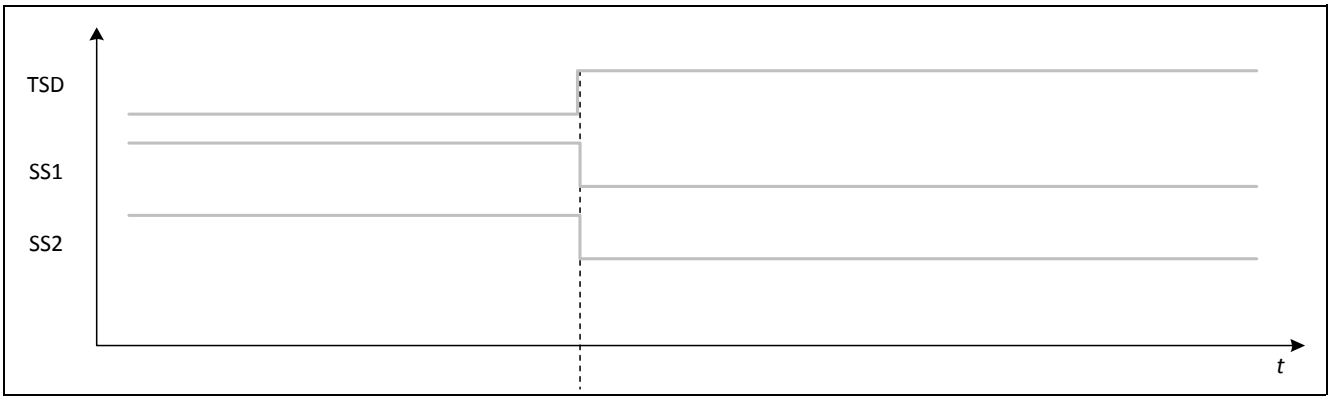


Figure73 Flow diagram reaction on TSD

Description:

- The rising edge of TSD signal (internal) is recognized as an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the rising edge of TSD
- Safe state signal 2 (at pin SS2) goes to low together with SS1 as the supplying post regulator LDO_µC is switched off when pin ROT goes to low

13 SPI - Serial Peripheral Interface

13.1 Introduction

Main functions

The serial peripheral interface bus or SPI bus is a synchronous serial data link that operates in full duplex mode. The TLF35584 communicates in slave mode where the master (µC) initiates the data frame. The TLF35584 should be addressed via a dedicated chip select line. This allows a connection of other slave devices to the SPI bus.

Data transmission

To begin a communication, the µC first configures the clock, using a frequency less than or equal to the maximum frequency the TLF35584 supports. The µC pulls down the chip select for the TLF35584.

Functional description

SPI basic access: All data on MOSI (pin SDI) is captured on the rising edge of SPI clock signal (pin SCL) and shifted on the falling edge of SPI clock signal (pin SCL). The same methodology needs to be applied in the SPI master for MISO (SDO). A read operation has to start with CMD-bit being 1’b0 and a write operation has to start with CMD-bit being 1’b1.

In case of a write operation is performed the written command to SDI is looped back to SDO.

The parity is calculated for the output data stream in case a read operation is performed. The data for the calculation consists of 1’b1, status [5:0] and rd_data[7:0]. The parity bit is set to ‘1’ if the number of ‘1’ in the output data stream is odd, i.e.XOR function between all 15 bits to send out.

Parity is checked on write data. The parity is calculated on the incoming bit stream for the cmd bit, the six address bits and the eight data bits.

Configuration via SPI can be done anytime, if the state machine (FSM) is in INIT state, NORMAL state, WAKE state or SLEEP state. During SLEEP state the SPI has a decreased maximum clock frequency, for details please refer to **Table 19**.

SPI access timing can be found in the following diagram:

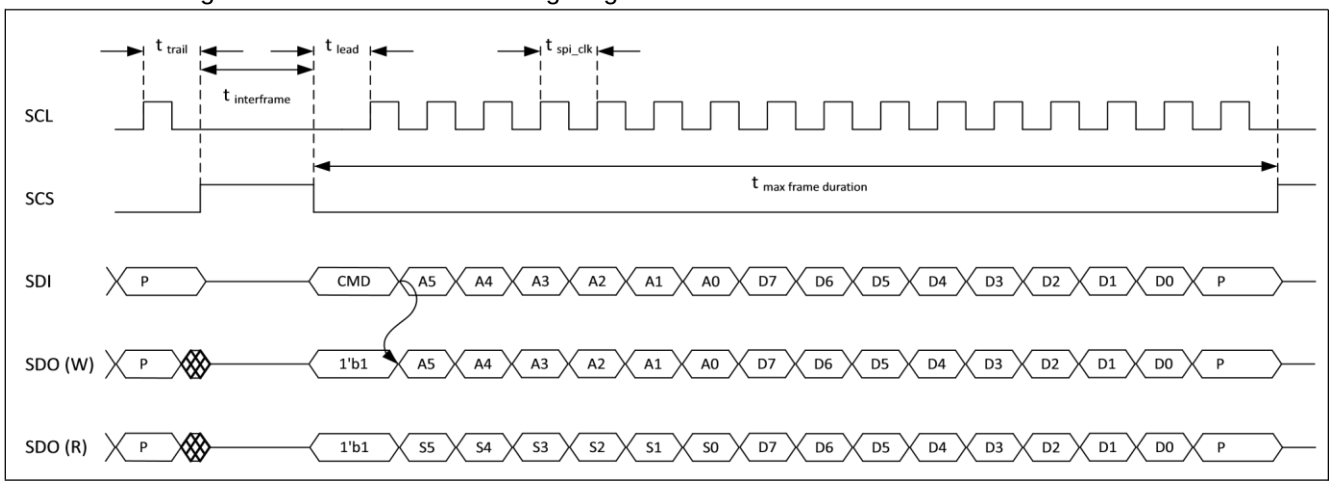


Figure 74 SPI - frame in normal mode

SPI MISO:

- During write, data from MOSI is directly looped back, during read, the addressed register content will be provided in the very same SPI frame
- The cmd bit is always set to 1’b1. All other status bits are set to zero.

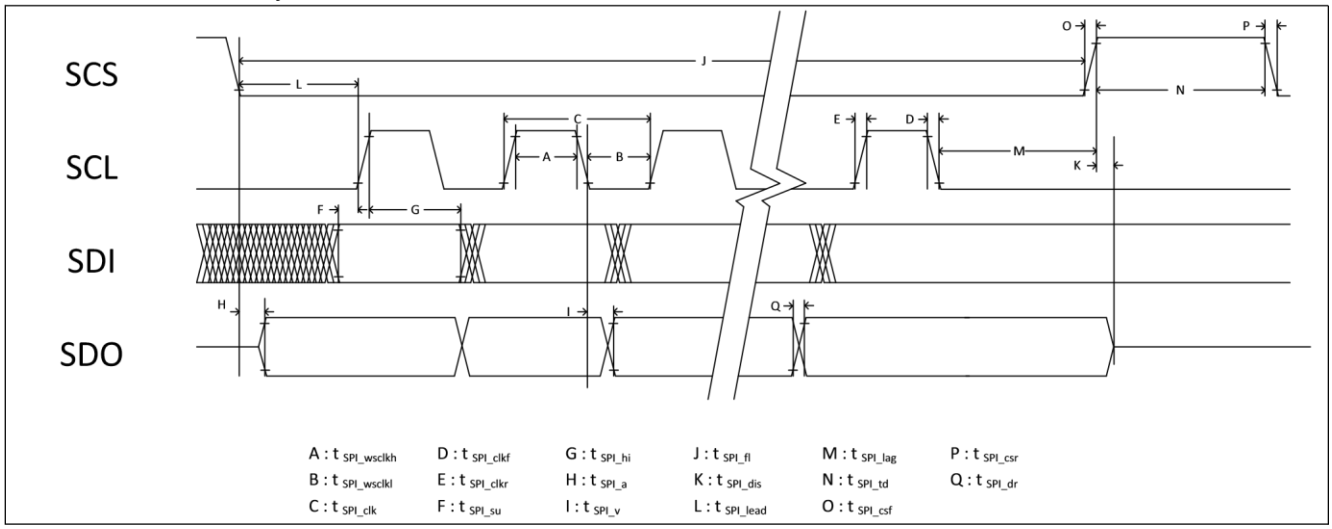


Figure 75 SPI - Timings

Table 19 Electrical Characteristics: SPI - Timings

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
CLK_SPI Operating Frequency	f_{SPI_clk}	–	–	10	MHz	1)	P_13.1.1
CLK_SPI Operating Frequency	f_{SPI_clk}	–	–	1.5	MHz	SLEEP state	P_13.1.2
CLK Signal duty cycle	D_{SCL}	45	50	55	%		P_13.1.3
CLK_SPI Operating Period	t_{SPI_clk}	100	–	–	ns		P_13.1.4
CLK_SPI High Time	t_{SPI_wsclkh}	45	–	–	ns		P_13.1.5
CLK_SPI Low Time	t_{SPI_wsclkl}	45	–	–	ns		P_13.1.6
CLK_SPI Fall Time	t_{SPI_clkf}	–	–	0.1*t_{SPI_fact}	[ns]	$t_{SPI\_fact} \leq t_{SPI\_clk}$; 100 ns ≤ t_{SPI_fact} ≤ 1 µs	P_13.1.7
CLK_SPI Rise Time	t_{SPI_clkr}	–	–	0.1*t_{SPI_fact}	[ns]	$t_{SPI\_fact} \leq t_{SPI\_clk}$; 100 ns ≤ t_{SPI_fact} ≤ 1 µs	P_13.1.8
CLK_SPI Lead Time	t_{SPI_lead}	100	–	–	ns		P_13.1.9

CLK_SPI Lag Time	t_{SPI_lag}	50	–	–	ns		P_13.1.10
SPI Chip Select (SCS) Rise Time	t_{SPI_csr}	–	–	0.2*t_{SPI_fact}	[ns]	$t_{SPI\_fact} \leq t_{SPI\_lag}$; 50 ns ≤ t_{SPI_fact} ≤ 500 ns	P_13.1.11

Table 19 Electrical Characteristics: SPI - Timings (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SPI Chip Select (SCS) Fall Time	t_{SPI_csf}	–	–	0.2*t_{SPI_fact}	[ns]	$t_{SPI\_fact} \leq t_{SPI\_lead}$; 100 ns ≤ t_{SPI_fact} ≤ 1 µs	P_13.1.12
SPI Data Input (SDI) Setup	t_{SPI_su}	10	–	–	ns		P_13.1.13
SPI Data Input (SDI) Hold Time	t_{SPI_hi}	10	–	–	ns		P_13.1.14
SPI Data Output (SDO) Valid after CLK_SPI	t_{SPI_v}	–	–	(0.1*t_{SPI_fact}) +36	[ns]	$C_{SDO,load}$= 50 pF; $t_{SPI\_fact} \geq t_{SPI\_clkf}$; 10 ns ≤ t_{SPI_fact} ≤ 100 ns	P_13.1.15
SPI Write Propagation Delay SDI to SDO	t_{SPI_wpd}	–	–	35	ns		P_13.1.16
SPI Data Output (SDO) Access	t_{SPI_a}	–	–	50	ns	$C_{SDO,load}$ = 50 pF	P_13.1.17
SPI Data Output (SDO) Disable Time	t_{SPI_dis}		–	100	ns	$C_{SDO,load}$ = 50 pF	P_13.1.18
Sequential Transfer Delay	t_{SPI_td}	350	–	–	ns		P_13.1.19
Sequential Transfer Delay	t_{SPI_td}	2	–	–	µs	SLEEP state	P_13.1.20
Frame duration (SCS low)	t_{SPI_fl}		–	1.85	ms		P_13.1.21

1) For max. achievable CLK_SPI operating frequency, please consider the CLK_SPI rise- and fall times (t_{SPI_clkr} and t_{SPI_clkf}).

SPI errors:

- Wrong parity bit during write, write data is ignored.
- Write to invalid address, write data is ignored.

- Wrong number of SPI clock cycles while SCS is low, write data is ignored, read data is provided by the device with each SPI clock cycle.
- Read from invalid address (all data bits zero returned on MISO for read data). For this case the parity bit is inverted/corrupted after complete calculation by the device.
- Invalid frame duration, write data is ignored and the output driver for SDO is turned off internally by the device after t_{SPI_fl}. Read data is provided with each SPI clock cycle as long as SCS is low for less than t_{SPI_fl}.
- If the number of SPI clock cycles is different than 16 and an invalid frame duration error is detected by the device, the invalid frame duration status flag is set and the wrong number of SPI clock cycle status flag is set.

In case of an SPI error occurs, an interrupt will be generated.

Interrupts on SPI errors are initiated only after SCS has been driven high or the frame time-out occurred.

13.2 SPI Write Access To Protected Registers

Certain internal registers (**SYSPCFG0**, **SYSPCFG1**, **WDCFG0**, **WDCFG1**, **FWDCFG**, **WWDCFG0**, **WWDCFG1**) need to be protected against being overwritten accidently. The status of the protection can be checked by reading the **LOCK** bit in the register **PROTSTAT**.

Write access to these registers is only possible after a dedicated 32 bit UNLOCK sequence has been sent via SPI. The four bytes need to be send without any other SPI write access in between. Error in doing so will reset the sequence detection, i.e. a new UNLOCK sequence has to be send. An interrupt is generated and the number of successfully detected UNLOCK sequence bytes is set to zero if a write access to any other register then **PROTCFG** is detected in between. The access to the protected registers is possible in INIT, NORMAL and WAKE state.

The UNLOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xAB; 2:0xEF; 3:0x56; 4:0x12) which have to be sent with no other SPI write access in between. The correctness of every written byte can be checked by reading the register **PROTSTAT**. Once the UNLOCK sequence has been performed successfully, any protected configuration request register can be written. In order to ensure proper writing to the protected configuration request registers the microcontroller shall read back the register values and verify the correctness by checking data. The data bits written to the protected configuration request registers are send back inverted during read operation, that means the microcontroller can calculate an XOR of the register data read and expected. The results should be 0xFF in case of correct register data. The TLF35584 will not check the correctness of the values in the register.

All protected configuration request register values are captured by the respective functions only after a successful LOCK sequence has been performed. A successful LOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xDF; 2:0x34; 3:0xBE; 4:0xCA) which have to be send with no other SPI write access in between. The correctness of every written byte can be checked by reading the register **PROTSTAT**.

Error in doing so will reset the sequence detection, i.e. a new LOCK sequence has to be sent. In this case (any SPI write access in between LOCK sequence) an interrupt is generated.

Upon detection of a successful LOCK sequence the configuration registers and all internal functions are updated with the values from the protected configuration request registers. It is the responsibility of the uC to ensure all registers are configured properly by either writing a new value into a particular register or by reading back a register which is supposed to be unchanged. Partial reconfiguration of the protected registers, i.e. configuring just a single function and leaving other functions unchanged is not supported as with the successful LOCK sequence all protected configuration request registers are taken over into the configuration (**RSYSPCFG0**, **RSYSPCFG1**, **RWDCFG0**, **RWDCFG1**, **RFWDCFG**, **RWWDCFG0**, **RWWDCFG1**).

After the LOCK sequence an internal configuration time of max. 60 µs has to be considered to ensure that the new configuration is taken over.

Affected functions:

- All watchdog configuration registers for WWD and FWD.

- Enabling of WD while the device is in SLEEP state
- All Error pin monitoring configuration registers
- Enabling of Error pin monitoring while the FSM is in SLEEP
- A dedicated register to enable or disable the STDBY LDO
- Configuration of SS2 delay time failure events not leading to FAILSAFE state Read access to any protected configuration request register is always possible.

13.3 SPI Write Initiated State Transition Request And Regulator Configuration

A State machine transition can be initiated via SPI command(s). In case the state of any selectable voltage source (post regular) is expected to change for the next state, this information has to be sent together with the command into the same register. In case the setting for a particular voltage source (post regulator) is supposed to change but the state needs to be unchanged, the same approach can be applied. This basically means, the SPI command contains the current state of the FSM but a different setting for configurable voltage source (post regulator).

In order to request a state transition and/or a change of the LDO configuration the request data have to be written to two separated registers **DEVCTRL** and **DEVCTRLN** after each other consequently. The data written to DEVCTRLN have to be inverted bitwise compared to the data written to DEVCTRL. The request will be only accepted when the two registers are written consecutively after each other (first **DEVCTRL** and second **DEVCTRLN**) and will be taken over with the rising edge of the CS at the end of the second command.
In case of an invalid request (wrong sequence or DEVCTRLN not inverted to DEVCTRL) it will be rejected, an interrupt is generated and the corresponding status flag (**NO_OP**) is set. Incase of an invalid state transition request according to the **State Machine** in **Chapter 11** the request is ignored without issuing an interrupt.

13.4 Registers Description

Table 20 Abbreviations

*R0)	Registers that are being reset only in case of a POR.
*R1)	Registers that are being reset only in case of STANDBY and a POR.
*R2)	Registers that are being reset only in case of FAILSAFE, STANDBY and a POR.
*R3)	Registers that are being reset in case of “Move to INIT” event, FAILSAFE, STANDBY and a POR.
r	Bits that are readable (read)
rw	Bits that are readable and writable (read-write)
rwp	Bits that are readable and writable but protected by register PROTCFG (read-writeprotected)

rw1c	Bits that are readable and to clear the bit you have to write a 1 to it. (read-write-1-to-clear). Flag-bits are updated based on the occurred condition.
rwhc	Bits that are readable and writable after writing the operation is triggered, once this is done successfully the bit is cleared by hardware. (read-write-hardware-cleared)
rwhu	Bits that are readable and writable, after the operation the bit is updated by hardware. (readwrite-hardware-updated)

Module	Base Address	End Address	Note
BusInterface	0_H	$3F_H$	Slave interface

Table 21 Register Address Space

Table 22 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
DEVCFG0	Device configuration 0 *R2)	00_H	08_H
DEVCFG1	Device configuration 1 *R0)	01_H	06_H
DEVCFG2	Device configuration 2 *R2)	02_H	00_H
PROTCFG	Protection register *R2)	03_H	00_H
SYSPCFG0	Protected System configuration request 0 *R1)	04_H	01_H
SYSPCFG1	Protected System configuration request 1 *R2)	05_H	00_H
WDCFG0	Protected Watchdog configuration request 0 *R2)	06_H	$9B_H$
WDCFG1	Protected Watchdog configuration request 1 *R2)	07_H	09_H
FWDCFG	Protected Functional watchdog configuration request *R2)	08_H	$0B_H$
WWDCFG0	Protected Window watchdog configuration request 0 *R2)	09_H	06_H
WWDCFG1	Protected Window watchdog configuration request 1 *R2)	$0A_H$	$0B_H$
RSYSPCFG0	System configuration 0 status *R0)	$0B_H$	01_H
RSYSPCFG1	System configuration 1 status *R3) [1)]	$0C_H$	00_H
RWDCFG0	Watchdog configuration 0 status *R3)	$0D_H$	$9B_H$

Table 22 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
RWDCFG1	Watchdog configuration 1 status *R3)	$0E_H$	09_H
RFWDCFG	Functional watchdog configuration status *R3)	$0F_H$	$0B_H$

RWWDCFG0	Window watchdog configuration 0 status *R3)	10_H	06_H
RWWDCFG1	Window watchdog configuration 1 status *R3)	11_H	09_H
WKTIMCFG0	Wake timer configuration 0 *R2)	12_H	00_H
WKTIMCFG1	Wake timer configuration 1 *R2)	13_H	00_H
WKTIMCFG2	Wake timer configuration 2 *R2)	14_H	00_H
DEVCTRL	Device control request *R2)	15_H	00_H
DEVCTRLN	Device control inverted request *R2)	16_H	00_H
WWDSCMD	Window watchdog service command *R2)	17_H	00_H
FWDRSP	Functional watchdog response command *R2)	18_H	00_H
FWDRSPSYNC	Functional watchdog response command with synchronization *R2)	19_H	00_H
SYSFAIL	Failure status flags *R1)	$1A_H$	00_H
INITERR	Init error status flags *R2)	$1B_H$	00_H
IF	Interrupt flags *R2)	$1C_H$	00_H
SYSSF	System status flags *R2)	$1D_H$	00_H
WKSF	Wakeup status flags *R2)	$1E_H$	00_H
SPISF	SPI status flags *R2)	$1F_H$	00_H
MONSF0	Monitor status flags 0 *R1)	20_H	00_H
MONSF1	Monitor status flags 1 *R1)	21_H	00_H
MONSF2	Monitor status flags 2 *R2)	22_H	00_H
MONSF3	Monitor status flags 3 *R1)	23_H	00_H
OTFAIL	Over temperature failure status flags *R1)	24_H	00_H
OTWRNSF	Over temperature warning status flags *R2)	25_H	00_H
VMONSTAT	Voltage monitor status *R2)	26_H	00_H
DEVSTAT	Device status *R2)	27_H	00_H
PROTSTAT	Protection status *R1)	28_H	01_H
WWDSTAT	Window watchdog status *R3)	29_H	00_H
FWDSTAT0	Functional watchdog status 0 *R3)	$2A_H$	30_H
FWDSTAT1	Functional watchdog status 1 *R3)	$2B_H$	00_H
ABIST_CTRL0	ABIST control0 *R2) [1)]	$2C_H$	00_H
ABIST_CTRL1	ABIST control1 *R2)	$2D_H$	00_H
ABIST_SELECT0	ABIST select 0 *R2)	$2E_H$	00_H
ABIST_SELECT1	ABIST select 1 *R2)	$2F_H$	00_H
ABIST_SELECT2	ABIST select 2 *R2)	30_H	00_H
GTM	Global testmode *R2)	$3F_H$	02_H
BCK_FREQ_CHANGE	Buck switching frequency change *R2)	31_H	00_H

Table 22 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
BCK_FRE_SPREAD	Buck Frequency spread *R2)	32_H	00_H

BCK_MAIN_CTRL	Buck main control *R2)	33_H	00_H

1) Reset class of single bits is different. See register for details.

The registers are addressed wordwise.

13.4.1 Device registers

Device configuration 0 *R2)

DEVCFG0	Offset	Reset Value
Device configuration 0 *R2)	**00_H**	**08_H**

7	6	5	4	3	2	1	0
WKTIMEN	WKTIMCYC	nu		TRDEL			
rw		rwrw					

Field	Bits	Type	Description
WKTIMEN	7	rw	**Wake timer enable** 0_D Wake timer disabled 1_D Wake timer enabled in SLEEP or STANDBY state Reset: 0_H
WKTIMCYC	6	rw	**Wake timer cycle period** 0_D 10 us 1_D 10 ms Reset: 0_H
nu	5:4	none	Reset: 0_H
TRDEL	3:0	rw	**Transition delay into low power states** For STANDBY and SLEEP transition. Defined as a step of 100 us. 0_D 100 us 1_D 200 us 2_D 300 us ..$_D$ ... 15_D 1600 us Reset: 8_H

	Offset	Reset Value
Device configuration 1 *R0)		

DEVCFG1

Device configuration 1 *R0)	**01_H**	**06_H**

7	6	5	4	3	2	1	0
nu						RESDEL	
						rw	

Field	Bits	Type	Description
nu	7:3	none	Reset: 00_H
RESDEL	2:0	rw	**Reset release delay time** 0_D 200 us 1_D 400 us 2_D 800 us 3_D 1ms 4_D 2 ms 5_D 4 ms 6_D 10 ms 7_D 15 ms Reset: 6_H

Device configuration 2 *R2)

DEVCFG2

Device configuration 2 *R2)	**02_H**	**00_H**

7	6	5	4	3	2	1	0
EVCEN	STU	FRE	CMONEN	CTHR		ESYNPHA	ESYNEN
r	r	r	rw	rw		rw	rw

Field	Bits	Type	Description

			Offset	Reset Value
EVCEN	7	r	**External core supply enable status** 0_D External core supply disabled 1_D External core supply enabled Reset: 0_H	
STU	6	r	**Step-up converter enable status** 0_D Disabled 1_D Enabled Reset: 0_H	
FRE	5	r	**Step-down converter frequency selection status** 0_D Step-down converter runs on low frequency range 1_D Step-down converter runs on high frequency range Reset: 0_H	
CMONEN	4	rw	**QUC current monitor enable for transition to a low power state** For STANDBY and SLEEP transition. The setting is overwritten in SLEEP as current monitoring is always enabled. 0_D Disabled 1_D Enabled Reset: 0_H	
CTHR	3:2	rw	**QUC current monitoring threshold value** 0_D 10 mA 1_D 30 mA 2_D 60 mA 3_D 100 mA Reset: 0_H	
ESYNPHA	1	rw	**External synchronization output phase** 0_D No phase shift 1_D 180 phase shift Reset: 0_H	
ESYNEN	0	rw	**Synchronization output for external switchmode regulator enable** 0_D Disable 1_D Enable Reset: 0_H	

Protection register *R2)

PROTCFG

Protection register *R2) **03_H** **00_H**

7	6	5	4	3	2	1	0

Offset	Reset Value

KEY
rw

Field	Bits	Type	Description
KEY	7:0	rw	**Protection key** Protection key register to request write access to protected registers. Unlock: write 32-bit sequence of 4 consecutive bytes (1: 0xAB 2:0xEF 3:0x56 4:0x12) to unlock access to protected registers. Lock: write 32-bit sequence of 4 consecutive bytes (1: 0xDF 2:0x34 3:0xBE 4:0xCA) to lock access to protected registers. All configured values are applied to SSC and WD module after the lock. AB_H Key 1 to unlock protected registers. EF_H Key 2 to unlock protected registers. 56_H Key 3 to unlock protected registers. 12_H Key 4 to unlock protected registers. DF_H Key 1 to lock protected registers. 34_H Key 2 to lock protected registers. BE_H Key 3 to lock protected registers. CA_H Key 4 to lock protected registers. Reset: 00_H

Protected System configuration request 0 *R1)

SYSPCFG0

Protected System configuration request 0 *R1) **04_H** **01_H**

7	6	5	4	3	2	1	0
nu							STBYEN

Field	Bits	Type	Description
nu	7:1	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 00_H

	Offset		Reset Value
STBYEN	0	rwp	**Request standby regulator QST enable** Valid for all device states except FAILSAFE. 0_D Disabled 1_D Enabled Reset: 1_H
			rwp

Offset **Reset Value**

Protected System configuration request 1 *R2)

SYSPCFG1

Protected System configuration request 1 *R2) **05_H** **08_H**

7	6	5	4	3	2	1	0
SS2DEL			ERRSLPEN	ERREN	ERRRECEN	ERRREC	
rwp			rwp	rwp	rwp	rwp	

Field	Bits	Type	Description
SS2DEL	7:5	rwp	**Request safe state 2 delay** Applied for transitions from NORMAL to INIT, WAKE and SLEEP state. 0_D no delay 1_D 10 ms 2_D 50 ms 3_D 100 ms 4_D 250 ms Rese :: 0_H
ERRSLPEN	4	rwp	**Request ERR pin monitor functionality enable while the system is in SLEEP** 0_D ERR pin monitor is disabled in SLEEP 1_D ERR pin monitor can be active in SLEEP depending on ERREN bit value. Reset: 0_H
ERREN	3	rwp	**Request ERR pin monitor enable** 0_D Disabled 1_D Enabled Reset: 1_H
ERRRECEN	2	rwp	**Request ERR pin monitor recovery enable** 0_D Disabled 1_D Enabled Reset: 0_H

			Offset	Reset Value
ERRREC	1:0	rwp	**Request ERR pin monitor recovery time** 0_D 1 ms 1_D 2.5 ms 2_D 5 ms 3_D 10 ms Reset: 0_H	

Protected Watchdog configuration request 0 *R2)

WDCFG0

Protected Watchdog configuration request 0 *R2) **06H** **9BH**

7	6	5	4	3	2	1	0
WWDETHR				WWDEN	FWDEN	WWDTSEL	WDCYC
rwp				rwp	rwp	rwp	rwp

Field	Bits	Type	Description
WWDETHR	7:4	rwp	**Request window watchdog error threshold** WWD error threshold to generate reset and enter into INIT state. Reset: 9_H
WWDEN	3	rwp	**Request window watchdog enable** 0_D Disabled 1_D Enabled Reset: 1_H
FWDEN	2	rwp	**Request functional watchdog enable** 0_D Disabled 1_D Enabled Reset: 0_H
WWDTSEL	1	rwp	**Request window watchdog trigger selection** This is ignored when window watchdog is disabled. 0_D External WDI input used as a WWD trigger 1_D WWD is triggered by SPI write to WWDSCMD register Reset: 1_H
WDCYC	0	rwp	**Request watchdog cycle time** 0_D 0,1 ms tick period 1_D 1 ms tick period Reset: 1_H

Protected Watchdog configuration request 1 *R2)

	Offset	Reset Value
WDCFG1		
Protected Watchdog configuration request 1 *R2)	**07H**	**09H**

7	6	5	4	3	2	1	0
nu			WDSLPEN	FWDETHR			
			rwp	rwp			

Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
WDSLPEN	4	rwp	**Request watchdog functionality enable while the device is in SLEEP** 0_D Disabled 1_D Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode Reset: 0_H
FWDETHR	3:0	rwp	**Request functional watchdog error threshold** FWD error threshold to generate reset and enter into INIT state. Reset: 9_H

Protected Functional watchdog configuration request *R2)

	Offset	Reset Value
FWDCFG **Protected Functional watchdog configuration request *R2)**	**08H**	**0BH**

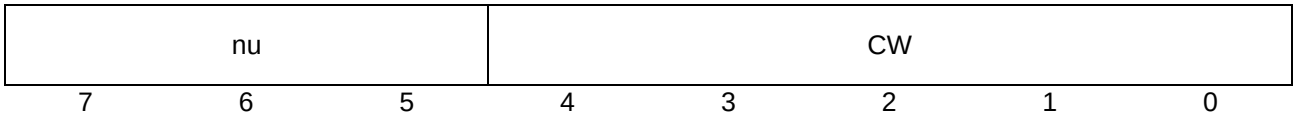
7	6	5	4	3	2	1	0
nu			WDHBTP				
			rwp				

Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H

Field	Bits	Type	Description
WDHBTP	4:0	rwp	**Request functional watchdog heartbeat timer period** Defined as a multiple of 50 watchdog cycles (**RWDCFG0.WDCYC**). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles ..$_D$ ... 31_D 1600 wd cycles Rese : $0B_H$

Protected Window watchdog configuration request 0 *R2)

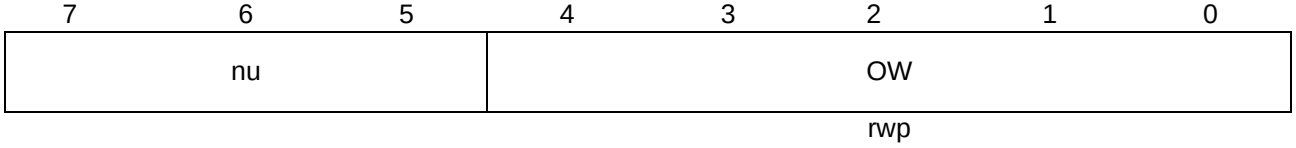
WWDCFG0 **Offset** **Reset Value**
Protected Window watchdog configuration request 0 *R2) **09_H** **06_H**



Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
CW	4:0	rwp	**Request window watchdog closed window time** Defined as a multiple of 50 watchdog cycles (**RWDCFG0.WDCYC**). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles ..$_D$ ... 31_D 1600 wd cycles Rese : 06_H

Protected Window watchdog configuration request 1 *R2)

WWDCFG1 **Offset** **Reset Value**
Protected Window watchdog configuration request 1 *R2) **$0A_H$** **$0B_H$**



Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
OW	4:0	rwp	**Request window watchdog open window time** Defined as a multiple of 50 watchdog cycles (**RWDCFG0.WDCYC**). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles ..$_D$ ... 31_D 1600 wd cycles Rese :: $0B_H$

System configuration 0 status *R0)

RSYSPCFG0 **Offset** **Reset Value**

System configuration 0 status *R0) **$0B_H$** **01_H**

7	6	5	4	3	2	1	0
nu							STBYEN
							r

Field	Bits	Type	Description
nu	7:1	none	Reset: 00_H
STBYEN	0	r	**Standby regulator QST enable status** Current configuration of standby regulator QST enable. Valid for all device states except FAILSAFE. 0_D Disabled 1_D Enabled Reset: 1_H

System configuration 1 status *R3) [1)]

RSYSPCFG1

System configuration 1 status *R3) **$0C_H$** **08_H**

7	6	5	4	3	2	1	0
SS2DEL			ERRSLPEN	ERREN	ERRRECEN	ERRREC	
r			r	r	r	r	

Field	Bits	Type	Description

[1]) Reset class of single bits is different. See register for details.

			Offset Reset Value
SS2DEL	7:5	r	**Safe state 2 delay status** Current configuration of safe state 2 delay applied for transitions from NORMAL to INIT, WAKE and SLEEP state. Bits have different reset class than whole register. The Bits are reset according to *R1) 0_D no delay 1_D 10 ms 2_D 50 ms 3_D 100 ms 4_D 250 ms Reset: 0_H
ERRSLPEN	4	r	**ERR pin monitor functionality enable status while the device is in SLEEP** Current configuration of ERR pin monitor functionality enable for SLEEP. 0_D ERR pin monitor is disabled in SLEEP 1_D ERR pin monitor can be active in SLEEP depending on ERREN bit value. Reset: 0_H
ERREN	3	r	**ERR pin monitor enable status** Current configuration of ERR pin monitor enable. 0_D Disabled 1_D Enabled Reset: 1_H
ERRRECEN	2	r	**ERR pin monitor recovery enable status** Current configuration of ERR pin monitor recovery enable. 0_D Disabled 1_D Enabled Reset: 0_H
Field	**Bits**	**Type**	**Description**
ERRREC	1:0	r	**ERR pin monitor recovery time status** Current configuration of ERR pin monitor recovery time. 0_D 1 ms 1_D 2.5 ms 2_D 5 ms 3_D 10 ms Reset: 0_H

Watchdog configuration 0 status *R3)

RWDCFG0 **Watchdog configuration 0 status *R3)**	**Offset** **$0D_H$**	**Reset Value** **$9B_H$**

7	6	5	4	3	2	1	0
WWDETHR				WWDEN	FWDEN	WWDTSEL	WDCYC

r r r r r

Field	Bits	Type	Description
WWDETHR	7:4	r	**Window watchdog error threshold status** Current configuration of WWD error threshold to generate reset and enter into INIT state. Reset: 9_H
WWDEN	3	r	**Window watchdog enable status** Current configuration of WWD enable. 0_D Disabled 1_D Enabled Reset: 1_H
FWDEN	2	r	**Functional watchdog enable status** Current configuration of FWD enable. 0_D Disabled 1_D Enabled Reset: 0_H
WWDTSEL	1	r	**Window watchdog trigger selection status** Current configuration of WWD trigger selection. This is ignored when window watchdog is disabled. 0_D External WDI input used as a WWD trigger 1_D WWD is triggered by SPI write to WWDSCMD register Reset: 1_H
WDCYC	0	r	**Watchdog cycle time status** Current configuration of watchdog cycle time. 0_D 0,1 ms tick period 1_D 1 ms tick period Reset: 1_H

Watchdog configuration 1 status *R3)

RWDCFG1

Watchdog configuration 1 status *R3) **$0E_H$** **09_H**

7	6	5	4	3	2	1	0
nu			WDSLPEN	FWDETHR			
			r	r			

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H

			Offset / Reset Value
WDSLPEN	4	r	**Watchdog functionality enable status while the device is in SLEEP** Current configuration of WD functionality enable for SLEEP. 0_D Disabled 1_D Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode Reset: 0_H
FWDETHR	3:0	r	**Functional watchdog error threshold status** Current configuration of FWD error threshold to generate reset and enter into INIT state. Reset: 9_H

Functional watchdog configuration status *R3)

RFWDCFG — **Functional watchdog configuration status *R3)** — **Offset** $0F_H$ — **Reset Value** $0B_H$

7	6	5	4	3	2	1	0
nu			WDHBTP				
			r				

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
Field	**Bits**	**Type**	**Description**
WDHBTP	4:0	r	**Functional watchdog heartbeat timer period status** Current configuration of FWD heartbeat timer period defined as a multiple of 50 watchdog cycles (**RWDCFG0.WDCYC**). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Rese : $0B_H$

Window watchdog configuration 0 status *R3)

RWWDCFG0 — **Window watchdog configuration 0 status *R3)** — **Offset** 10_H — **Reset Value** 06_H

7	6	5	4	3	2	1	0
nu			CW				
			r				

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
CW	4:0	r	**Window watchdog closed window time status** Current configuration of WWD closed window time defined as a multiple of 50 watchdog cycles (**RWDCFG0.WDCYC**). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles ..$_D$ ... 31_D 1600 wd cycles Rese : 06_H

Window watchdog configuration 1 status *R3)

RWWDCFG1

Window watchdog configuration 1 status *R3) **11_H** **$0B_H$**

7	6	5	4	3	2	1	0
nu			OW				
			r				

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
OW	4:0	r	**Window watchdog open window time status** Current configuration of WWD open window time defined as a multiple of 50 watchdog cycles (**RWDCFG0.WDCYC**). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles ..$_D$ ... 31_D 1600 wd cycles Rese : $0B_H$

Offset **Reset Value**

Wake timer configuration 0 *R2)

WKTIMCFG0

Wake timer configuration 0 *R2) **12H** **00H**

7	6	5	4	3	2	1	0
TIMVALL							
rw							

Field	Bits	Type	Description
TIMVALL	7:0	rw	**Wake timer value lower bits** Bits (7:0) of wake time defined as a multiple of wake timer cycles (**DEVCFG0.WKTIMCYC**). Reset: 00_H

Wake timer configuration 1 *R2)

WKTIMCFG1 **Offset** **Reset Value**

Wake timer configuration 1 *R2) **13H** **00H**

7	6	5	4	3	2	1	0
TIMVALM							
rw							

Field	Bits	Type	Description
TIMVALM	7:0	rw	**Wake timer value middle bits** Bits (15:8) of wake time defined as a multiple of wake timer cycles (**DEVCFG0.WKTIMCYC**). Reset: 00_H

Wake timer configuration 2 *R2)

WKTIMCFG2

Wake timer configuration 2 *R2) **14H** **00H**

7	6	5	4	3	2	1	0

Offset	Reset Value

TIMVALH
rw

Field	Bits	Type	Description
TIMVALH	7:0	rw	**Wake timer value higher bits** Bits (23:16) of wake time defined as a multiple of wake timer cycles (**DEVCFG0.WKTIMCYC**). Reset: 00_H

Device control request *R2)

DEVCTRL

Device control request *R2) **15_H** **00_H**

7	6	5	4	3	2	1	0
TRK2EN	TRK1EN	COMEN	nu	VREFEN	STATEREQ		
rw	rw	rw		rw	rwhc		

Field	Bits	Type	Description
TRK2EN	7	rw	**Request tracker2 QT2 enable** 0_D QT2 will be disabled after valid request 1_D QT2 will be enabled after valid request Reset: 0_H
TRK1EN	6	rw	**Request tracker1 QT1 enable** 0_D QT1 will be disabled after valid request 1_D QT1 will be enabled after valid request Reset: 0_H
COMEN	5	rw	**Request communication ldo QCO enable** 0_D QCO will be disabled after valid request 1_D QCO will be enabled after valid request Reset: 0_H
nu	4	none	Reset: 0_H

	Offset		Reset Value
VREFEN	3	rw	**Request voltage reference QVR enable** 0_D QVR will be disabled after valid request 1_D QVR will be enabled after valid request Reset: 0_H
STATEREQ	2:0	rwhc	**Request for device state transition** Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW. 7_D RESERVED 6_D RESERVED 5_D WAKE 4_D STANDBY 3_D SLEEP 2_D NORMAL 1_D INIT 0_D NONE Reset: 0_H

Device control inverted request *R2)

DEVCTRLN

Device control inverted request *R2) **16_H** **00_H**

7	6	5	4	3	2	1	0
TRK2EN	TRK1EN	COMEN	nu	VREFEN	STATEREQ		
rw	rw	rw		rw	rwhc		

Field	Bits	Type	Description
TRK2EN	7	rw	**Request tracker2 QT2 enable** 1_D QT2 will be disabled after valid request 0_D QT2 will be enabled after valid request Reset: 0_H

			Offset Reset Value
TRK1EN	6	rw	**Request tracker1 QT1 enable** 1_D QT1 will be disabled after valid request 0_D QT1 will be enabled after valid request Reset: 0_H
COMEN	5	rw	**Request communication ldo QCO enable** 1_D QCO will be disabled after valid request 0_D QCO will be enabled after valid request Reset: 0_H
nu	4	none	Reset: 0_H
VREFEN	3	rw	**Request voltage reference QVR enable** 1_D QVR will be disabled after valid request 0_D QVR will be enabled after valid request Reset: 0_H
STATEREQ	2:0	rwhc	**Request for device state transition** Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW. 7_D NONE 6_D INIT 5_D NORMAL 4_D SLEEP 3_D STANDBY 2_D WAKE 1_D RESERVED 0_D RESERVED Reset: 0_H

Window watchdog service command *R2)

WWDSCMD

Window watchdog service command *R2) **17_H** **00_H**

7	6	5	4	3	2	1	0
TRIG_STATUS	nu						TRIG

	Offset	Reset Value
r		rw

Field	Bits	Type	Description
TRIG_STATUS	7	r	**Last SPI trigger received** Reset: 0_H
nu	6:1	none	 Reset: 00_H
TRIG	0	rw	**Window watchdog SPI trigger command** Read **TRIG_STATUS** bit first and write inverted value to **TRIG** bit. Reset: 0_H

Functional watchdog response command *R2)

FWDRSP Functional watchdog response command *R2)	Offset 18_H	Reset Value 00_H

7	6	5	4	3	2	1	0
FWDRSP							
rw							

Field	Bits	Type	Description
FWDRSP	7:0	rw	**Functional watchdog response** Write functional watchdog response bytes to this field. Reset: 00_H

Reset Value

Functional watchdog response command with synchronization *R2)

FWDRSPSYNC	Offset	
Functional watchdog response command with synchronization *R2)	**19_H**	**00_H**

7	6	5	4	3	2	1	0
FWDRSPS							
rw							

Field	Bits	Type	Description
FWDRSPS	7:0	rw	**Functional watchdog heartbeat synchronization response** Write the last functional watchdog response byte to this field to synchronize/restart the heartbeat. Reset: 00_H

Failure status flags *R1)

SYSFAIL

Failure status flags *R1)	$1A_H$	00_H

7	6	5	4	3	2	1	0
INITF	ABISTERR	nu			VMONF	OTF	VOLTSEL ERR
rw1c	rw1c				rw1c	rw1c	rw1c

Field	Bits	Type	Description
INITF	7	rw1c	**INIT failure flag** INIT failure due to the third INIT failure in row. i.e. The device restarts INIT phase from FAILSAFE. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H

			Offset Reset Value
ABISTERR	6	rw1c	**ABIST operation interrupted flag** ABIST interrupted by any fault/event which is not part of ABIST. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
nu	5:3	none	Reset: 0_H
VMONF	2	rw1c	**Voltage monitor failure flag** Voltage monitor failure occured which lead to FAILSAFE. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags, read **MONSF0**, **MONSF1** and **MONSF3** for details Reset: 0_H
OTF	1	rw1c	**Over temperature failure flag** 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags, read **OTFAIL** for details Reset: 0_H
VOLTSELERR	0	rw1c	**Double Bit error on voltage selection flag** Device entered FAILSAFE state due to internal voltage selection failure. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H

Init error status flags *R2)

INITERR

Init error status flags *R2) **$1B_H$** **00_H**

7	6	5	4	3	2	1	0
HARDRES	SOFTRES	ERRF	FWDF	WWDF	VMONF	nu	
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c		

Field	Bits	Type	Description

			Offset Reset Value
HARDRES	7	rw1c	**Hard reset flag** Hard reset has been generated due to the second INIT failure in row. i.e. The device restarts INIT phase for the 3rd time. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
SOFTRES	6	rw1c	**Soft reset flag** Soft reset has been generated due to the first INIT failure. i.e. The device restarts INIT phase for the 2nd time. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
ERRF	5	rw1c	**MCU error monitor failure flag** 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
FWDF	4	rw1c	**Functional watchdog error counter overflow failure flag** Functional watchdog error counter reached the error threshold. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
WWDF	3	rw1c	**Window watchdog error counter overflow failure flag** Window watchdog error counter reached the error threshold. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
VMONF	2	rw1c	**Voltage monitor failure flag** Voltage monitor failure occured which lead to INIT. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags, read **MONSF2** for details Reset: 0_H
nu	1:0	rw1c	Reset: 0_H

Interrupt flags *R2)

IF

Interrupt flags *R2) **$1C_H$** **00_H**

7	6	5	4	3	2	1	0

Offset							Reset Value
INTMISS	ABIST	OTF	OTW	MON	SPI	WK	SYS
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
INTMISS	7	r	**Interrupt not serviced in time flag** Interrupt has not been serviced within $t_{INT,TO}$ time 0_D No interrupt timeout happened 1_D Interrupt timeout happened, cleared by hardware when all other flags in IF are cleared. Reset: 0_H
ABIST	6	rw1c	**Requested ABIST operation performed flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag Reset: 0_H
OTF	5	rw1c	**Over temperature failure interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **OTFAIL** for details Reset: 0_H
OTW	4	rw1c	**Over temperature warning interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **OTWRNSF** for details Reset: 0_H
MON	3	rw1c	**Monitor interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **MONSF0**, **MONSF1**, **MONSF2** and **MONSF3** for details Reset: 0_H
SPI	2	rw1c	**SPI interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **SPISF** for details Reset: 0_H
WK	1	rw1c	**Wake interrupt flag** Only set if device generates an interrupt when leaving SLEEP state. 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **WKSF** for details Reset: 0_H

Field	Bits	Type	Description
SYS	0	rw1c	**System interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **SYSSF** for details Reset: 0_H

System status flags *R2)

SYSSF **Offset** **Reset Value**

System status flags *R2) **$1D_H$** **00_H**

7	6	5	4	3	2	1	0
nu		NO_OP	TRFAIL	ERRMISS	FWDE	WWDE	CFGE
		rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
nu	7:6	none	Reset: 0_H
NO_OP	5	rw1c	**State transition request failure flag** Requested state transition via DEVCTRL & DEVCTRLN could not be performed because of wrong protocol. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRFAIL	4	rw1c	**Transition to low power failed flag** Transition to low power failed either due to the QUC current monitor, WAK high level or a rising edge on ENA during TRDEL time. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
ERRMISS	3	rw1c	**MCU error miss status flag** Set only when SYSPCFG1.ERRRECEN='1' 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
FWDE	2	rw1c	**Functional watchdog error interrupt flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
Field	**Bits**	**Type**	**Description**
WWDE	1	rw1c	**Window watchdog error interrupt flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

CFGE	0	rw1c	**Protected configuration double bit error flag** Double bit error occurred on protected configuration register. Status registers shall be read in order to determine which configuration has changed. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

Wakeup status flags *R2)

WKSF **Offset** **Reset Value**

Wakeup status flags *R2) **$1E_H$** **00_H**

nu			WKSPI	WKTIM	CMON	ENA	WAK
7	6	5	4	3	2	1	0
			rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
ENA	1	rw1c	**ENA signal wakeup flag** Bit will also be set if FAILSAFE or STANDBY state left because of ENA. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
WKSPI	4	rw1c	**Wakeup from SLEEP by SPI flag (GoToWAKE)** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
WKTIM	3	rw1c	**Wake timer wakeup flag** Bit will also be set if STANDBY state left because of wake timer expired. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
CMON	2	rw1c	**QUC current monitor threshold wakeup flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

WAK	0	rw1c	**WAK signal wakeup flag** Bit will also be set if FAILSAFE or STANDBY state left because of WAK. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
LOCK	4	rw1c	**LOCK or UNLOCK procedure error flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
DURE	3	rw1c	**SPI frame duration error flag** SCS low for more than 2 ms. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
ADDRE	2	rw1c	**SPI address invalid flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

LENE	1	rw1c	**SPI frame length invalid flag** Number of detected SPI clock cycles different than 16. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
Field	**Bits**	**Type**	**Description**
PARE	0	rw1c	**SPI frame parity error flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

SPI status flags *R2)

SPISF **Offset** **Reset Value**

SPI status flags *R2) **$1F_H$** **00_H**

7	6	5	4	3	2	1	0
nu			LOCK	DURE	ADDRE	LENE	PARE
			rw1c	rw1c	rw1c	rw1c	rw1c

	Offset	Reset Value
Monitor status flags 0 *R1)		

MONSF0

Monitor status flags 0 *R1)	**20_H**	**00_H**

7	6	5	4	3	2	1	0
TRK2SG	TRK1SG	VREFSG	COMSG	VCORESG	STBYSG	UCSG	PREGSG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
TRK2SG	7	rw1c	**Tracker2 short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRK1SG	6	rw1c	**Tracker1 short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VREFSG	5	rw1c	**Voltage reference short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COMSG	4	rw1c	**Communication LDO short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VCORESG	3	rw1c	**Core voltage short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
STBYSG	2	rw1c	**Standby LDO short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
UCSG	1	rw1c	**uC LDO short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

			Offset	Reset Value
PREGSG	0	rw1c	**Pre-regulator voltage short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H	

Monitor status flags 1 *R1)

MONSF1

Monitor status flags 1 *R1) **21_H** **00_H**

7	6	5	4	3	2	1	0
TRK2OV	TRK1OV	VREFOV	COMOV	VCOREOV	STBYOV	UCOV	PREGOV
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
TRK2OV	7	rw1c	**Tracker2 over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRK1OV	6	rw1c	**Tracker1 over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VREFOV	5	rw1c	**Voltage reference over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COMOV	4	rw1c	**Communication LDO over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VCOREOV	3	rw1c	**Core voltage over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
STBYOV	2	rw1c	**Standby LDO over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

			Offset	Reset Value
UCOV	1	rw1c	**uC LDO over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H	
PREGOV	0	rw1c	**Pre-regulator voltage over voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H	

Monitor status flags 2 *R2)

MONSF2

Monitor status flags 2 *R2) **22_H** **00_H**

7	6	5	4	3	2	1	0
TRK2UV	TRK1UV	VREFUV	COMUV	VCOREUV	STBYUV	UCUV	PREGUV
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
TRK2UV	7	rw1c	**Tracker2 under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRK1UV	6	rw1c	**Tracker1 under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VREFUV	5	rw1c	**Voltage reference under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COMUV	4	rw1c	**Communication LDO under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VCOREUV	3	rw1c	**Core voltage under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

			Offset	Reset Value
STBYUV	2	rw1c	**Standby LDO under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H	
UCUV	1	rw1c	**uC LDO under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H	
PREGUV	0	rw1c	**Pre-regulator voltage under voltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H	

Monitor status flags 3 *R1)

MONSF3

Monitor status flags 3 *R1) **23_H** **00_H**

7	6	5	4	3	2	1	0
BIASHI	BIASLOW	BG12OV	BG12UV	nu			VBATOV
rw1c	rw1c	rw1c	rw1c				

Field	Bits	Type	Description
BIASHI	7	rw1c	**Bias current too high flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
BIASLOW	6	rw1c	**Bias current too low flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
BG12OV	5	rw1c	**Bandgap comparator over voltage condition flag** (VBG1 ≥ VBG2 + 4%) 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
BG12UV	4	rw1c	**Bandgap comparator under voltage condition flag** (VBG1 ≤ VBG2 - 4%) 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

			Offset Reset Value
nu	3:1	none	Reset: 0_H
VBATOV	0	rw1c	**Supply voltage VSx over voltage flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

Over temperature failure status flags *R1)

OTFAIL

Over temperature failure status flags *R1) **24_H** **00_H**

7	6	5	4	3	2	1	0
MON	nu		COM	nu		UC	PREG
rw1c			rw1c			rw1c	rw1c

Field	Bits	Type	Description
MON	7	rw1c	**Monitoring over temperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	6:5	none	Reset: 0_H
COM	4	rw1c	**Communication LDO over temperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	3:2	none	Reset: 0_H
UC	1	rw1c	**uC LDO over temperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREG	0	rw1c	**Pre-regulator over temperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

Over temperature warning status flags *R2)

OTWRNSF | **Offset** | **Reset Value**

Over temperature warning status flags *R2) | **25H** | **00H**

7	6	5	4	3	2	1	0
nu		VREF	COM	nu	STDBY	UC	PREG
		rw1c	rw1c		rw1c	rw1c	rw1c

Field	Bits	Type	Description
nu	7:6	none	Reset: 0_H
VREF	5	rw1c	**Voltage reference over load flag** (over current for more than 1ms) 0_D Write 0 no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COM	4	rw1c	**Communication LDO over temperature warning flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	3	none	Reset: 0_H
STDBY	2	rw1c	**Standby LDO over load flag** (over current for more than 1ms) 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
UC	1	rw1c	**uC LDO over temperature warning flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREG	0	rw1c	**Pre-regulator over temperature warning flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

Voltage monitor status *R2)

VMONSTAT

Voltage monitor status *R2)	Offset	Reset Value
	26H	00H

7	6	5	4	3	2	1	0
TRK2ST	TRK1ST	VREFST	COMST	VCOREST	STBYST	nu	
r	r	r	r	r	r		

Field	Bits	Type	Description
TRK2ST	7	r	**Tracker2 voltage ready status** 0D Voltage is out of range or not enabled 1D Voltage is OK Reset: 0H
TRK1ST	6	r	**Tracker1 voltage ready status** 0D Voltage is out of range or not enabled 1D Voltage is OK Reset: 0H
VREFST	5	r	**Voltage reference voltage ready status** 0D Voltage is out of range or not enabled 1D Voltage is OK Reset: 0H
COMST	4	r	**Communication LDO voltage ready status** 0D Voltage is out of range or not enabled 1D Voltage is OK Reset: 0H
VCOREST	3	r	**Core voltage ready status** 0D Voltage is out of range or not enabled 1D Voltage is OK Reset: 0H
STBYST	2	r	**Standby LDO voltage ready status** 0D Voltage is out of range or not enabled 1D Voltage is OK Reset: 0H
nu	1:0	none	Reset: 0H

Device status *R2)

DEVSTAT

Device status *R2)	27H	00H

Offset **Reset Value**

7	6	5	4	3	2	1	0
TRK2EN	TRK1EN	COMEN	STBYEN	VREFEN	STATE		
r	r	r	r	r	r		

Field	Bits	Type	Description
TRK2EN	7	r	**Tracker2 voltage enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
TRK1EN	6	r	**Tracker1 voltage enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
COMEN	5	r	**Communication LDO enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
STBYEN	4	r	**Standby LDO enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
VREFEN	3	r	**Reference voltage enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
STATE	2:0	r	**Devi :e state** 7_D RESERVED 6_D RESERVED 5_D WAKE 4_D STANDBY 3_D SLEEP 2_D NORMAL 1_D INIT 0_D NONE Rese :: 0_H

Protection status *R1)

PROTSTAT

Protection status *R1) **28_H** **01_H**

Offset	Reset Value

7	6	5	4	3	2	1	0
KEY4OK	KEY3OK	KEY2OK	KEY1OK	nu			LOCK
r	r	r	r				r

Field	Bits	Type	Description
KEY4OK	7	r	**Key4 ok status** Information about validity of the 4th received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
KEY3OK	6	r	**Key3 ok status** Information about validity of the 3rd received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
KEY2OK	5	r	**Key2 ok status** Information about validity of the 2nd received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
KEY1OK	4	r	**Key1 ok status** Information about validity of the 1st received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
nu	3:1	none	Reset: 0_H
LOCK	0	r	**Protected register lock status** 0_D Access is unlocked 1_D Access is locked Reset: 1_H

Window watchdog status *R3)

WWDSTAT

Window watchdog status *R3) **29_H** **00_H**

7	6	5	4	3	2	1	0

		Offset	Reset Value
nu	WWDECNT		
	r		

Field	Bits	Type	Description
nu	7:4	none	Reset: 0_H
WWDECNT	3:0	r	**Window watchdog error counter status** Reset: 0_H

Functional watchdog status 0 *R3)

FWDSTAT0 **Offset** **Reset Value**

Functional watchdog status 0 *R3) **$2A_H$** **30_H**

7	6	5	4	3	2	1	0
nu	FWDRSPOK	FWDRSPC		FWDQUEST			
	r	r		r			

Functional watchdog status 1 *R3)

FWDSTAT1

Functional watchdog status 1 *R3) **$2B_H$** **00_H**

Field	Bits	Type	Description
nu	7	none	Reset: 0_H
FWDRSPOK	6	r	**Functional watchdog response check error status** 0_D Response message is wrong 1_D All received bytes in response message are correct Reset: 0_H
FWDRSPC	5:4	r	**Functional watchdog response counter value** Reset: 3_H
FWDQUEST	3:0	r	**Functional watchdog question** Reset: 0_H

7	6	5	4	3	2	1	0

Offset	Reset Value

nu	FWDECNT
	r

Field	Bits	Type	Description
nu	7:4	none	Reset: 0_H
FWDECNT	3:0	r	**Functional watchdog error counter value** Reset: 0_H

ABIST control 0 *R2)

ABIST_CTRL0

ABIST control0 *R2) $2C_H$ 00_H

7	6	5	4	3	2	1	0
STATUS				INT	SINGLE	PATH	START
r				rw	rw	rw	rwhc

Field	Bits	Type	Description
STATUS	7:4	r	**ABIST global error status** ABIST status information after requested operation has been performed, information shall only be considered valid, once START bit is cleared. Bits have different reset class than whole register. The Bits are reset according to *R1). 5_D Selected ABIST operation performed with no errors 10_D Selected ABIST operation performed with errors, check respective SELECT registers Reset: 0_H
INT	3	rw	**Safety path selection** Select whether safe state or interrupt related comparator shall be tested. 0_D safe state related comparators shall be tested 1_D interrupt related comparators shall be tested Reset: 0_H

	Offset		Reset Value
SINGLE	2	rw	**ABIST Sequence selection** Select whether a single comparator shall be tested or all comparators in predefined sequence 0_D Predefined sequence 1_D Single comparator test Reset: 0_H
PATH	1	rw	**Full path test selection** Select the path which should be covered by ABIST operation 0_D Comparator only 1_D Comparator and corresponding deglitching logic, shall be selected in case contribution to respective safety measure needs to be tested Reset: 0_H
START	0	rwhc	**Start ABIST operation** The ABIST operation itself will be started. This bit is cleared after ABIST operation has been performed 0_D Operation done 1_D Start operation Reset: 0_H

ABIST control 1 *R2)

ABIST_CTRL1

ABIST control1 *R2) **2^D_H** **00_H**

7	6	5	4	3	2	1	0
nu						ABIST_CLK_EN	OV_TRIG
						rw	rw

Field	Bits	Type	Description
nu	7:2	none	Reset: 00_H
ABIST_CLK_EN	1	rw	**ABIST clock check enable** Select ABIST clock to check its functionality 0_D Disable 1_D Enable Reset: 0_H

			Offset	Reset Value
OV_TRIG	0	rw	**Overvoltage trigger for secondary internal monitor enable** 0_D Disable 1_D Enable Reset: 0_H	

ABIST select 0 *R2)

ABIST_SELECT0

ABIST select 0 *R2) **2^E_H** **00_H**

7	6	5	4	3	2	1	0
TRK2OV	TRK1OV	VREFOV	COMOV	VCOREOV	STBYOV	UCOV	PREGOV
rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu

Field	Bits	Type	Description
TRK2OV	7	rwhu	**Select TRK2 OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
TRK1OV	6	rwhu	**Select TRK1 OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
VREFOV	5	rwhu	**Select VREF OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
COMOV	4	rwhu	**Select COM OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

	Offset		Reset Value
VCOREOV	3	rwhu	**Select Core voltage OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
STBYOV	2	rwhu	**Select Standby LDO OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
UCOV	1	rwhu	**Select uC LDO OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

Field	Bits	Type	Description
PREGOV	0	rwhu	**Select Pre-regulator OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

ABIST select 1 *R2)

ABIST_SELECT1 **Offset** **Reset Value**

ABIST select 1 *R2) **$2F_H$** **00_H**

7	6	5	4	3	2	1	0
TRK2UV	TRK1UV	VREFUV	COMUV	VCOREUV	STBYUV	UCUV	PREGUV
rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu

Field	Bits	Type	Description
TRK2UV	7	rwhu	**Select TRK2 UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
TRK1UV	6	rwhu	**Select TRK1 UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this voltage Reset: 0_H
VREFUV	5	rwhu	**Select VREF UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
COMUV	4	rwhu	**Select COM UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

VCOREUV	3	rwhu	**Select VCORE UV comparator for ABIST operation** 0_D Not selected 1_D selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
Field	**Bits**	**Type**	**Description**
STBYUV	2	rwhu	**Select STBY UV comparator for ABIST operation** 0_D Not selected 1_D selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
UCUV	1	rwhu	**Select uC UV comparator for ABIST operation** 0_D Not selected 1_D selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
PREGUV	0	rwhu	**Select pre regulator UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

ABIST select 2 *R2)

ABIST_SELECT2 **ABIST select 2 *R2)**	**Offset** **30_H**	**Reset Value** **00_H**

7	6	5	4	3	2	1	0
BIASHI	BIASLOW	BG12OV	BG12UV	INTOV	nu		VBATOV
rwhu	rwhu	rwhu	rwhu	rwhu			rwhu

Field	**Bits**	**Type**	**Description**
BIASHI	7	rwhu	**Select bias current too high** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

BIASLOW	6	rwhu	**Select bias current too low** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
BG12OV	5	rwhu	**Select bandgap comparator OV condition** (VBG1 ≥ VBG2 + 4%) 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
Field	**Bits**	**Type**	**Description**
BG12UV	4	rwhu	**Select bandgap comparator UV condition** (VBG1 ≤ VBG2 - 4%) 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
INTOV	3	rwhu	**Select internal supply OV condition** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
nu	2:1	none	Reset: 0_H
VBATOV	0	rwhu	**Select supply VSx overvoltage** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

Global testmode *R2)

GTM **Global testmode *R2)**	**Offset** **$3F_H$**	**Reset Value** **02_H**

7	6	5	4	3	2	1	0
nu						NTM	TM
						r	r

Field	Bits	Type	Description
nu	7:2	none	Reset: 00_H
NTM	1	r	**Test mode inverted status** 0_D Device is in test mode 1_D Device is in normal mode Reset: 1_H
TM	0	r	**Test mode status** 0_D Device is in normal mode 1_D Device is in test mode Reset: 0_H

13.4.2 Buck registers

Buck switching frequency change *R2)

BCK_FREQ_CHANGE Buck switching frequency change *R2)	Offset 31_H	Reset Value 00_H

7	6	5	4	3	2	1	0
nu					BCK_FREQ_SEL		
					rw		

Field	Bits	Type	Description
nu	7:3	none	Reset: 00_H
BCK_FREQ_SEL	2:0	rw	**BUCK switching frequency change** For hi and low switching mode. New value needs to be validated via data_valid procedure 7_D Change buck frequency by approx. -4.5% from $f_{OSC,step\text{-}down}$ 6_D Change buck frequency by approx. -3.0% from $f_{OSC,step\text{-}down}$ 5_D Change buck frequency by approx. -1.5% from $f_{OSC,step\text{-}down}$ 4_D No change 3_D Change buck frequency by approx. +4.5% from $f_{OSC,step\text{-}down}$ 2_D Change buck frequency by approx. +3.0% from $f_{OSC,step\text{-}down}$ 1_D Change buck frequency by approx. +1.5% from $f_{OSC,step\text{-}down}$ 0_D No Change Reset: 0_H

Buck Frequency spread *R2)

BCK_FRE_SPREAD **Offset** **Reset Value**
Buck Frequency spread *R2) **32H** **00H**

7	6	5	4	3	2	1	0
FRE_SP_THR							
rw							

Field	Bits	Type	Description
FRE_SP_THR	7:0	rw	**Spread spectrum** Select the percentage of frequency spread(+/-). The mean frequency is reduced by the percentage as well keeping the maximum frequency at the nominal frequency selected by FRE. 00_H No spread $2B_H$ 1% 55_H 2% 80_H 3% AA_H 4% $D5_H$ 5% FF_H 6% Reset: 00_H

Buck main control *R2)

BCK_MAIN_CTRL **Offset** **Reset Value**
Buck main control *R2) **33H** **00H**

7	6	5	4	3	2	1	0
BUSY	DATA_VALID	nu					
r	rw						

Field	Bits	Type	Description
BUSY	7	r	**DATA_VALID parameter update ready status** 0_D update done 1_D update ongoing Reset: 0_H

Field	Bits	Type	Description

DATA_VALID	6	rw	**Enable buck update** Update Command to load new parameter for stepdown regulator (after configuration write 1 to update and write 0 after BUSY flag is cleared to proceed operation) 0_D No action 1_D Load new parameters Reset: 0_H
nu	5:0	none	 Reset: 00_H

13.5 Electrical Characteristics

Table 23 Electrical Characteristics: SPI signals

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Data input valid high level	$V_{SDI, hi}$	3.6	–	–	V	V_{SDI} increasing, V_{QUC} = 5.0 V	P_13.5.17
Data input valid low level	$V_{SDI, lo}$	–	–	0.8	V	V_{SDI} decreasing, V_{QUC} = 5.0 V	P_13.5.18
Data input hysteresis	$V_{SDI, hyst}$	–	350	–	mV	V_{QUC} = 5.0 V	P_13.5.19

Data input valid high level	$V_{SDI, hi}$	2.0	–	–	V	V_{SDI} increasing, V_{QUC} = 3.3 V	P_13.5.20
Pin SCS, Chip Select							
Chip select valid high level	$V_{SCS, hi}$	3.6	–	–	V	V_{SCS} increasing, V_{QUC} = 5.0 V	P_13.5.1
Chip select valid low level	$V_{SCS, lo}$	–	–	0.8	V	V_{SCS} decreasing, V_{QUC} = 5.0 V	P_13.5.2
Chip select hysteresis	$V_{SCS, hyst}$	–	350	–	mV	V_{QUC} = 5.0 V	P_13.5.3
Chip select valid high level	$V_{SCS, hi}$	2.0	–	–	V	V_{SCS} increasing, V_{QUC} = 3.3 V	P_13.5.4
Chip select valid low level	$V_{SCS, lo}$	–	–	0.8	V	V_{SCS} decreasing, V_{QUC} = 3.3 V	P_13.5.5
Chip select hysteresis	$V_{SCS, hyst}$	–	160	–	mV	V_{QUC} = 3.3 V	P_13.5.6
Chip select pull-up current	I_{SCS}	-175	-120	–	µA	V_{SCS} = 0 V	P_13.5.7
Chip select input capacitance	C_{SCS}	–	4	15	pF	1)	P_13.5.8
Pin SCL, Clock							
Clock signal valid high level	$V_{SCL, hi}$	3.6	–	–	V	V_{SCL} increasing, V_{QUC} = 5.0 V	P_13.5.9
Clock signal valid low level	$V_{SCL, lo}$	–	–	0.8	V	V_{SCL} decreasing, V_{QUC} = 5.0 V	P_13.5.10
Clock hysteresis	$V_{SCL, hyst}$	–	350	–	mV	V_{QUC} = 5.0 V	P_13.5.11
Clock signal valid high level	$V_{SCL, hi}$	2.0	–	–	V	V_{SCL} increasing, V_{QUC} = 3.3 V	P_13.5.12
Clock signal valid low level	$V_{SCL, lo}$	–	–	0.8	V	V_{SCL} decreasing, V_{QUC} = 3.3 V	P_13.5.13
Clock hysteresis	$V_{SCL, hyst}$	–	160	–	mV	V_{QUC} = 3.3 V	P_13.5.14
Clock signal pull-down current	I_{SCL}	–	150	330	µA	V_{SCL} = V_{QUC}	P_13.5.15
Clock input capacitance	C_{SCL}	–	4	15	pF	1)	P_13.5.16

Pin SDI, Data Input, MOSI

Table 23 Electrical Characteristics: SPI signals (cont'd)

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Data input valid low level	$V_{SDI, lo}$	–	–	0.8	V	V_{SDI} decreasing, V_{QUC} = 3.3 V	P_13.5.21
Data input hysteresis	$V_{SDI, hyst}$	–	160	–	mV	V_{QUC} = 3.3 V	P_13.5.22

Data input signal pull-down current	I_{SDI}	–	150	330	µA	$V_{SDI} = V_{QUC}$	P_13.5.23
Data input capacitance	C_{SDI}	–	4	15	pF	1)	P_13.5.24
Pin SDO, Data Output, MISO							
Data output high level TLF35584xxVS1	$V_{SDO, hi}$	4.0	–	–	V	V_{QUC} = 5.0 V, I_{SDO} = -9 mA	P_13.5.25
Data output low level TLF35584xxVS1	$V_{SDO, lo}$	–	–	0.7	V	V_{QUC} = 5.0 V I_{SDO} = 7 mA	P_13.5.26
Data output high level TLF35584xxVS2	$V_{SDO, hi}$	2.3	–	–	V	V_{QUC} = 3.3 V I_{SDO} = -7 mA	P_13.5.27
Data output low level TLF35584xxVS2	$V_{SDO, lo}$	–	–	0.7	V	V_{QUC} = 3.3 V I_{SDO} = 5.5 mA	P_13.5.28
Data output rise time 1)	$t_{SDO, rise}$	–	–	25	ns	$C_{SDO,load}$ = 50 pF	P_13.5.29
Data output fall time 1)	$t_{SDO, fall}$	–	–	25	ns	$C_{SDO,load}$ = 50 pF	P_13.5.30
Data output tristate capacitance	$C_{SDO, tri}$	–	4	15	pF	1)	P_13.5.31
Data output tristate leakage	$I_{SDO, tr, leaki}$	-10	–	10	µA	–	P_13.5.32

1) Specified by design, not subject to production test

14 Interrupt Generation

A dedicated interrupt generation block is implemented which is handling requests from independent sources to generate an interrupt. The different requesters are as follows:

- State machine in case:
  - A requested state transition has not been performed successfully, e.g. SLEEP state could not be entered because of LDO_µC current consumption above the selected threshold level.
  - A requested state transition from SLEEP has been performed successfully, i.e. the system has either successfully entered WAKE state. The uC may only send (additional) SPI commands after an interrupt event has been generated by the system. The purpose of the interrupt event is to inform the uC that a state transition has been performed successfully and that the system is capable of performing SPI communication at full SPI speed.
- Watchdog, an interrupt request is generated if the Watchdog is not serviced properly and configured in a way to allow service errors to occur, i.e. an error counter threshold value of more than 2 is configured. In this case an interrupt is generated only if the error counter threshold is not exceeded due to this error.
- Error pin monitoring, an interrupt request is generated if the error pin monitoring block detects an error and is configured in a way to allow occurrence of this error for a certain amount of time (recovery delay action enabled). In this case an interrupt is requested if an error is detected by the error pin monitoring and the recovery delay has not expired.
- Monitoring Block, an interrupt request is generated based on the defined system reaction described in **Chapter 11.4**.
- Overtemperature warnings and over temperature shutdown of communication LDO
- Overcurrent conditions of voltage reference or standby LDO
- SPI block in case an SPI error has occurred
- ABIST operation has been completed
- Double bit error in the protected configuration

An interrupt is generated to inform a connected uC that a non-severe system condition has occurred. This allows the uC to perform proper action based on the source of the interrupt. A single interrupt line exists, which is high on default. All Internal interrupt sources are enabled by default and cannot be disabled.

An interrupt is signaled by pulling the interrupt line low for at least t_{INT} (interrupt min. pulse width) after an internal interrupt condition occurs. The interrupt line will be driven high if all of the **IF** register flag(s) has/have been cleared via SPI operation earliest after t_{INT} has expired but latest after t_{INTTO} has expired.

Special cases:

- If an interrupt is signaled by pulling INT low and not all interrupt status flags are cleared by the uC within t_{INTTO}, the INT will stay low until t_{INTTO} has expired, but no additional interrupt will be generated. Information about a pending interrupt event can be derived via the INTMISS status flag. This status flag is cleared each time the interrupt line is driven low.
- If an interrupt is signaled by pulling INT low and an additional bit is set in the **IF** register interrupt flag after the interrupt bits have been read by the uC and this outdated information is used to clear the interrupt flags, the interrupt line will stay low until t_{INTTO} has expired, but no additional interrupt will be generated. Information about a pending interrupt event can be derived via a status flag.

- After releasing the interrupt line to high, the interrupt line will stay high for at least t_{INTTO} regardless if any additional internal interrupt condition has occurred or not. If a new interrupt event occurs during the delay time out (t_{INTTO}), this will be signaled by generating a new pulse after the delay time out t_{INTTO}.

All interrupt sources can only be cleared by a “write-1-to-clear” (w1c) SPI operation, i.e. writing a logic one to the corresponding bit(s) in the interrupt register will clear the event.

Interrupt events are organized in a two level approach. The first level (interrupt flag) provides information about different groups of interrupt events. The second level (status flags) provides detailed information about which particular event(s) generated the interrupt. To service an interrupt one would only need to write the interrupt flag register (**IF**). The status flag registers are only meant to provide detailed information. However all status flags can be cleared as well.

Recommended interrupt service routine:

After an interrupt has been detected by an uC, the recommended interrupt service routine would need to perform the following tasks via SPI:

1. Read interrupt flag register (**IF**)
2. Read status flag register(s) based on information from first read
3. Take the proper action based on interrupt flag(s) and status flag(s)
4. Write back the status flag register(s) to clear particular status flag(s)
5. Write back the interrupt flag register (**IF**) with the previously read value to clear
6. Recommended: Read interrupt flag register (**IF**) again to check for occurrence of another interrupt event. In case step back to 2).
7. Writing back the interrupt register (**IF**) will release the interrupt line INT if all bits are cleared (interrupt timing requirements will be fulfilled).

An interrupt is only generated after the reset signal to the uC has been released. An interrupt event which occurred while the reset line for the uC is still active is not signaled at the interrupt line but the particular status bit for this event is set.

Details about the timing of the interrupt line are depicted in the following figure:

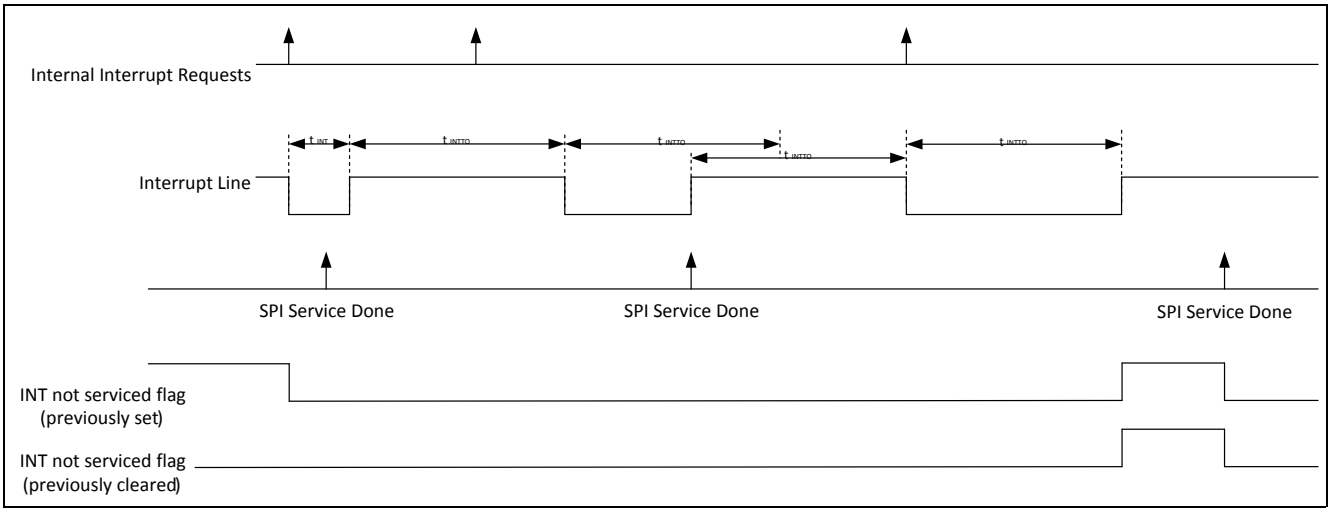


Figure 76 Interrupt timing

Table 24 Electrical Characteristics: Interrupt - Timings

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Minimum interrupt pulse width	$t_{INT,min}$	90	100	150	µs		P_14.1
Interrupt time out	t_{INTTO}	270	300	350	µs		P_14.2

Details about the system behavior in case not all interrupt status flags have been cleared are depicted in the following figure:

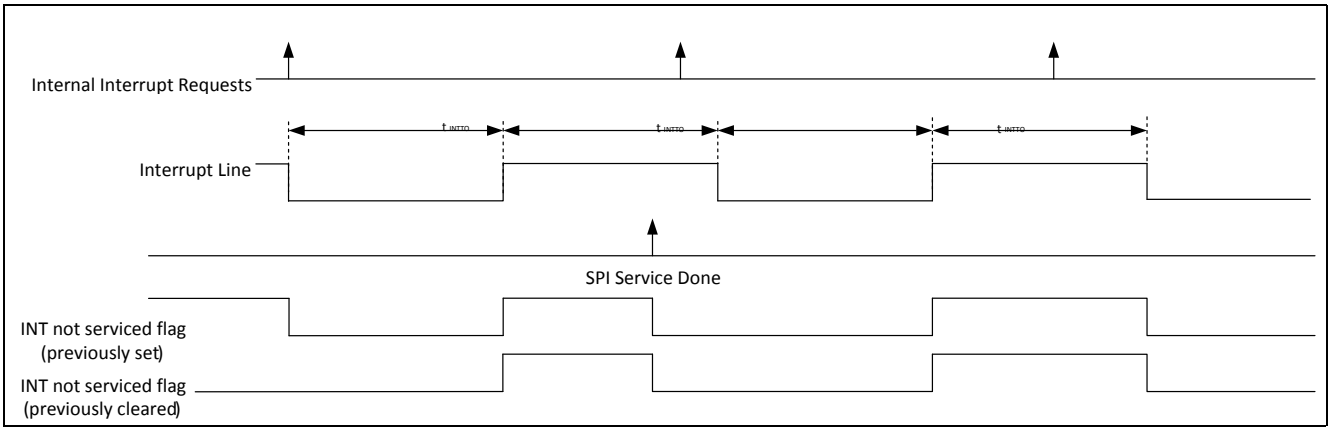


Figure 77 Interrupt timing without service in time

An interrupt is always generated if an internal status flag is set, irrespective of the current state of this status flag. For example, if a parity error on SPI communication is detected for the first time, the flag SPISF.PARE is set and an interrupt is generated. This flag will also set the corresponding SPI interrupt flag (IF.SPI). If the flag IF.SPI is not cleared, but a second SPI parity error occurs, a new interrupt will be generated regardless. The timings shown in the two figures above will be fulfilled for generating a new interrupt.

15 Window Watchdog And Functional Watchdog

15.1 Introduction

Two independent types of watchdogs are implemented in the TLF35584:

- A standalone window watchdog (WWD) with programmable input trigger signal (either pin WDI or trigger via SPI command to **WWDSCMD** register)
- A standalone functional or question/answer watchdog (FWD).

The watchdogs have independent timers and error counters, which allows to run both watchdogs in parallel.

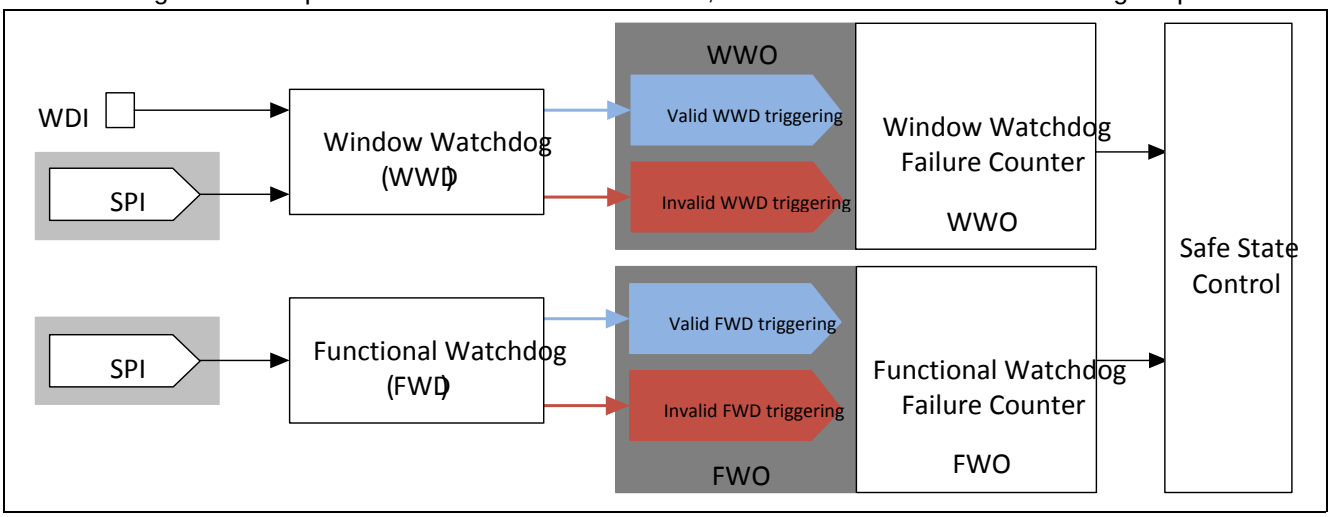


Figure 78 Window watchdog and functional watchdog

Description:

- The functional watchdog is not synchronized to the window watchdog, both are fully independent.
- The functional watchdog and the window watchdog can be activated and deactivated independently.
- The result of the watchdogs (valid or invalid triggering) are monitored independently by the related watchdog failure counters.
- The status of the window watchdog is WWO, it may have the values “Valid WWD triggering” or “Invalid WWD triggering”
- The status of the functional watchdog is FWO, it may have the values “Valid FWD triggering” or “Invalid FWD triggering
- The influence of the settings of both watchdogs on safe state control is described in chapter safe state control for better understanding

15.2 Window Watchdog

Principle of Operation

The window watchdog is integrated in the TLF35584 to monitor the microcontroller. The microcontroller that is being monitored has to provide periodical triggering within the "Open Windows". A triggering can consist of a falling edge on the WDI pin or writing to the register **WWDSCMD** by an SPI command depending on the configuration. This triggering terminates the “Open Window”. The watchdog output indicates a “Valid” or “Invalid” WWD triggering to the WWD failure counter. In case of a “Valid” triggering a “Closed Window” is started.In case

there is no triggering during the “Open Window” or a triggering during a "Closed Window", the watchdog output indicates an “Invalid WWD triggering” to the WWD failure counter and a new “Open Window” is started.

In case the microcontroller is not able to trigger the window watchdog with a correct timing, it is assumed that the microcontroller doesn’t work as expected. The microcontroller will get informed by the TLF35584 and a reset in case of multiple failure events.

Configuration

The following parameters of the window watchdog can be configured in INIT, NORMAL and WAKE state:

- The triggering can be set either to pin triggering (pin WDI) or triggering via SPI command (register **WWDSCMD**). The default configuration is the triggering via SPI.
- The length of open and closed window can be modified according to the application needs by SPI. (combination of cycle time **WDCYC** and number of cycles for open **OW** and closed **CW** window)
- The threshold for the window watchdog failure counter overflow can defined by SPI

Initialization

The window watchdog will become active in INIT state as soon as reset output pin ROT turns from low to high. After activation the watchdog opens a so called “Long Open Window” (LOW) of duration of t_{LOW}. During the ”Long Open Window” the window watchdog expects a valid triggering, which has to be provided via SPI in case the default configuration is kept, since any signal to watchdog trigger pin WDI is ignored. This is to avoid wrong triggering at pin WDI due to glitches at the micro controller outputs during startup and initialization.

The microcontroller can change the configuration of the window watchdog during the “Long Open Window” to change the trigger selection as well as the times for the “Open” and “Closed Window”. With a reconfiguration the window watchdog will be restarted with the new configuration. A “Open Window” will be started accordingly, expecting a valid triggering by the selected triggering input.

If no valid triggering or configuration of the watchdog takes place during the “Long Open Window”, the window watchdog recognizes an “invalid WWD triggering”. If the INIT timer expires with an invalid WWD triggering present, a so-called “Soft Reset” will be issued. After the so-called “Soft-Reset” the window watchdog opens a new “Long Open Window”. This is not indicated by interrupt. The repetition of “Long Open Windows” is limited. Should within the second “Long Open Window” the window watchdog not be triggered correctly, a normal or “hard” reset will occur, which means that pin ROT goes to zero and the post regulator output voltages will be switched off. After the third “Long Open Window” without valid triggering in a row the state machine will bring the device into “FAILSAFE state (for details please refer to chapter State machine).

Normal Operation

A trigger signal within the "Long Open Window" will terminate the "Long Open Window" and start the "Closed Window". The "Closed Window" has a fixed duration for operation without invalid triggering.. During normal operation no valid trigger signal is allowed during the "Closed Window”. If a valid trigger signal is received within the “Closed Window”, the window watchdog recognizes “invalid WWD triggering”. The “Closed Window” will be terminated with this invalid triggering and an “Open Window” will be started.

An “invalid WWD triggering” will increment the window watchdog failure counter by two. This is indicated by interrupt.

After the “Closed Window” has ended, the window watchdog starts an “Open Window”.

Within the “Open Window” a valid trigger signal is expected. If a valid trigger signal is received within the "Open Window" the watchdog terminates the "Open Window" and starts the "Closed Window". “Valid WWD triggering”

will decrement the window watchdog failure counter by one in case it is greater than zero, this is not indicated by interrupt.

If no valid triggering should be received during the “Open Window”, the window watchdog recognizes “Invalid WWD triggering” and increments the window watchdog failure counter by two and a new “Open Window” is started. This is indicated by interrupt.

In normal operation, the watchdog continues to cycle between the "Open Window" and "Closed Window" as long as valid triggering is received.

Window watchdog output WWO

The window watchdog output WWO is an internal signal: It is connected to the safe window watchdog failure counter. The value of WWO is either “Valid WWD triggering” or “Invalid WWD Triggering”.

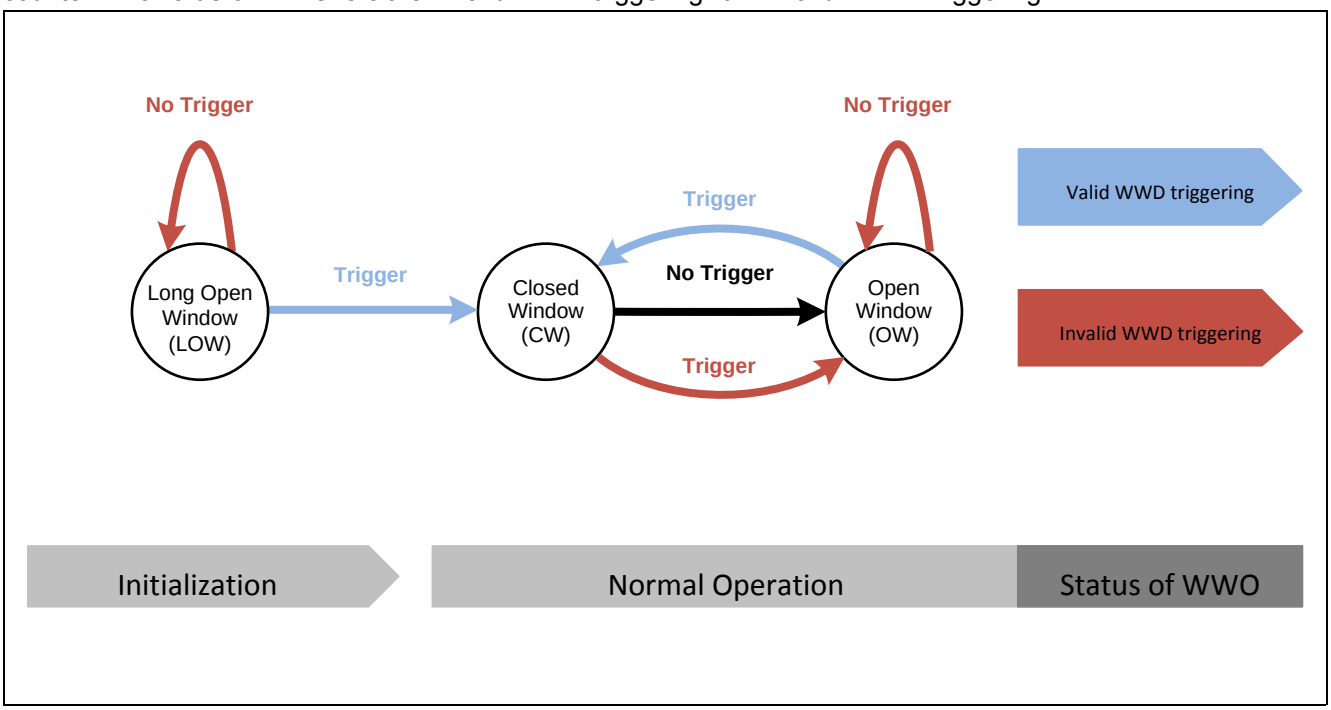


Figure79 Watchdog state diagram

Description:

- “Trigger” is either a SPI command to **WWDSCMD** register or a valid watchdog trigger at pin WDI
- “No Trigger” in the “Long open Window” is considered as “Invalid WWD triggering”, the watchdog opens again a ”Long Open Window”
- “Trigger” within the “Long Open Window” is considered as “Valid WWD triggering”, the watchdog closes the “Long Open Window” and opens the “Closed Window”
- “Trigger” within the “Closed Window” is considered as “Invalid WWD triggering”
- “No Trigger” within the “Closed Window” moves the watchdog to the “Open Window”, after the “Closed Window” has ended.
- “Trigger” within the “Open Window” is considered as “Valid WWD triggering”, the watchdog closes the “Open Window” and opens the “Closed Window”
- “No Trigger” in the “Open Window” is considered as “Invalid WWD triggering”,.

Window watchdog trigger pin WDI

The watchdog input pin WDI has an integrated pull-down current I_{WDI}. The watchdog input WDI can transition to high within the "Closed Window" or during the following "Open Window".

Valid Trigger Signal at WDI

Watchdog input WDI is periodically sampled with a period of T_{SAM}. A valid trigger signal is a falling edge from $V_{WDI,high}$ to $V_{WDI,low}$. To improve immunity against noise or glitches on the WDI input, at least two high samples followed by two low samples are required for a valid trigger signal, the valid triggering is considered with the second consecutive sampling point measuring low signal. For example, if the first three samples (two high one low) of the trigger pulse at pin WDI are inside the “Closed Window” and only the fourth sample (the second low sample) is taken in the “Open Window” then the watchdog output WWO will indicate “valid WWD triggering”.

Invalid Triggering at WDI

No trigger signal detected during the "Open Window" or a trigger signal detected during the "Closed Window", is considered invalid triggering. Watchdog output WDO indicates “invalid triggering” immediately after no valid trigger during the "Open Window" or immediately if a trigger signal is detected during the "Closed Window".

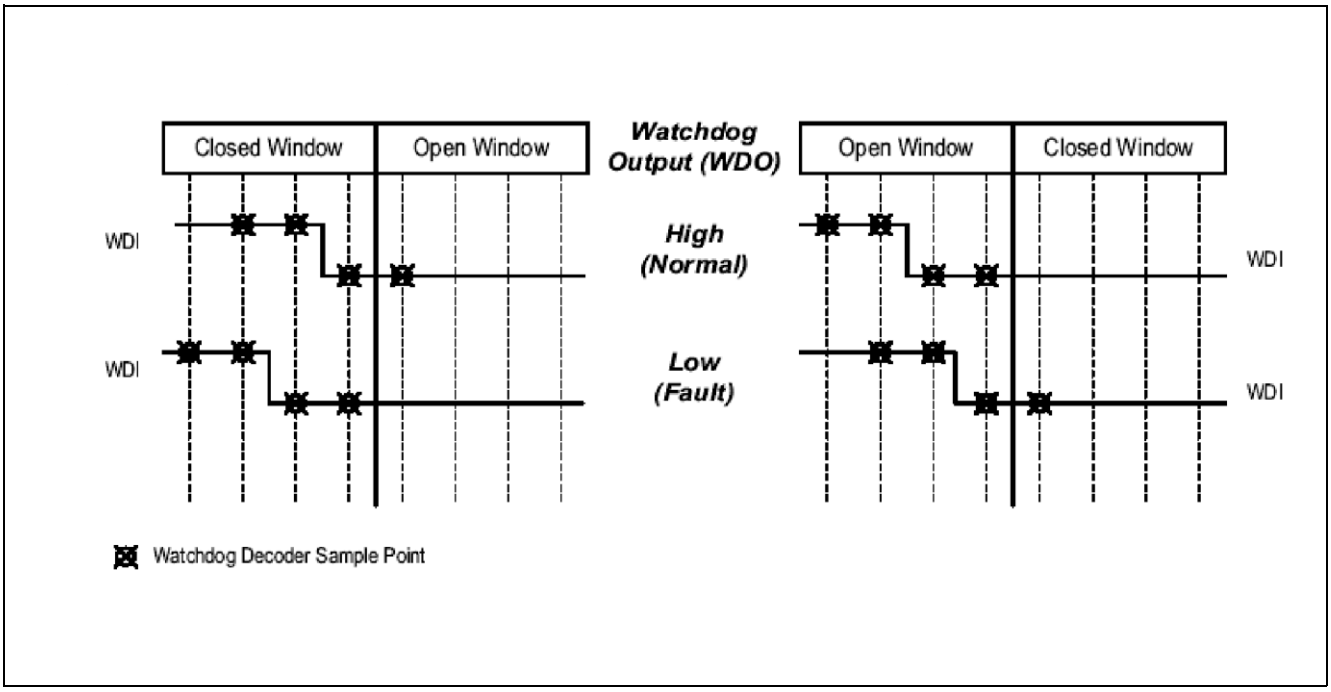


Figure 80 Valid and invalid trigger pulses at pin WDI

15.2.1 Timing Diagrams

15.2.1.1 Normal operation: Correct triggering

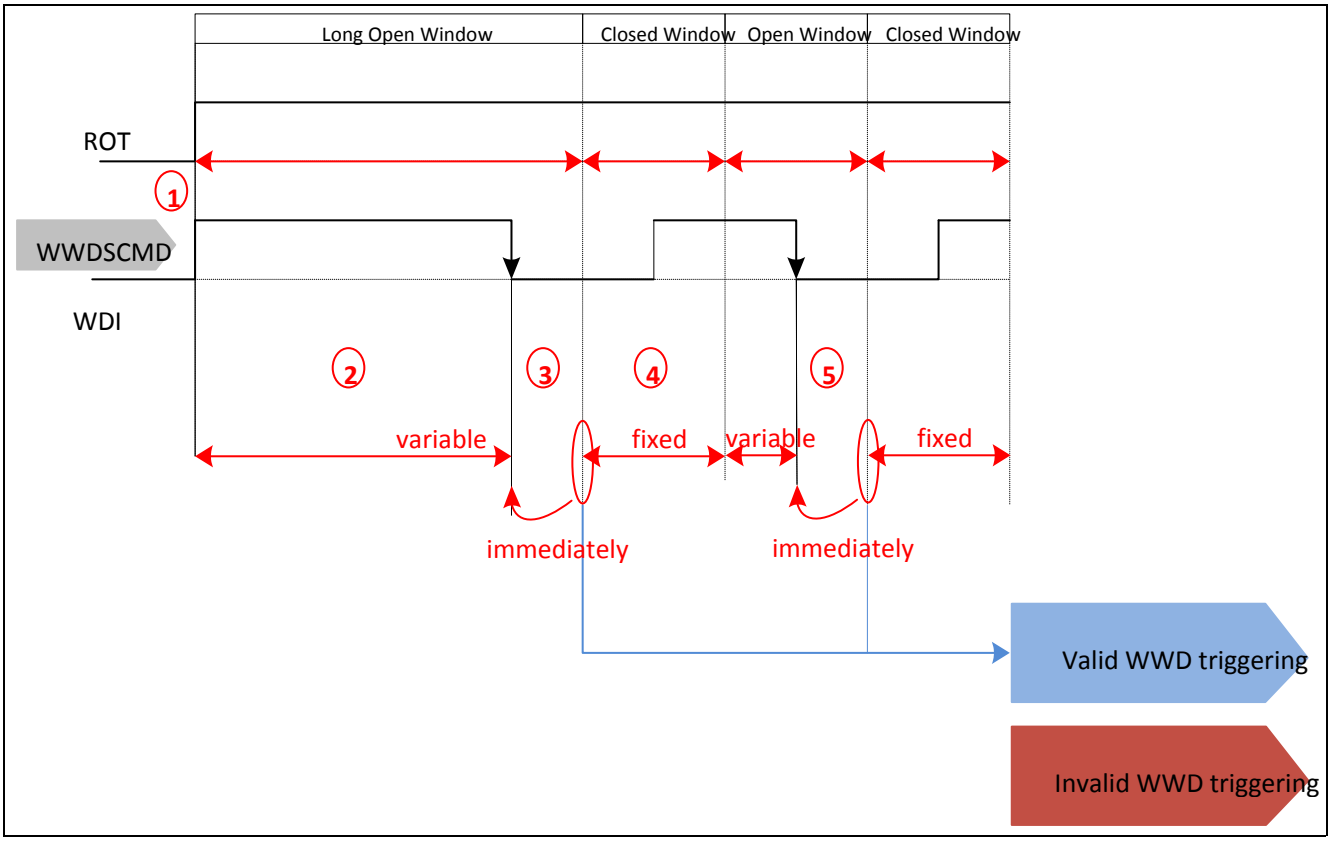


Figure 81 Normal operation: Correct triggering

1. The “Long Open Window” starts in INIT state if the reset output of ROT (monitoring the microcontroller related voltages) turned high. In case the window watchdog was deactivated in SLEEP, the first Open Window starts with the transition from SLEEP state to WAKE state which is indicated by interrupt. The time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60 ms (**WDCYC** = 0)
2. During the “Long Open Window” valid triggering of the WWD according to the configured trigger selection is expected. The maximum time of the “Long Open Window” is fixed, but it will be terminated as soon as a “Valid WWD triggering” is recognized.
3. The window watchdog will enter now the ”Closed Window”. After receiving this first valid trigger the device will be allowed to move from INIT to NORMAL state or from WAKE to NORMAL state.
4. The “Closed Window” has a fixed duration $t_{WD,CW}$ (can be determined by SPI command). It starts right after the valid trigger signal, that closes the “Open Window” or the “Long Open Window”. During the “Closed Window” no trigger signal should be applied. A transition from low to high at the WDI pin is not detected and will not lead to a trigger event,
5. A valid trigger signal terminates the “Open Window” immediately, thus the time of the “Open Window” is variable and depending on the time the microcontrollers schedules the triggering. This is counted as a “Valid WWD triggering”

15.2.1.2 Fault operation: No trigger in open window after initialization

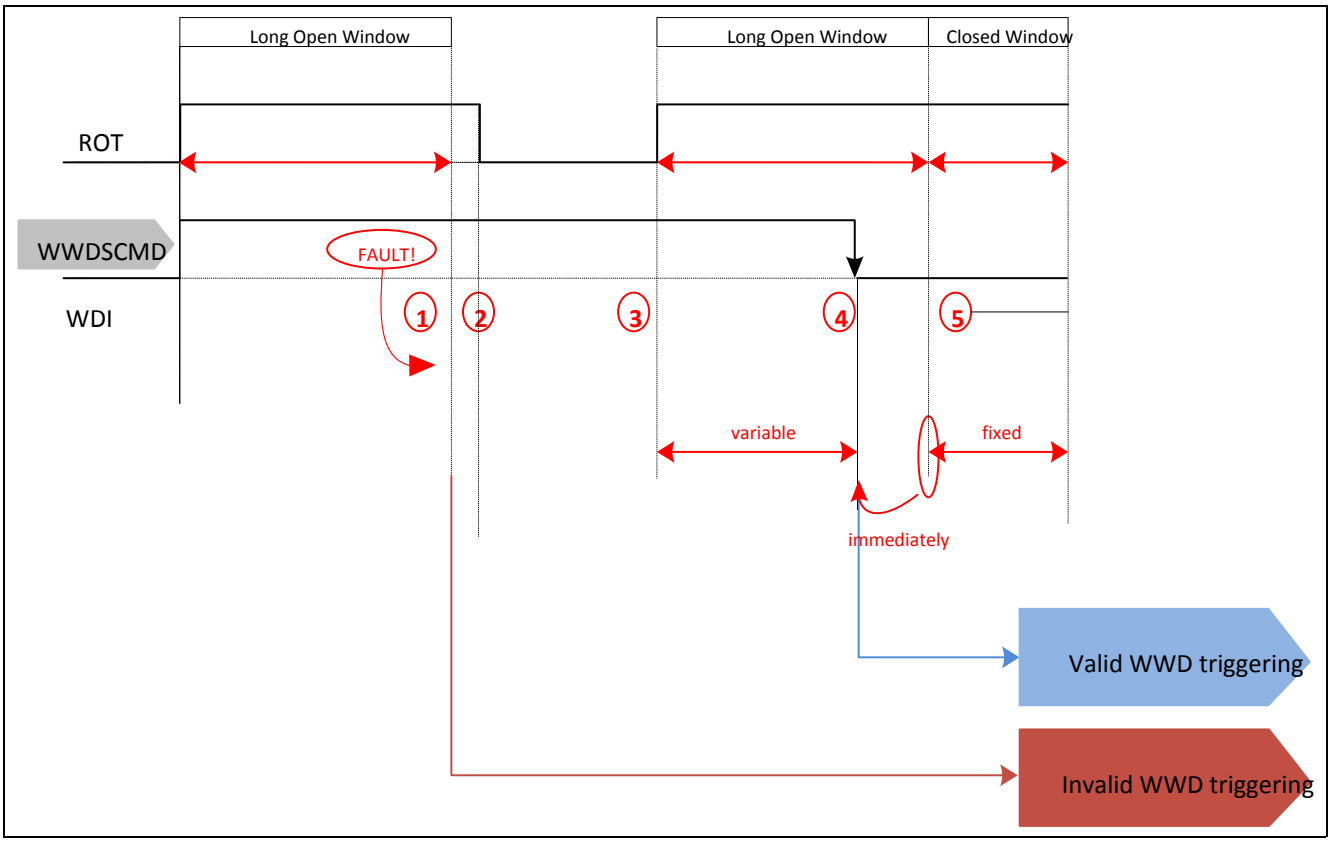


Figure 82 Fault operation: No trigger in Open Window after initialization

1. The initialization timeout and the long open window (LOW) do have the same typ. length. Usually this leads to the initialization timeout finishing at the slightly before or at same time as the LOW, which would skip the interrupt event (1). Even though due to the given accuracy, the missing valid triggering within the “Long Open Window” might lead to an interrupt event after the LOW has ended which is increasing the window watchdog failure counter by two.
2. The INIT state timer expires for the first time. As no valid triggering of the window watchdog was received during INIT state as expected, a so-called “Soft-Reset” will be issued: Pin ROT goes to zero, but the output voltages of the post regulators remain on.
   Additional information: In case the window watchdog should not be triggered correctly within the next “Long Open Window” of the following INIT phase, a “Hard-Reset” will be issued, which means pin ROT will go to zero and the output voltages will also be switched off. After a third invalid triggering during INIT phase the device will go into FAILSAFE state.
3. After the so-called “Soft-Reset” pin ROT turns high again after the power-on reset delay time t_{rd} and the watchdog opens a “Long Open Window” to give the microcontroller the chance to trigger and synchronize to the watchdog period.
4. A valid triggering terminates the “Long Open Window”, which makes the duration of the “Long Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
5. The following “Closed Window” lasts for the time $t_{WD,CW}$. Triggering within this time will be considered as an ”Invalid WWD triggering”.

15.2.1.3 Fault operation: No trigger in Open Window in steady state

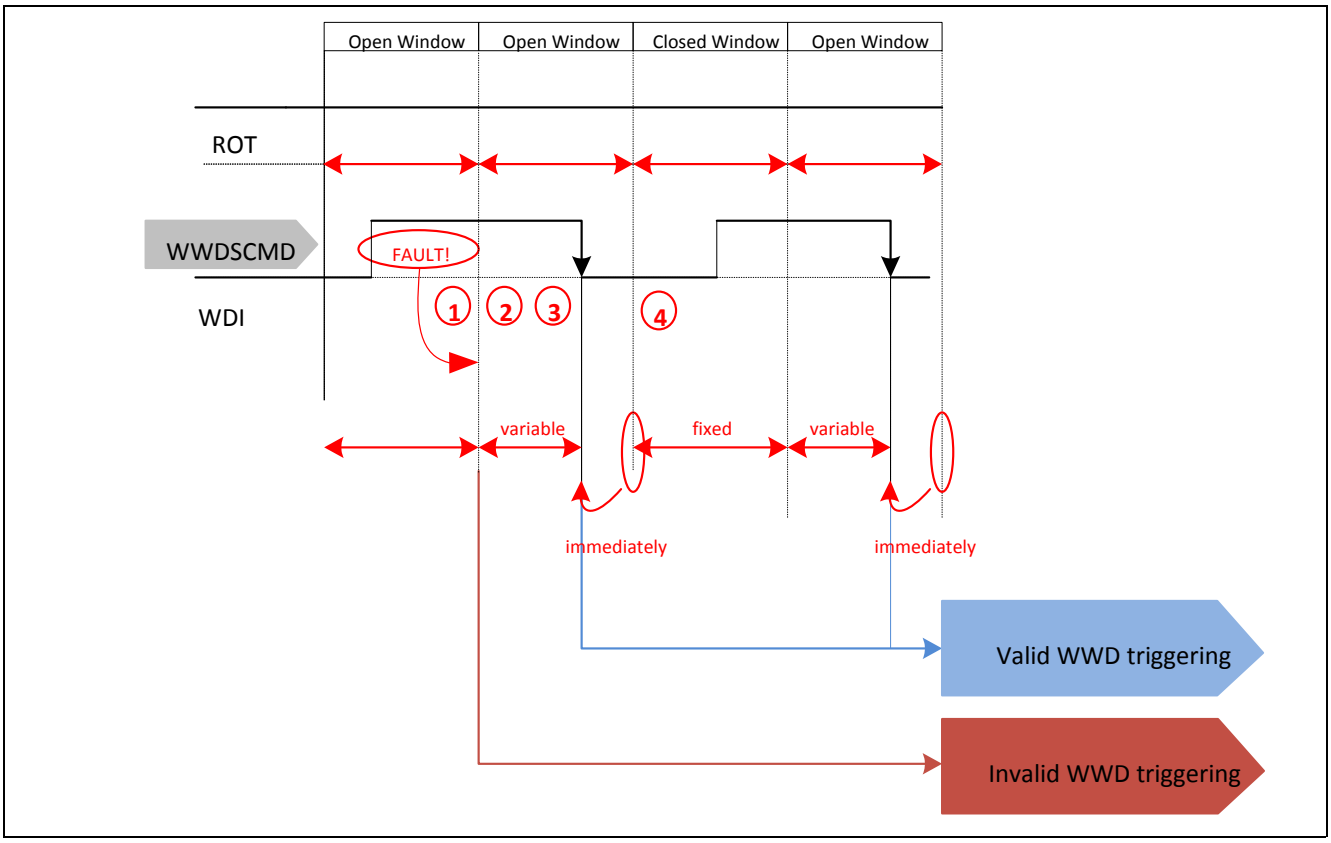


Figure 83 Fault operation: No trigger in Open Window in steady state

1. A missing valid triggering within the “Open Window” leads after the window has ended to an “Invalid WWD triggering”. This event is indicated by an interrupt, the window watchdog failure counter increases by two.
2. Having detected an “Invalid WWD triggering” the watchdog will start a new “Open Window” with duration $t_{WD,OW}$ to give the microcontroller the chance to trigger and synchronize to the watchdog period.
3. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started.
   The window watchdog failure counter will be decremented by one without an interrupt issued.
   Additional informations: In case of multiple “Invalid WWD triggering” within the “Open Windows”, the window watchdog failure counter would be incremented again by two until it reaches the configured threshold. In this case a reset will be issued.
4. The following “Closed Window” lasts for the time $t_{WD,CW}$. Triggering within this time will be considered as an ”Invalid WWD triggering”.

The behavior of pin ROT is depending on the value of Σ WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold Σ WWO.

15.2.1.4 Fault operation: False trigger in Closed Window after initialization

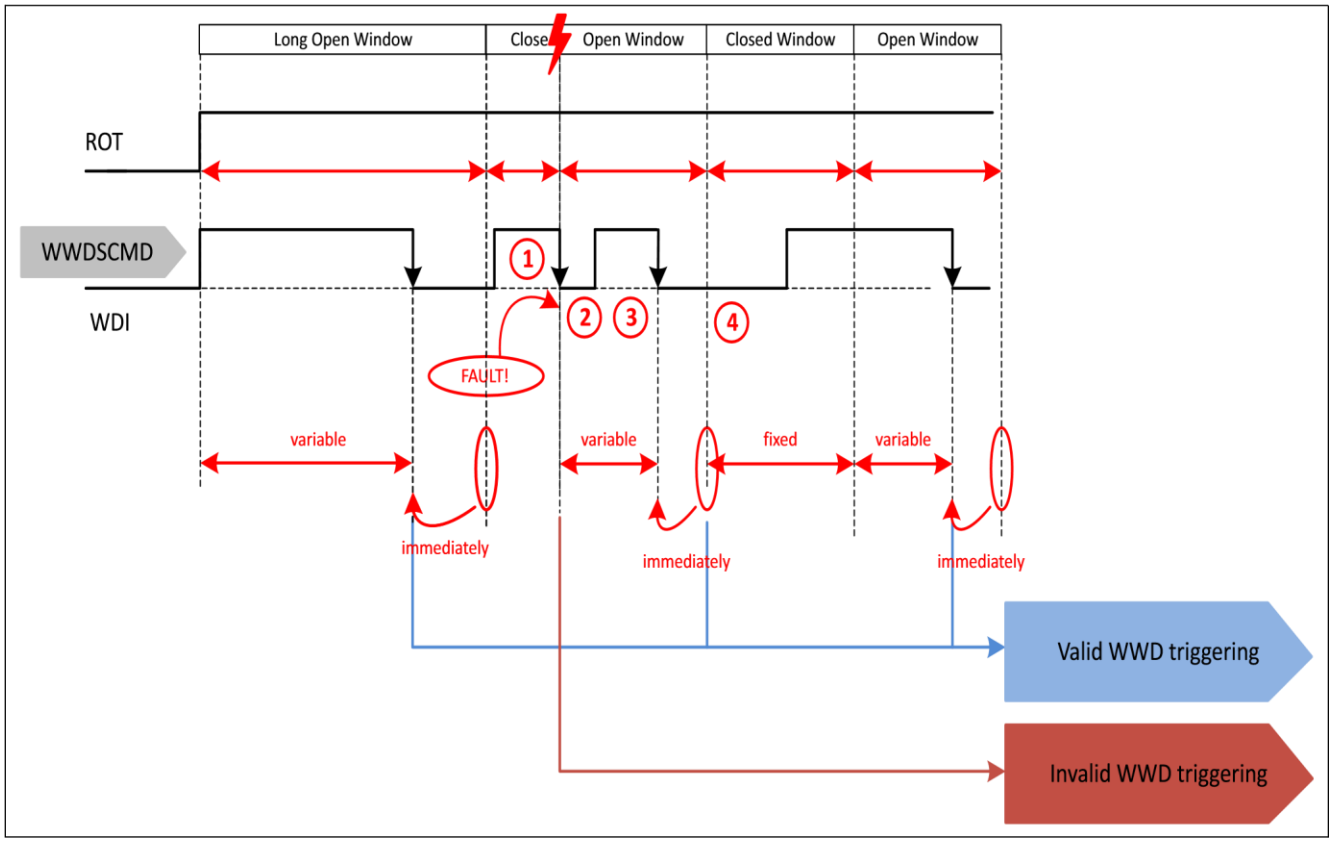


Figure 84 Fault operation: False trigger in Closed Window after initialization

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an interrupt and the window watchdog failure counter increases by two.
2. The “Closed Window” will be closed with the “Invalid WWD triggering”. Originally it would last for the time $t_{WD,CW}$. The false triggering terminates the “Closed Window” and starts an “Open Window” to give the micro processor the opportunity to synchronize to the window watchdog period.
3. Within this “Open Window” a valid triggering is expected. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
4. The following “Closed Window” lasts for the time $t_{WD,CW}$. Triggering within this time will be considered as an ”Invalid WWD triggering”.

The behavior of pin ROT is depending on the value of Σ WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold Σ WWO.

15.2.1.5 Fault operation: False trigger in Closed Window in steady state

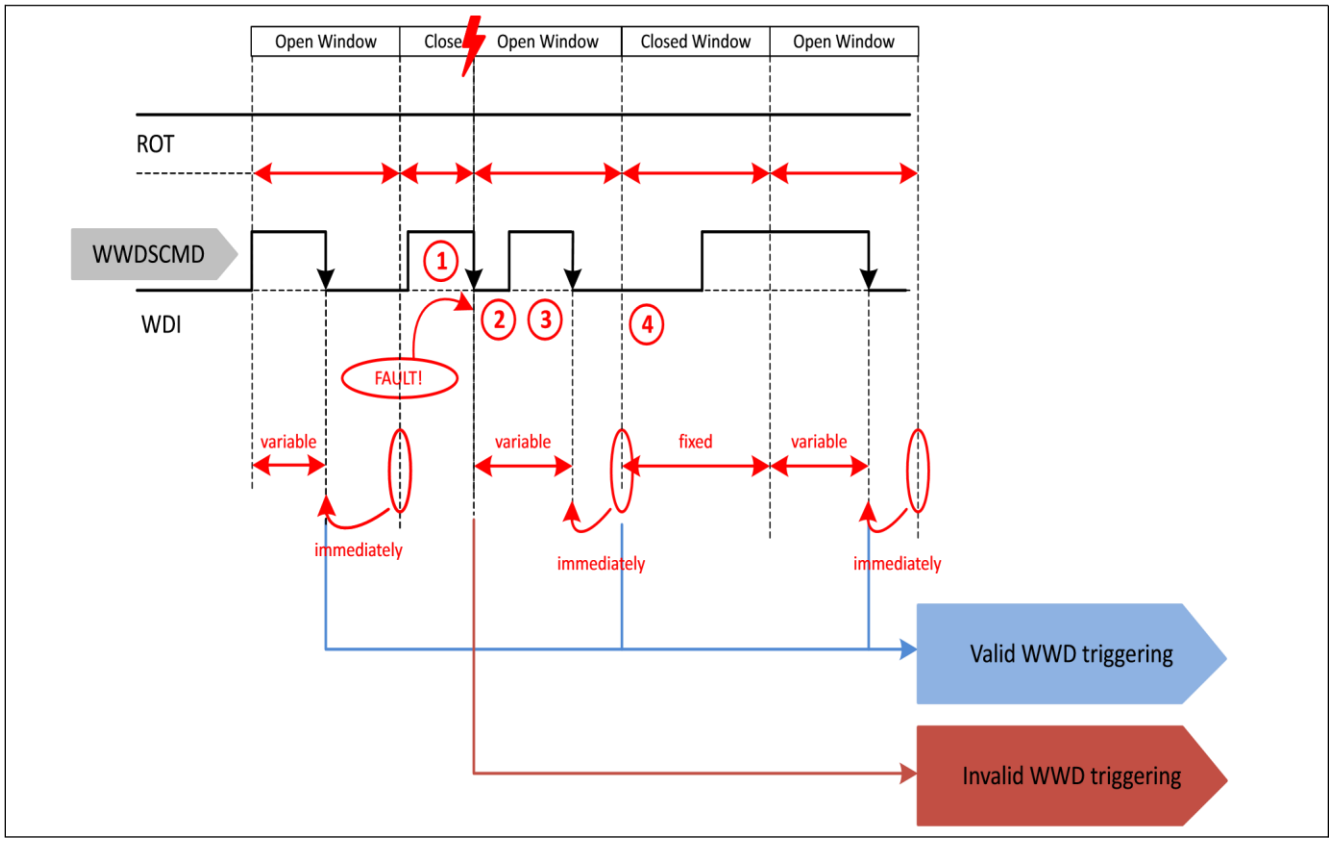


Figure 85 Fault operation: False trigger in Closed Window

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an interrupt and the window watchdog failure counter increases by two.
2. The “Closed Window” will be closed with the “Invalid WWD triggering”. Originally it would last for the time $t_{WD,CW}$. The false triggering terminates the “Closed Window” and starts an “Open Window” to give the micro processor the opportunity to synchronize to the window watchdog period.
3. Within this “Open Window” a valid triggering is expected. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
4. The following “Closed Window” lasts for the time $t_{WD,CW}$. Triggering within this time will be considered as an ”Invalid WWD triggering”.

The behavior of pin ROT is depending on the value of Σ WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold Σ WWO.

15.2.2 Electrical characteristics

Table 25 Electrical Characteristics: Window watchdog function

V_{VS} =6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
General timing parameters watchdog (WWD and FWD)							
Watchdog cycle time	t_{CYCLE}	94	100	106.5	µs	selectable by SPI command	P_15.2.2.1
Watchdog cycle time, default setting	t_{CYCLE}	940	1000	1065	µs	selectable by SPI command	P_15.2.2.2
Long open window time	t_{LOW}	564	600	639	ms	–	P_15.2.2.3
Watchdog input WDI							
Watchdog sampling time	t_{SAM}	188	200	213	µs	–	P_15.2.2.4
WDI valid high level	$V_{WDI, high}$	3.6	–	–	V	V_{WDI} increasing, V_{QUC} = 5.0 V	P_15.2.2.5
WDI valid low level	$V_{WDI, low}$	–	–	0.8	V	V_{WDI} decreasing, V_{QUC} = 5.0 V	P_15.2.2.6
WDI hysteresis	$V_{WDI, hyst}$	–	350	–	mV	V_{QUC} = 5.0 V	P_15.2.2.7
WDI valid high level	$V_{WDI, high}$	2.0	–	–	V	V_{WDI} increasing, V_{QUC} = 3.3 V	P_15.2.2.8
WDI valid low level	$V_{WDI, low}$	–	–	0.8	V	V_{WDI} decreasing, V_{QUC} = 3.3 V	P_15.2.2.9
WDI hysteresis	$V_{WDI, hyst}$	–	160	–	mV	V_{QUC} = 3.3 V	P_15.2.2.10
WDI pull-down current	I_{WDI}	–	150	330	µA	V_{WDI} = V_{QUC}	P_15.2.2.11
WDI input capacitance	C_{WDI}	–	4	15	pF	1)	P_15.2.2.12

1) Specified by design, not subject to production test

15.3 Functional Watchdog

Principle of Operation

A functional or question/answer watchdog is integrated in the TLF35584 to monitor the microcontroller. In a steady state a question is generated (taken out of table), in parallel the so called heartbeat counter starts counting from zero. The heartbeat counter counts up, until the heartbeat period has ended. The duration of the heartbeat period is set to a default value, but can be adjusted via SPI command. The question consists of 4 bits, the expected answer consists of 4 responses of 8 bits each. The four responses shall be sent before the heartbeat period has ended. The last response shall be written to the synchronized response register to reset the heartbeat counter.

Initialization

The functional watchdog is off per default when the device is powered up for the first time. It can be enabled by SPI writing to **WDCFG0.FWDEN**.

Configuration

The functional watchdog can be configured in INIT, NORMAL and WAKE state. “Configured” means:

- Modify the length of the heartbeat period by SPI command, depending on the needs of the application. (combination of cycle time **WDCYC** and number of cycles for heartbeat **WDHBTP**) •

The threshold for the functional watchdog failure counter overflow can defined by SPI

The heartbeat period is based on the cycle time t_{CYCLE} specified in **Table 25**.

Normal Operation

The question is taken out of the **Table 26**, the correct responses are listed in the same row. The sequence of responses must be kept and can be derived from the response counter **FWDSTAT0**.**FWDRSPC** before sending the response.

The response to the actual question defined in the table shall be composed by four subsequent response bytes. A correct response to the given question in **FWDSTAT0**.**FWDQUEST** register shall be done in the following way.

- The first three responses shall be written into **FWDRSP**
- The last response should be written into **FWDRSPSYNC** to reset the heartbeat timer All four responses must be written before the heartbeat period expires.

If the complete response (32 bits) is correct and if the last response byte was sent with synchronized respond, the heartbeat counter will be reset and set to zero. If the complete answer (all four responses - 32 bits) is correct, it is regarded as “Valid FWD triggering”, the functional watchdog error counter Σ FWO is decremented by 1. If the last response was sent with synchronized response, the heartbeat counter will be reset, but if the answer is wrong, this is regarded as “Invalid FWD triggering” and the functional watchdog error counter Σ FWO is incremented by 2.

An overflow of the functional watchdog error counter Σ FWO will trigger a “Move to INIT” event, reset the heartbeat counter and set the functional watchdog error counter Σ FWO to zero.

QUESTION	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74

C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

Table 26 Functional watchdog response definition

Functional watchdog output FWO

The functional watchdog output FWO is an internal signal: It is connected to the FWD failure counter. The value of the functional watchdog FWO output is either “Valid FWD triggering” or “Invalid FWD Triggering”.

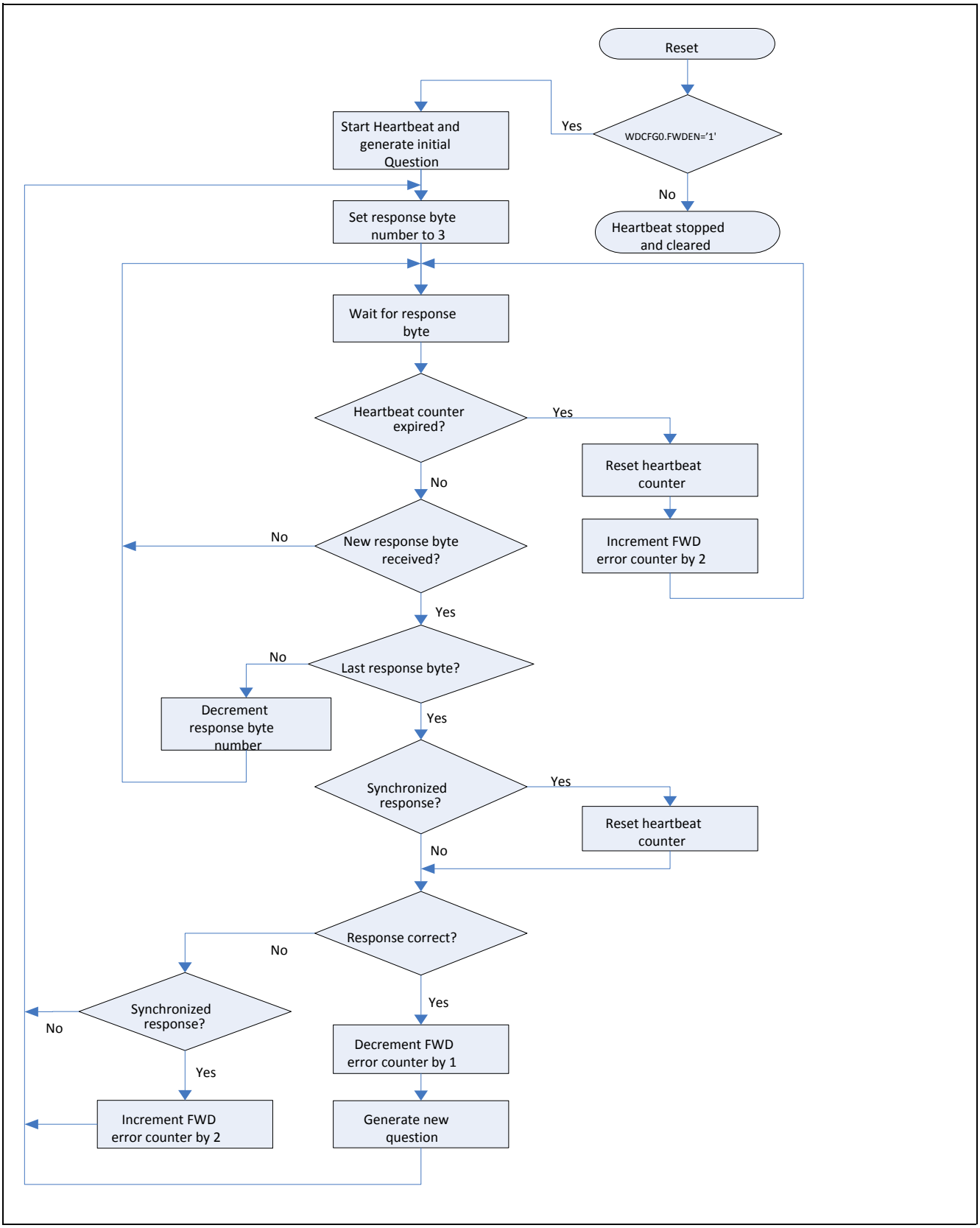


Figure 86 Functional watchdog flowchart diagram

15.3.1 Timing Diagrams

15.3.1.1 Normal operation: Correct triggering

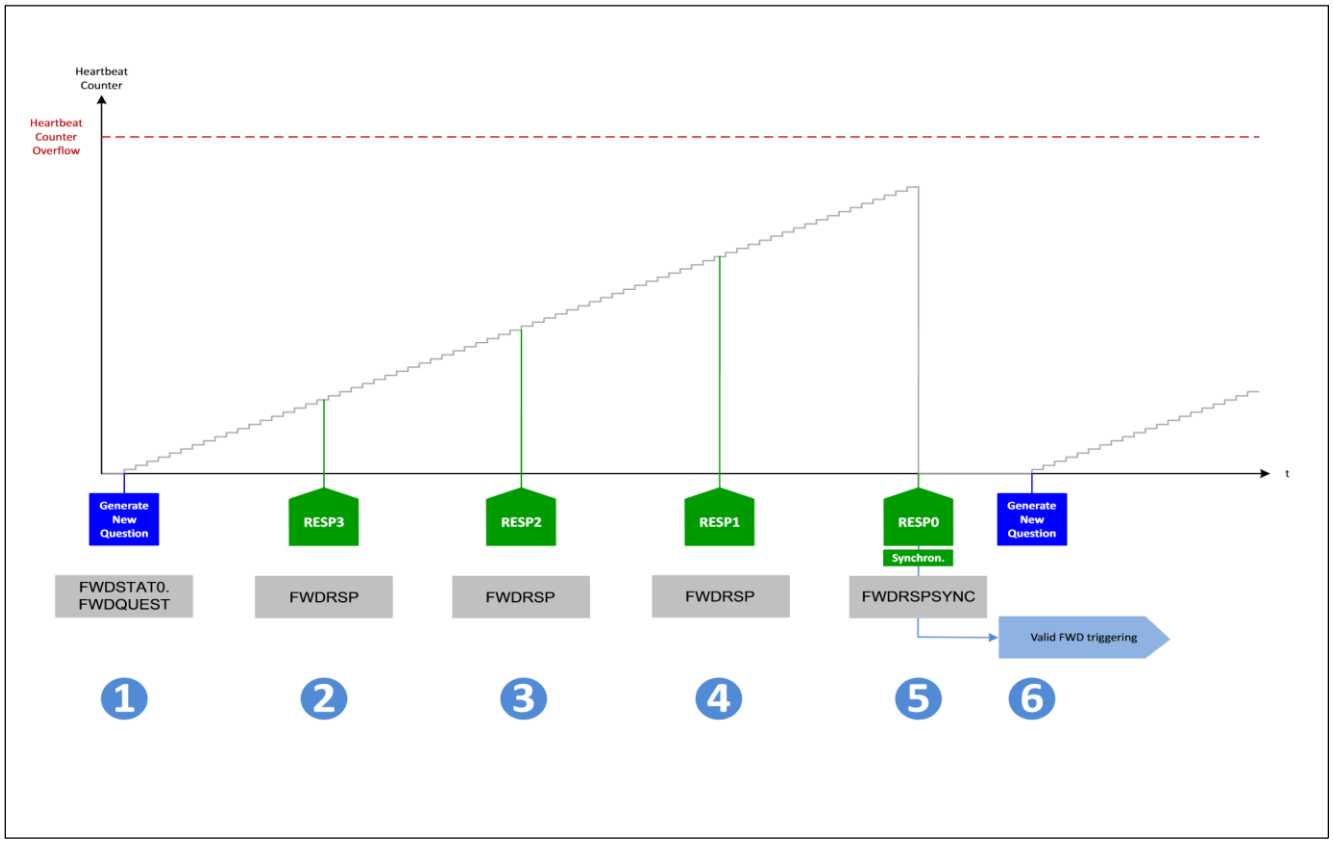


Figure 87 Normal operation: Correct triggering

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct synchronized response is received (RESP0). All responses are correct, the sequence of responses is correct and the last synchronized response was received before the heartbeat counter overflowed. The heartbeat counter will be reset (set to zero). This is regarded as “Valid FWD triggering”, the functional watchdog error counter Σ FWO is decremented by 1 (if the functional watchdog error counter value is higher than zero).
6. A new question is generated, in parallel the heartbeat counter starts counting up

15.3.1.2 Fault operation: Synchronization is missing

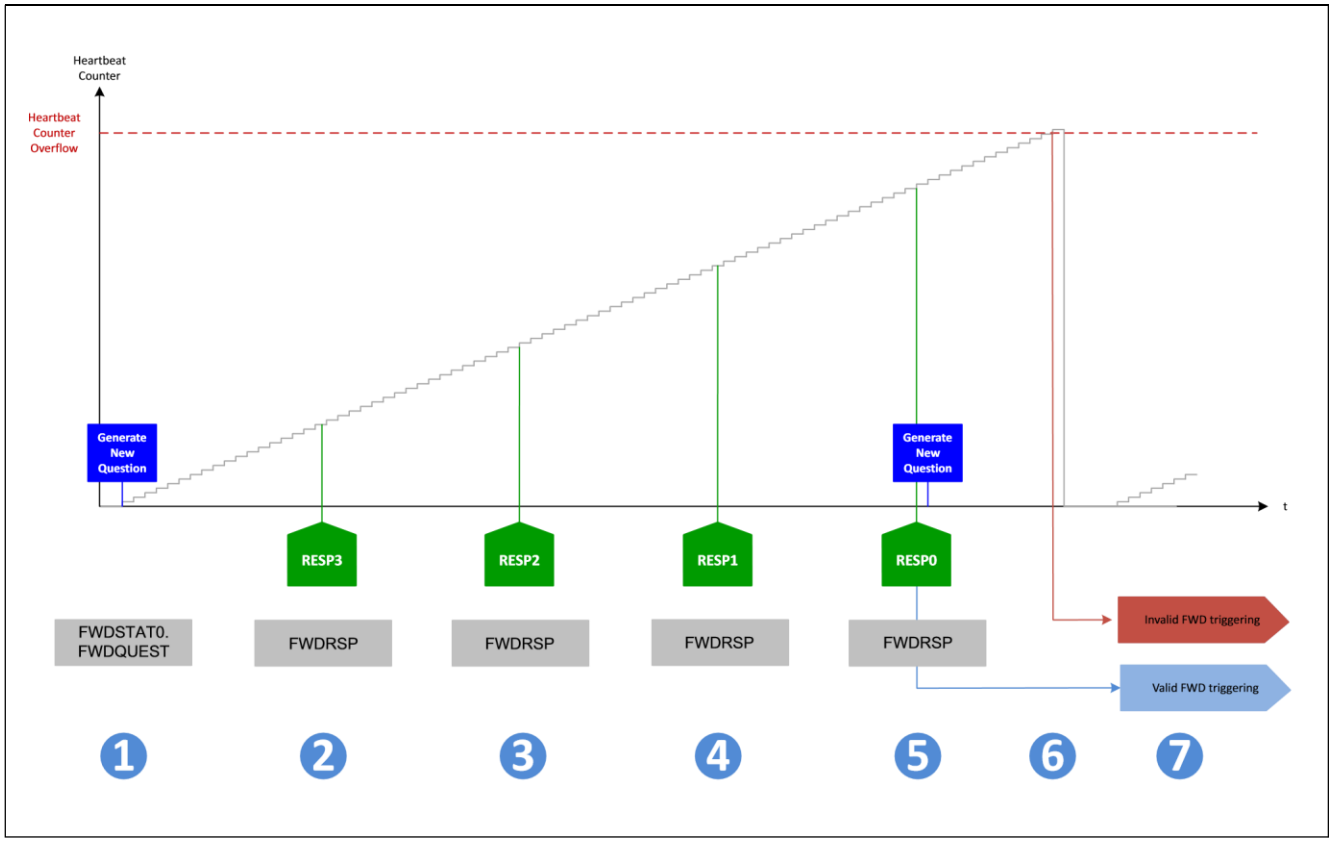


Figure 88 Fault operation: Synchronization is missing

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct response is received (RESP0), but not synchronized (written in wrong register). So far, all responses are correct, the sequence of responses is correct and the last not synchronized response was received before the heartbeat counter overflow occurred. The heartbeat counter will not be reset and continue to count. This is regarded as “Valid FWD triggering”, the functional watchdog error counter Σ FWO is decremented by 1 (if the functional watchdog error counter value is higher than zero). A new question is generated.
6. The heartbeat counter is still counting up, waiting for the answer on the new question. Later in time the heartbeat counter will expire and an overflow occurs. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter Σ FWO is incremented by 2. The heartbeat counter is reset.

7. The heartbeat counter starts counting up. No new question is generated.

15.3.1.3 Fault operation: Answer is wrong

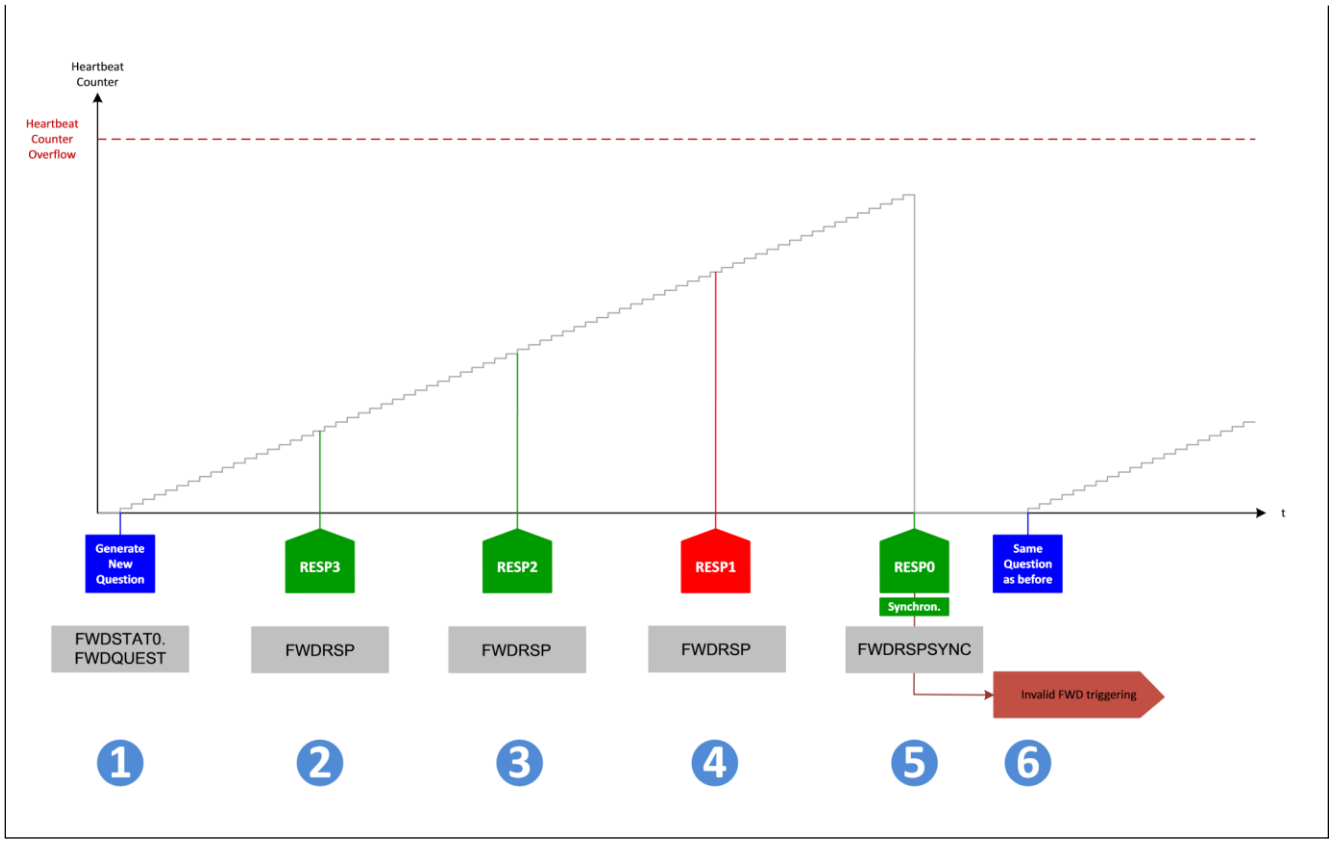


Figure 89 Fault operation: Answer is wrong

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before)
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. An incorrect response is received (RESP1)
5. A correct response is received (RESP0). The heartbeat counter will be reset (set to zero). The complete answer is not correct. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter Σ FWO is incremented by 2. The heartbeat counter is reset.
6. No new question is generated, but the heartbeat counter starts counting up.

Note: If i.e. RESP2 and RESP1 would be mixed, than both responses would be regarded as incorrect - the responses have to be sent in correct order.

15.3.1.4 Fault operation: Missing response

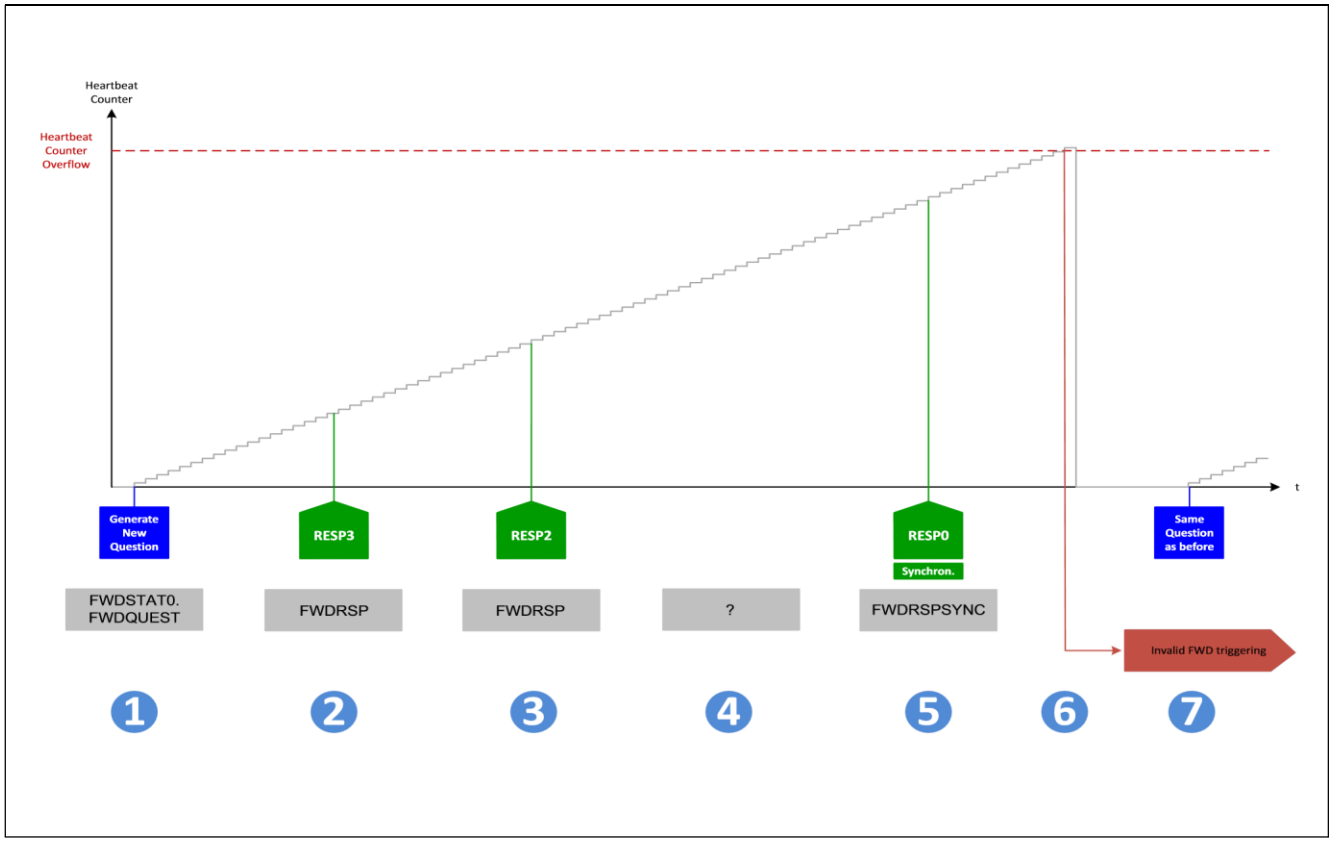


Figure 90 Fault operation: Answer is not complete

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A response is missing (RESP1)
5. A correct response is received (RESP0). So the last response is not the last response but the second last due to the missing response (in this example RESP1). The functional watchdog will wait for all four responses to be written, while the heartbeat counter keeps on counting. There is no fixed time for all four responses, but they must be sent in correct order before the heartbeat counter expires.
6. The complete answer is not correct due to missing response RESP1. Although the last response is synchronized, the heartbeat counter will not be reset and continue counting up until an overflow occurs. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter Σ FWO is incremented by 2. The heartbeat counter is reset.

7. No new question is generated and the heartbeat counter starts counting up.

16 Application Information

This is the description how the IC is used in its environment

Note:The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

- Please contact us for addtional supportive documentation.
- For further information you may contact **http://www.infineon.com/**

Note:This following figure is a very simplified example of an application circuit. The function must be verified in the real application.

Table 27 Recommended values for parts in application diagram

Name	Value	Switching frequency range
Inductor step up	22 µH	500 kHz
Capacitor step up	100 µF	500 kHz
Filter inductor step down	4.7 µH	2.2 MHz
filter capacitor step down	10 - 47 µF	2.2 MHz
Filter inductor step down	22 µH	400 kHz
filter capacitor step down	68 - 100 µF	400 kHz

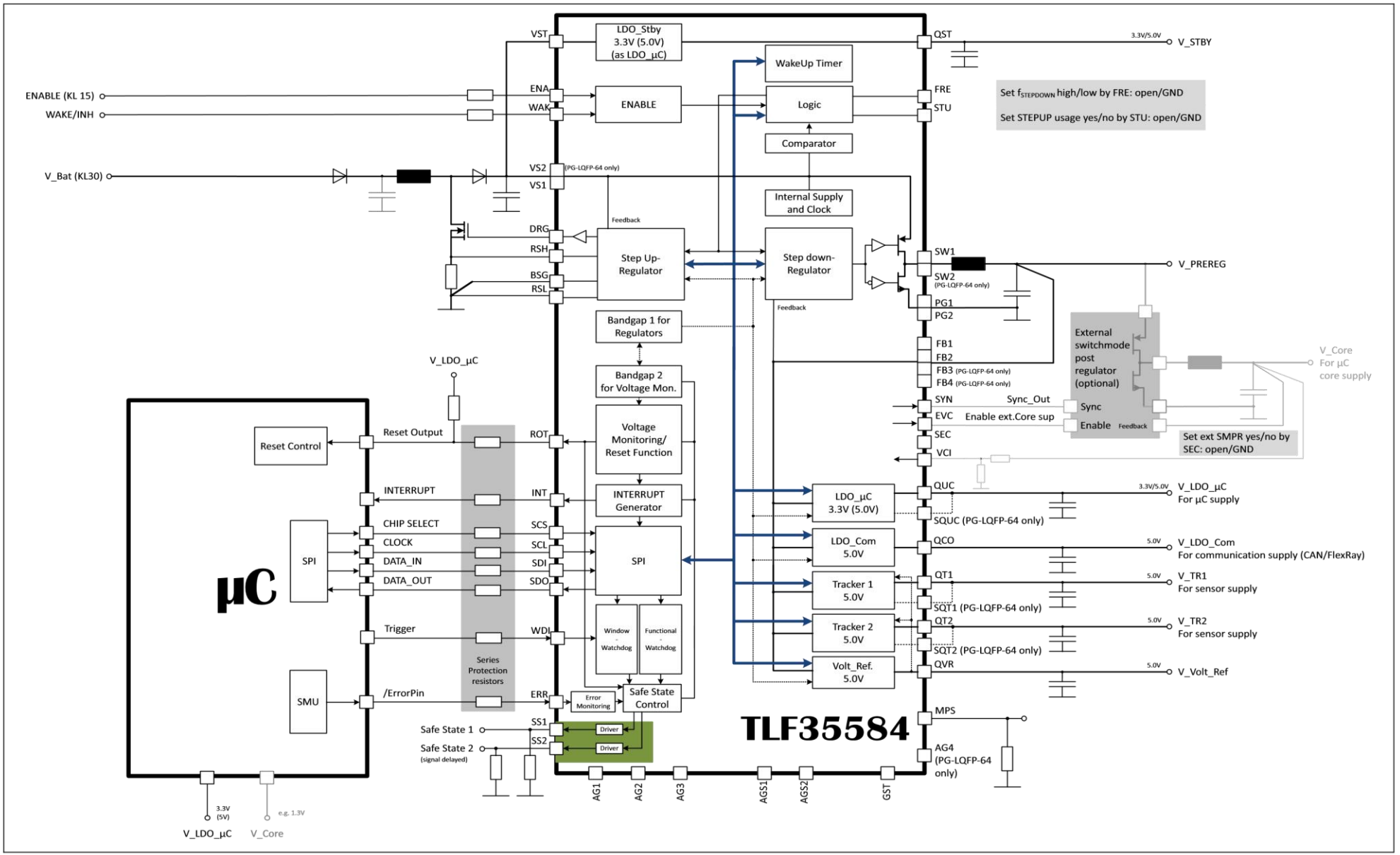


Figure 91 Application Diagram

17 Package Outlines

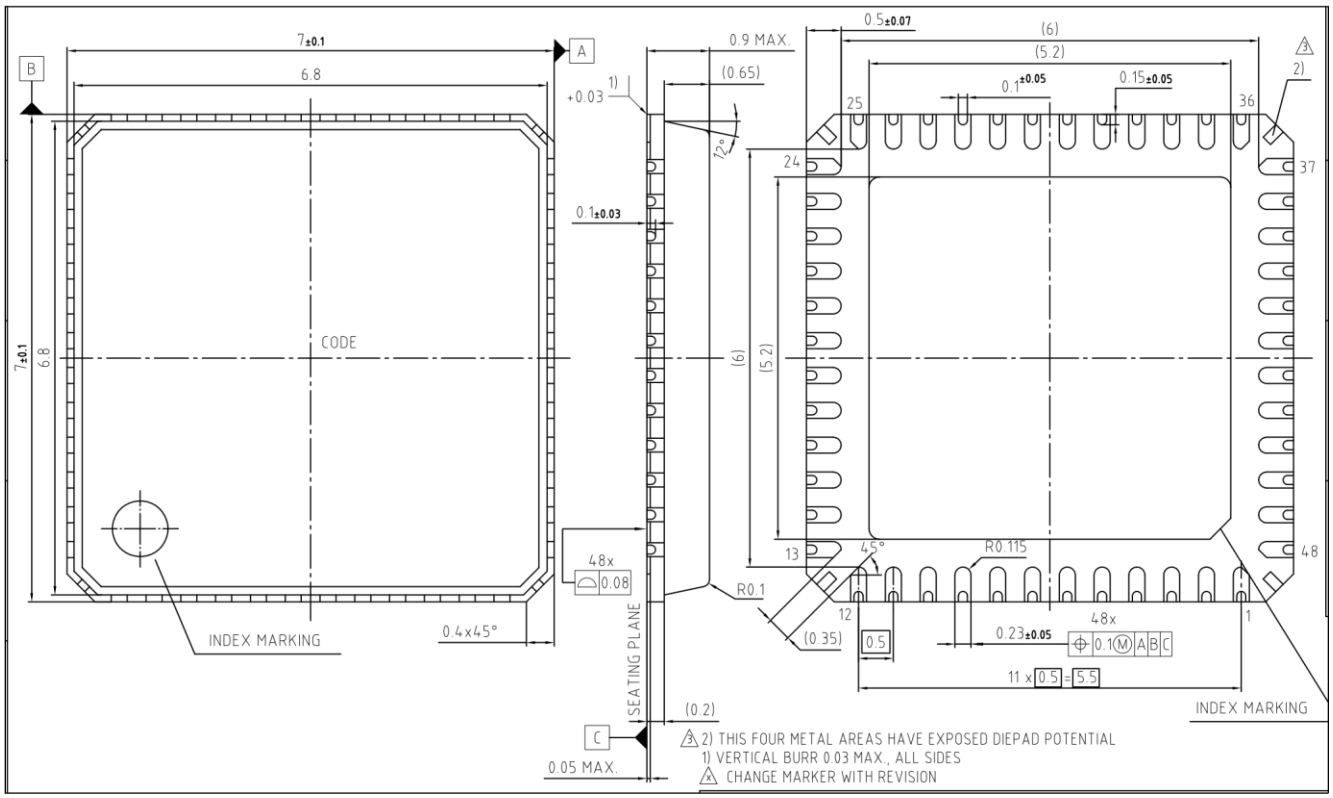


Figure 92 PG-VQFN-48

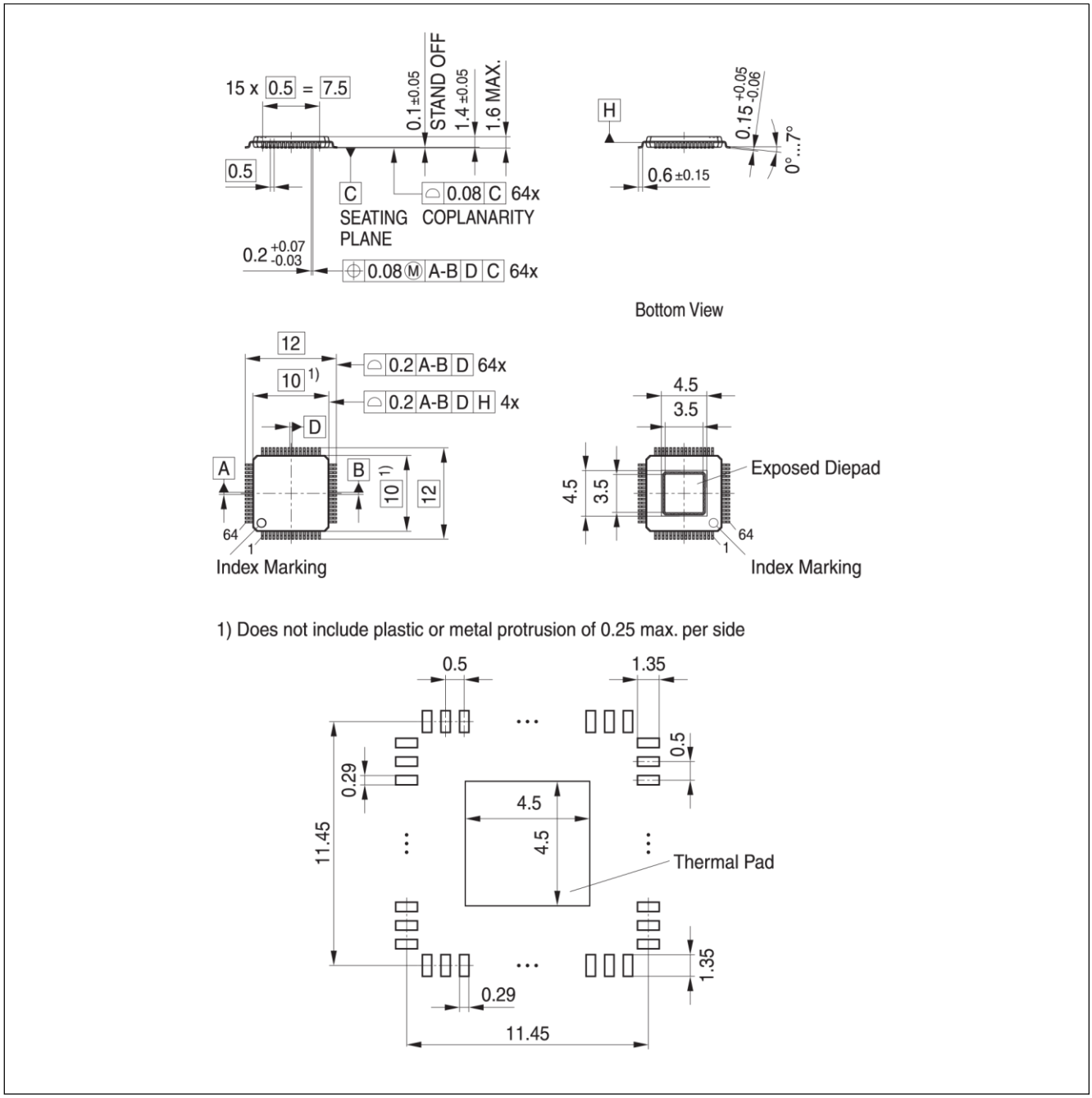


Figure 93 PG-LQFP-64

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb?free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

Revision History

18 Revision History

Revision	Date	Changes
2.0	2017-03-16	Data sheet for TLF35584 C14 silicon. **Page 6**: **Chapter 1**: Component marking changed. **Page 8**: **Chapter 3**: Pin Assignment changed: PG-VQFN-48: Pins 44, 45, 39, 36, 35 and 34 changed to internally not connected. Corresponding update of figures, text and tables: **Figure 1**, **Figure 2**, **Chapter 3.2**, **Figure 3**, **Chapter 3.4**, **Figure 7**, **Figure 8**, **Figure 9**, **Figure 10**, **Figure 11**, **Figure 12**, **Figure 13**, **Figure 14**, **Chapter 8** **Page 8**: **Chapter 3**: Voltage $V_{S1/2}$ changed to V_{VS} in the entire document. **Page 31**: **Figure 8**: Pin AG5 (typo) removed from figure. **Page 34**: **Chapter 6.3.2**: **Table 8**: Highside Rdson changed from 580 to 630 mΩ. **Page 45**: **Chapter 7.2.2**: **Table 10**: $PSRR_{QUC}$ test condition corrected. **Page 51**: **Chapter 7.3.2**: **Table 11**: $PSRR_{QCO}$ test condition corrected. **Page 54**: **Figure 13**: Typo corrected. **Page 54**: **Chapter 7.4.2**: **Table 12**: $PSRR_{QVR}$ test condition corrected. **Page 57**: **Chapter 7.5.2**: **Table 13**: $PSRR_{QTx}$ test condition corrected. **Page 78**: **Figure 23**: Typo corrected. **Page 221**: **Figure 77**: INTMISS flag behavior in case of multiple events corrected. All pages: Figures corrected to imply pin configuration for both package variants (**Figure 7**, **Figure 8**, **Figure 9**, **Figure 10**, **Figure 11**, **Figure 12**, **Figure 13**, **Figure 14**, **Figure 91**).
1.0	2016-02-15	Initial release of Data Sheet.

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