PRELIMINARY

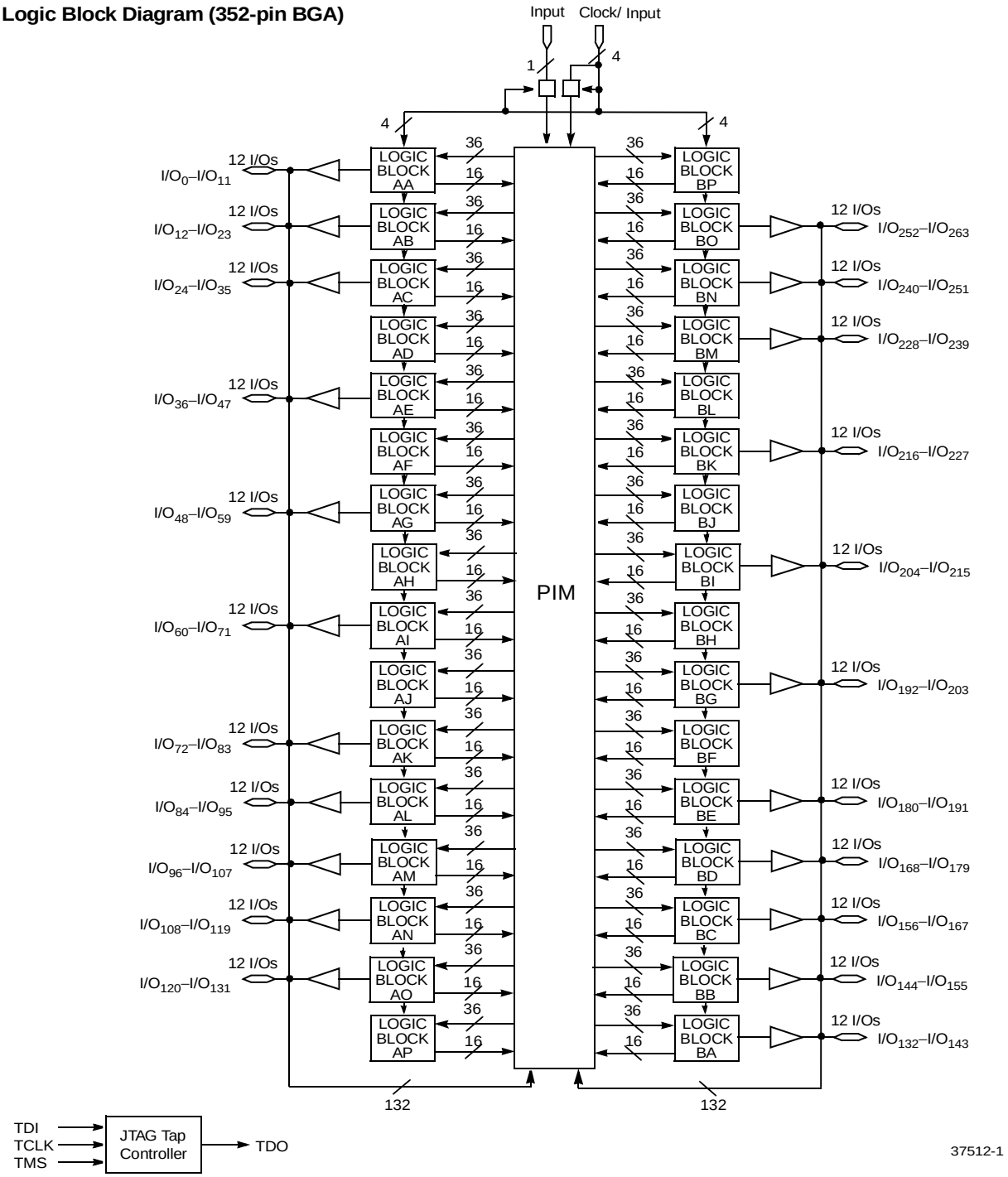
CY37512

UltraLogic™ 512-Macrocell ISR™ CPLD

Features

- 512 macrocells in 32 logic blocks
- In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- Up to 264 I/Os
  - plus 5 dedicated inputs including 4 clock inputs
- High speed
  - f_{MAX} = 125 MHz
  - t_{PD} = 10 ns
  - t_S = 5.5 ns
  - t_{CO} = 6 ns
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- 5V and 3.3V I/O capability
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant
- Available in 208-pin PQFP and 256/352-lead BGA packages
- Pinout compatible with the CY37512V, 37256/37256V, CY37384/37384V

Logic Block Diagram (352-pin BGA)



Selection Guide

	CY37512-154	CY37512-143	CY37512-125	CY37512-83
Maximum Propagation Delay, t_{PD} (ns)	7.5	8.5	10	15
Minimum Set-Up, t_S (ns)	5	5.0	5.5	8.0
Maximum Clock to Output, t_{CO} (ns)	4.5	6.0	6.5	8.0
Typical Supply Current, I_{CC} (mA) in Low Power Mode	240	240	240	240

Shaded areas contain advanced information.

Functional Description

The CY37512 is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37512 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

# of Pins	# Buried Macrocells	# I/O Macrocells	Package Types
208	352	160	PQFP
256	320	192	BGA
352	248	264	BGA

For a more detailed description of the architecture and features of the CY37512 see the Ultra37000 family data sheet.

Fully Routable with 100% Logic Utilization

The CY37512 is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

Simple Timing Model

The CY37512 features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low Power Operation

Each Logic Block of the CY37512 can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes approximately 50% less power and slows down by t_{LP}.

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

3.3V or 5V I/O Operation

The CY37512 operates with a 5V supply, and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. A nominal timing delay is incurred on output buffers when V_{CCO} is set to 3.3V. This device requires 5V ISR programming.

In System Reprogramming

The CY37512 can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37512 can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3*™ programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to InSRkit: ISR Programming data sheet (CY3600i).

User-Programmable Bus Hold

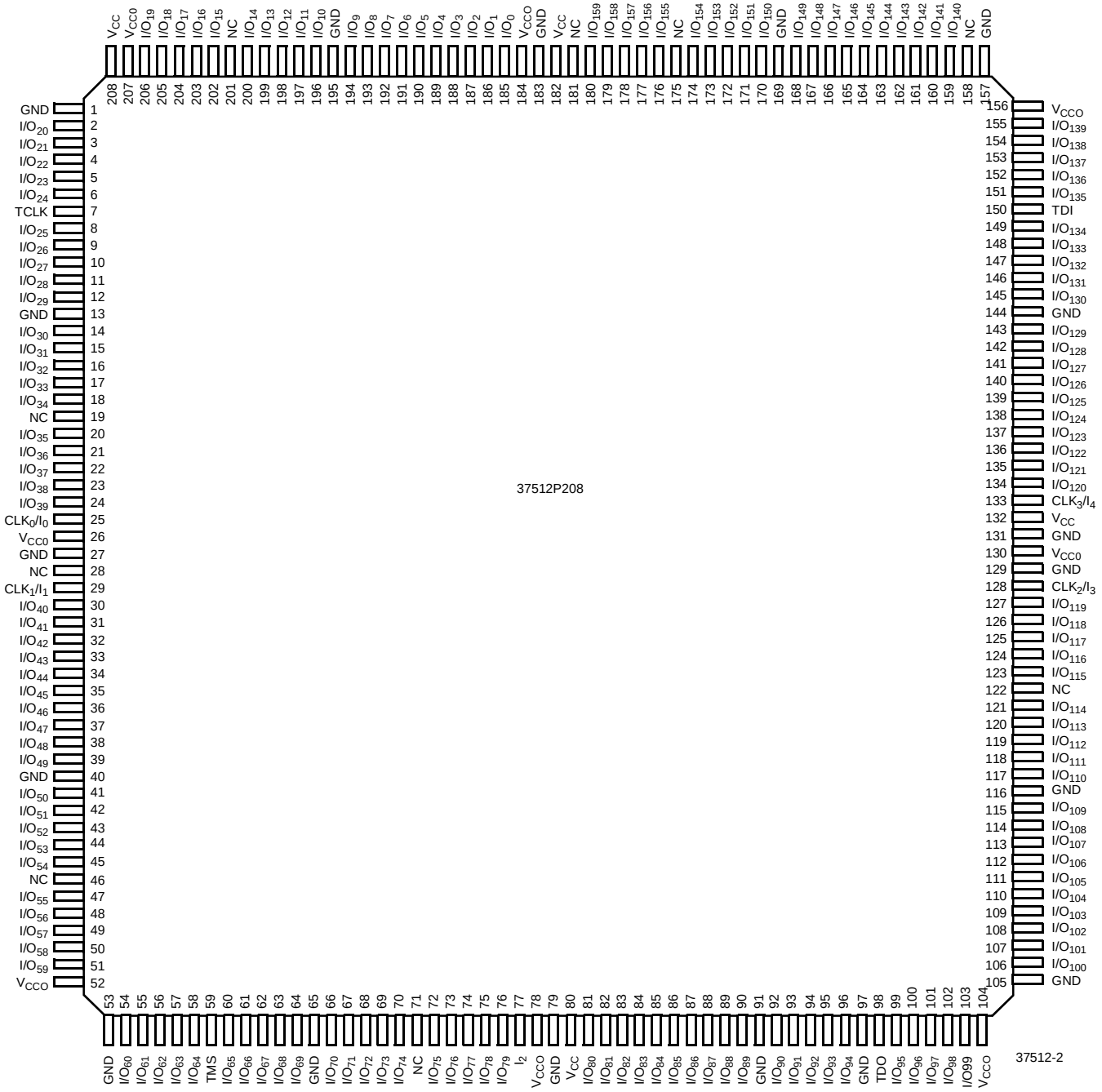
All outputs of the CY37512 can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

Design Tools

Development software for the CY37512 is available from Cypress's *Warp*™ or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

Pin Configurations

208-pin PQFP/CQFP
Top View



Pin Configurations (continued)

256-ball BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_{9}	I/O_{7}	I/O_{4}	I/O_{0}	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{1}	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_{6}	I/O_{2}	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_{3}	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

***NOTE: Center pins must be connected to GND to aid thermal dissipation.**

Pin Configurations (continued)

352-ball BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	GND	I/O_{19}	I/O_{15}	I/O_{13}	I/O_{34}	I/O_{31}	I/O_{28}	I/O_{25}	I/O_{10}	I/O_{7}	I/O_{4}	I/O_{1}	I/O_{263}	I/O_{260}	I/O_{257}	I/O_{254}	I/O_{239}	I/O_{237}	I/O_{232}	I/O_{229}	I/O_{250}	I/O_{248}	I/O_{244}	GND	GND	A
B	GND	NC	I/O_{18}	I/O_{17}	I/O_{14}	I/O_{35}	I/O_{32}	I/O_{29}	I/O_{26}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{2}	V_{CC}	I/O_{261}	I/O_{258}	I/O_{255}	I/O_{252}	I/O_{234}	I/O_{231}	I/O_{228}	I/O_{249}	I/O_{246}	I/O_{245}	I/O_{240}	GND	B
C	I/O_{23}	I/O_{38}	I/O_{37}	I/O_{16}	I/O_{12}	I/O_{33}	I/O_{30}	I/O_{27}	I/O_{24}	I/O_{9}	I/O_{6}	I/O_{3}	I/O_{0}	I/O_{262}	I/O_{259}	I/O_{256}	I/O_{253}	I/O_{238}	I/O_{235}	I/O_{233}	I/O_{230}	I/O_{251}	I/O_{247}	I/O_{225}	I/O_{224}	I/O_{227}	C
D	I/O_{39}	I/O_{40}	I/O_{36}	NC	NC	I/O_{21}	I/O_{20}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{236}	I/O_{243}	NC	NC	I/O_{226}	I/O_{222}	I/O_{223}	D
E	I/O_{42}	TCK	I/O_{41}	NC																			NC	TDI	I/O_{221}	I/O_{220}	E
F	I/O_{45}	I/O_{44}	I/O_{43}	I/O_{22}																			I/O_{242}	I/O_{219}	I/O_{218}	I/O_{217}	F
G	I/O_{48}	I/O_{47}	I/O_{46}	I/O_{63}																			I/O_{241}	I/O_{216}	I/O_{215}	I/O_{214}	G
H	I/O_{49}	I/O_{50}	I/O_{51}	V_{CCO}																			V_{CCO}	I/O_{211}	I/O_{212}	I/O_{213}	H
J	I/O_{52}	I/O_{53}	I/O_{54}	V_{CCO}																			V_{CCO}	I/O_{208}	I/O_{209}	I/O_{210}	J
K	I/O_{55}	I/O_{56}	I/O_{57}	NC																			NC	I/O_{205}	I/O_{206}	I/O_{207}	K
L	I0	I/O_{59}	I/O_{58}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{204}	I4	I/O_{197}	L
M	I/O_{61}	I/O_{60}	I1	GND							GND	GND	GND	GND	GND	GND							GND	I3	I/O_{203}	I/O_{202}	M
N	I/O_{64}	V_{CC}	I/O_{62}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{201}	I/O_{200}	I/O_{199}	N
P	I/O_{65}	I/O_{66}	I/O_{67}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{196}	V_{CC}	I/O_{198}	P
R	I/O_{68}	I/O_{69}	I/O_{70}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{193}	I/O_{194}	I/O_{195}	R
T	I/O_{71}	I/O_{84}	I/O_{85}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{178}	I/O_{179}	I/O_{192}	T
U	I/O_{88}	I/O_{87}	I/O_{86}	NC																			NC	I/O_{177}	I/O_{176}	I/O_{175}	U
V	I/O_{91}	I/O_{90}	I/O_{89}	V_{CCO}																			V_{CCO}	I/O_{174}	I/O_{173}	I/O_{172}	V
W	I/O_{94}	I/O_{93}	I/O_{92}	V_{CCO}																			V_{CCO}	I/O_{171}	I/O_{170}	I/O_{169}	W
Y	I/O_{95}	I/O_{72}	I/O_{73}	I/O_{110}																			I/O_{153}	I/O_{190}	I/O_{191}	I/O_{168}	Y
AA	I/O_{74}	I/O_{75}	I/O_{76}	I/O_{111}																			I/O_{152}	I/O_{187}	I/O_{188}	I/O_{189}	AA
AB	I/O_{77}	I/O_{78}	I/O_{79}	N/C																			NC	I/O_{184}	I/O_{185}	I/O_{186}	AB
AC	I/O_{81}	I/O_{80}	I/O_{108}	N/C	NC	I/O_{112}	I/O_{113}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{150}	I/O_{151}	NC	NC	I/O_{155}	I/O_{183}	I/O_{182}	AC
AD	I/O_{109}	I/O_{82}	I/O_{83}	I/O_{117}	I/O_{97}	I/O_{100}	I/O_{102}	I/O_{105}	I/O_{120}	I/O_{123}	I/O_{126}	I/O_{129}	I2	I/O_{133}	I/O_{136}	I/O_{139}	I/O_{142}	I/O_{157}	I/O_{159}	I/O_{161}	I/O_{163}	I/O_{166}	I/O_{146}	I/O_{180}	I/O_{181}	I/O_{154}	AD
AE	GND	NC	I/O_{115}	I/O_{116}	I/O_{119}	I/O_{98}	I/O_{101}	I/O_{103}	I/O_{106}	I/O_{121}	I/O_{124}	I/O_{127}	V_{CC}	I/O_{130}	I/O_{134}	I/O_{137}	I/O_{140}	I/O_{143}	I/O_{160}	I/O_{162}	I/O_{165}	I/O_{144}	I/O_{147}	I/O_{148}	NC	GND	AE
AF	GND	GND	I/O_{114}	I/O_{118}	I/O_{96}	I/O_{99}	TMS	I/O_{104}	I/O_{107}	I/O_{122}	I/O_{125}	I/O_{128}	I/O_{131}	I/O_{132}	I/O_{135}	I/O_{138}	I/O_{141}	I/O_{156}	I/O_{158}	TDO	I/O_{164}	I/O_{167}	I/O_{145}	I/O_{149}	GND	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range[1]

Range	Ambient Temperature[1]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +125°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[2]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Shaded areas contain advance information.

Notes:

1. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[3]	2.4			V
			I_{OH} = –2.0 mA (Mil)[3]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[7]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l/Ind)[4]			4.0	V
			I_{OH} = –50 µA (Com'l/Ind)[4]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[3]			0.5	V
			I_{OL} = 12 mA (Mil)[3]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[5]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[5]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled		–50		50	µA
		V_{CC} = Max., V_O = 3.3V, Output Disabled[4]		0	–70	–125	µA
I_{OS}	Output Short Circuit Current[6, 7]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Inductance[7]

Parameter	Description	Test Conditions	208-lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	11	nH

Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF

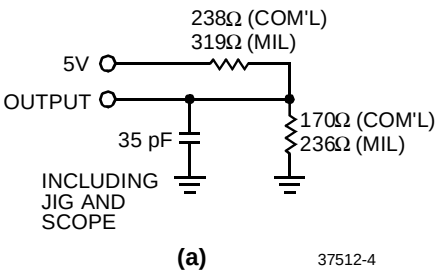
Endurance Characteristics[7]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[1]	1,000	10,000	Cycles

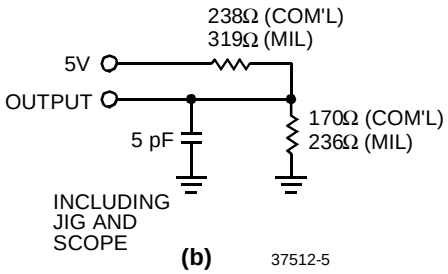
Notes:

3. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
4. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

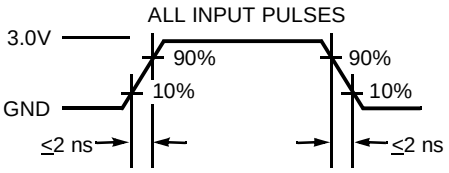
AC Test Loads and Waveforms



(a) 37512-4

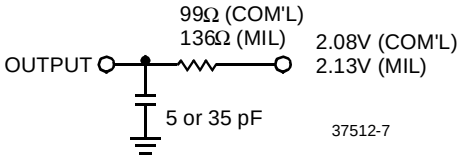


(b) 37512-5

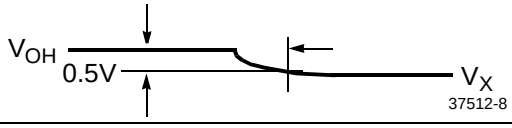
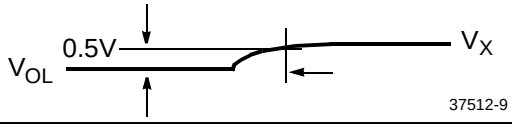
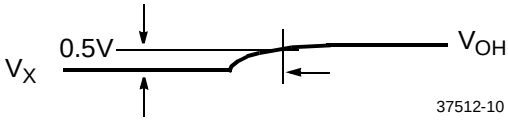
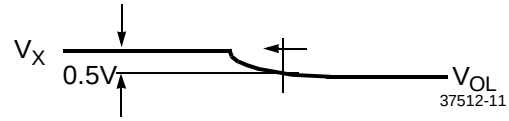


(c) 37512-6

Equivalent to: THÉVENIN EQUIVALENT



37512-7

Parameter[8]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 37512-8
$t_{ER(+)}$	2.6V	 37512-9
$t_{EA(+)}$	1.5V	 37512-10
$t_{EA(-)}$	V_{the}	 37512-11

(d) Test Waveforms

Note:

8. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[9]

Parameter	Description	37512-154		37512-143		37512-125		37512-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}[10, 11, 12]	Input to Combinatorial Output		7.5		8.5		10		15	ns
t_{PDL}[10, 11, 12]	Input to Output Through Transparent Input or Output Latch		12		12		13		18	ns
t_{PDLL}[10, 11, 12]	Input to Output Through Transparent Input and Output Latches		13		13.5		15		19	ns
t_{EA}[10, 11, 12]	Input to Output Enable		11		13		14		19	ns
t_{ER}[10]	Input to Output Disable		11		13		14		19	ns
Input Register Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[7]	2.5		2.5		4		4		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[7]	2.5		2.5		4		4		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		3		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		3		ns
t_{ICO}[10, 11, 12]	Input Register Clock or Latch Enable to Combinatorial Output		11		12.5		19		19	ns
t_{ICOL}[10, 11, 12]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		12		14		21		21	ns
Synchronous Clocking Parameters										
t_{CO}[11,12]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output		4.5		6		6.5		8	ns
t_S[10]	Set-Up Time from Input to Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	5		5		5.5		8		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}[10, 11, 12]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		11		12		14		19	ns
t_{SCS}[10]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	6.5		7		8		12		ns
t_{SL}[10]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	8.5		9		10		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	0		0		0		0		ns
Product Term Clocking Parameters										
t_{COPT}[10, 11, 12]	Product Term Clock or Latch Enable (PTCLK) to Output		10		13		13		15	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	2.5		3		3		4.5		ns

Shaded areas contain advanced information.

Notes:

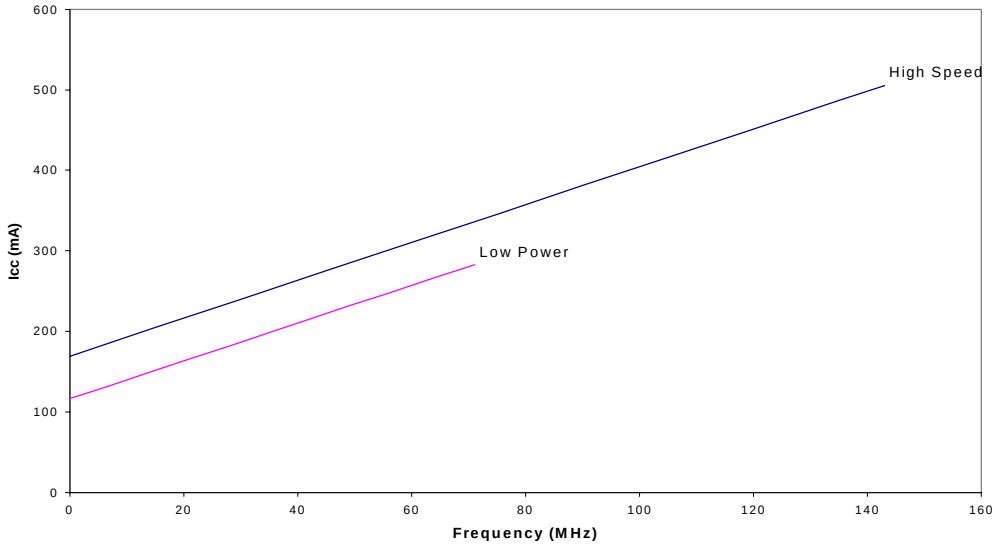
9. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
10. Logic Blocks operating in low power mode, add t_{LP} to this spec.
11. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
12. When V_{CCO}= 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range[9] (continued)

Parameter	Description	37512-154		37512-143		37512-125		37512-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPT}	Register or Latch Data Hold Time	2.5		3		3		4.5		ns
t_{ISPT}[10]	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		–2		–2		–2		–2	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time		6.5		7.5		9		14	ns
t_{CO2PT}[10, 11, 12]	Product Term Clock or Latch Enable (PT-CLK) to Output Delay (Through Logic Array)		15		19		19		24	ns
Pipelined Mode Parameters										
t_{ICS}[10]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	6		7		8		12		ns
Operating Frequency Parameters										
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[7]	154		143		125		83		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	200		167		158		125		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)	105		91		83		67		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	143		125		125		67		MHz
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[7]	8		8		10		15		ns
t_{RR}[10]	Asynchronous Reset Recovery Time[7]	10		10		12		17		ns
t_{RO}[10, 11, 12]	Asynchronous Reset to Output		13		14		15		21	ns
t_{PW}	Asynchronous Preset Width[7]	8		8		10		15		ns
t_{PR}[10]	Asynchronous Preset Recovery Time[7]	10		10		12		17		ns
t_{PO}[10, 11, 12]	Asynchronous Preset to Output		13		14		15		21	ns
User Option Parameters										
t_{LP}	Low Power Adder		4		4		4		4	ns
t_{SLEW}	Slow Output Slew Rate Adder		2		2		2		2	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder		0.1		0.1		0.1		0.1	ns
JTAG Timing Parameters										
$t_{S\ JTAG}$	Set-Up Time from TDI and TMS to TCK	0		0		0		0		ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS	20		20		20		20		ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO		20		20		20		20	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency		20		20		20		20	MHz

Shaded areas contain advance information.

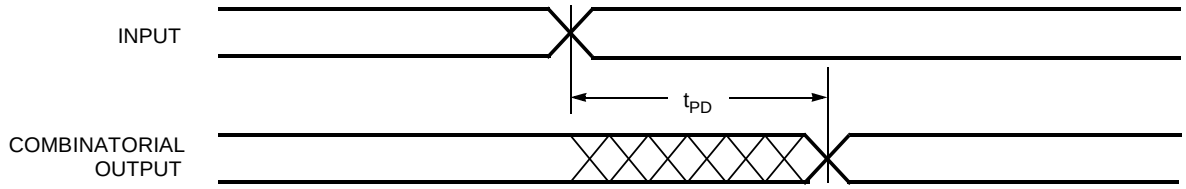
Typical I_{cc} Characteristics



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{cc} = 5.0V, T_A = Room Temperature

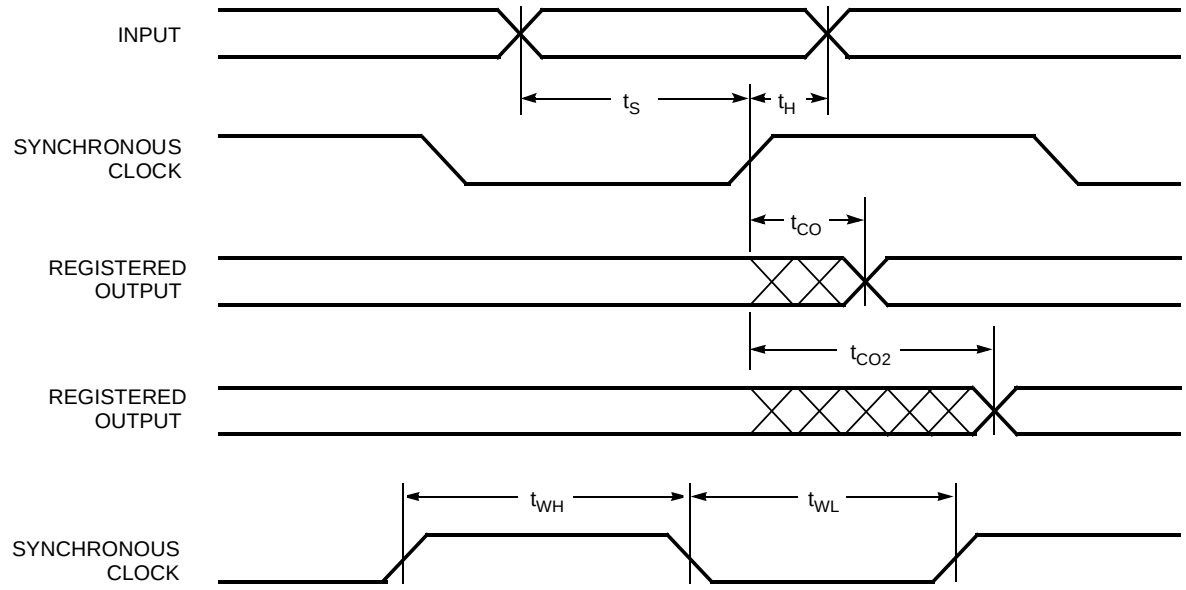
Switching Waveforms

Combinatorial Output



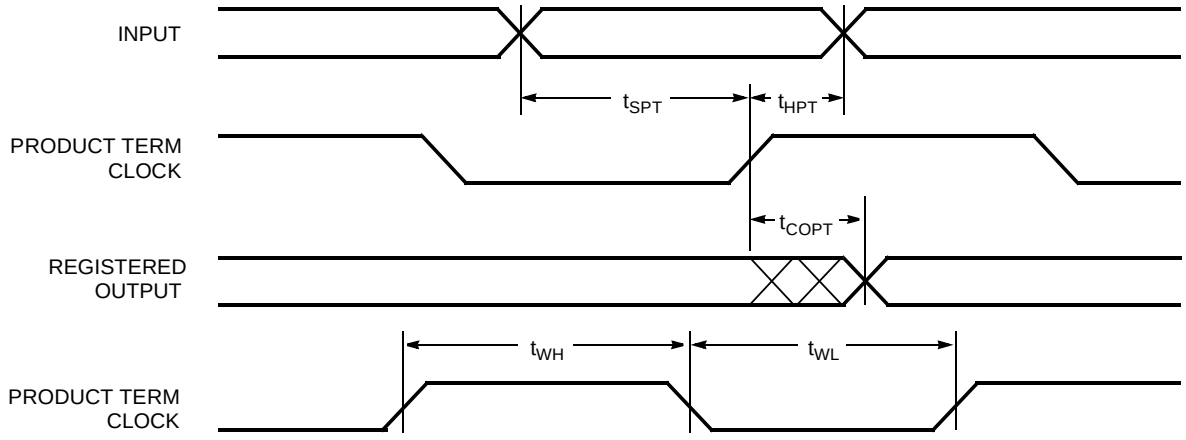
37512-12

Registered Output with Synchronous Clocking



37512-13

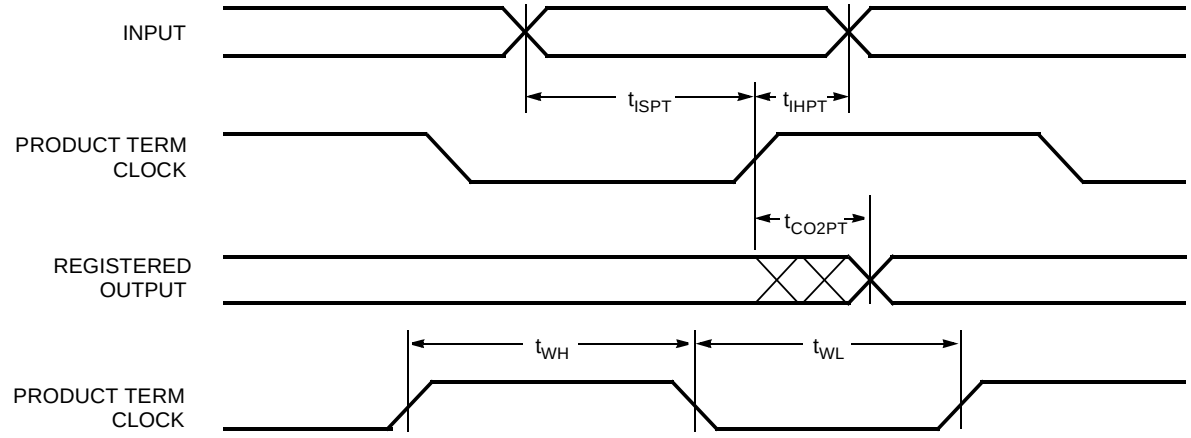
Registered Output with Product Term Clocking Input Going Through the Array



37512-14

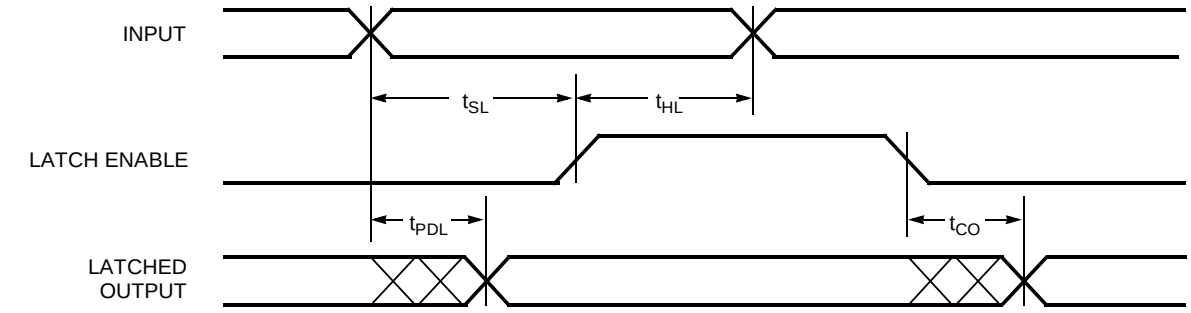
Switching Waveforms (continued)

Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



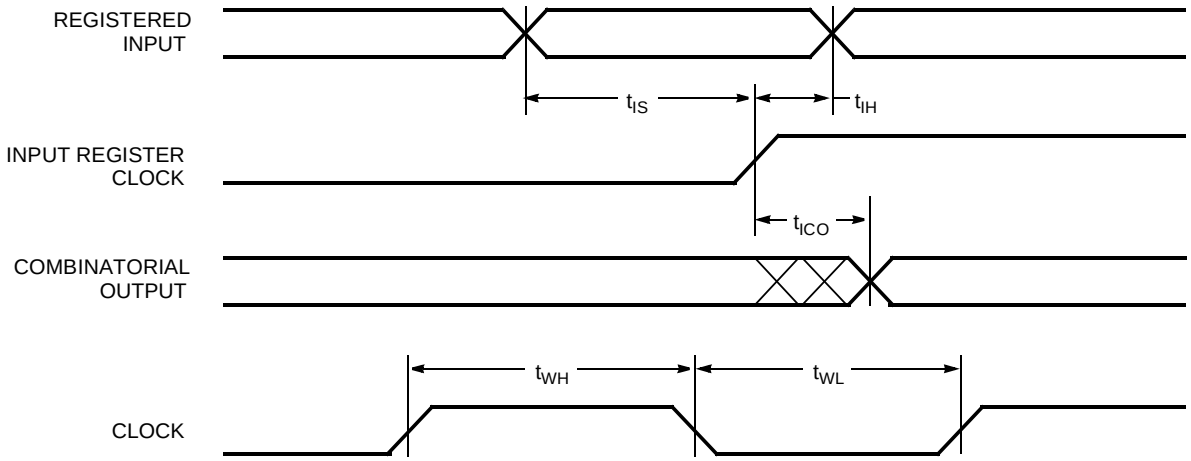
37512-15

Latched Output



37512-16

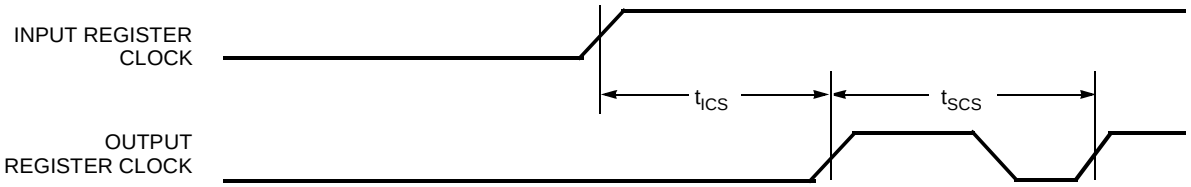
Registered Input



37512-17

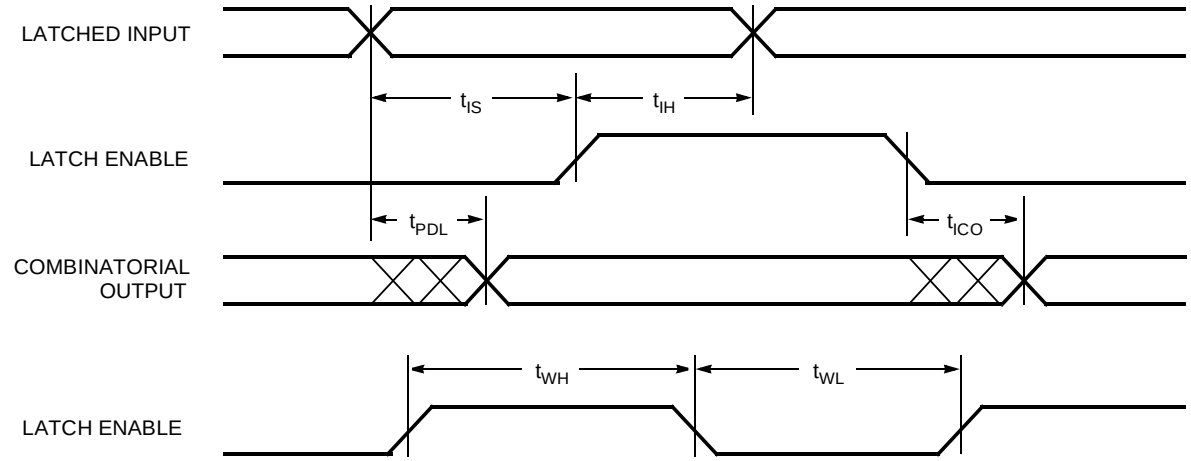
Switching Waveforms (continued)

Clock to Clock



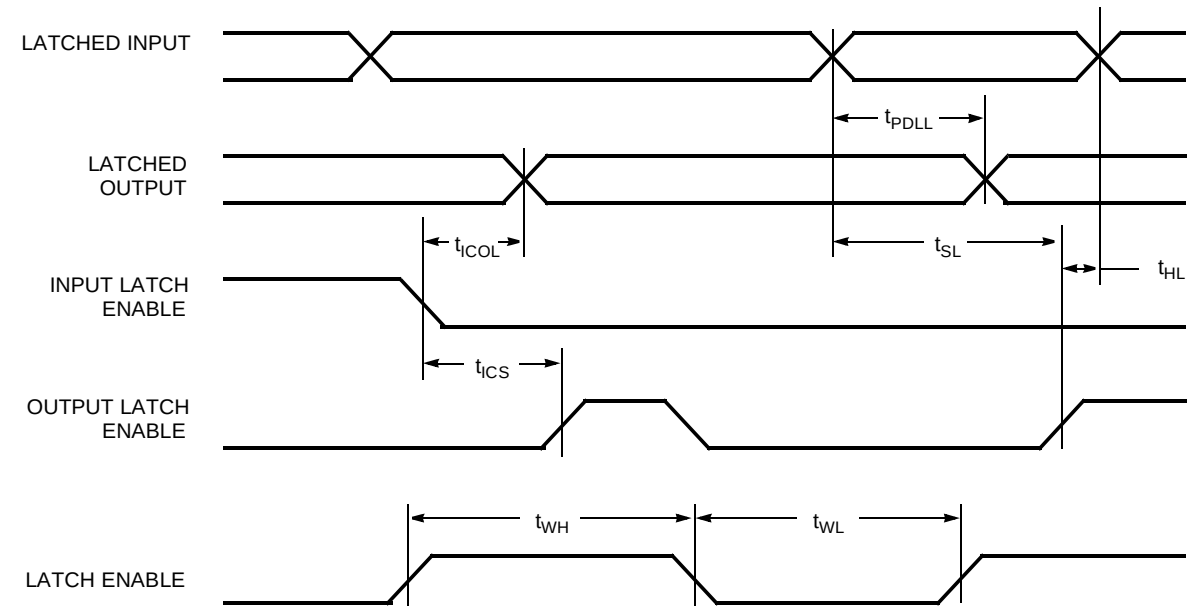
37512-18

Latched Input



37512-19

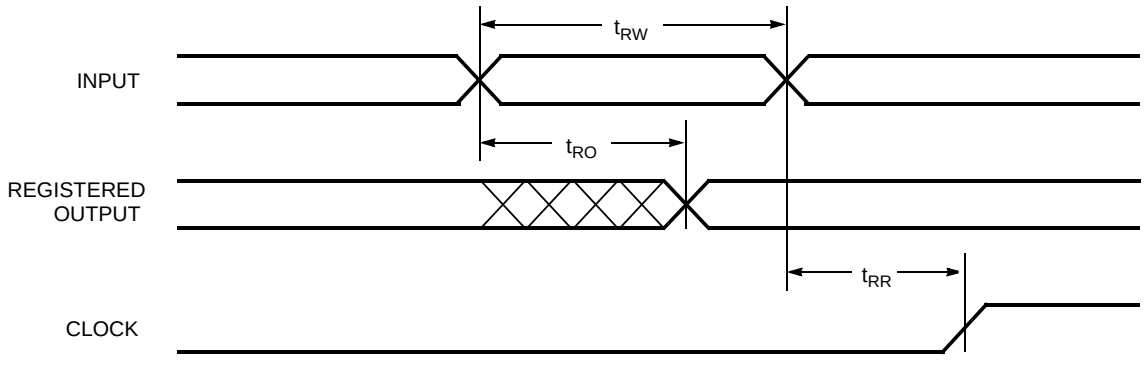
Latched Input and Output



37512-20

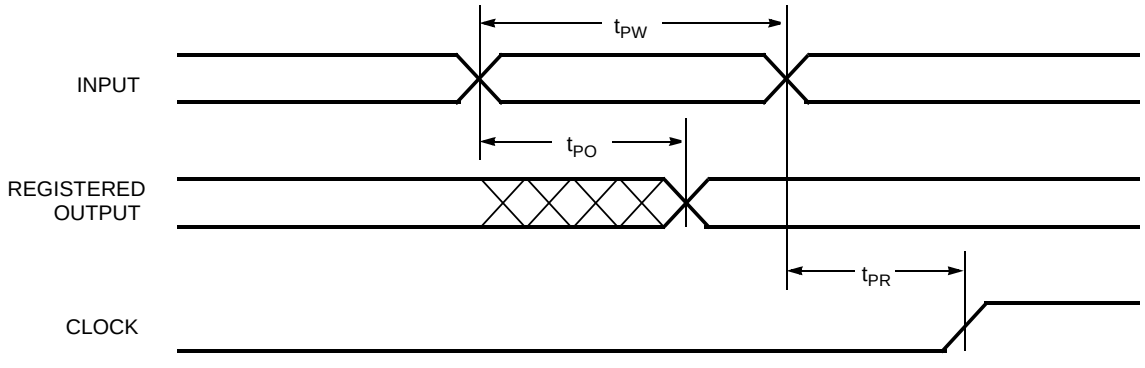
Switching Waveforms (continued)

Asynchronous Reset



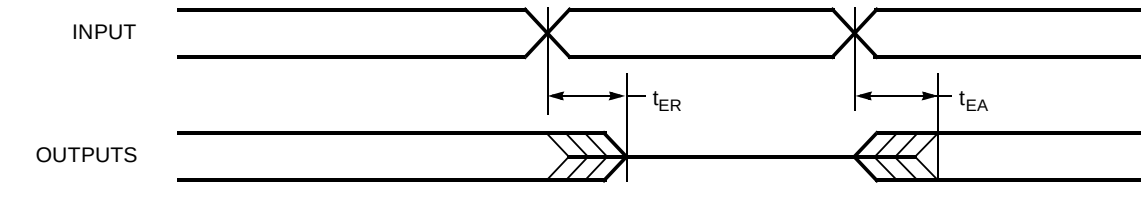
37512-21

Asynchronous Preset



37512-22

Output Enable/Disable



37512–23

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
154	CY37512P208-154NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37512P256-154BGC	BG256	256-Pin Ball Grid Array	
	CY37512P352-154BGC*	BG352	352-Pin Ball Grid Array	
143	CY37512P208-143NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37512P256-143BGC	BG256	256-Pin Ball Grid Array	
	CY37512P352-143BGC*	BG352	352-Pin Ball Grid Array	
125	CY37512P208-125NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37512P256-125BGC	BG256	256-Pin Ball Grid Array	
	CY37512P352-125BGC*	BG352	352-Pin Ball Grid Array	
	CY37512P208-125NI	N208	208-Pin Plastic Quad Flatpack	Industrial
	CY37512P256-125BGI	BG256	256-Pin Ball Grid Array	
	CY37512P352-125BGI*	BG352	352-Pin Ball Grid Array	
	CY37512P208-125UMB	U208	208-Pin Ceramic Quad Flatpack	Military
83	CY37512P208-83NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37512P256-83BGC	BG256	256-Pin Ball Grid Array	
	CY37512P352-83BGC*	BG352	352-Pin Ball Grid Array	
	CY37512P208-83NI	N208	208-Pin Plastic Quad Flatpack	Industrial
	CY37512P256-83BGI	BG256	256-Pin Ball Grid Array	
	CY37512P352-83BGI*	BG352	352-Pin Ball Grid Array	
	CY37512P208-83UMB	U208	208-Pin Ceramic Quad Flatpack	Military

Shaded areas contain advance information.

*Contact your Cypress Semiconductor representative for Pin Configuration/Package Diagram information

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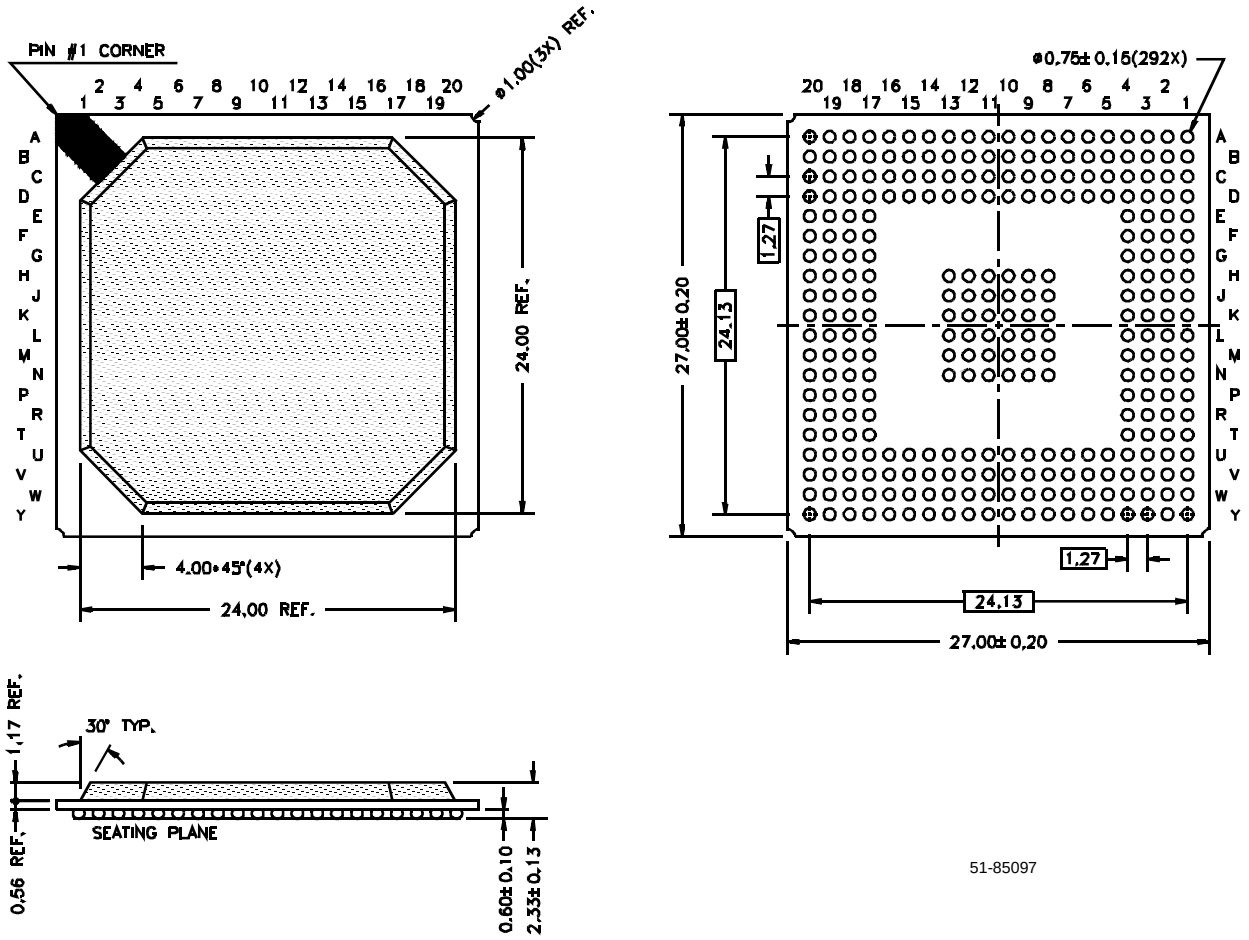
Package Diagrams

256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256



51-85097

Package Diagrams (continued)

208-Lead Plastic Quad Flatpack / Ceramic Quad Flat Pack N208