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NCP4588

200 mA, Output Capacitor Free, LDO Linear Voltage Regulator

The NCP4588 is a CMOS 200mA LDO which is stable without an output capacitor. This results in a reduction in component count, cost and board area, as well as contributing to a more robust solution in hostile environments. With quiescent current < 9.5 μA and PSRR > 60 dB, the device is an excellent trade off between the two features. The family is available in a variety of packages: SC−70, SOT23 and a small, ultra thin 1.2 x 1.2 x 0.4 mm XDFN.

Features

- Operating Input Voltage Range: 1.4 V to 5.25 V
- Output Voltage Range: 1.0 to 4.2 V (available in 0.1 V steps)
- Output Voltage Accuracy: 1%
- Quiescent Current: 9.5 μA
- Standby Current: 0.1 μA
- Very Low Dropout: 270 mV (I_{OUT} = 200 mA, V_{IN} = 3.0 V)
- High PSRR: 70 dB at 1 kHz, $V_{OUT} \leq 1.2$ V
  65 dB at 1 kHz, $1.2 < V_{OUT} < 2.2$ V
  60 dB at 1 kHz, $V_{OUT} \geq 2.2$ V
- Line Regulation 0.02%/V Typ.
- Current Fold Back Protection: 50 mA at short
- Stable with no Output Capacitor
- Available in SC−70, XDFN and SOT23 Package
- These are Pb−Free Devices

Typical Applications

- Battery Powered Equipments
- Portable Communication Equipments
- Cameras, VCRs and Camcorders

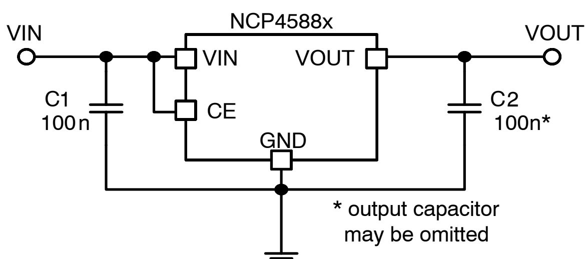

Figure 1. Typical Application Schematic

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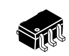
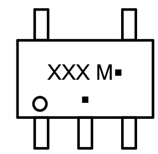
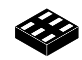
MARKING DIAGRAMS

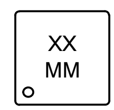


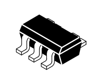
SC−70
CASE 419A



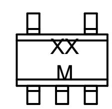


XDFN6
CASE 711AA





SOT−23−5
CASE 1212



XX, XXX	= Specific Device Code
M, MM	= Date Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

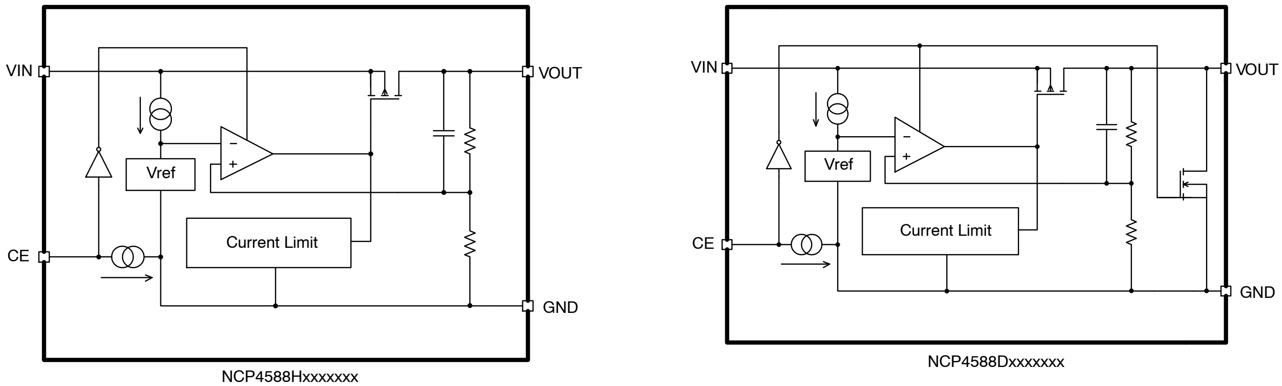


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. XDFN	Pin No. SC−70	Pin No. SOT23	Pin Name	Description
4	5	1	VIN	Input pin
2	3	2	GND	Ground
3	1	3	CE	Chip enable pin (Active “H”)
6	4	5	VOUT	Output pin
1, 5	2	4	NC	No connection

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	6.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	−0.3 to 6.0	V
Output Current	I_{OUT}	400	mA
Power Dissipation XDFN	P_D	400	mW
Power Dissipation SC70		380	
Power Dissipation SOT23		420	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Thermal Characteristics, SOT23 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC−70 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V; $I_{OUT} = 1$ mA; $C_{IN} = C_{OUT} = 1$ μF; unless otherwise noted. Typical values are at $T_A = +25°C$.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.4		5.25	V
Output Voltage	$T_A = +25$ °C	$V_{OUT} > 2.0$ V	V_{OUT}	x0.99		x1.01	V
		$V_{OUT} \le 2.0$ V		−20		20	mV
	$-40°C \le T_A \le 85°C$	$V_{OUT} > 2.0$ V		x0.980		x1.015	V
		$V_{OUT} \le 2.0$ V		−40		30	mV
Output Voltage Temp. Coefficient	$-40°C \le T_A \le 85°C$				¿100		ppm/°C
Line Regulation	$V_{OUT(NOM)} + 0.5\ V \le V_{IN} \le 5.0$ V		$Line_{Reg}$		0.02	0.2	%/V
Load Regulation	$I_{OUT} = 1$ mA to 200 mA		$Line_{Reg}$		25	50	mV
Dropout Voltage	$I_{OUT} = 200$ mA	$1.0\ V \le V_{OUT} < 1.3$ V	V_{DO}		0.64	0.92	V
		$1.1\ V \le V_{OUT} < 1.5$ V			0.59	0.84	
		$1.2\ V \le V_{OUT} < 1.8$ V			0.55	0.76	
		$1.5\ V \le V_{OUT} < 2.3$ V			0.44	0.60	
		$2.0\ V \le V_{OUT} < 3.0$ V			0.35	0.49	
		$2.6\ V \le V_{OUT} < 4.0$ V			0.27	0.36	
Output Current			I_{OUT}	200			mA
Short Current Limit	$V_{OUT} = 0$ V		I_{SC}		50		mA
Quiescent Current			I_Q		9.5	25	μA
Standby Current	$V_{CE} = 0$ V, $T_A = 25°C$		I_{STB}		0.1	3.0	μA
CE Pin Threshold Voltage	CE Input Voltage “H”		V_{CEH}	1.0			V
	CE Input Voltage “L”		V_{CEL}			0.4	
CE Pull Down Current			I_{CEPD}		0.1		μA
Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 1$ V or 2.2 V whichever is higher, $\Delta V_{IN} = 0.2\ V_{pk-pk}$, $I_{OUT} = 30$ mA, f = 1 kHz		PSRR				dB
	$V_{OUT} \le 1.2$ V				70		
	$1.2\ V < V_{OUT} \le 2.2$ V				65		
	$2.2\ V \le V_{OUT}$				60		
Output Noise Voltage	$V_{OUT} = 1$ V, $I_{OUT} = 30$ mA, f = 10 Hz to 100 kHz		V_N		80		μV_{rms}
Low Output Nch Tr. On Resistance	$V_{IN} = 4$ V, $V_{CE} = 0$ V, D version only		R_{LOW}		30		Ω

TYPICAL CHARACTERISTICS

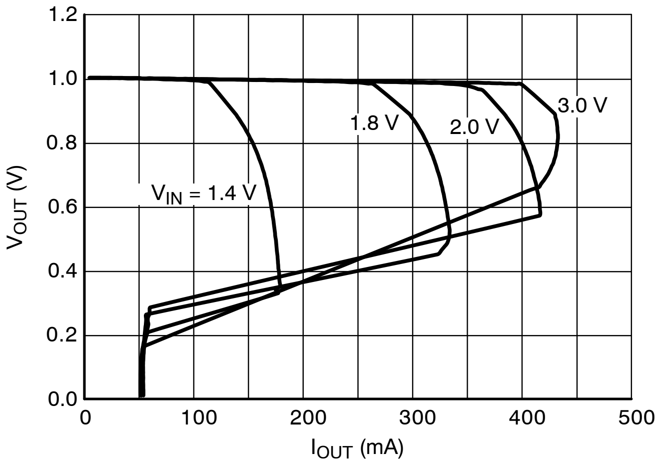


Figure 3. Output Voltage vs. Output Current 1.0 V Version (T_A = 25°C)

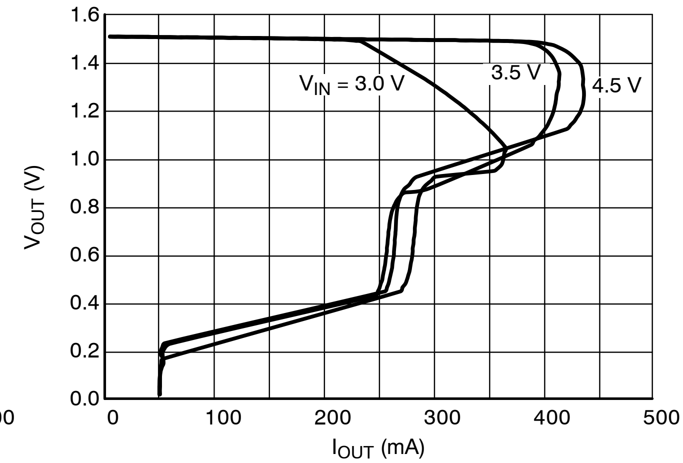


Figure 4. Output Voltage vs. Output Current 1.5 V Version (T_A = 25°C)

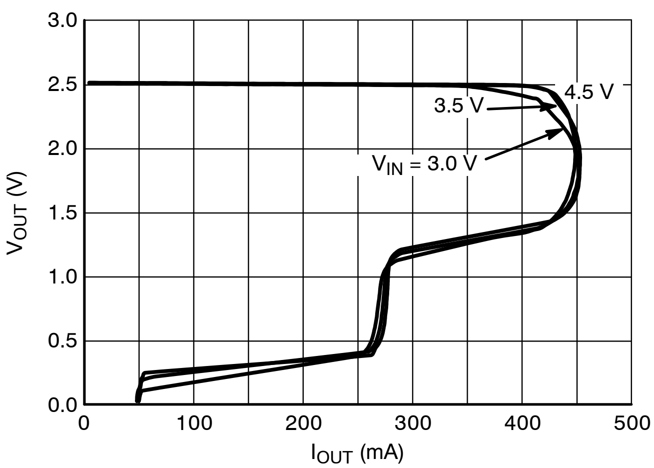


Figure 5. Output Voltage vs. Output Current 2.5 V Version (T_A = 25°C)

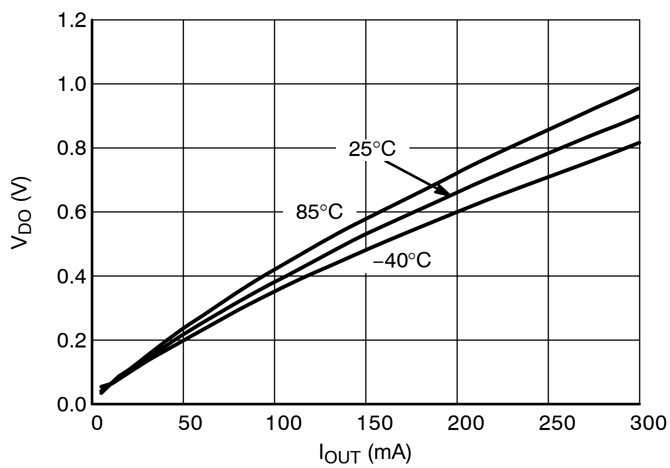


Figure 6. Dropout Voltage vs. Output Current 1.0 V Version

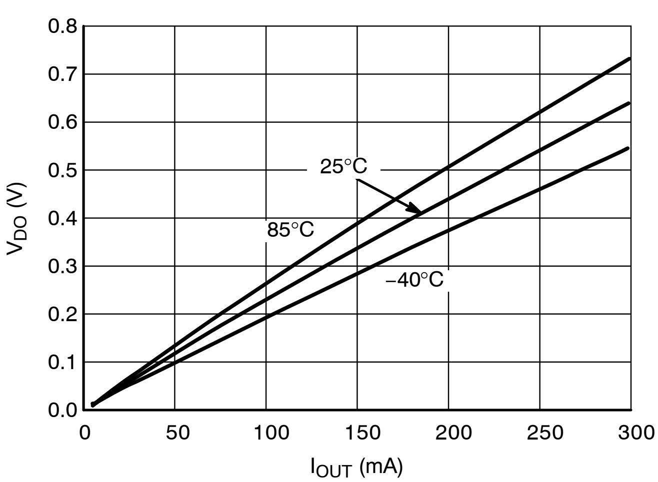


Figure 7. Dropout Voltage vs. Output Current 1.5 V Version

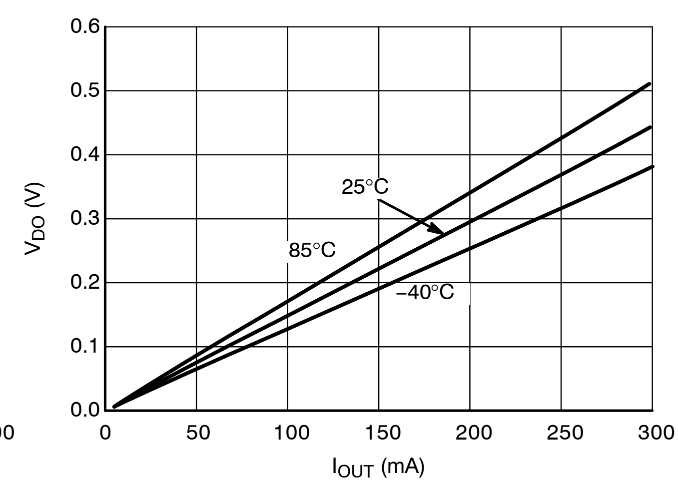


Figure 8. Dropout Voltage vs. Output Current 2.5 V Version

TYPICAL CHARACTERISTICS

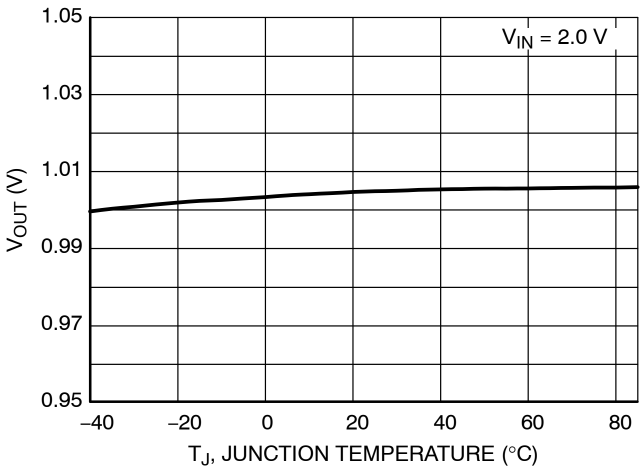


Figure 9. Output Voltage vs. Temperature, 1.0 V Version

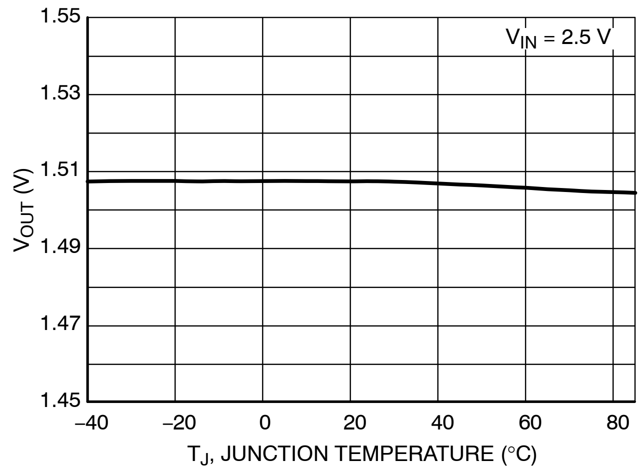


Figure 10. Output Voltage vs. Temperature, 1.5 V Version

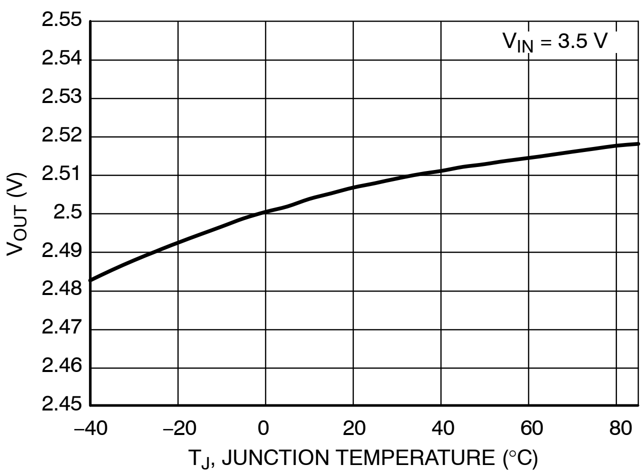


Figure 11. Output Voltage vs. Temperature, 2.5 V Version

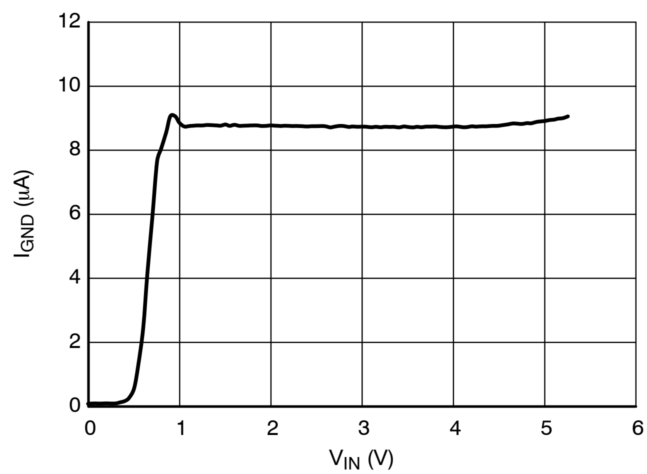


Figure 12. Supply Current vs. Input Voltage, 1.0 V Version

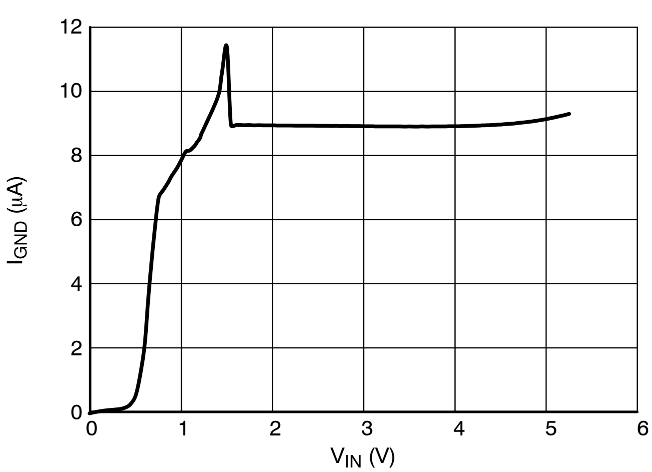


Figure 13. Supply Current vs. Input Voltage, 1.5 V Version

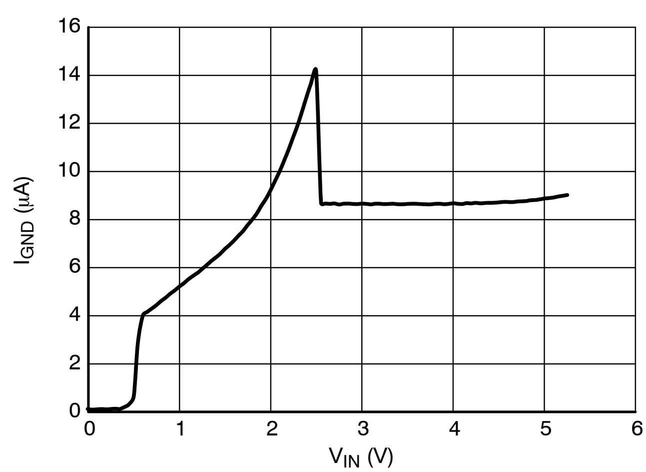


Figure 14. Supply Current vs. Input Voltage, 2.5 V Version

TYPICAL CHARACTERISTICS

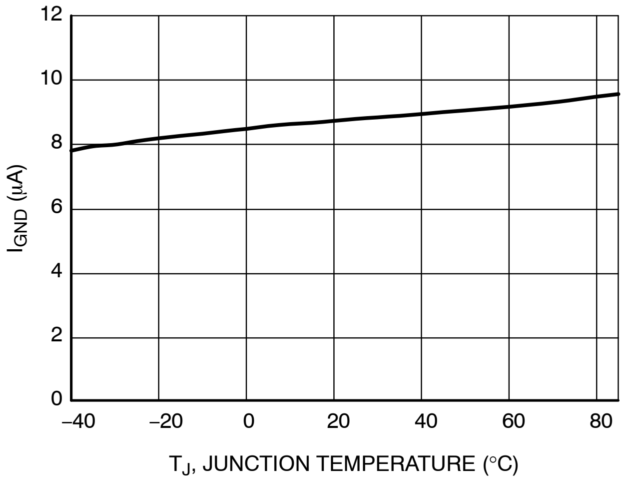


Figure 15. Supply Current vs. Temperature, 1.0 V Version

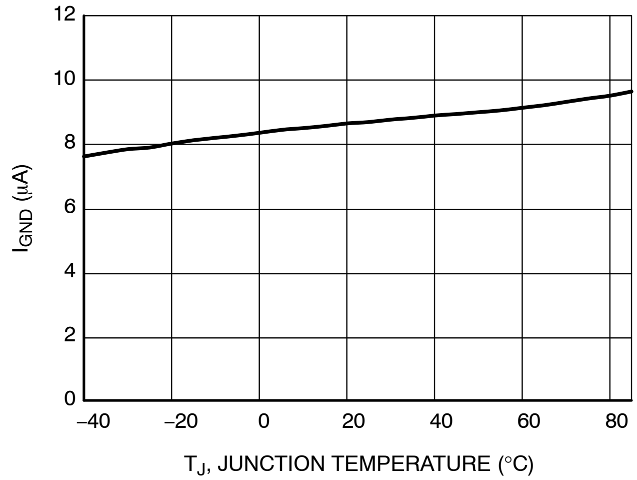


Figure 16. Supply Current vs. Temperature, 1.5 V Version

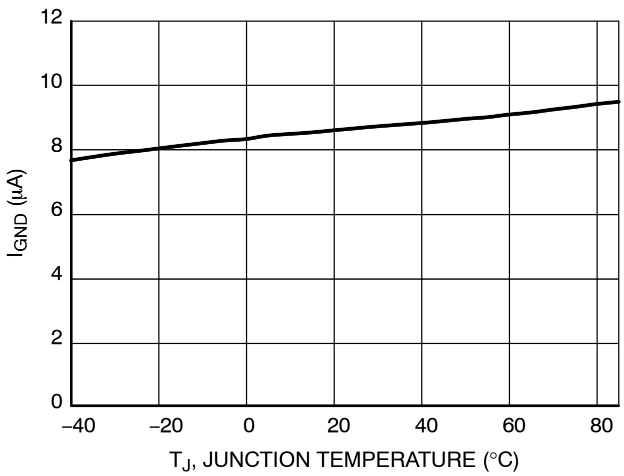


Figure 17. Supply Current vs. Temperature, 2.5 V Version

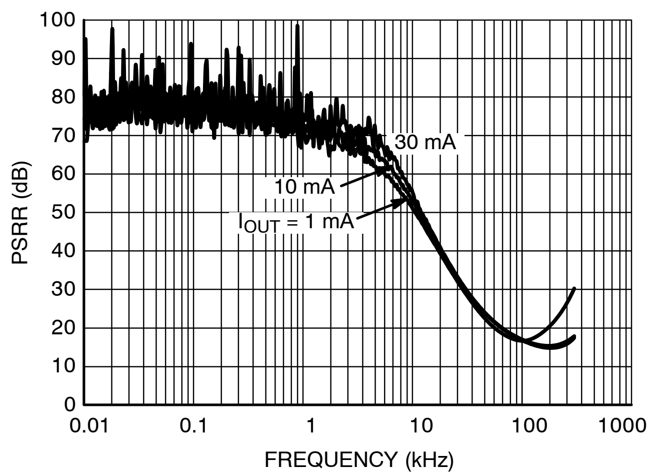


Figure 18. PSRR, 1.0 V Version, C_{OUT} = 100 nF

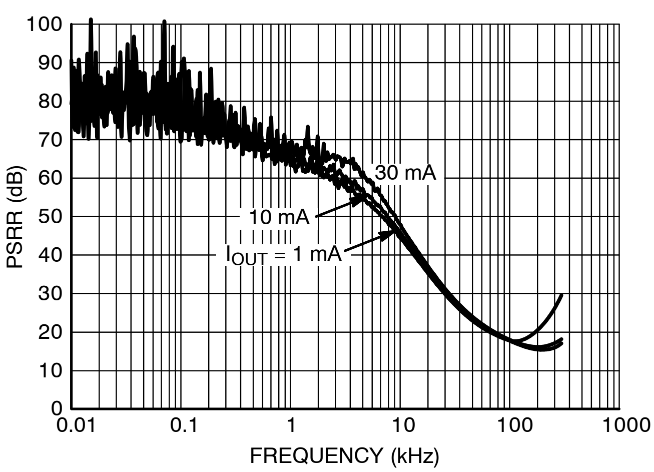


Figure 19. PSRR, 1.5 V Version, C_{OUT} = 100 nF

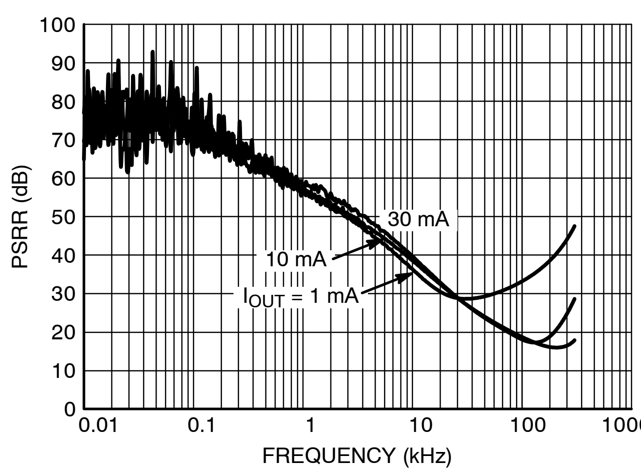


Figure 20. PSRR, 2.5 V Version, C_{OUT} = 100 nF

TYPICAL CHARACTERISTICS

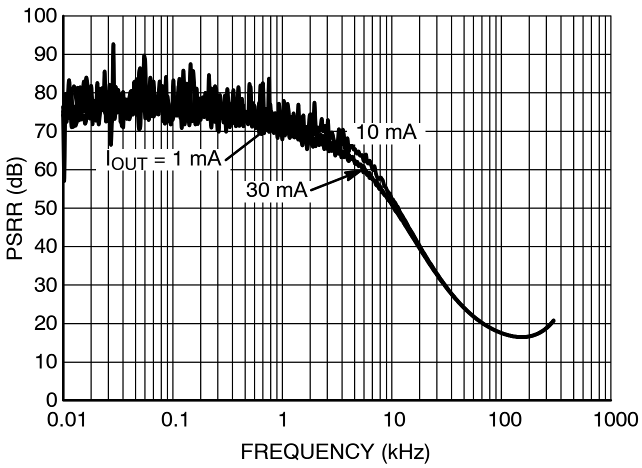


Figure 21. PSRR, 1.0 V Version, C_{OUT} = 0 μF

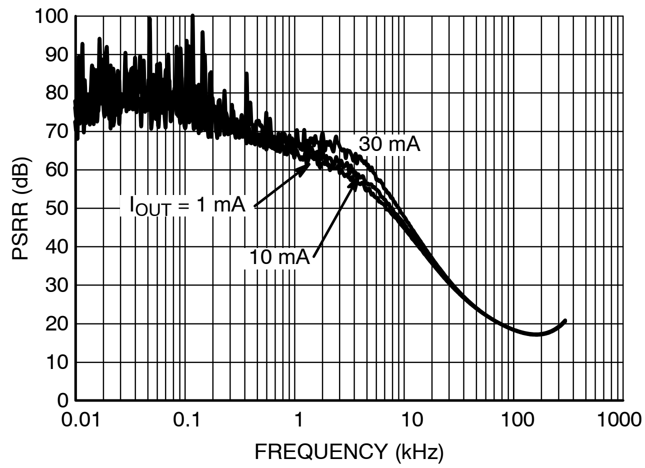


Figure 22. PSRR, 1.5 V Version, C_{OUT} = 0 μF

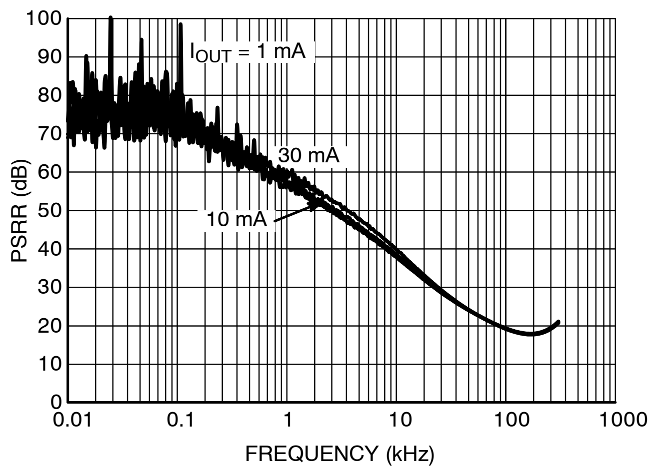


Figure 23. PSRR, 2.5 V Version, C_{OUT} = 0 μF

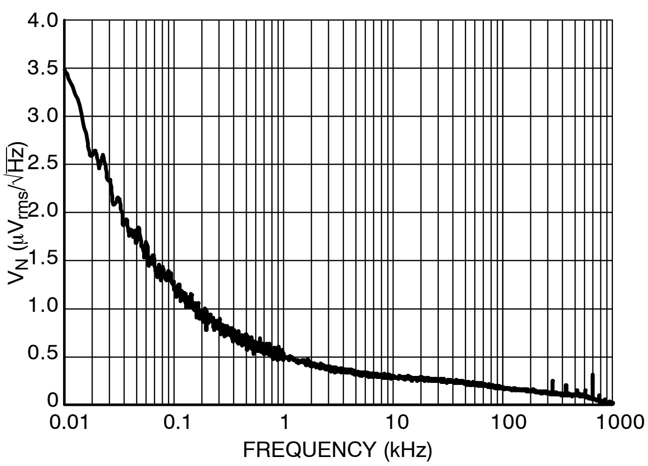


Figure 24. Output Voltage Noise, 1.0 V Version

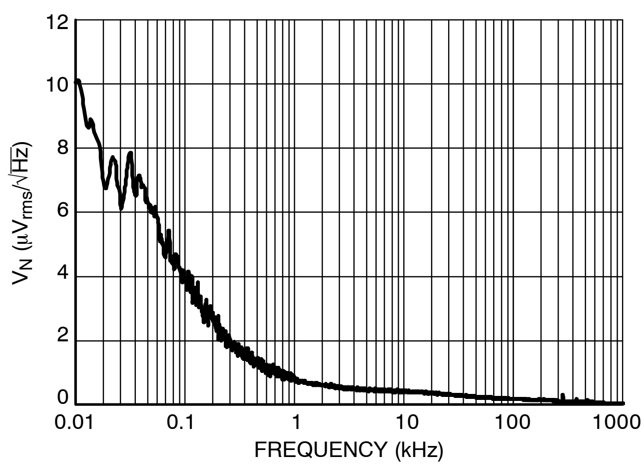


Figure 25. Output Voltage Noise, 1.5 V Version

TYPICAL CHARACTERISTICS

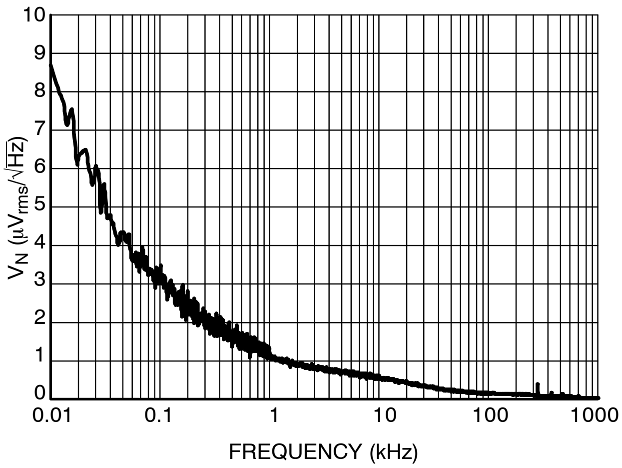


Figure 26. Output Voltage Noise, 2.5 V Version

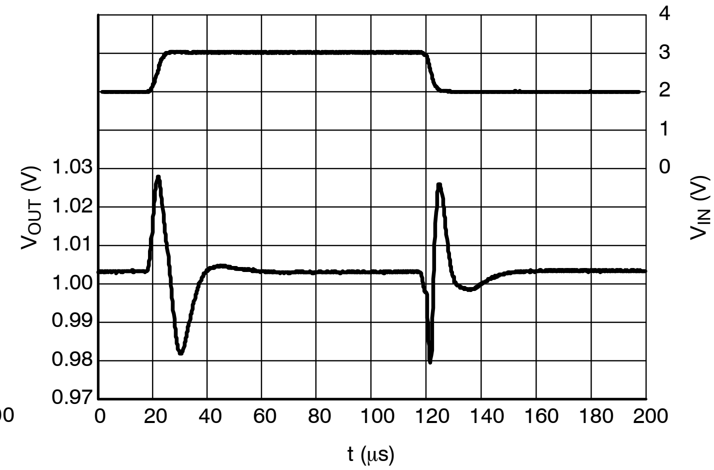


Figure 27. Line Transients, 1.0 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30\ mA$, $C_{OUT} = 0\ nF$

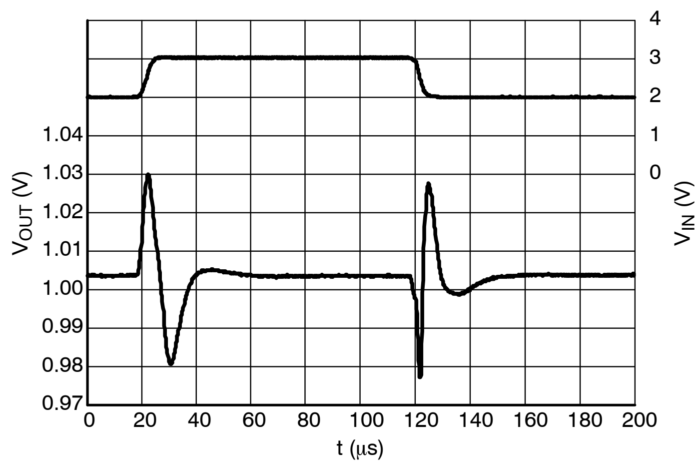


Figure 28. Line Transients, 1.0 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30\ mA$, $C_{OUT} = 100\ nF$

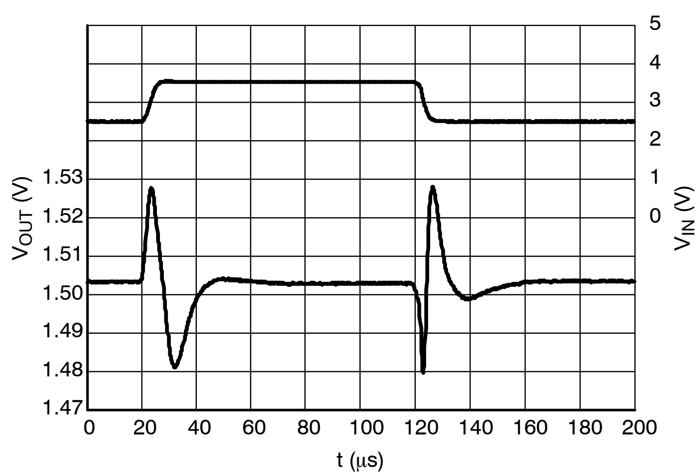


Figure 29. Line Transients, 1.5 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30\ mA$, $C_{OUT} = 0\ nF$

TYPICAL CHARACTERISTICS

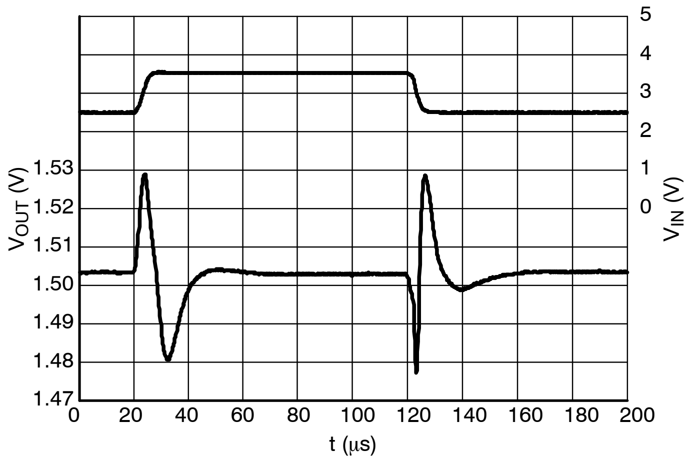


Figure 30. Line Transients, 2.5 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30\ mA$, $C_{OUT} = 100\ nF$

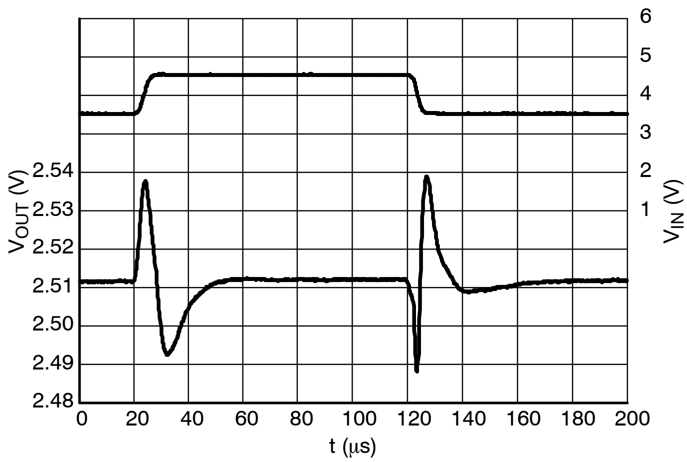


Figure 31. Line Transients, 2.5 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30\ mA$, $C_{OUT} = 0\ nF$

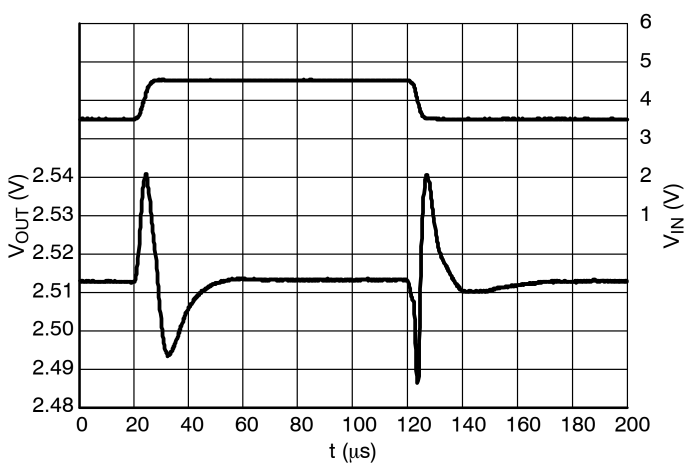


Figure 32. Line Transients, 2.5 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30\ mA$, $C_{OUT} = 100\ nF$

TYPICAL CHARACTERISTICS

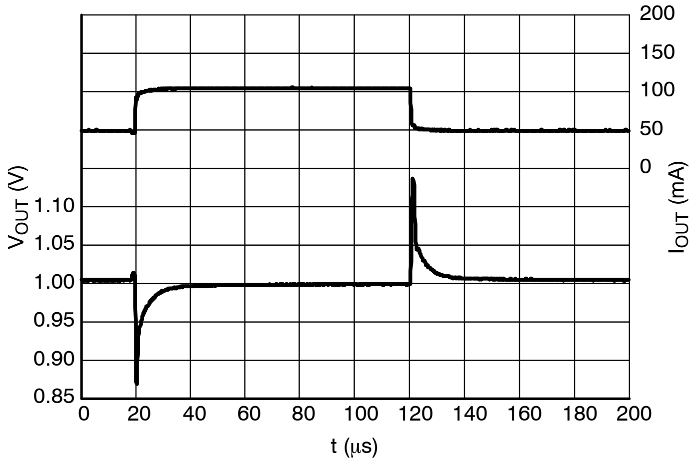


Figure 33. Load Transients, 1.0 V Version, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 2.0\ V$

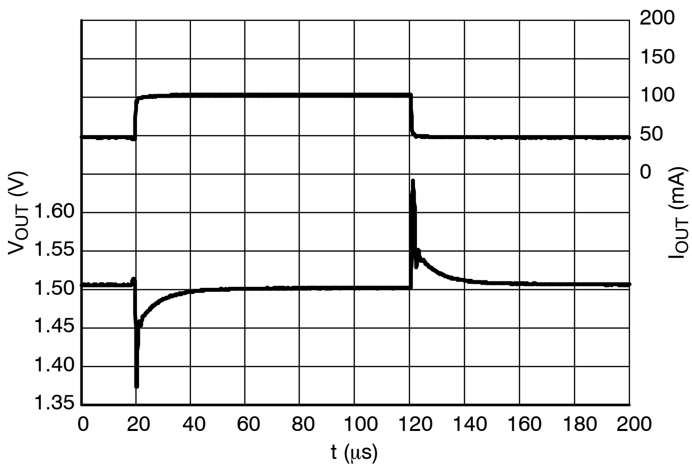


Figure 34 - Load Transients, 1.5 V Version, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 1.5\ V$

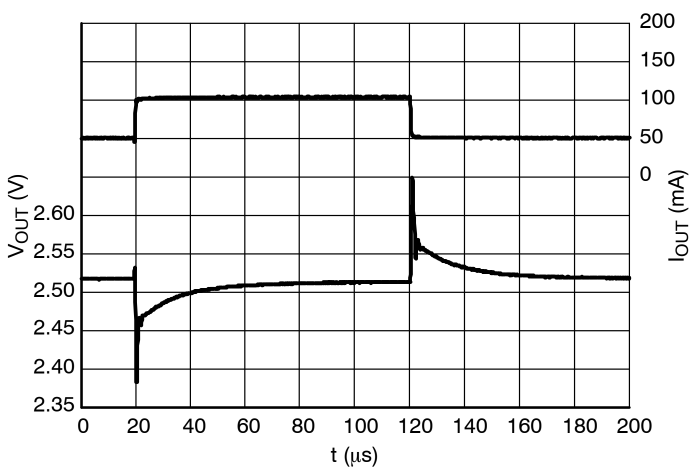


Figure 35. Load Transients, 2.5 V Version, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 3.5\ V$

TYPICAL CHARACTERISTICS

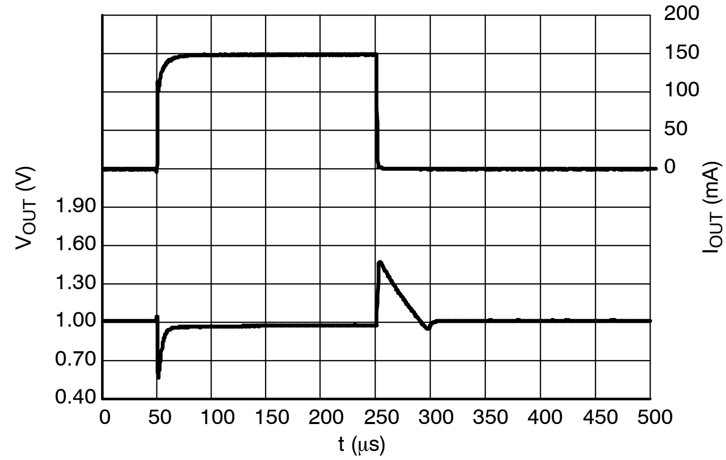


Figure 36. Load Transients, 1.0 V Version, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 2.0$ V

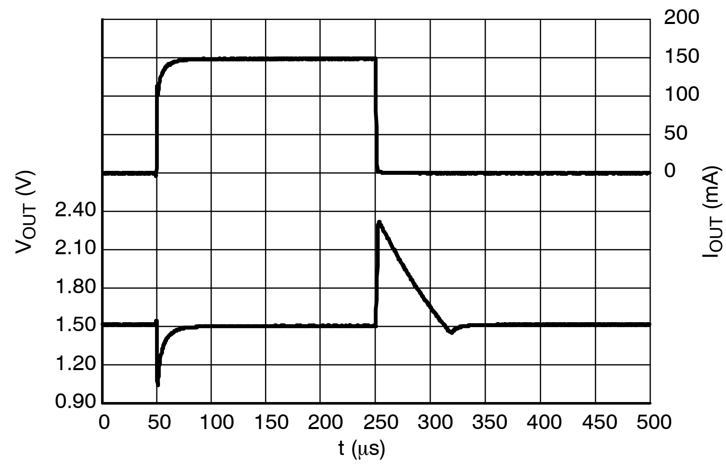


Figure 37. Load Transients, 1.5 V Version, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 2.5$ V

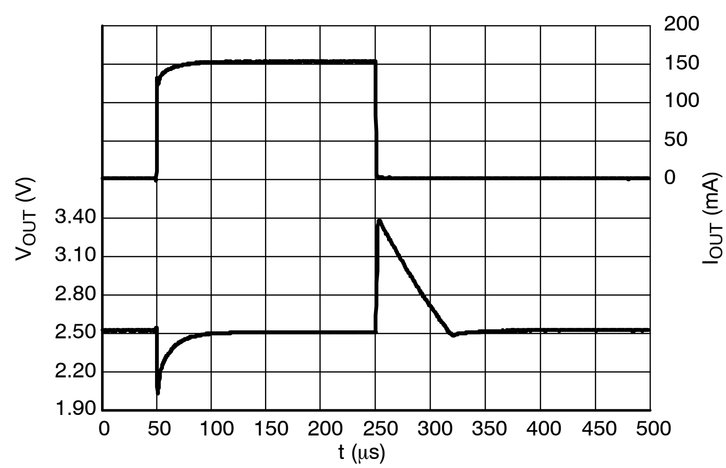


Figure 38. Load Transients, 2.5 V Version, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 3.5$ V

TYPICAL CHARACTERISTICS

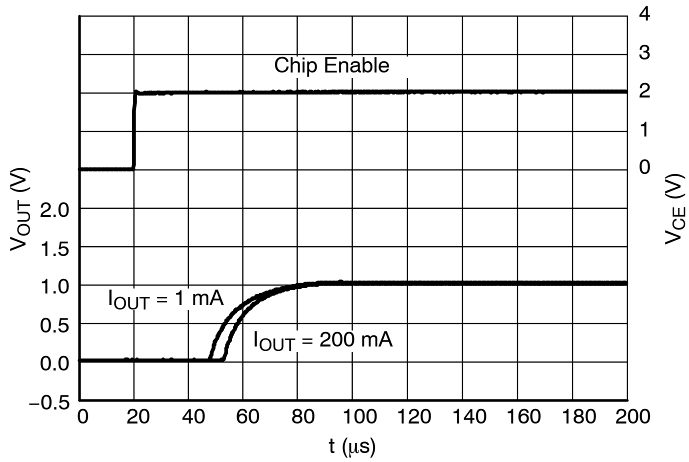


Figure 39. Start−up, 1.0 V Version, V_{IN} = 2.0 V

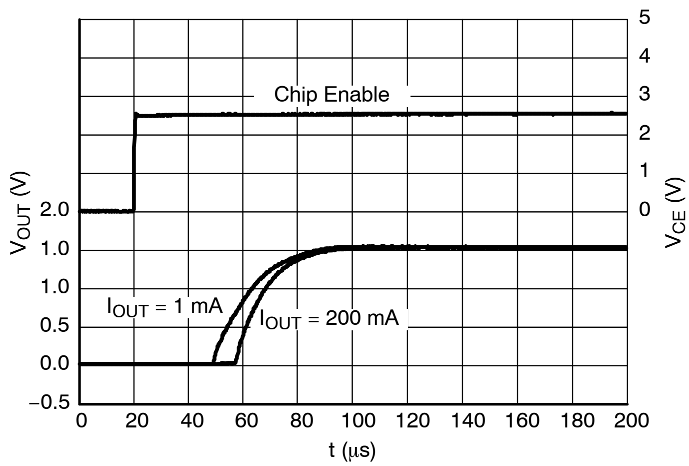


Figure 40. Start−up, 1.5 V Version, V_{IN} = 2.5 V

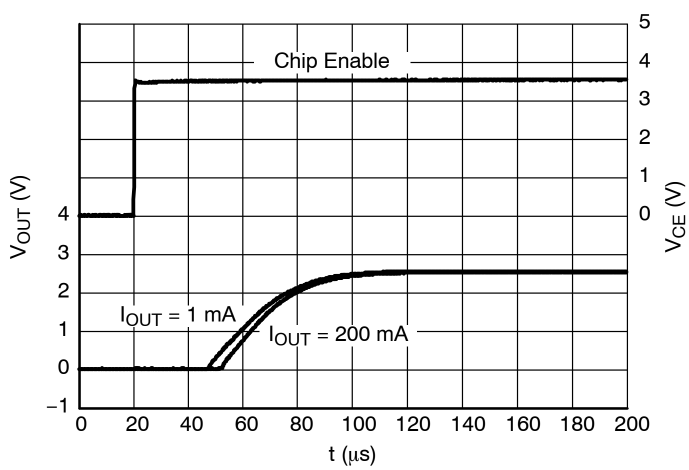


Figure 41. Start−up, 2.5 V Version, V_{IN} = 3.5 V

TYPICAL CHARACTERISTICS

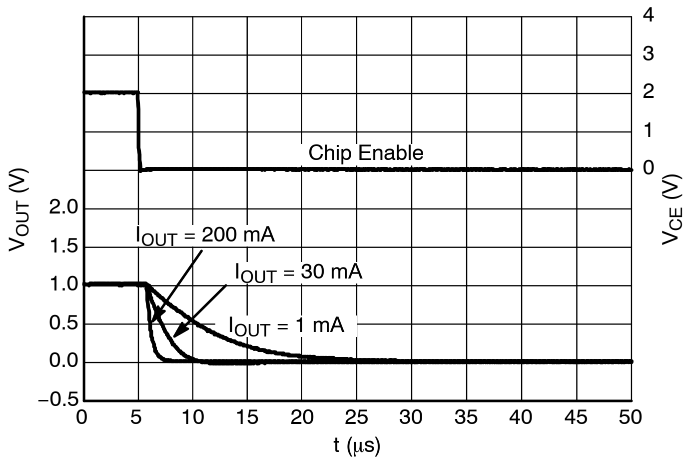


Figure 42. Shutdown, 1.0 V Version D, V_{IN} = 2.0 V

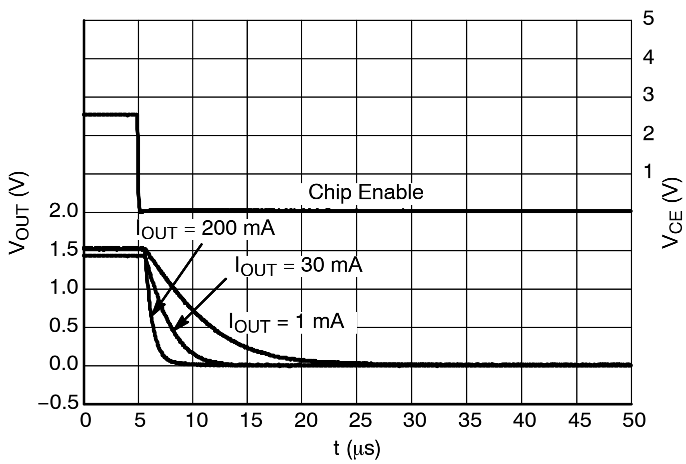


Figure 43. Shutdown, 1.5 V Version D, V_{IN} = 2.5 V

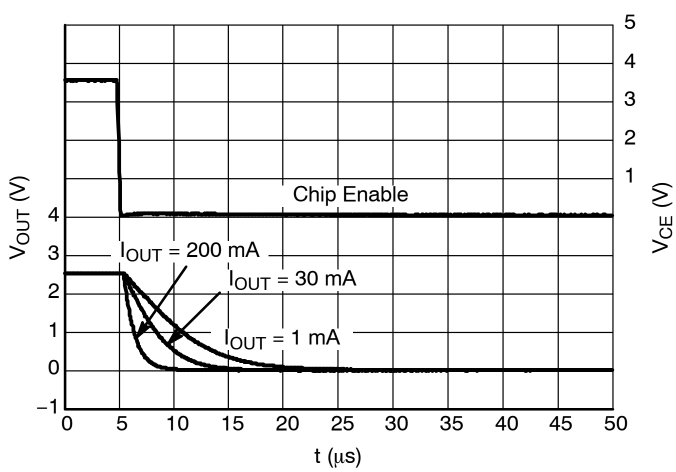


Figure 44. Shutdown, 2.5 V Version D, V_{IN} = 3.5 V

APPLICATION INFORMATION

A typical application circuit for NCP4588 series is shown in Figure 45.

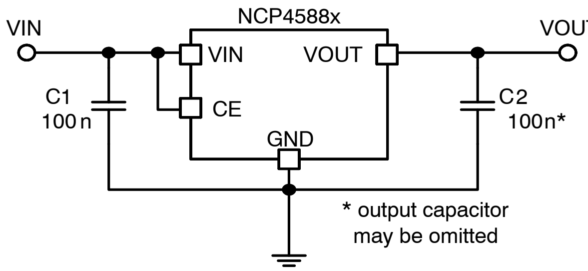


Figure 45. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 100 nF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4588. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

The output capacitor may be not used even if the load current is varied, but if load variation is very large it is better to use an output capacitor in the range of 0.1 μF to 10 μF. It is recommended to use ceramic capacitor; tantalum capacitor with higher ESR may cause unstable output.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The regulator is switched on when the CE pin voltage is above logic high level. The enable pin has internal pull down current source. If enable function is not needed connect CE pin to VIN.

Output Discharger

The D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As power across the IC increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature rise for the part. That is to say, when the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

PCB layout

Make VIN and GND line sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 (if it is used) as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

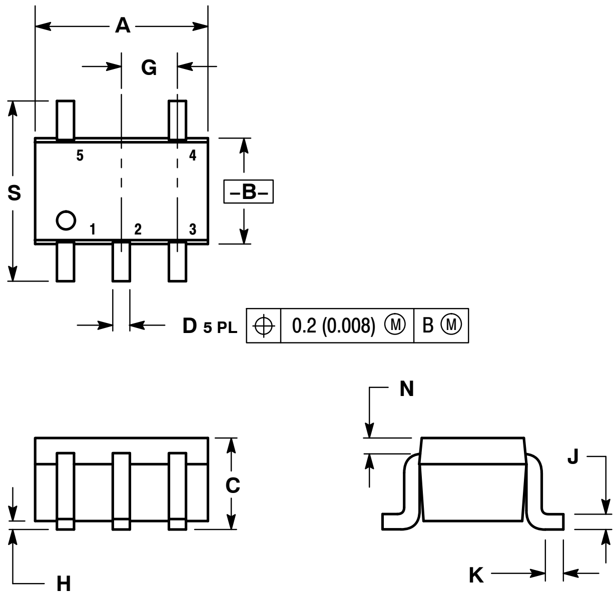
Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4588DSQ10T1G	1.0 V	Auto discharge	P010	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4588DSQ15T1G	1.5 V	Auto discharge	P015	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4588DSQ25T1G	2.5 V	Auto discharge	P025	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4588DMX10TCG	1.0 V	Auto discharge	LA	XDFN (Pb−Free)	5000 / Tape & Reel
NCP4588DMX15TCG	1.5 V	Auto discharge	LF	XDFN (Pb−Free)	5000 / Tape & Reel
NCP4588DMX25TCG	2.5 V	Auto discharge	LR	XDFN (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: To order other package and voltage variants, please contact your ON Semiconductor sales representative.

PACKAGE DIMENSIONS

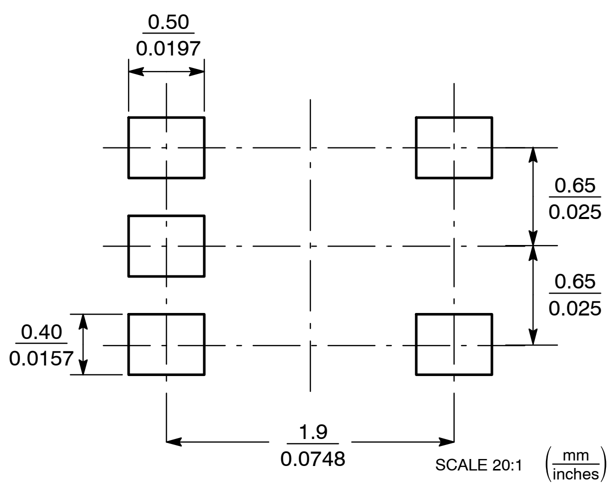
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

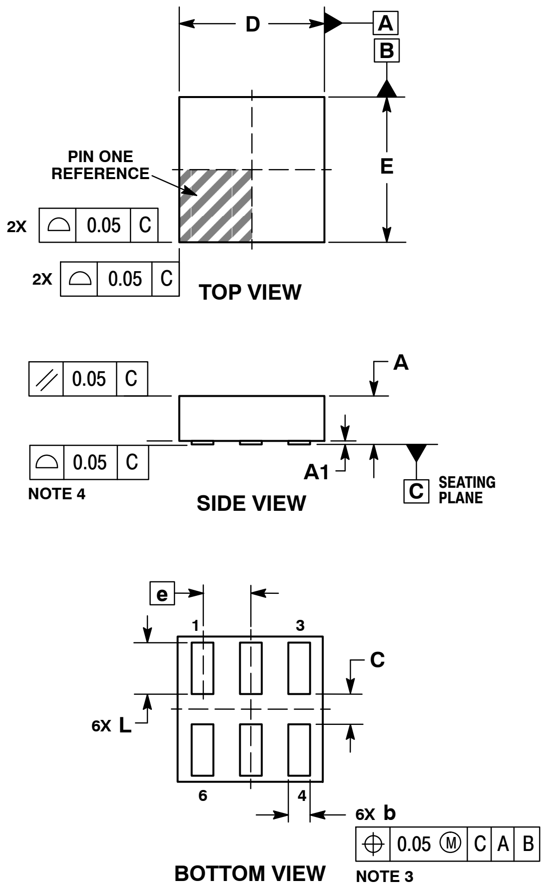
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



PACKAGE DIMENSIONS

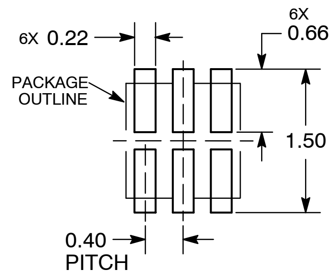
XDFN6 1.2x1.2, 0.4P
CASE 711AA
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM TERMINAL TIPS.
4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.13	0.23
C	0.20	0.30
D	1.20 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.37	0.48

RECOMMENDED MOUNTING FOOTPRINT*

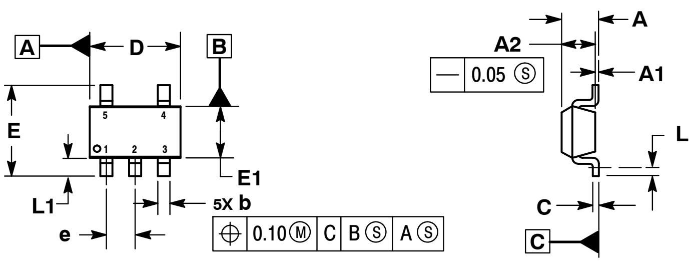


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

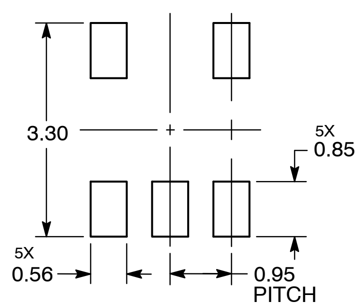
SOT−23 5−LEAD
CASE 1212
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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